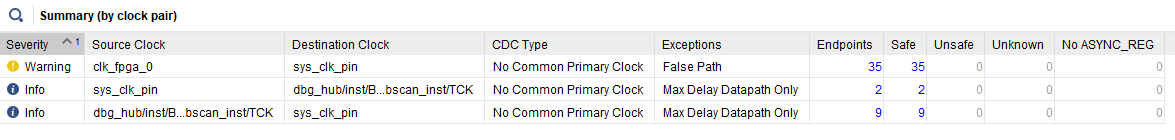
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525.742.8VL System-on-a-Chip FPGA Design Laboratory

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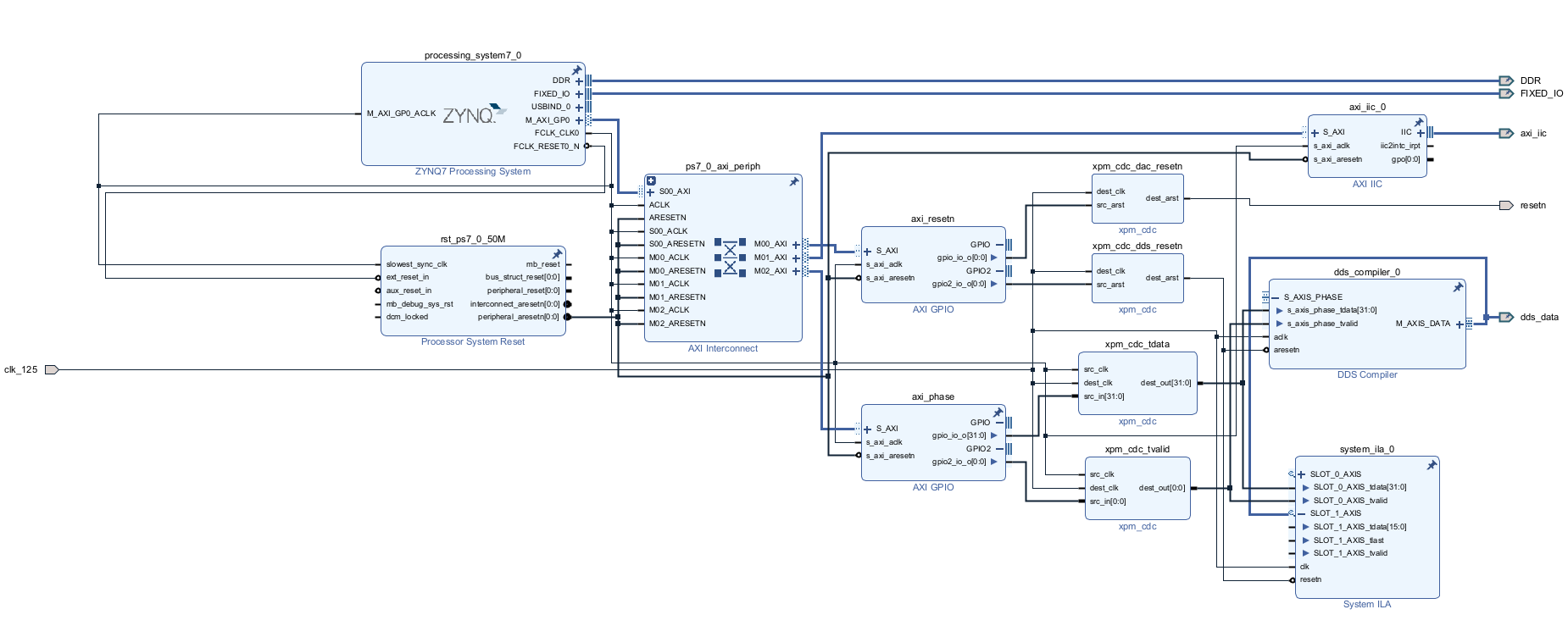
Lab 3B: SDR Signal Source

**CDC Report**



*Figure 1: CDC report showing that all 35 clock crossings are safely handled.*

**Block Diagram**



*Figure 2: Block diagram showing the full design with xpm\_cdcs added.*

There were 35 bits of signals created by the processor, and thus on the processor clock, which were routed through GPIOs to XPM\_CDC blocks before being passed to the DDS compiler, ILA, or output. The axi\_resetn GPIO passes two single-bit resetn signals, one for the DAC and one for the DDS, which both start on the processor clock. I used XPM\_CDC blocks set for asynchronous resets to pass them over to the 125 MHz system clock on which the DDS and DAC running. Similarly, the axi\_phase GPIO passes a single-bit tvalid signal and a 32-bit tdata signal through XPM\_CDCs to cross from the processor clock domain to the 125 MHz system clock domain. The output is then used to feed the DDS.