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Lab 4B: FIR Filter Implementation

**Measured to Modeled Analysis**

To generate the simulated signal for the following plots, I used a signal amplitude of 214with 2,621,440 points (1024 \* 2560, or the total decimation rate). As visible in figures 1 and 2, the transition band signal is extremely similar between both the ILA capture and simulated data. For the stopband signal shown in figure 3, the two are nearly perfectly matched as well. The slight phase offset is expected, since there is no way to align the signals with a reset (given that there is latency in the filter chain). While this could be accounted for in post-processing, a qualitative analysis clearly shows good agreement between the measured and modeled filter data.

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*Figure 1: Simulated versus ILA recorded data for a transition band signal at 25 kHz.*

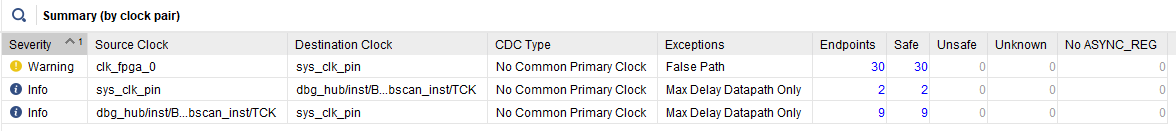
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*Figure 2: A zoomed in view of the plot from figure 1 showing the similarity in amplitude and frequency between the two signals.*

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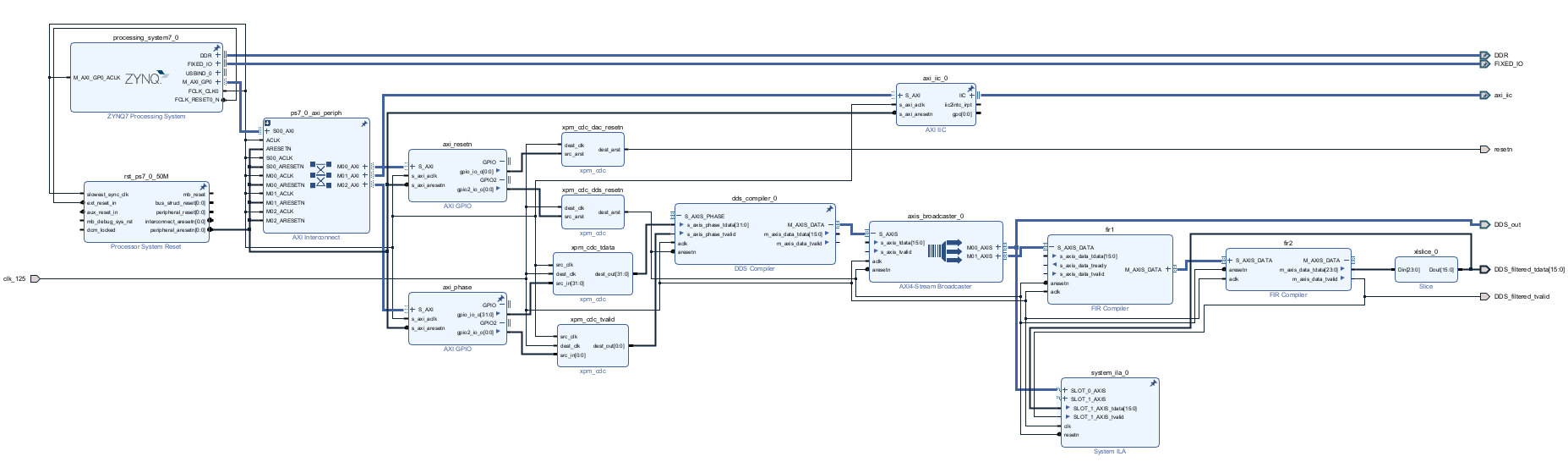
*Figure 3: Simulated versus ILA recorded data for a stopband signal at 50 kHz.*

**CDC Report**



*Figure 4: Implementation CDC report showing that all clock crossings are safely handled.*

**Block Diagram**



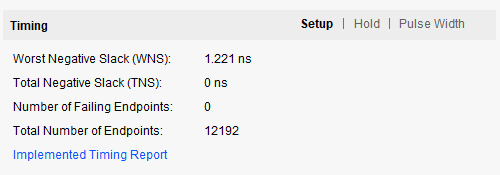
*Figure 5: Block diagram showing the full design with xpm\_cdcs added.*

**Clock Handling**

There were 35 bits of signals created by the processor, and thus on the processor clock, which were routed through GPIOs to XPM\_CDC blocks before being passed to the DDS compiler, ILA, or output. The axi\_resetn GPIO passes two single-bit resetn signals, one for the DAC and one for the DDS, which both start on the processor clock. I used XPM\_CDC blocks set for asynchronous resets to pass them over to the 125 MHz system clock on which the DDS and DAC running. Similarly, the axi\_phase GPIO passes a single-bit tvalid signal and a 32-bit tdata signal through XPM\_CDCs to cross from the processor clock domain to the 125 MHz system clock domain. The output is then used to feed the DDS.

While this portion of the design matches my lab 3B implementation, it is unclear why the implementation CDC report suggests there are only 30 endpoints instead of 35 (as shown in the report from lab 3B). Worth noting, the CDC report from synthesis does match the expected endpoints with a total of 35 safely crossed. I suspect that as the design was implemented, there was some optimization done to reduce the total number of crossings, but even this does not make complete sense given all 35 bits should be utilized in the design.

**Timing**



*Figure 6: Timing analysis for setup violations*

Given a worst negative slack of 1.221ns and assuming no changes are made to the design or the generation process, one could run the clock up to 147.5 MHz without incurring any setup violations. This is based on the following equation: . The design is presently running at 125 MHz (8ns period), so until the clock period is less than 8ns – 1.221ns 🡪 6.779ns, we should not violate the setup time for the worst path. This corresponds to a clock rate of 147.5 MHz. However, it is worth noting that on each implementation of the design, the routing of the paths might vary slightly and cause the worst negative slack value to fluctuate some. Thus, a design clocked to the limit of WNS shown above might show timing hazards in some builds (without making some modifications or getting the tools to optimize better).