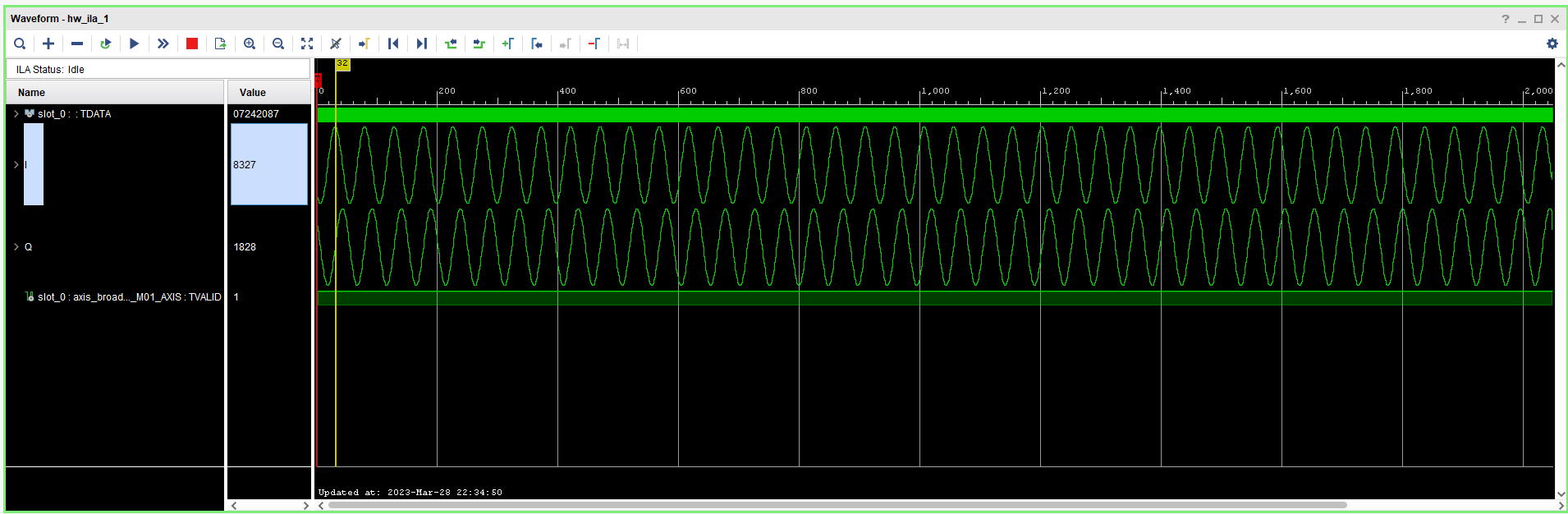
Dirk Holzman

525.742.8VL System-on-a-Chip FPGA Design Laboratory

March 29, 2023

Lab 5: Full Microprocessor-controlled Digital Downconverter

In general, the most challenging part of this lab was determining how to setup the complex multiply in terms of which bits to truncate (from the bottom) and which to slice (off the top). I also found that the DAC IP had a swapped polarity reset from my design, which caused quite a bit of confusion until adding the latched\_data signal to an ILA. To demonstrate the output matches the Matlab model, see the following figures. Otherwise, the lab should run as described by the prompt and rubric.



*Figure 1: Output visualized in the ILA for tune = 30 MHz, signal = 30.001 MHz.*

*Figure 2: Data plotted in Excel for cross-comparison for the same signal.*



*Figure 3: Results from the Matlab model for tune = 30 MHz, signal = 30.001 MHz.*