From ZEBRA to PandA: A New Open Hardware Platform

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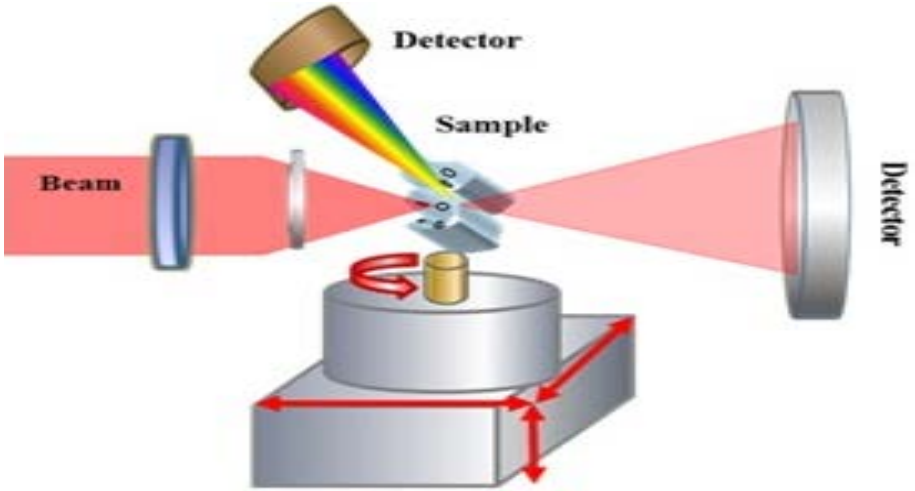
Accelerator Controls Team

diamond

On-The-Fly Scanning



Motion control → **Encoder Processing** → **Data Acquisition**

Synchronous Operation

Instruments varies from beamline to beamline:

- Motion controllers
- Area Detectors
- ADC cards
- Counter/timer
- Multi Channel Analysers
- Timing system Receiver cards

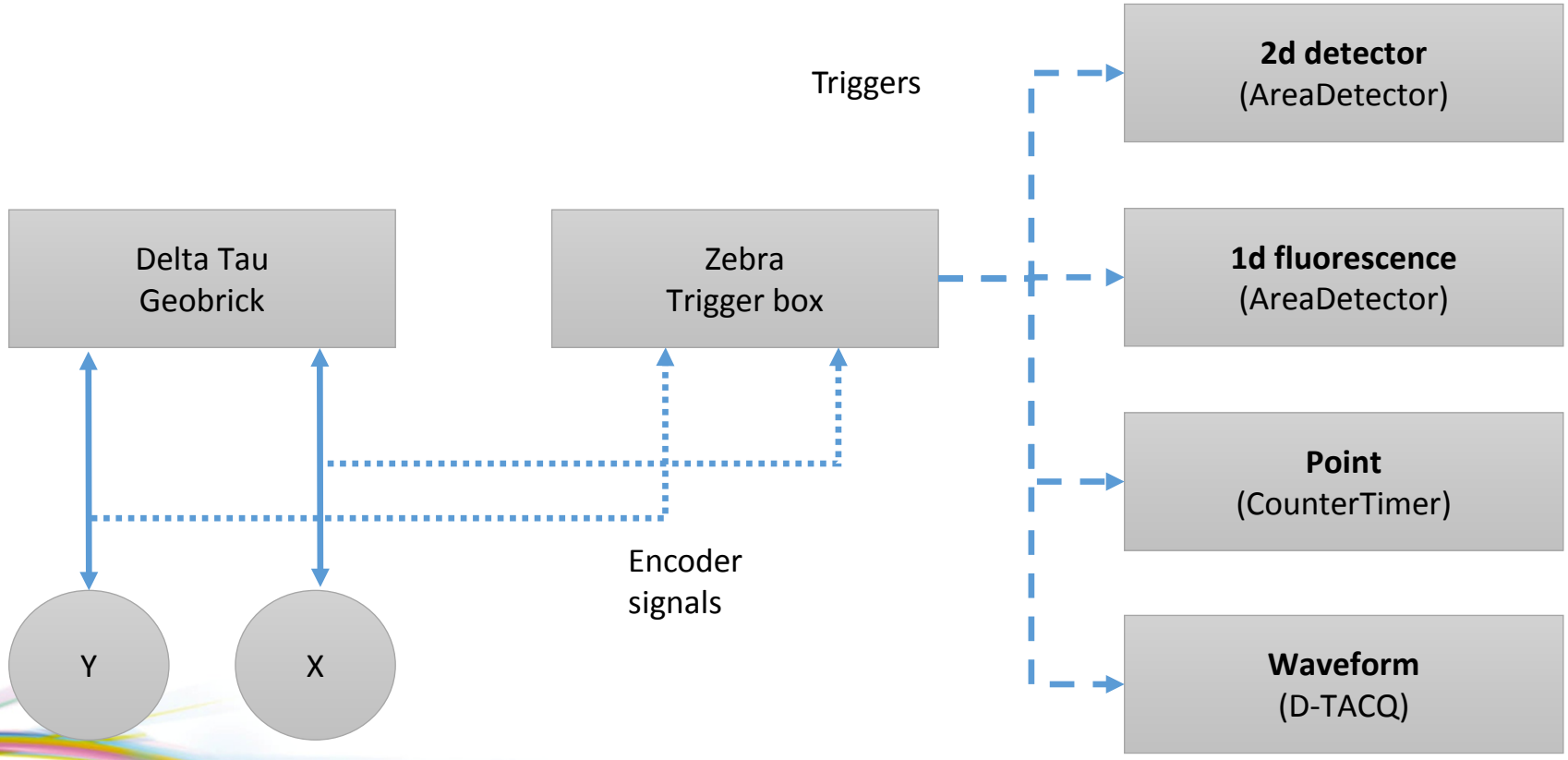
Challenges

- Electrical I/O compatibility between instruments
- Synchronous triggering/operation of all instruments
- Control System Integration of many instrument
- Overall cost (especially VME-based hardware)

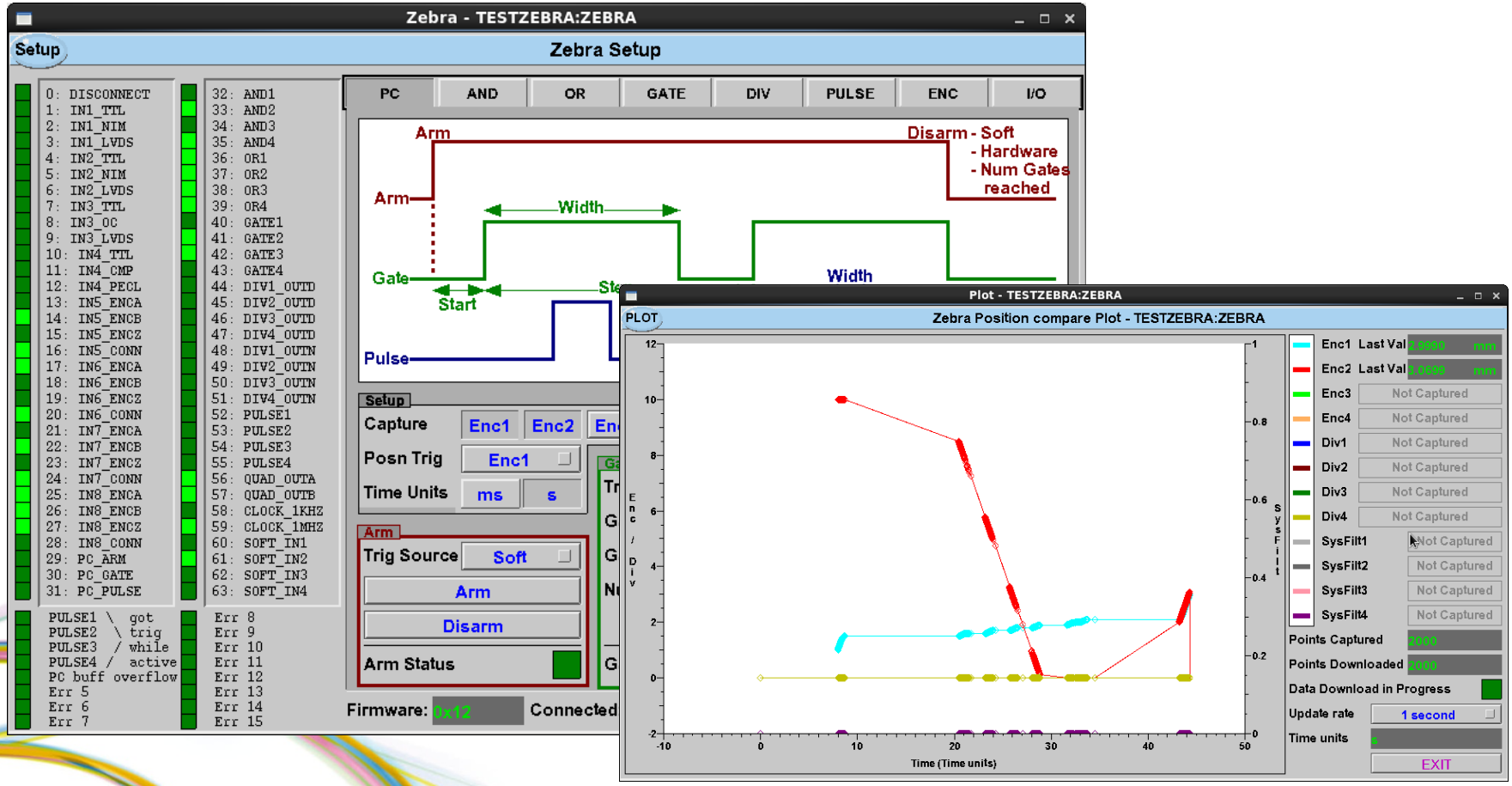
Zebra

- All-in-one:
  - Digital signal level converter
  - Triggering
  - Position compare
  - Data acquisition
- Developed in 2013 at Diamond
  - Available from Quantum Detectors
  - Used around the world

Zebra Application



Zebra – Flexibility via EPICS



Zebra's logic and data capture functions are fully configurable via EPICS interface.

Motivation behind PandA

- Analogue
- Signals < 20ns
- Absolute encoder protocols
- Sequencing
- Multi channel Position Compare
- Table-based Position Compare
- High bandwidth data transfer
- More FPGA resources

PandA Project Collaboration

Zebra **SPIETBOX**

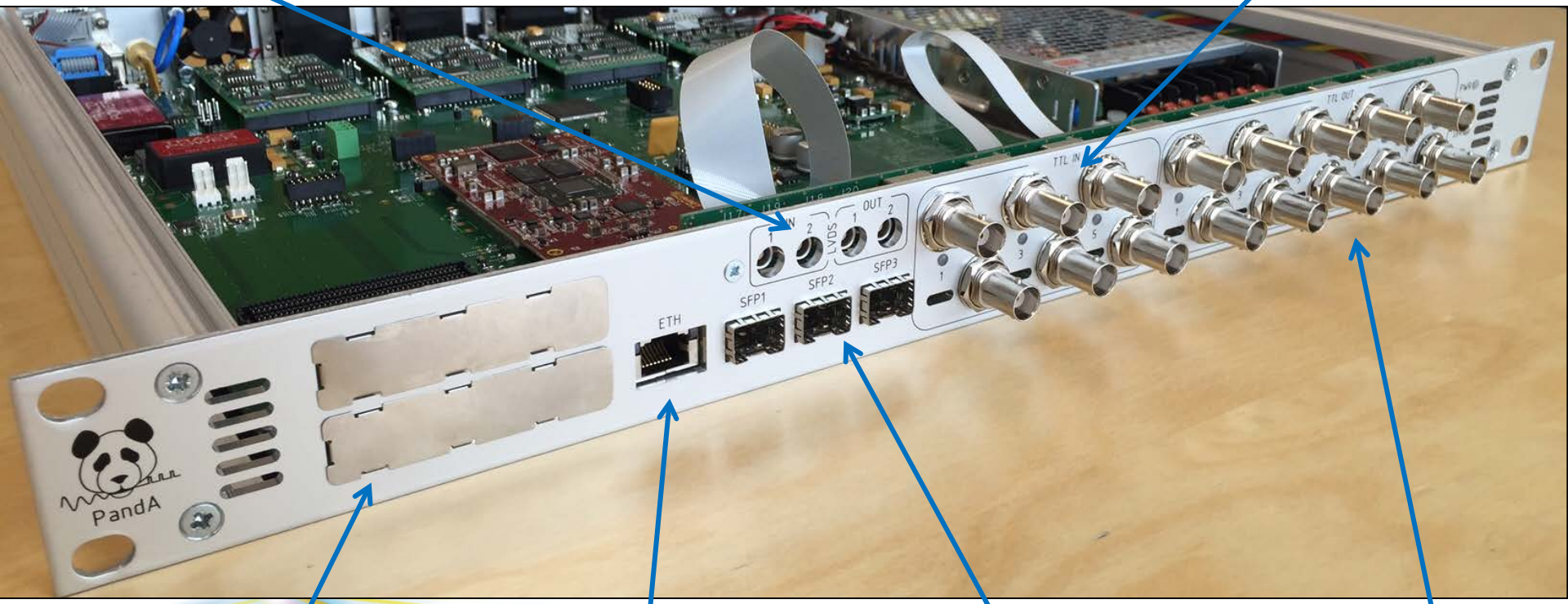
« PandA » Motion Project

- Started in 2015.
- SOLEIL → Electronics and Mechanics
- Diamond → Firmware, Software and Web GUI

Front Panel

2x LVDS Input
2x Outputs

6x TTL Inputs
(Switchable termination)



Low Pin Count FMC

Gigabit Ethernet

3x SFPs (6.8Gbps)

10x TTL Outputs

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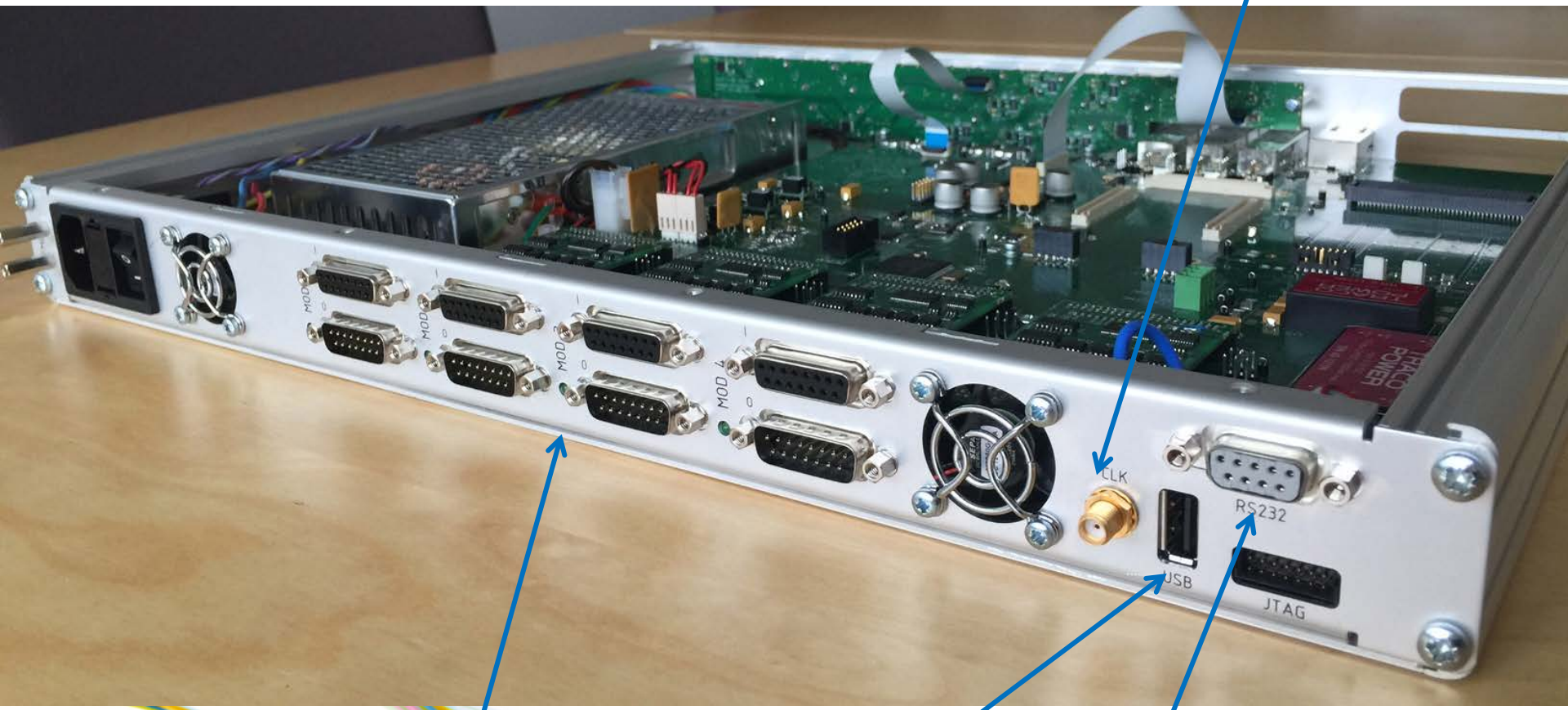
Rear Panel



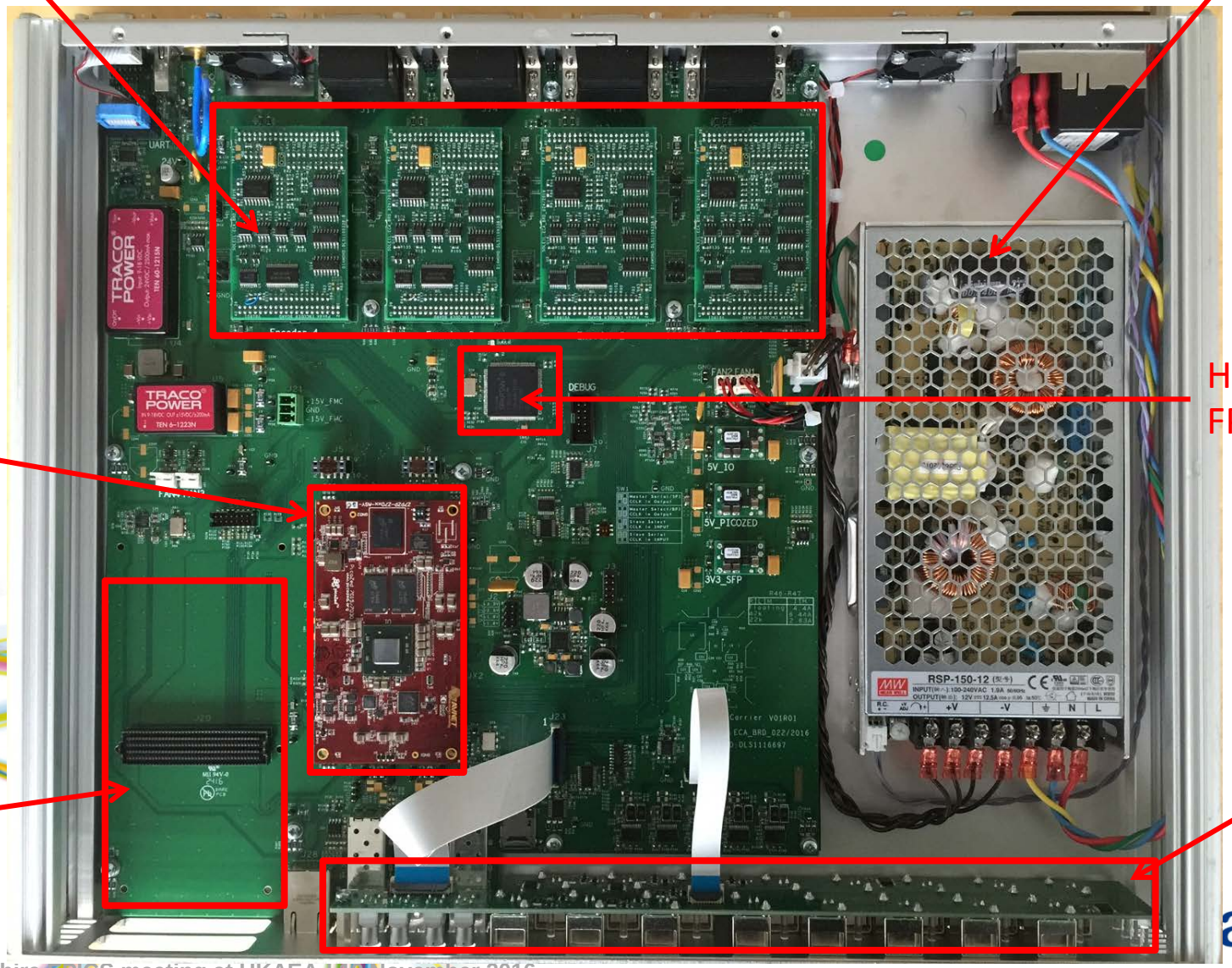
External FPGA Clock

4-Channel RS-485 Encoder

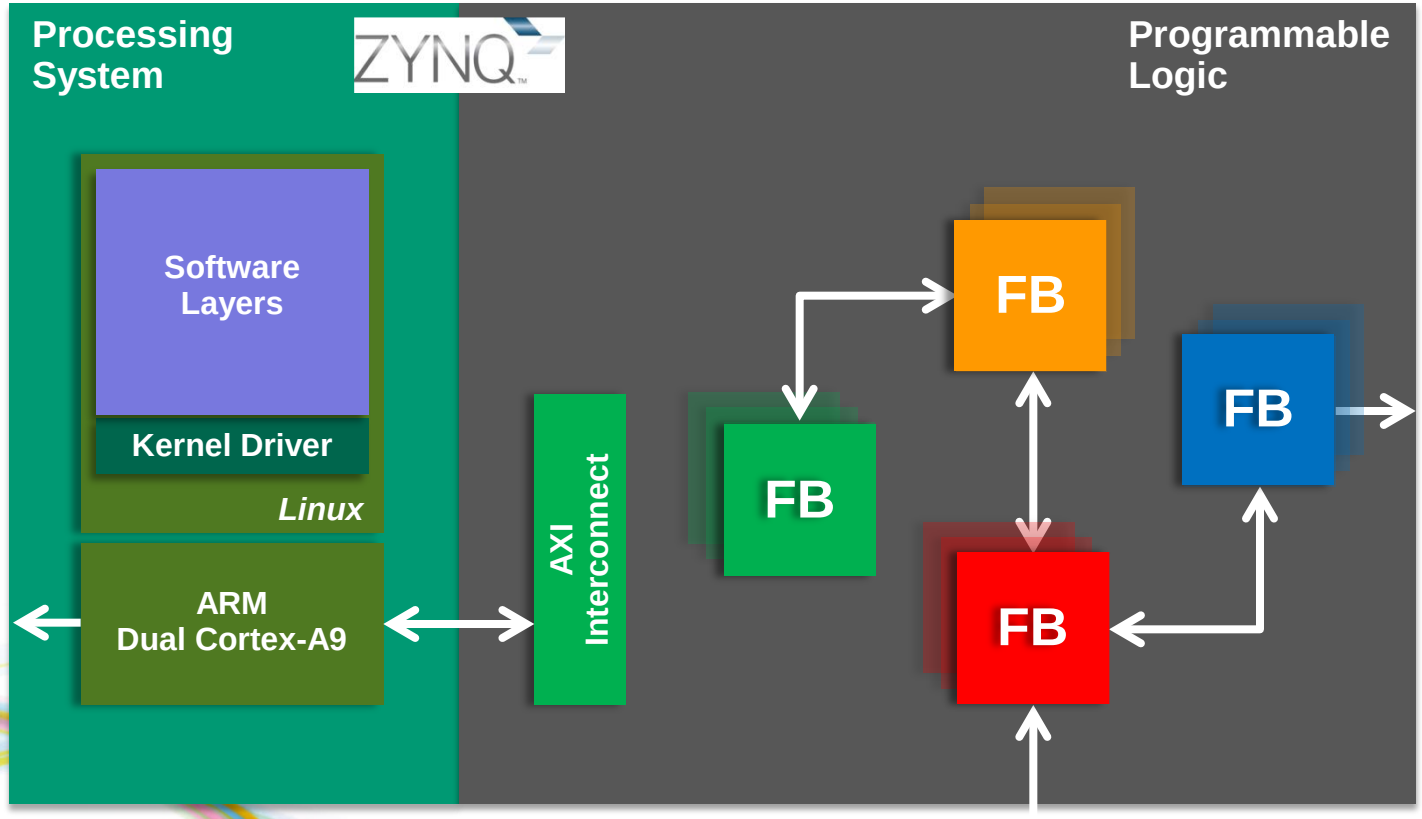
USB Host

ARM Terminal Console

Inside

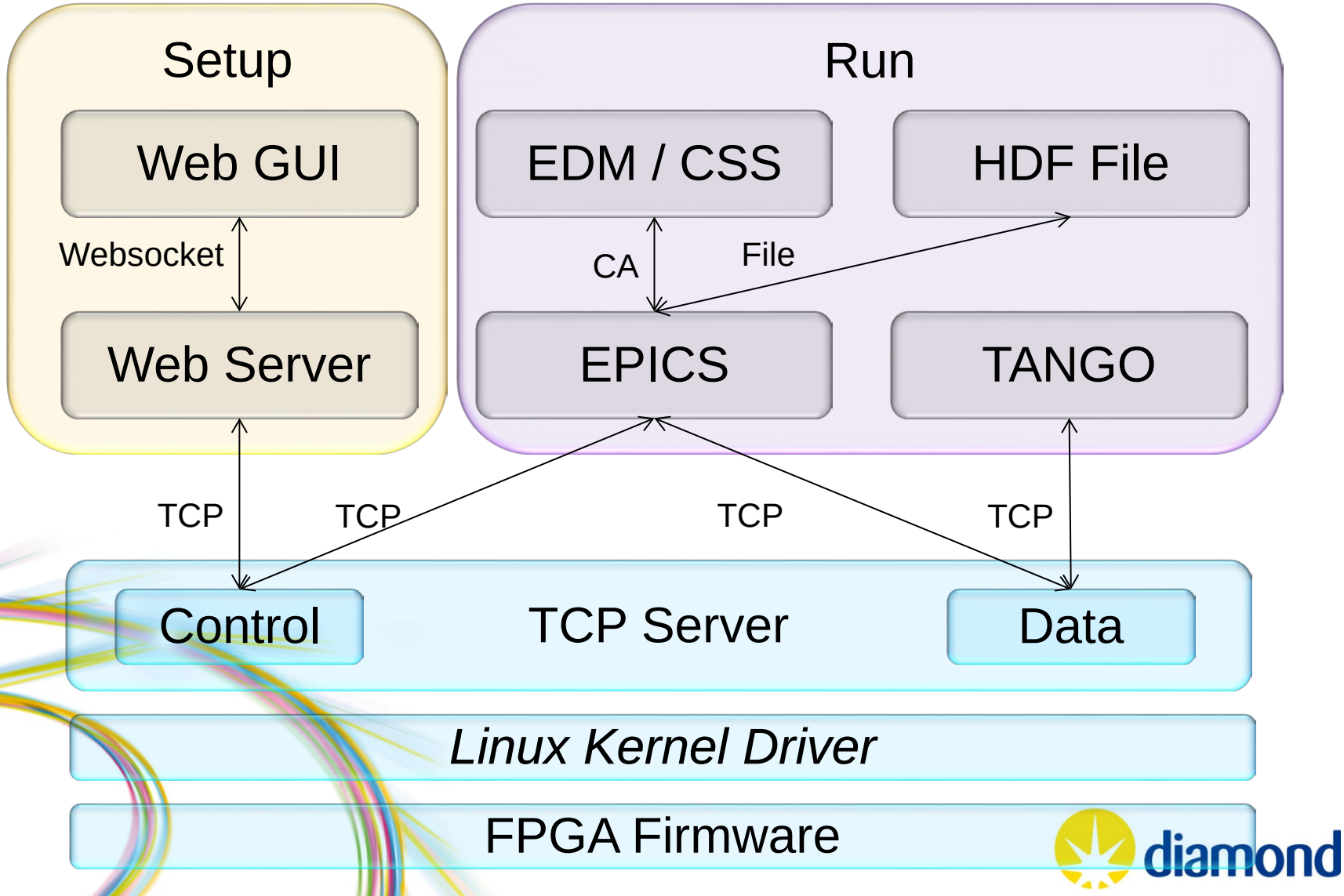

4x Encoder Daughter Modules
130W PSU
Housekeeping FPGA
Avnet Picozed
LPC FMC
Front Panel PCB
TRACO POWER
DEBUG
5V_IO
5V_PICOZED
3V3_SFP
RSP-150-12

Firmware Architecture



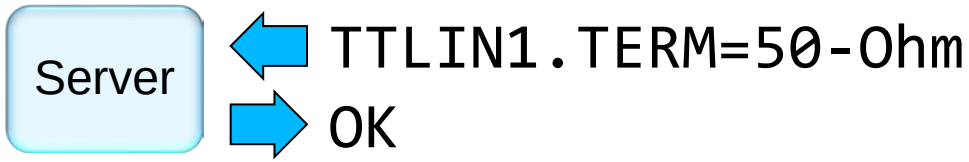
- Large set of highly configurable Function Blocks
- Fully rewirable (in run-time) architecture

Software Architecture



TCP Server

- Control
  - Interfaces to FPGA over registers
  - Publishes socket endpoint with simple ASCII command response protocol, E.g.



  - Block structure defined in configuration file
- Data
  - Received from FPGA via DMA using kernel driver
  - Publishes socket endpoint with ASCII, BASE64 or BINARY data frame encoding

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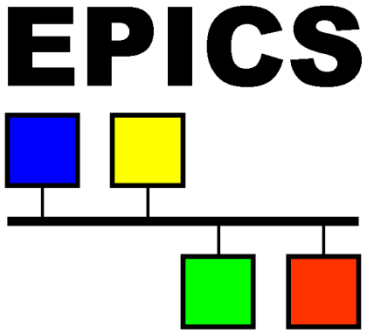
Web Server

- Malcolm
- Publishes websocket endpoint with JSON protocol
- Block structure defined by querying TCP server
- Save/Load functionality
- Can be run on or off the box
- When run off the box allows setup of areaDetector plugin chain for file writing

EPICS Interface



- Fixed block setup for common use cases
- Static CS-Studio or EDM GUI
- Connects to DATA port
- areaDetector driver produces NDArrays that are written to HDF file
- Used for runtime
- TANGO will be similar for SOLEIL

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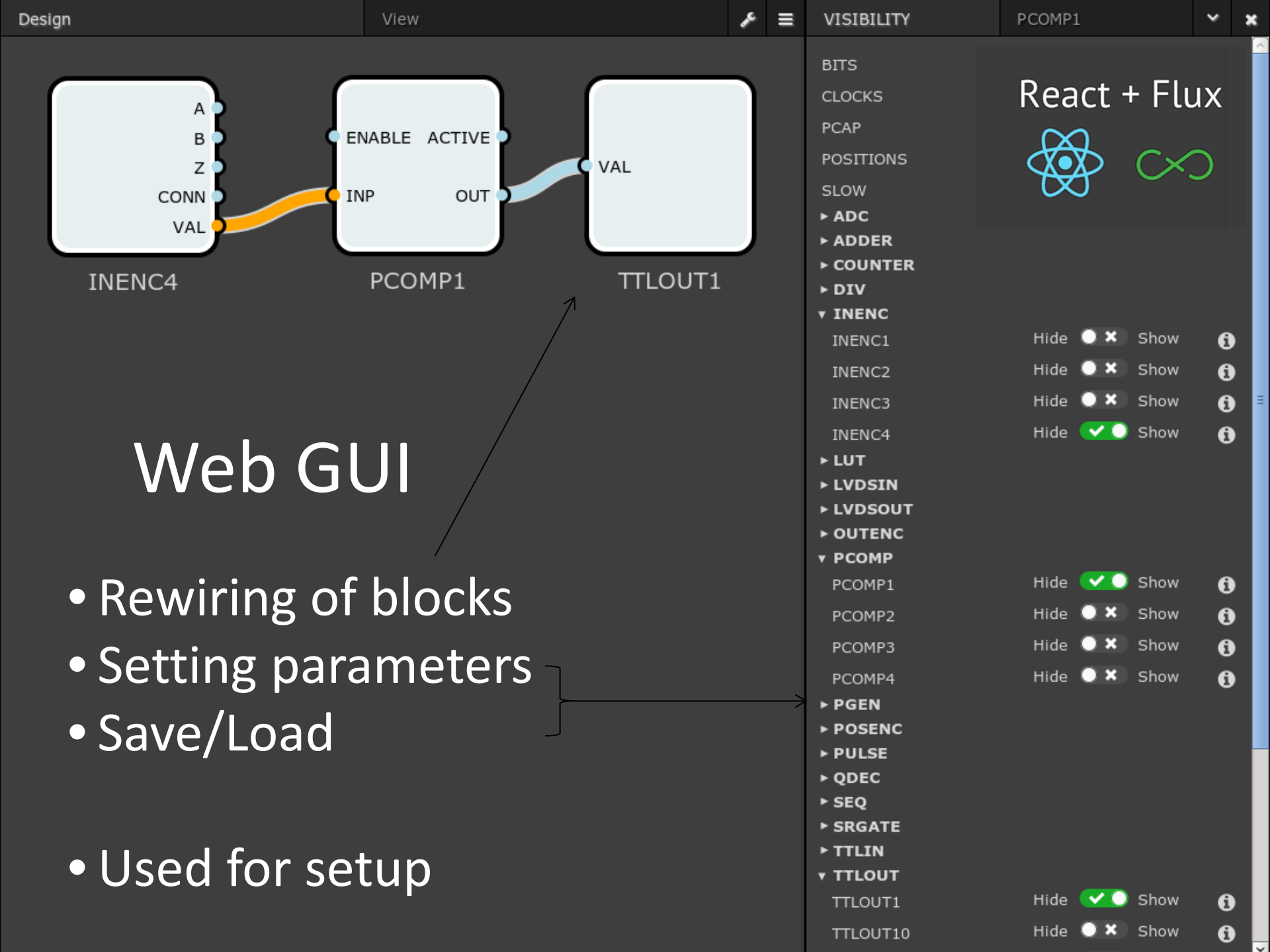
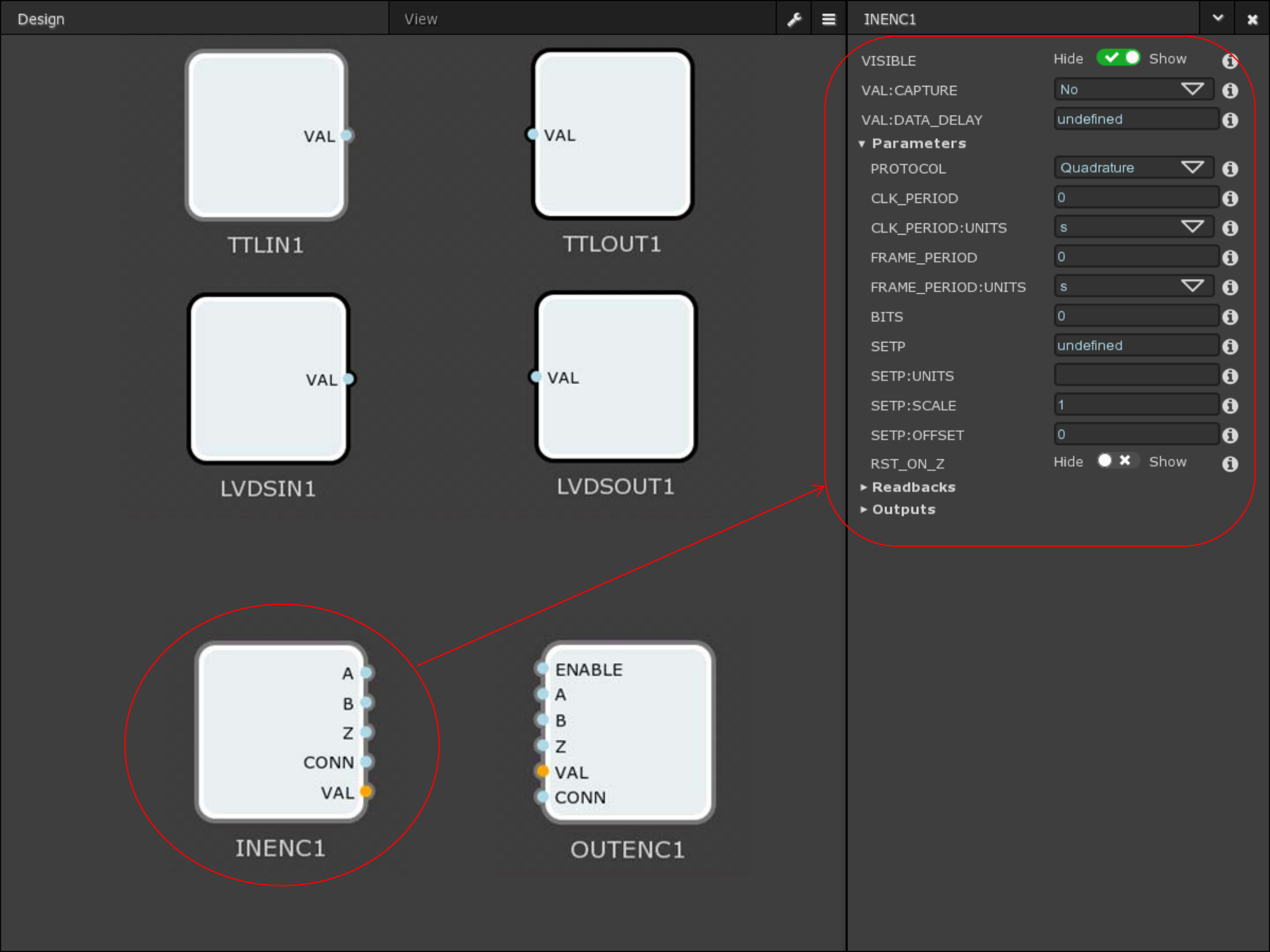

Design
View
VISIBILITY
PCOMP1
A
B
Z
CONN
VAL
ENABLE
ACTIVE
INP
OUT
VAL
INENC4
PCOMP1
TTLOUT1
BITS
CLOCKS
PCAP
POSITIONS
SLOW
ADC
ADDER
COUNTER
DIV
INENC
INENC1
INENC2
INENC3
INENC4
LUT
LVDSIN
LVDSOUT
OUTENC
PCOMP
PCOMP1
PCOMP2
PCOMP3
PCOMP4
PGEN
POSENC
PULSE
QDEC
SEQ
SRGATE
TTLIN
TTLOUT
TTLOUT1
TTLOUT10
Hide
Show
React + Flux
Web GUI
• Rewiring of blocks
• Setting parameters
• Save/Load
• Used for setup

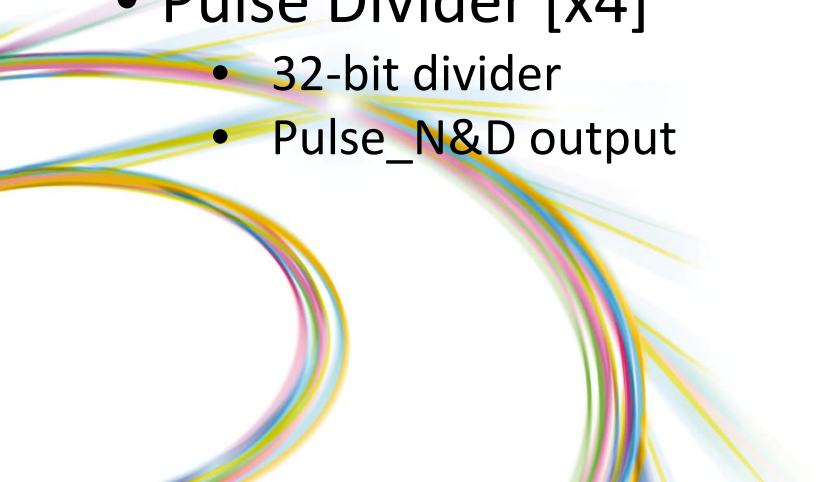
Firmware – Physical Interface

- TTL Input and Output
  - Front panel BNCs
  - Switchable termination
- LVDS Input and Output
  - Front panel Lemos
- Encoder Input and Output
  - Rear panel DB15s
  - Support for Quadrature, SSI, BiSS and EnDat
- FMC and SFP


Design
View
INENC1
VISIBLE
Hide
Show
VAL:CAPTURE
No
VAL:DATA_DELAY
undefined
Parameters
PROTOCOL
Quadrature
CLK_PERIOD
0
CLK_PERIOD:UNITS
s
FRAME_PERIOD
0
FRAME_PERIOD:UNITS
s
BITS
0
SETP
undefined
SETP:UNITS
SETP:SCALE
1
SETP:OFFSET
0
RST_ON_Z
Hide
Show
Readbacks
Outputs
VAL
TTLIN1
VAL
TTLOUT1
VAL
LVDSIN1
VAL
LVDSOUT1
A
B
Z
CONN
VAL
INENC1
ENABLE
A
B
Z
VAL
CONN
OUTENC1

Firmware – Functional Blocks

- LUT [x8]
  - 5-inputs
  - OUT = (A?B:C)=(A&B|~A&D)
- SRGate [x4]
- Pulse Generator [x4]
  - WIDTH/DELAY config
  - Support for pulse trains
- Pulse Divider [x4]
  - 32-bit divider
  - Pulse_N&D output
- Counter [x8]
  - 32-bit UP/DOWN
  - START&STEP config
- Sequencer [x4]
  - Auto-execution
  - 4 inputs/6-outputs
  - 1024 Frames
  - Frame and Table repeat
- Quadrature Encoder/Decoder [4x]
  - Internal wiring only



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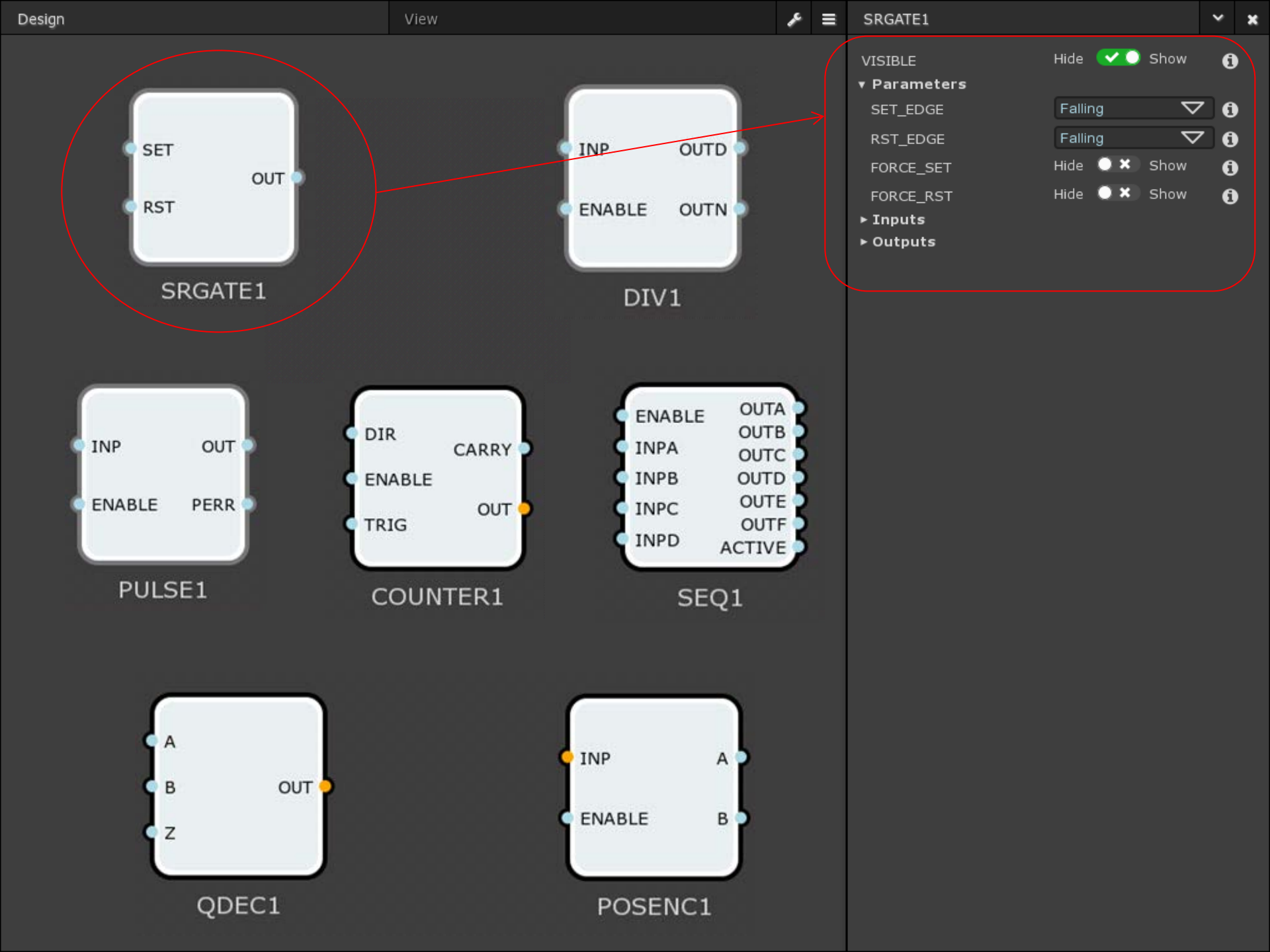
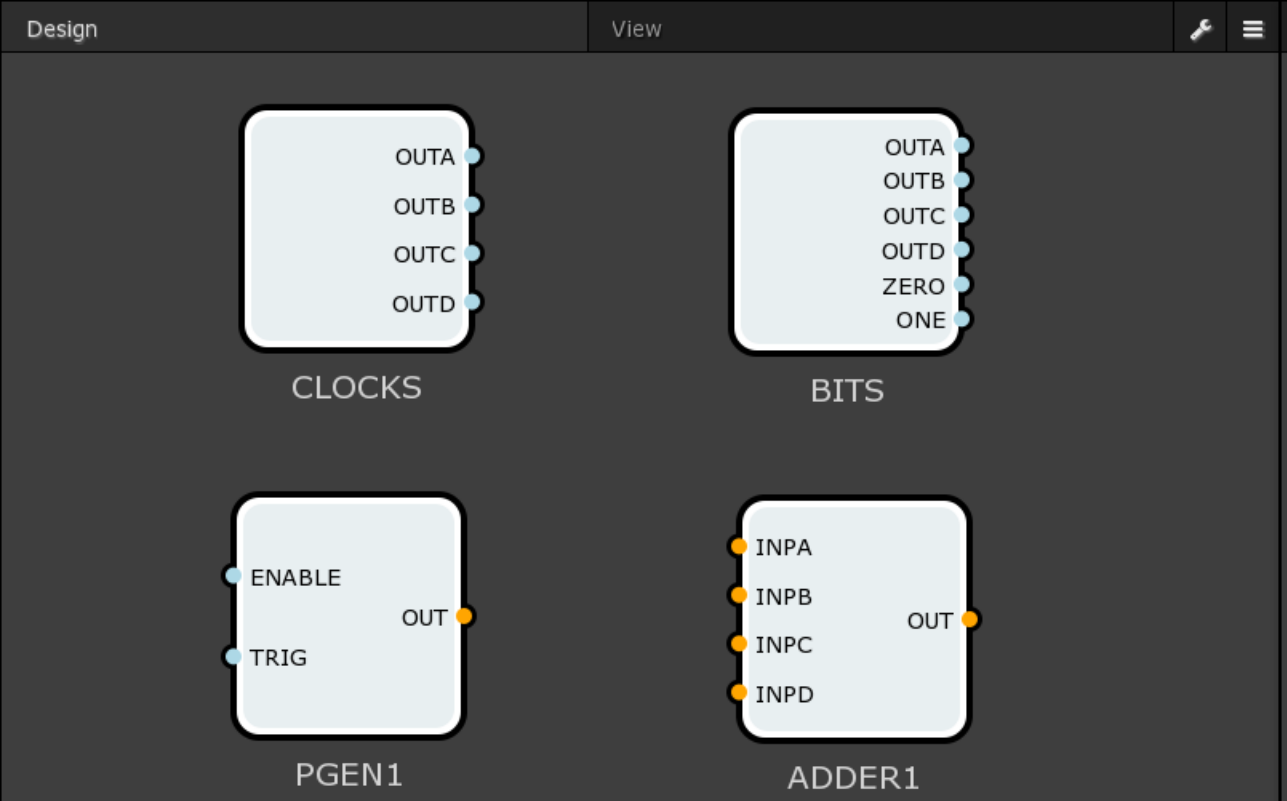
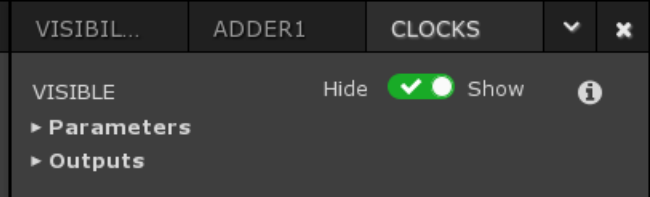

Design
View
SRGATE1
SET
RST
OUT
SRGATE1
INP
ENABLE
OUTD
OUTN
DIV1
VISIBLE
Hide
Show
Parameters
SET_EDGE
Falling
RST_EDGE
Falling
FORCE_SET
Hide
Show
FORCE_RST
Hide
Show
Inputs
Outputs
INP
ENABLE
OUT
PERR
PULSE1
DIR
ENABLE
TRIG
CARRY
OUT
COUNTER1
ENABLE
INPA
INPB
INPC
INPD
OUTA
OUTB
OUTC
OUTD
OUTE
OUTF
ACTIVE
SEQ1
A
B
Z
OUT
QDEC1
INP
ENABLE
A
B
POSENC1



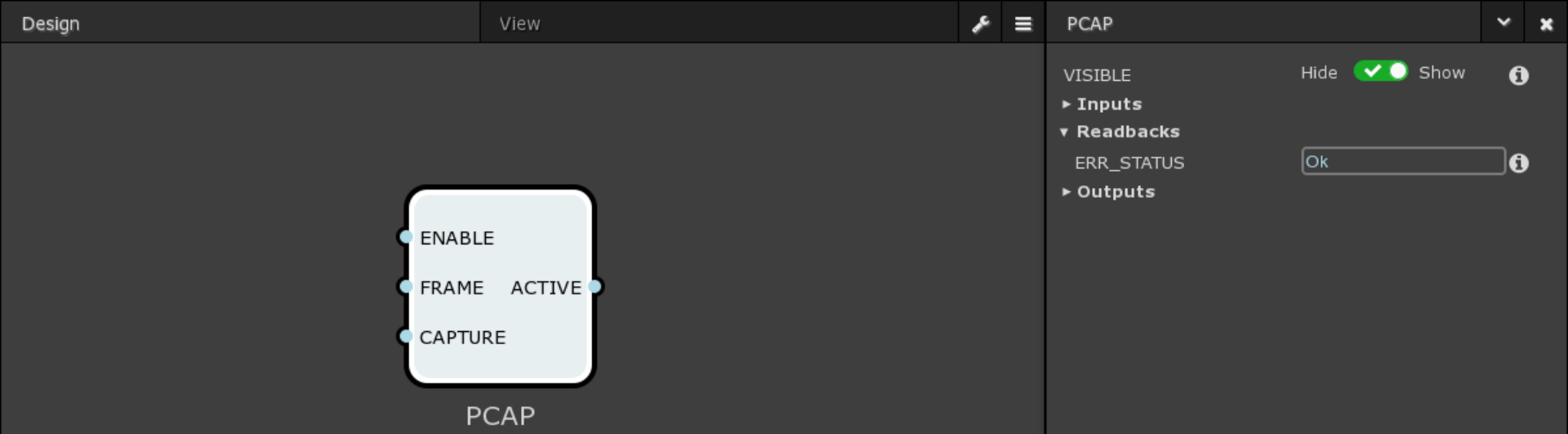


Misc Blocks

- [4x] Clocks
- [4x] Soft Bits
- [2x] Table-based Position Generator
- [2x] Position Adder

Position Compare [x4]

- Inputs from any Encoder, Counter and ADCs
- Linearly spaced pulse outputs
  - (START, STEP and WIDTH)
- User-defined table for irregular pulse outputs

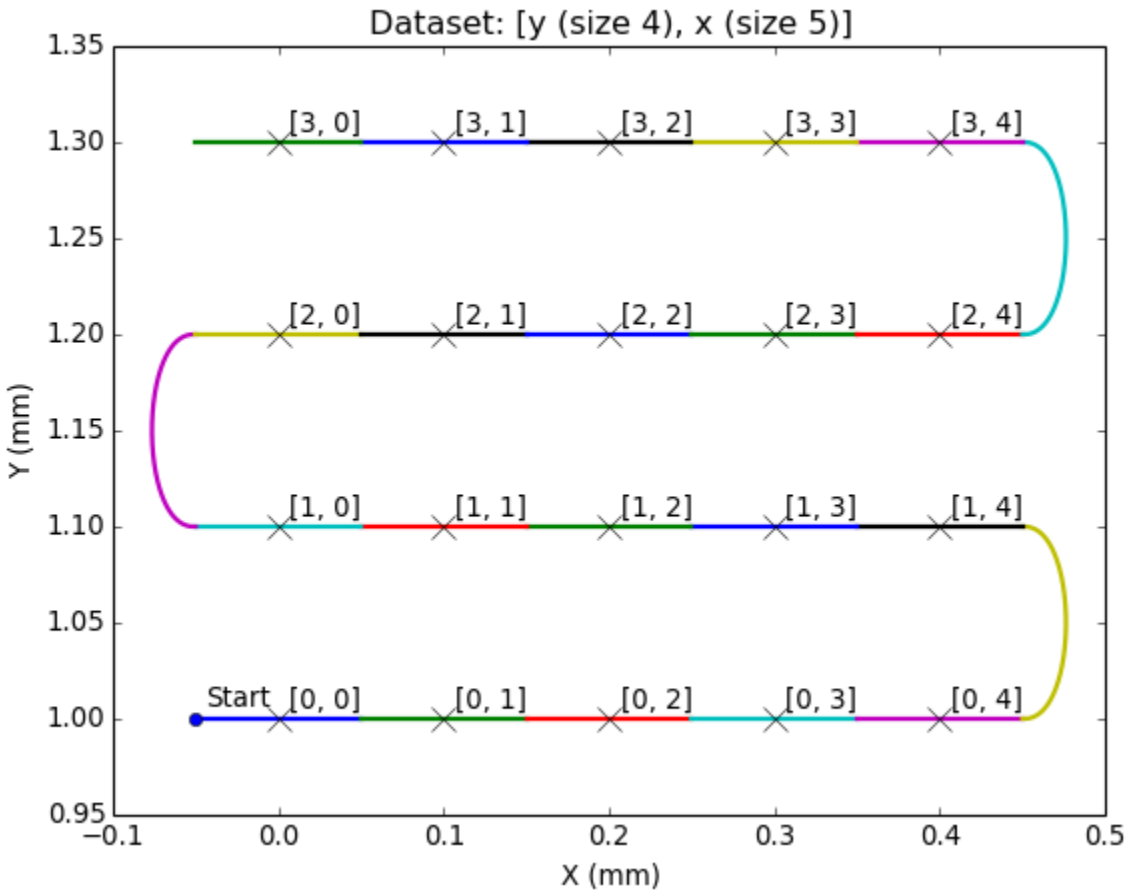


Position Capture

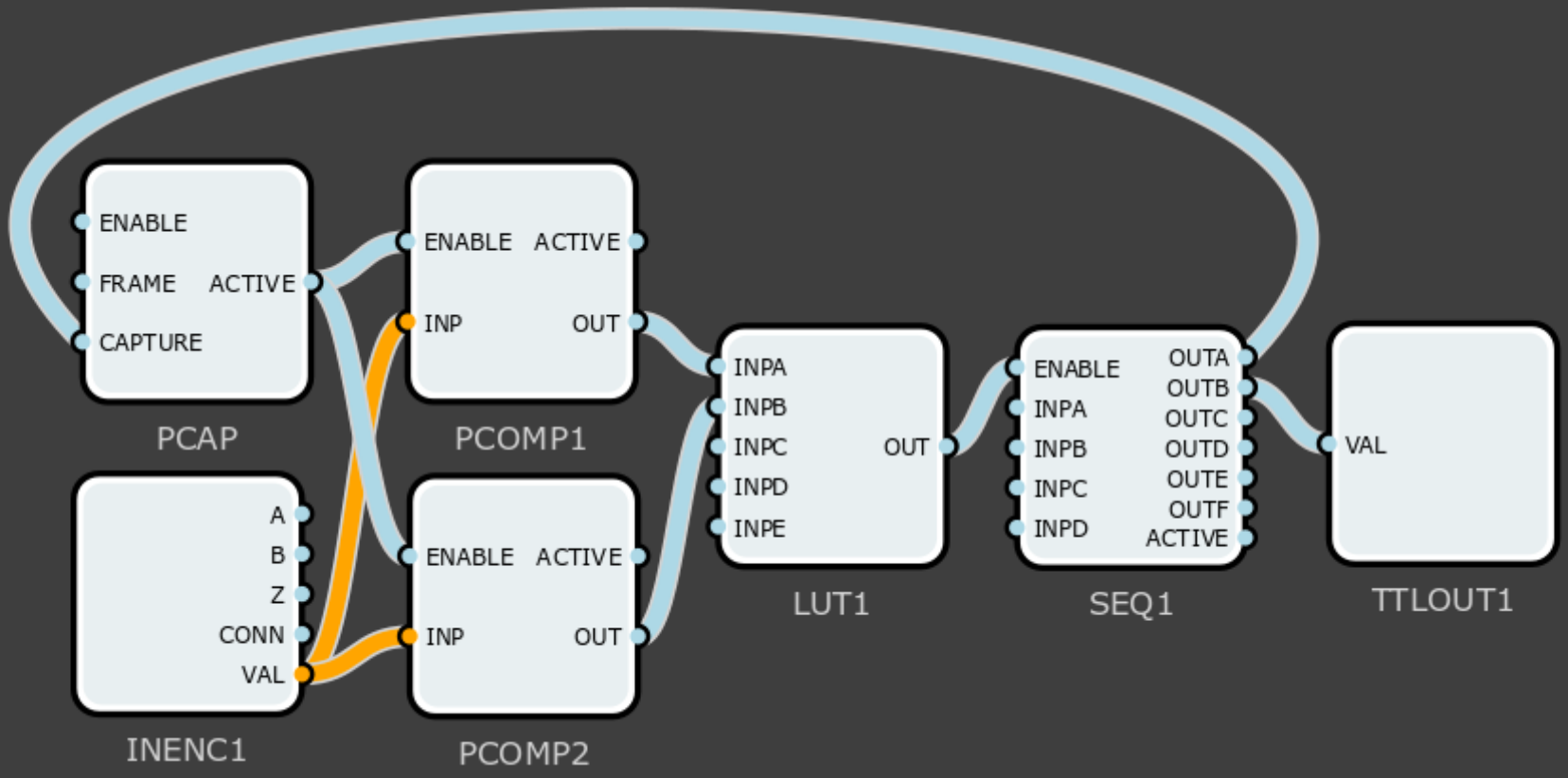
- Captures EVERYTHING internal - configurable
  - Encoder, Counter, ADC values
  - All discrete block outputs
  - Timestamps
- Frame mode for averaging (48-bits)
- Data throughput is limited by Gb Ethernet via Zynq
  - (Trigger Rate x Number of Fields)

Example App: Snake Scan

- Position compare to start each row
- Regularly spaced time based pulses within each row
- Reverse alternate rows
- Capture motor positions at centre of each frame



Snake scan with time based pulses



- 2 PCOMP blocks produce start of row
- SEQ block produces time based pulses
- Delay ½ deadtime for Det
- Delay ½ (deadtime + exposure) for PCAP

Project Status

- 4 prototypes received, and tested successfully
- Deployment on I18 and I08 in progress
- Initial production order placed via Quantum Detectors
- CERN Open Hardware Project created

http://www.ohwr.org/projects/pandabox

SOLEIL SYNCHROTRON diamond

Future Plans

- FMC-24VIO and FMC-OCL under development
- D-TACQ Solutions, FMC-ADC integration
  - 8 channel 1MS/s 18-bit FMC
  - Position compare and capture
- Micro Research Event Receiver
- Sin/Cos Interpolator
- 1Gb UDP over SFP for software triggering
- PandA-to-PandA Communication Networking

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Acknowledgements

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Thank you

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