```
1   `timescale 1ps/1ps
2
3   module tb_RegFile_Alu ();
4      reg [3:0] RdestRegLoc, RsrcRegLoc;
5      reg Clk, En, Rst, Imm_s;
6      reg [15:0] Imm;
7      reg [4:0] OpCode;
8
9      wire [4:0] Flags;
10     wire [15:0] RdestOut;
11
12     parameter ADD     = 4'b0000;
13     parameter SUB     = 4'b0001;
14     parameter CMP     = 4'b0010;
15     parameter AND     = 4'b0011;
16     parameter OR      = 4'b0100;
17     parameter XOR     = 4'b0101;
18     parameter NOT     = 4'b0110;
19     parameter LSH     = 4'b0111;
20     parameter RSH     = 4'b1000;
21     parameter ARSH    = 4'b1001;
22
23     integer i, j, k, l;
24
25     RegFile_Alu uut(
26        .RdestRegLoc(RdestRegLoc),
27        .RsrcRegLoc(RsrcRegLoc),
28        .Clk(Clk),
29        .En(En),
30        .Rst(Rst),
31        .Imm(Imm),
32        .Imm_s(Imm_s),
33        .OpCode(OpCode),
34        .RdestOut(RdestOut),
35        .Flags(Flags)
36     );
37
38     initial begin
39
40        $display("Starting integrated testbench");
41
42        $display("Setup");
43
44        Clk = 0;
45        Rst = 1;
46        En = 0;
47        #5; //Clk=1
48        Rst = 0;
49        #5; //Clk=0
50        Rst = 1;
51        RdestRegLoc = 4'b0000;
52        En =  1;
53        OpCode = ADD;
54        Imm_s = 1;
55        Imm = 1;
56        #10; //Clk=0
57        En = 0;
58        Imm_s = 0;
59        if (RdestOut != 1) begin
60           $display("Setup Failed");
61           $stop;
62        end
63        $display("Setup finished without error.");
64
65
66        $display("Test adding to different register");
67        for (i = 1; i < 16; i = i + 1) begin
68           RsrcRegLoc = 4'b0;
69           RdestRegLoc = i;
70           En = 1;
71           #10; //Clk = 0
72           En = 0;
73           if (RdestOut != 1) begin
```

```
74                $display("Test failed");
75                $stop;
76             end
77             #10; //Clk = 0
78          end
79
80          $display("Setup Fib");
81
82          Rst = 1;
83          #5; //Clk=1
84          Rst = 0;
85          #5; //Clk=0
86          Rst = 1;
87          RdestRegLoc = 4'b0001;
88          En =  1;
89          OpCode = ADD;
90          Imm_s = 1;
91          Imm = 1;
92          #10; //Clk=0
93          En = 0;
94          Imm_s = 0;
95          if (RdestOut != 1) begin
96             $display("Setup Fib Failed");
97             $stop;
98          end
99          $display("Setup Fib finished without error.");
100
101         j = 1; k = 1; l = 1;
102         for(i = 1; i < 15; i = i + 1) begin
103            RsrcRegLoc = i;
104            RdestRegLoc = i - 1;
105            En = 1;
106            #10; // Clk = 0
107            En = 0;
108            if(RdestOut != j)begin
109               $display("Test Fib Failed");
110               $stop;
111            end
112
113            #10; // Clk = 0
114            RdestRegLoc = i + 1;
115            RsrcRegLoc = i - 1;
116            En = 1;
117            #10; // Clk = 0
118            En = 0;
119            if(RdestOut != j)begin
120               $display("Test Fib Failed");
121               $stop;
122            end
123
124            // Fibonacci
125            k = k + l; j = l; l = k; k = j; j = l;
126            #10;
127         end
128
129         Rst = 1;
130         #5; //Clk=1
131         Rst = 0;
132         #5; //Clk=0
133         Rst = 1;
134         RdestRegLoc = 4'b0000;
135         En =  1;
136         OpCode = ADD;
137         Imm_s = 1;
138         Imm = 1;
139         #10; //Clk=0
140         En = 0;
141         Imm_s = 0;
142         if (RdestOut != 1) begin
143            $display("Setup LSH Failed");
144            $stop;
145         end
146         OpCode = LSH;
```

```
147         $display("Setup LSH finished without error.");
148
149
150         $display("Test LSH same register");
151         j = 2;
152         for (i = 0; i < 15; i = i + 1) begin
153            En = 1;
154            #10; //Clk = 0
155            En = 0;
156            if (RdestOut != j) begin
157               $display("RdestOut: %b", RdestOut);
158               $display("j: %b", j);
159               $display("Test failed");
160               $stop;
161            end
162            j = j * 2;
163            #10; //Clk = 0
164         end
165
166         Rst = 1;
167         #5; //Clk=1
168         Rst = 0;
169         #5; //Clk=0
170         Rst = 1;
171         RdestRegLoc = 4'b0100;
172         En =  1;
173         OpCode = ADD;
174         Imm_s = 1;
175         Imm = 16'b1101000110101100;
176         #10; //Clk=0
177         En = 0;
178         Imm_s = 0;
179         if (RdestOut != 16'b1101000110101100) begin
180            $display("Setup Boolean Operations Failed");
181            $stop;
182         end
183
184         RsrcRegLoc = 4'b0100;
185         RdestRegLoc = 4'b0011;
186         En = 1;
187         #10;
188         En = 0;
189         if (RdestOut != 16'b1101000110101100) begin
190            $display("Setup Boolean Operations Failed");
191            $stop;
192         end
193         OpCode = AND;
194         $display("Setup Boolean Operations finished without error.");
195         #10;
196         En = 1;
197         #10;
198         En = 0;
199         if (RdestOut != 16'b1101000110101100) begin
200            $display("Setup Boolean Operations Failed");
201            $stop;
202         end
203         OpCode = OR;
204         #10;
205         En = 1;
206         #10;
207         En = 0;
208         if (RdestOut != 16'b1101000110101100) begin
209            $display("Setup Boolean Operations Failed");
210            $stop;
211         end
212         $display("Boolean Operations Passed");
213
214
215
216         $display("All Tests passed");
217      end
218      always #5 Clk = ~Clk;
219   endmodule
```