Dmitrii Semenov

Analog IC designer & researcher

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Education

2024 – 2026 (projected)
Brno University of Technology, Czech Republic (BUT)
Department of Radio Electronics
MS in Electronics and Communication Technologies,
with a transition to a Ph.D if admitted

- Follow-up master's degree in Electronics and Communication Technologies

2021 – 2024
Brno University of Technology, Czech Republic (BUT)
Department of Radio Electronics
BS in Electronics and Communication Technologies

- GPA: 3.92/4.0, **diploma with honors**
- Thesis: Software for extraction of impedance model circuit parameters
- Advisor: Dr. Roman Sotner, Ph.D.

Research Experience

2022 – Present
Electronically-configurable analog IC design (supervised by Dr. Roman Sotner, Brno University of Technology)

- Developed high Q-Factor active Comb filter based on transconductance amplifiers (OTA) with band-rejection and inverted band-rejection behavior that can be electronically adjusted to the frequency range (up to 1MHz) based on custom fabricated chipsets in TSMC 180nm process
- Developed electronically-configurable constant phase elements (fractal capacitors) in "ON Semiconductor" I3T25 350nm process with complete circuit characterization and post-layout simulations

2023 – Present
Silicon nanowire-based circuits with memristive behavior (collaboration with Bio/CMOS Interfaces group, EPFL, Switzerland)

- Developed memristor emulator for biosensing applications based on transconductance amplifiers (OTA) and voltage differencing current conveyors (VDCC) in "ON Semiconductor" I3T25 350nm process using Cadence Virtuoso
- Built 2-layer test PCB in EAGLE PCB Editor, coordinated manufacture, and verified that current-voltage characteristics from 2 kHz to 500kHz aligned with memristor simulations by tuning capacitors and resistors values
- Developed readout circuit for memristive biosensors (voltage gap detection) for precise post-manufacture silicon nanowires specification and validation (sub-nA operating current range)

2023 – 2024
Bioimpedance emulator for hardware validation (supervised by Todd Freeborn, onsite at the University of Alabama, US)

- Developed switchable-impedance design (using analog multiplexers ADG1612 with low ON resistance) with a frequency range up to 500kHz and controlled resistance and reactance range
- Simulated switchable circuits in PSPICE for stability and parasitic analysis
- Built test breadboard and verified circuit behavior by measuring dynamic characteristics with an impedance analyzer E4990A, performed accuracy analysis

Internships

January 2023 – Present time
Analog Design Intern, company "onsemi", Czech Republic

- **Analog IC design** in Bipolar, CMOS, DMOS (BCD) 65nm and 180nm process for automotive applications using Cadence Virtuoso platform and Siemens Solido Design Environment (OPAMPs, voltage/current references, receiver/transmitter blocks, voltage monitors, temperature sensors, ADC, IO interfaces), **owner of 2 IP blocks**
- **Design-for-test methodology development** and implementation using loopback testing, current consumption, and internal nodes voltage measurement for testability purposes - total achieved test time for individual block **< 1 us**
- **Low voltage design** for 1.0V supply voltage using low-threshold CMOS transistors with small output resistance, developed new circuit topologies

- **Mixed-mode simulations** in AMS simulator on top-level (start-up, chip test-mode, and normal operation mode simulations), behavioral model definition in VerilogA
- **Coding in SKILL language** for custom functions implementation into Cadence Virtuoso environment (actions with project hierarchy and data integrity control)

July 2024 – August 2024 ***Digital Design Intern***, company "onsemi", Czech Republic

- **SystemVerilog model development** for SPI interface verification (automated checkers, procedures, custom macros), achieved 100% functional and code coverage
- **Documentation preparation**: verification test plan, technical specification and requirements, A/D interface description

July 2022 – January 2023 ***Layout Mask Design Intern***, company "onsemi", Czech Republic

- **Layout of IC mixed-signal circuits** (in high voltage 180nm process) for automotive and industrial applications using Cadence Virtuoso Layout Editor. Worked on separate blocks and top routing in collaboration with other design centers, performed layout section optimization
- **PEX post-layout simulations** with further EMC analysis

Publications

2024 Roman Sotner, Marek Svoboda, **Dmitrii Semenov**, Ladislav Polak, Jan Jerabek, Radek Theumer, Winai Jaikla "Special transfer section for selective rejecting and amplification response in pre-equalization", ***IEEE Transactions on Circuits and Sytems I***, DOI: 10.1109/TCSI.2024.3408691

2024 Kapil Bhardwaj, **Dmitrii Semenov**, Roman Sotner, Junrui Chen, Sandro Carrara, Mayank Srivastava "Emulating multi-memristive behavior of Silicon Nanowire-based biosensors by using CMOS-based implementations", ***IEEE Sensors***, DOI: 10.1109/JSEN.2024.3353669

2024 **D. Semenov**, R. Sotner, L. Polak, J. Jerabek, J. Petrzela, L. Langhammer "Comparison of analytical and algorithm-based design of two-port using two bilinear sections", ***IEEE Access***, DOI: 10.1109/ACCESS.2024.3434741

2024 **Dmitrii Semenov**, Todd J. Freeborn "Digitally controllable multi-frequency impedance emulator for bioimpedance hardware validation", ***International Journal on Circuit Theory and Applications***, DOI: 10.1002/cta.4324

2024 Roman Sotner, **Dmitrii Semenov**, Darius Andriukaitis, Marek Svoboda, Ladislav Polak "Novel second-order transfer section for frequency selective response generation in comb filters", ***submitted to IEEE Transactions on Instrumentation and Measurement***

Conferences

2025 **Dmitrii Semenov**, Roman Sotner, Jan Jerabek, Theumer Radek "Gate-controlled 3.3V CMOS transistor-based constant phase element design", ***submitted to 2025 IEEE International Symposium on Circuits and Systems***, *London, UK*

Course Projects

2023 Auxiliary Arithmetic Unit (AAU)

- Designed essential blocks in VHDL (Serial Peripheral Interface, Finite State Machine, Arithmetic Unit) for VLSI
- Made a design implementation by Synthesis, Place & Route, Static Time Analysis (STA), Gate-level verification. Prepared documentation with simulation results

2023 Morse coder and decoder

- Block modeling in VHDL(shift registers, debouncer, decoder, and display drivers) using Vivado software (later verified on FPGA Nexys A7-50)
- **Team leader**, received a **best project award**

Skills

Programming

- MATLAB, Python, VHDL, C, SKILL, SystemVerilog, VerilogA

Electrical Engineering software

- Cadence Spectre, Cadence Virtuoso Layout, Siemens Solido Design Environment for IC design and verification, EAGLE PCB editor, Spice, Xilinx ISE, Xilinx Vivado

Scholarships & Awards

2024 **Rector's award** for an exceptional academic achievement (2 students each year)

2024 **Dean's award** for an exceptional Bachelor thesis

2023 – Present **Ranked #1** out of 57 students in "Electronics and Communication Technologies" major

2023 **Research grant** for summer internship in bioelectronics area (onsite at University of Alabama, US)

2022 – Present **Scholarship** for excellent academic achievements, Brno University of Technology

September 2020 **Bronze medal** in International Young Physicists Tournament (IYPT) (Team competition), 11 participating countries