Dmitrii Semenov

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Education

2021 – 2024 (expected)

Brno University of Technology, Czech Republic (BUT)
Department of Radio Electronics
BS in Electronics and Communication Technologies

- GPA: 3.9/4.0
- Thesis: Electronically tunable Cole-Cole circuit prototype using VDCC-OTA structure with experimental verification
- Advisor: Dr. Roman Sotner

Research Experience

October 2023 – Present

Comparison of analytical and algorithm-based approaches to the design of constant phase two-port circuit using two bilinear sections
(Supervised by Dr. Sotner R., Brno University of Technology)

- Developed optimization algorithm for zeros/poles frequency calculation of constant phase element (CPE) circuit implemented by two bilinear sections using MATLAB

September 2023 – Present

Active Notch filter with high Q-Factor and electronically configurable frequency range
(Supervised by Dr. Sotner R., MS Svoboda.M., Brno University of Technology)

- Developed high Q-Factor active Notch filter based on transconductance amplifiers (OTA) with several band-pass and band-rejection modules with electronically adjustable frequency range (up to 1MHz) based on TSMC 180nm technology using Cadence Virtuoso

July 2023 – August 2023

Programmable test impedance circuit development for biomedical applications
(Supervised by Dr. Todd Freeborn, on-site at the University of Alabama)

- Developed switchable-impedance design (using analog multiplexers ADG1612 with low on resistance) with a frequency range up to 500kHz and controlled resistance and reactance range
- Simulated switchable circuits in PSPICE for stability and parasitic analysis
- Built test breadboard and verified circuit behavior by measuring dynamic characteristics with an impedance analyzer E4990A, performed accuracy analysis

August 2022 – November 2023

Electronically tunable memristor-behavior circuit based on VDCC-OTA structure
(Supervised by Dr. Sotner R., MS Bhardwaj K., Brno University of Technology)

- Developed memristor emulator with transconductance amplifiers (OTA) and voltage differencing current conveyors (VDCC) based on "ONSEMI" I3T25 350nm technology using Cadence Virtuoso
- Built 2-layer test PCB in EAGLE PCB Editor, coordinated manufacture, and verified that current-voltage characteristics from 2 kHz to 500kHz aligned with memristor simulations by tuning capacitors and resistors values

Internships

January 2023 – Present

Analog Design Internship, company ON Semiconductor (ONSEMI)

- Developed a transistor-level analog design of IC cells (in CMOS 65nm technology) for automotive applications using the Cadence Spectre Simulation platform and Solido Design Environment
- Collaborated with Layout and Test team for design-for-test methodology development, its further verification, and PEX post-layout simulations

July 2022 – January 2023

Layout Mask Design Internship, company ON Semiconductor (ONSEMI)

- Made a layout of IC mixed-signal circuits (in high voltage "ONSEMI" I4TE 180nm technology) for automotive and industrial applications using Cadence Virtuoso
- Worked on separate blocks and top routing in collaboration with other design centers, performed layout section optimization

June 2022 – July 2022

Summer Analog Design Internship, company ON Semiconductor (ONSEMI)

- Designed basic analog IC(operational amplifier, voltage reference, current bias reference, Analog to Digital converter (ADC)) in CMOS 180nm based technology
- Final project: Low drop voltage regulator, **best project award out of 14**

Publications

2023 Kapil Bhardwaj, **Dmitrii Semenov**, Roman Sotner, Junrui Chen, Sandro Carrara, Mayank Srivastava "Emulating multi-memristive behavior of Silicon Nanowire-based biosensors by using CMOS-based implementations", **submitted to Q1 IEEE Sensors**

2023 **Dmitrii Semenov**, Roman Sotner " Comparison of analytical and algorithm-based approaches to the design of constant phase two-port circuit using two bilinear sections", **submitted to Q2 MDPI Sensors**

2023 **Dmitrii Semenov**, Todd J. Freeborn "Digitally controllable multi-frequency impedance emulator for bioimpedance hardware validation", **in preparation**

Conference Proceedings

2021 Geit T.S., **Semenov D.A.**, Sidorenko F.A. "Direct measurement of the critical diving depth of a Cartesian diver" // Problems of educational physical experiment: Collection of scientific papers. INSTRAO, Issue 32, 49, in Russian

2020 **Semenov D.A.**, Sidorenko F.A. "Friction oscillator investigation" // Problems of educational physical experiment: Collection of scientific papers. INSTRAO, Issue 31, 75-76, in Russian

2019 **Semenov D.A.**, Sidorenko F.A. "Looping pendulum on a thread of varying length" // Problems of educational physical experiment: Collection of scientific papers. INSTRAO, Issue 30, 68, in Russian

2018 Sidorenko F.A., **Semenov D.A.**, Snigirev E.S. "Diffraction while photographing a distant light source" // Problems of educational physical experiment: Collection of scientific papers. INSTRAO, Issue 28, 114, in Russian

Course Projects

2023 Auxiliary Arithmetic Unit (AAU)

- Designed essential blocks in VHDL(Serial Peripheral Interface, Finite State Machine, Arithmetic Unit) using RTL coding for VLSI
- Made a design implementation by Synthesis, Place & Route, Static Time Analysis (STA), Gate-level verification

2023 Morse coder and decoder

- Completed code in VHDL(shift registers, debouncer, decoder, and display drivers were developed) using Vivado software(later verified on FPGA Nexys A7-50)
- **Team leader**, received **best project award**

Scholarships & Awards

2023 – Present **Ranked #1** out of 57 students in "Electronics and Communication Technologies" major

2022 – Present **Scholarship** for excellent academic achievements, Brno University of Technologies

September 2020 **Bronze medal** in International Young Physicists Tournament (IYPT) (Team competition), 11 participating countries

March 2018 **First place** in Russian Young Physicists Tournament (RYPT) (Team competition), city Novosibirsk

Skills

Programming and modeling

- Matlab, Python, VHDL, C, Solidworks

Electrical Engineering software

- Cadence Spectre for IC design, Cadence Virtuoso Layout for IC layout, Siemens Solido Design Environment for IC design and verification, EAGLE PCB editor, Spice, Xilinx ISE, Xilinx Vivado

Languages

- Russian (native), English (fluent,TOEFL iBT 94), Czech (fluent), German (beginner)