Dmitrii Semenov

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Education

2021 – 2024 (expected)

Brno University of Technology, Czech Republic (BUT)
Department of Radio Electronics
BS in Electronics and Communication Technologies

- GPA: 3.92/4.0
- Thesis: Software for extraction of impedance model circuit parameters
- Advisor: Dr. Roman Sotner, Ph.D.

2024 – 2026 (expected)

Brno University of Technology, Czech Republic (BUT)
Department of Radio Electronics
Follow-up Master's Degree in Electronics and Communication Technologies

Internships

January 2023 – Present

Analog Design Internship, company "onsemi", Czech Republic

- **Analog IC design** in Bipolar, CMOS, DMOS (BCD) 65nm process for automotive applications using Cadence Virtuoso platform and Siemens Solido Design Environment (OPAMPs, voltage/current references, receiver/transmitter blocks, voltage monitors, temperature sensors, ADC, IO interfaces), **owner of 2 IP blocks**
- **Design-for-test methodology development** and implementation using loopback testing and current consumption measurement for testability purposes
- **Mixed-mode simulations** in AMS simulator on top-level (start-up, chip test-mode, and normal operation mode simulations), performed troubleshooting with the Digital design team
- **Chip experimental verification** in a lab using an oscilloscope with voltage probes and a custom-developed Python script for measurement automatization, IP blocks verification
- **Coding in SKILL language** for custom functions implementation into Cadence Virtuoso environment (actions with project hierarchy and data integrity control)

July 2022 – January 2023

Layout Mask Design Internship, company "onsemi", Czech Republic

- **Layout of IC mixed-signal circuits** (in high voltage 180nm process) for automotive and industrial applications using Cadence Virtuoso Layout Editor. Worked on separate blocks and top routing in collaboration with other design centers, performed layout section optimization
- **PEX post-layout simulations** with further EMC analysis

June 2022 – July 2022

Summer Analog Design Internship, company "onsemi", Czech Republic

- **Analog IC design** in CMOS 180nm process (amplifiers, comparators, voltage references)
- **Final project**: 1.6V Low drop voltage regulator, **best project award out of 14**

Course Projects

2023

Auxiliary Arithmetic Unit (AAU)

- Designed essential blocks in VHDL (Serial Peripheral Interface, Finite State Machine, Arithmetic Unit) for VLSI
- Made a design implementation by Synthesis, Place & Route, Static Time Analysis (STA), Gate-level verification. Prepared documentation with simulation results

2023

Morse coder and decoder

- Block modeling in VHDL(shift registers, debouncer, decoder, and display drivers) using Vivado software (later verified on FPGA Nexys A7-50)
- **Team leader**, received a **best project award**

Skills

Programming

- MATLAB, Python, VHDL, C, SKILL

Electrical Engineering software

- Cadence Spectre, Cadence Virtuoso Layout, Siemens Solido Design Environment for IC design and verification, EAGLE PCB editor, Spice, Xilinx ISE, Xilinx Vivado

Languages

- Russian (native), English (fluent, TOEFL iBT 94), Czech (fluent), German (beginner)

Publications

2024 Kapil Bhardwaj, **Dmitrii Semenov**, Roman Sotner, Junrui Chen, Sandro Carrara, Mayank Srivastava "Emulating multi-memristive behavior of Silicon Nanowire-based biosensors by using CMOS-based implementations", ***published in IEEE Sensors***

2024 **D. Semenov**, R. Sotner, L. Polak, J. Jerabek, J, Petrzela, L. Langhammer "Comparison of analytical and algorithm-based design of two-port using two bilinear sections", ***submitted to IEEE Transactions on Circuits and Systems***

2024 **Dmitrii Semenov**, Todd J. Freeborn "Digitally controllable multi-frequency impedance emulator for bioimpedance hardware validation", ***submitted to IEEE Transactions on Instrumentation and Measurement***

2024 Roman Sotner, Marek Svoboda, **Dmitrii Semenov**, Ladislav Polak, Jan Jerabek, Radek Theumer, Winai Jaikla "Special transfer section for selective rejecting and amplification response in pre-equalization", ***in preparation***

Research Experience

October 2023 – December 2023 **Comparison of analytical and algorithm-based approaches to the design of constant phase two-port circuit using two bilinear sections**
(Supervised by Dr. Sotner R., Brno University of Technology)

- Developed optimization algorithm for zeros/poles frequency calculation of constant phase element (CPE) circuit implemented by two bilinear sections using MATLAB

September 2023 – Present **Comb filter with high Q-Factor and electronically configurable central frequencies**
(Supervised by Dr. Sotner R., Brno University of Technology)

- Developed high Q-Factor active Comb filter based on transconductance amplifiers (OTA) with band-rejection and inverted band-rejection behavior that can be electronically adjusted to the frequency range (up to 1MHz) based on TSMC 180nm technology using Cadence Virtuoso

July 2023 – January 2024 **Switchable test impedance circuit development for biomedical applications**
(Supervised by Dr. Todd Freeborn, on-site at the University of Alabama)

- Developed switchable-impedance design (using analog multiplexers ADG1612 with low on resistance) with a frequency range up to 500kHz and controlled resistance and reactance range
- Simulated switchable circuits in PSPICE for stability and parasitic analysis
- Built test breadboard and verified circuit behavior by measuring dynamic characteristics with an impedance analyzer E4990A, performed accuracy analysis

August 2022 – November 2023 **Electronically tunable memristor-behavior circuit based on VDCC-OTA structure**
(Supervised by Dr. Sotner R., Brno University of Technology)

- Developed memristor emulator with transconductance amplifiers (OTA) and voltage differencing current conveyors (VDCC) based on "onsemi" I3T 350nm process using Cadence Virtuoso
- Built 2-layer test PCB in EAGLE PCB Editor, coordinated manufacture, and verified that current-voltage characteristics from 2 kHz to 500kHz aligned with memristor simulations by tuning capacitors and resistors values

Scholarships & Awards

2023 – Present **Ranked #1** out of 57 students in "Electronics and Communication Technologies" major

2022 – Present **Scholarship** for excellent academic achievements, Brno University of Technology

September 2020 **Bronze medal** in International Young Physicists Tournament (IYPT) (Team competition), 11 participating countries