ECE 486 Project Report

Team:
Dmitrii Fotin
John Michael Mertz
Joshua Varughese

1. Total number of instructions and a breakdown of instruction frequencies for the following instruction types: Arithmetic, Logical, Memory Access, Control Transfer.

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Instruction counts:

Total number of instructions: 911
Arithmetic instructions: 375
Logical Instructions: 61
Memory access instructions: 300
Control transfer instructions: 175
```

2. Final state of program counter, general purpose registers and memory (You only need to include the register and memory locations whose state has changed during the program execution)

```
Final Register State:

Program Counter: 112
R11: 1044
R12: 1836
R13: 2640
R14: 25
R15: -188
R16: 213
R17: 29
R18: 3440
R19: -1
R20: -2
R21: -1
R22: 76
R23: 3
R24: -1
R25: 3
Address: 2400 Contents: 2
Address: 2404 Contents: 4
Address: 2408 Contents: 6
Address: 2412 Contents: 8
Address: 2416 Contents: 10
Address: 2420 Contents: 12
Address: 2424 Contents: 14
Address: 2428 Contents: 16
Address: 2432 Contents: 18
Address: 2436 Contents: 29
Address: 2440 Contents: 22
Address: 2444 Contents: 24
Address: 2448 Contents: 26
Address: 2452 Contents: 28
Address: 2456 Contents: 30
Address: 2460 Contents: 32
Address: 2464 Contents: 34
Address: 2468 Contents: 36
Address: 2472 Contents: 38
Address: 2476 Contents: 59
Address: 2480 Contents: 42
Address: 2484 Contents: 44
Address: 2488 Contents: 46
Address: 2492 Contents: 48
Address: 2496 Contents: 50
Address: 2500 Contents: 52
Address: 2504 Contents: 54
Address: 2508 Contents: 56
Address: 2512 Contents: 58
Address: 2516 Contents: 89
Address: 2520 Contents: 62
Address: 2524 Contents: 64
Address: 2528 Contents: 66
Address: 2532 Contents: 68
Address: 2536 Contents: 70
Address: 2540 Contents: 72
Address: 2544 Contents: 74
Address: 2548 Contents: 76
Address: 2552 Contents: 78
Address: 2556 Contents: 119
Address: 2560 Contents: 82
Address: 2564 Contents: 84
Address: 2568 Contents: 86
Address: 2572 Contents: 88
Address: 2576 Contents: 90
Address: 2580 Contents: 92
Address: 2584 Contents: 94
Address: 2588 Contents: 96
Address: 2592 Contents: 98
Address: 2596 Contents: 149
Address: 2600 Contents: 2
Address: 2604 Contents: 4
Address: 2608 Contents: 6
Address: 2612 Contents: 8
Address: 2616 Contents: 10
Address: 2620 Contents: 12
Address: 2624 Contents: 14
Address: 2628 Contents: 16
Address: 2632 Contents: 18
Address: 2636 Contents: 29
```

3. Describe the stall conditions in both the “no forwarding” and “forwarding” cases and how long you stalled the pipeline for each stall condition (e.g., in the “no forwarding” case, if a consumer instruction comes right after a producer instruction, then the stall penalty is 2 cycles)

No forwarding would have two stalls whenever a consumer instruction comes right after the producer instruction and one stall when the consumer instruction and the producer instruction have one other instruction in between them.

For forwarding there is only one scenario when one stall would happen - when a LDW instruction is followed directly by a consumer instruction.

4. In the case of “no forwarding”, the total number of data hazards and the average stall penalty per hazard

   Non-forwarding - 301 hazards, 542 stalls -> 1.8 stalls per hazard

5. In the case of “forwarding”, the number of data hazards which could not be fully eliminated by forwarding.

   120 stalls could not be fully eliminated by forwarding

   120 hazards, 120 stalls -> 1 stall per hazard

6. Execution time in terms of number of clock cycles for the “no forwarding” and the “forwarding” scenarios.

   Total **Forwarding** Total Clock Cycles: **1273**

   Total **Non-Forwarding** Clock Cycles: **1695**

7. Speedup achieved by “forwarding” as compared to “no forwarding”.

   Speedup = 1695 / 1273 = 33.15%

Member Contribution

Dmitrii: Code for memory instructions (LDW, STW), branch instructions (BZ, BEQ, JR) and halt instruction
John Michael: Worked on Logical Instruction (XOR, XORi, OR, ORi, AND, ANDi).
Josh: Worked on Arithmetic Instructions (ADD, ADDI, SUB, SUBI, MUL, MULI)