A Simple Parallel Bus Computer Control System for Atomic Physics Experiments

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Here we present a simple computer control system concept based on a parallel 16-bit bidirectional data bus, parallel 8-bit address bus, and strobe signal. This represents a particularly simple to understand and flexible system that is suited for a wide range of experimental control. In particular, we use it for cold atom experiments. Nothing here is specific to atom physics, many experimental systems could benefit from such a control system. Although these concepts are well known in the hardware community and everything here represents old technology, much has been unknown to the experimental atom physics community. Our implementation may be considered a brute-force method were most devices used can largely be considered unintegrated whereas they are very flexible and appropriate for use as laboratory electronics. The simplicity of the parallel bus allows easy interfacing with many devices including Digital-to-Analog Converter (DAC), Analog-to-Digital Converter (ADC), Direct Digital Synthesis (DDS), microprocessors, etc. Another important aspect of this method is simplicity of construction in that the hardware is available from many electronics distributors and can be fabricated in a few weeks by undergraduates or graduate students.

Figure 1 gives an overview of the system we are using. This setup involves a National Instruments board, however, see below for other implementation ideas. The elements of Figure 1 are as follows:

- Part A: The National instruments card requires a special cable using a peculiar hardware connector. The order of the signal lines are awkward on this cable. Adapter board A sorts the signals out and distributes them to four 8 bit flat ribbon connectors.

- Part B: Cable B has to be constructed combining those four 8 bit flat ribbon cables in one 25 bit and one 7 bit flat ribbon cable. The bit order of this cable

[1]Please send comments, questions, corrections, insults to *meyrath@physics.utexas.edu*

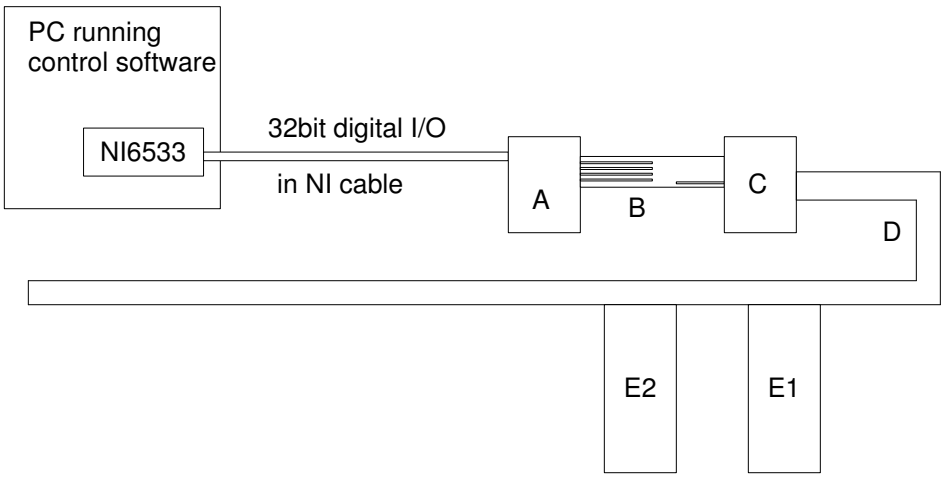


Figure 1: General layout of the control system.

is the obvious one, port A,B,C, and bit 0 of port D go to the 50 pin header (see below) and bits 1 to 7 of port D go to the 7pin header. Signal and ground lines alternate in the flat ribbon cables. The headers must be crimped in the correct orientation on the cable so that bit zero of port A goes to bit 0 of the 25 bit bus and so forth. We used a 50 line flat ribbon cable and an additional 14 line cable next to it.

- Part C is the strobe bit generator and transceiver board. It buffers the NI6533 card signals in addition to producing a time shortened strobe bit signal. The schematic and layout are at the end of this document.

- Part D is the bus system 50 line flat ribbon cable. The pin configuration compatible with our output devices is given below. It is suggested that an additional buffer board be used if the ribbon cable it to travel a long distance.

- Part E1: 16-bit devices.

Concept: The concept of the system is illustrated in Figure 3. The system consists of a 16-bit data bus, an 8-bit address bus, and a clock. The clock is converted into a strobe signal. The strobe commands the device to update its data, see next

section. All 25 bits are sent to all devices but only one accepts the data. Each device has a local 8-bit address which is set on the Printed Circuit Board (PCB) of that device with DIP switches. Only when the input 8-bit address bus matches does the device accept the strobe signal. With this system, one may add up to 2^8 devices onto the bus, one of which is accessed each clock cycle.
The data bus, in fact, may be bidirectional which allows for input data as well. Our buffer/strobe generator board (see below) includes transceiver buffers which can operate bidirectionally. This requires an additional bit in the bus which talks to this board and chooses the data bus direction. In this case, it is the responsibility of the computer to address the appropriate input device. As of this writing, we have not implemented the use of this input option, but it is in principle a simple addition.

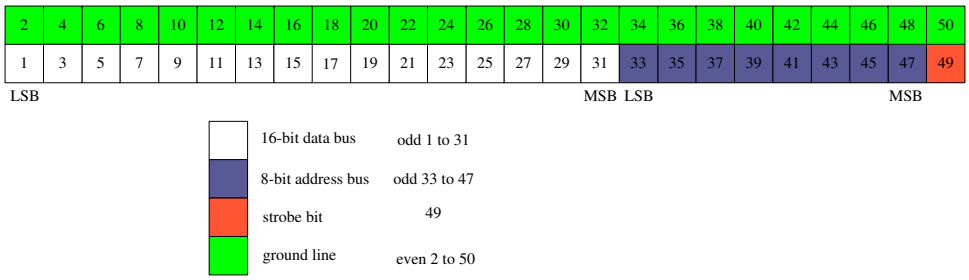


Figure 2: Pin configuration for 50-pin connector.

Why a Strobe? The strobe serves two purposes: increase data rate and signal error protection. Firstly, the data loading implementation in a similar system is typically accomplished in three clock cycles: data input, strobe on, strobe off. This can be improved by using a time shortened pulse for the strobe rather than full clock cycles. The strobe pulse occurs in the center of each clock period and has no dependance on clock state, only state change. Our strobe pulses are typically order 100 ns in length in the middle of the order 2 μs (500 kHz clock) clock periods. This concept, along with out circuit implementation schematic is shown in Figure 4. The figure inset shows a pictorial diagram of the strobe timing.

Computer Output: How the computer actually generates the needed bus bits is flexible. The method we currently use involves a N16533 from National Instruments. This device gives an synchronous 32-bit parallel bus and clock signal which we have typically run between 500 kHz and 750 kHz. Such a fancy device is not totally needed (we used it because we had it). The computer outputs can be produced synchronously using other methods, a few of which we will suggest here in words. One method that could be used is the computer's built-in parallel printer port. This port has an 8-bit parallel I/O and various handshaking bits. In this case, the clock would be put external to the computer along with an 8-bit output FIFO, 24 or 32-bits worth of latches (74LS573) and a few logic chips. The basic idea is to put the asynchronous computer output of the parallel port into the FIFO which is synchronously triggered by the local clock and multiplexed to 24 or 32 bits and latched. The FIFO is First In First Out and consists of a triggered buffer, there are bunches of single

chip FIFOs available. A similar option is to use a USB device such as DLP-USB245M (available from mouser electronics for $25). This device accepts a USB (Universal Serial Bus) connection from the computer and has a built-in synchronous FIFO 8-bit parallel output and would require only a few logic chips and latches to implement. Evidently the manufacturer of this USB-FIFO device provides all the simple codes for programming the device, although we have not used it. The only real disadvantage of these two suggestions to the National Instruments card is the bus speed which may be limited to a few hundred kHz. The two major advantages of these systems are: they are really cheap (order $50) compared to NI cards (order $1500), and secondly, with the printer port or USB port implementation, it is portable to any computer. Another interesting option could be to use a Firewire port and implement it similar to the USB as discussed here if some convenient protocol devices exist. Firewire has the advantage of running at 300Mbps (так быстро!).

Example Devices: Our goal here is flexible laboratory electronics. A common laboratory implementation uses BNC type outputs which connect devices under computer control to the real-world experimental (analog) devices. Typically, desired computer output comes in the form of lone digital trigger signals and analog signals. We, therefore, have built two device types for this bus system. The first is a simple buffered set of digital outputs. In this case a single '16-bit device' as discussed in Figure 3 consists of 16 latched digital outputs equipped with line drivers. The second device type is analog. In this design, we use some very nice modern 16-bit DAC ICs. Here, a single analog line is a 16-bit device. Our design for this includes 8 analog outputs on a single PCB, each of which has a full -10 to +10 V range and 16 bit accuracy as well as 1/4 A line driving capacity. Schematics, layouts and detailed descriptions for both of these device types are available at the web site:
`george.ph.utexas.edu/~control`

Because of the generality of this system, one could easily make other output devices such as DDS type radio frequency generators, etc. Additionally, as discussed before, ADC's could be added using the input mode of the data bus.

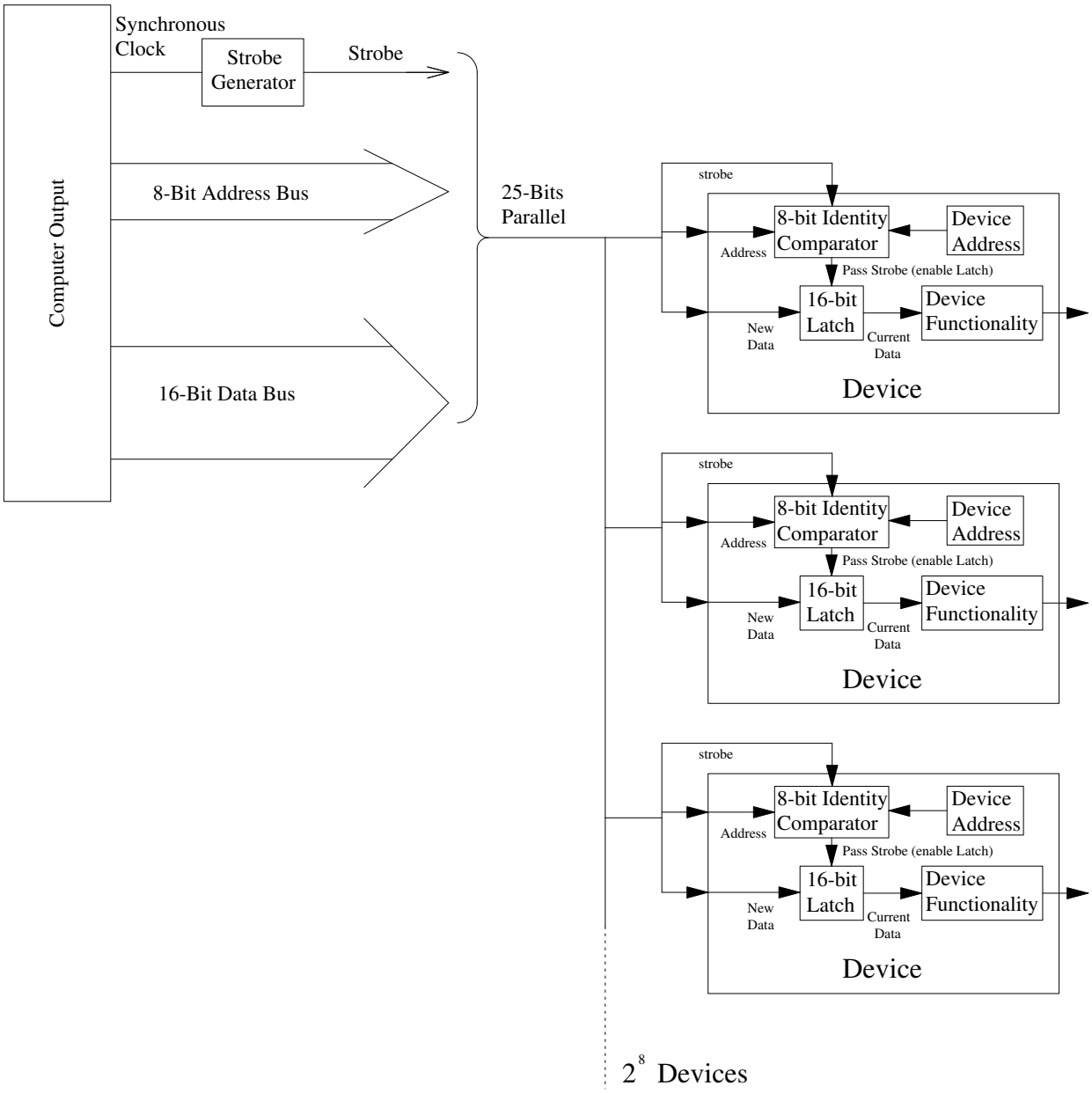
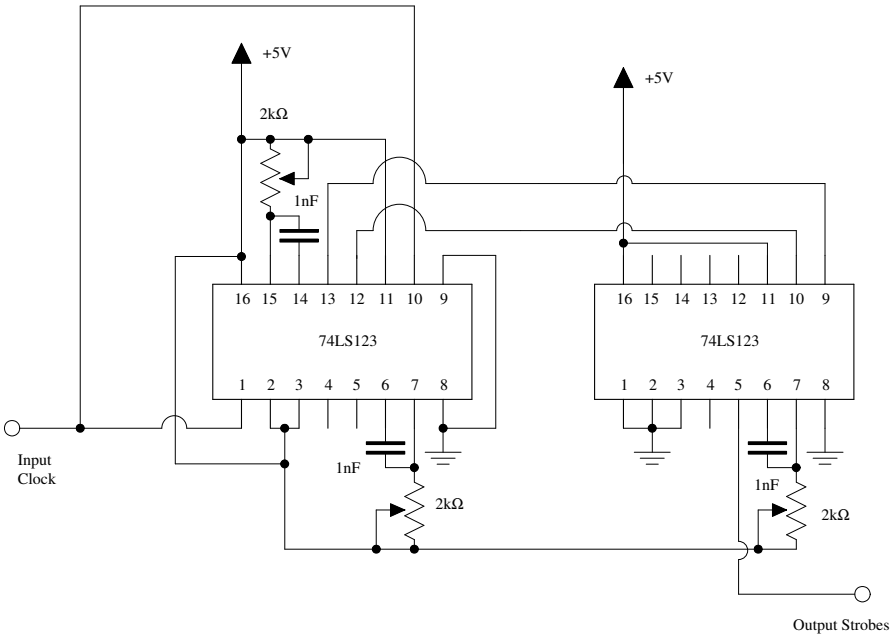
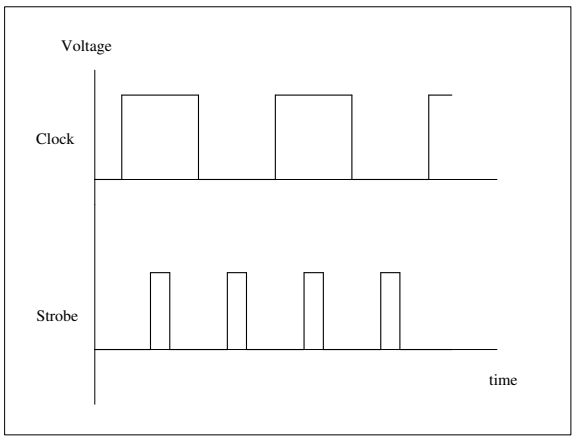


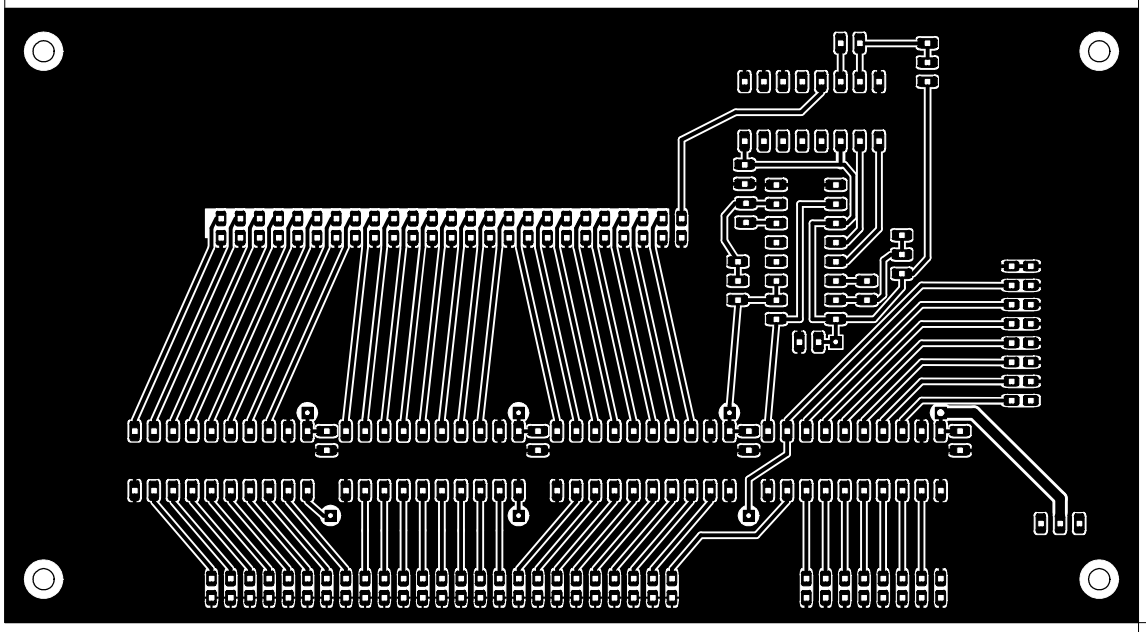
Figure 3: Output Concept. Each 16-bit device has its own 8-bit address which typically may be set locally with DIP switches. All devices receive all 25 bits on each clock cycle, but only the device with matching address accepts the strobe bit which commands it to take the new data.

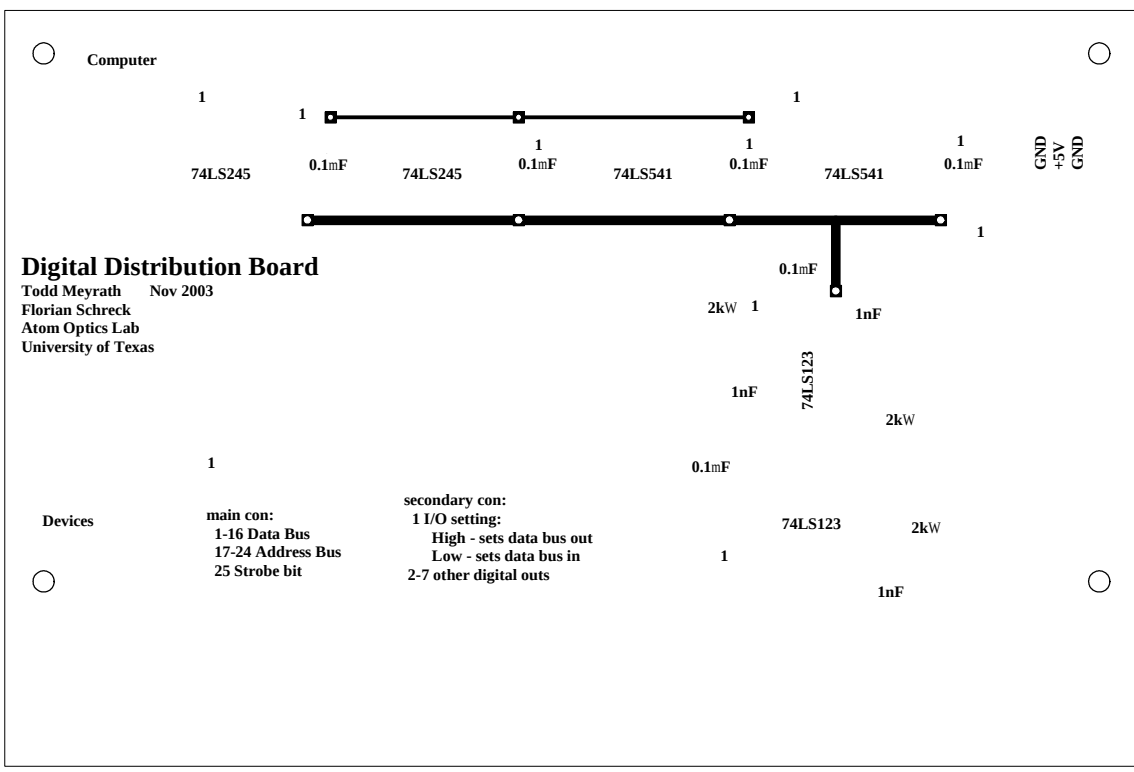




Triple Data Rate Strobe

Figure 4: Strobe Generator. Note, that the strobe bit can be high or low active (switching output pins 12 to 5). In this design, we have chosen it to be high because that is the logic used on our digital output board designs. Please note in the case of the analog output board, that the active strobe may be chosen to be high or low. Which is to say, for using this strobe generator design, the analog output boards must always have the DIP switch set to properly accept a high strobe. See documentation on the digital and analog output board designs.





Digital Distribution Board

Todd Meyrath **Nov 2003**
Florian Schreck
Atom Optics Lab
University of Texas

Bus buffer, strobe generator and NI6533 adapter board

Gerhard Hendl, Florian Schreck and Todd Meyrath

This board provides several functions: it is an adapter between the NI6533 cable and the 50 pin header of the bus system, it can generate a strobe signal and it can have input lines for the NI6533 external clock and trigger. It can also be used just as a signal refreshing board within the 50 pin bus cable. It is possible to add zener diodes between the bus signal lines and ground to improve the signal quality. The remaining normally unused 7 bits of the NI6533 are available on a independent connecter. Those bits can for example be used in conjunction with an address decoder chip to put the strobe signal to the bus only if a certain bit pattern appears on these higher seven bits. In that way it is possible to use more than 256 different addresses. Or these bits can be used as additional digital outputs.

This board was designed by Gerhard Hendl of the institute for quantumoptics and quantuminformation of the Austrian academy of sciences at Innsbruck (gerhard.hendl at oeaw.ac.at).

P1
Header 8X2

P2
Header 25X2

P3
Header 8X2

P4
Header 3

P5
Header 25X2

P6
Header 8X2

P7
Header 2

P8
Header 2

P9
Header 2

P10
Header 25X2

P11
Header 8X2

J1
3-174682-7

U1 M74HCT541B1R
U2 M74HCT541B1R
U3 M74HCT541B1R
U4 M74HCT541B1R
U5 M74HCT541B1R

U6A M74HC123AB1R
U6B M74HC123AB1R
U7A M74HC123AB1R
U7B M74HC123AB1R

U8 L7805AB-V

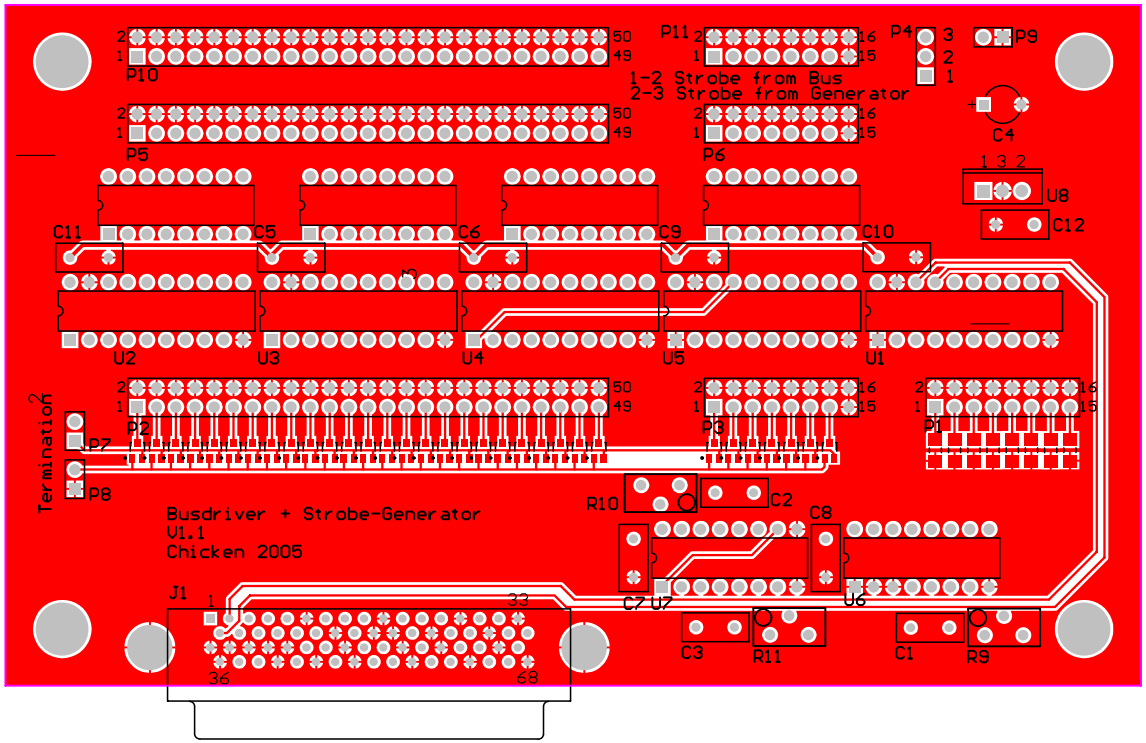
R1 Res2
R2 Res2
R3 Res2
R4 Res2
R5 Res2
R6 Res2
R7 Res2
R8 Res2
R9 RPot 2k
R10 RPot 2k
R11 RPot 2k

R15A Res Pack2
R15B Res Pack2
R15C Res Pack2
R15D Res Pack2

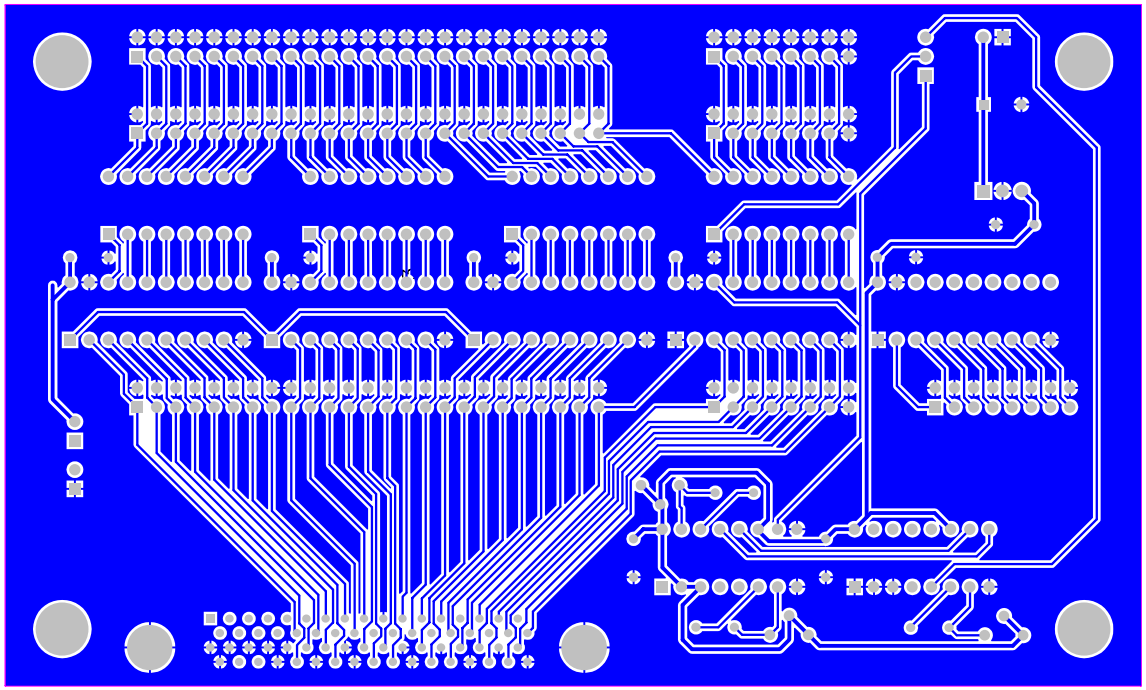
C1 Cap 100pF
C2 Cap 470pF
C3 Cap 470pF
C4 Cap Pol1 220uF
C5 Cap 0.1uF
C6 Cap 0.1uF
C7 Cap 0.1uF
C8 Cap 0.1uF
C9 Cap 0.1uF
C10 Cap 0.1uF
C11 Cap 0.1uF
C12 Cap 0.1uF

D1 D2 D3 D4 D5 D6 D7 D8 D9 D10 D11 D12 D13 D14 D15 D16 D17 D18 D19 D20 D21 D22 D23 D24
1PS70SB14
D25 D26 D27 D28 D29 D30 D31 D32
1PS70SB14

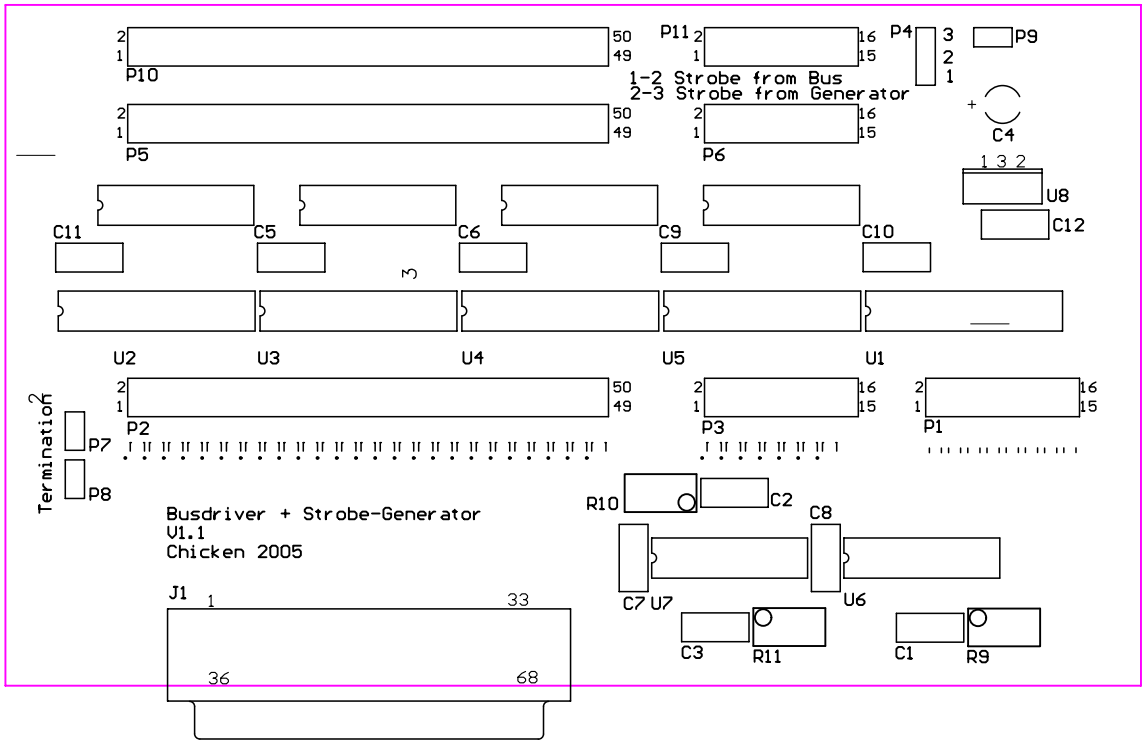
Title	Adapterkarte 68-50polig mit Strobegenerator	
Size A3	Number	Revision
Date: 12.08.2005	Sheet of	
File: E:\projekte\..\Strobe 68-50 V3.SchDoc	Drawn By:	



Altium Limited 12a Rodborough Rd Frenchs Forest NSW 2086	ENGINEER:	TITLE: Adapterkarte 68-50 polig mit Strobegenerator Top Layer	
	PCB DESIGNER:		
	DATE: 15.07.2005	PART NO.:	REV:
	FILE NAME: Strobe 68-50 V3GNDplane.PcbDoc	DWG NO:	SCALE:



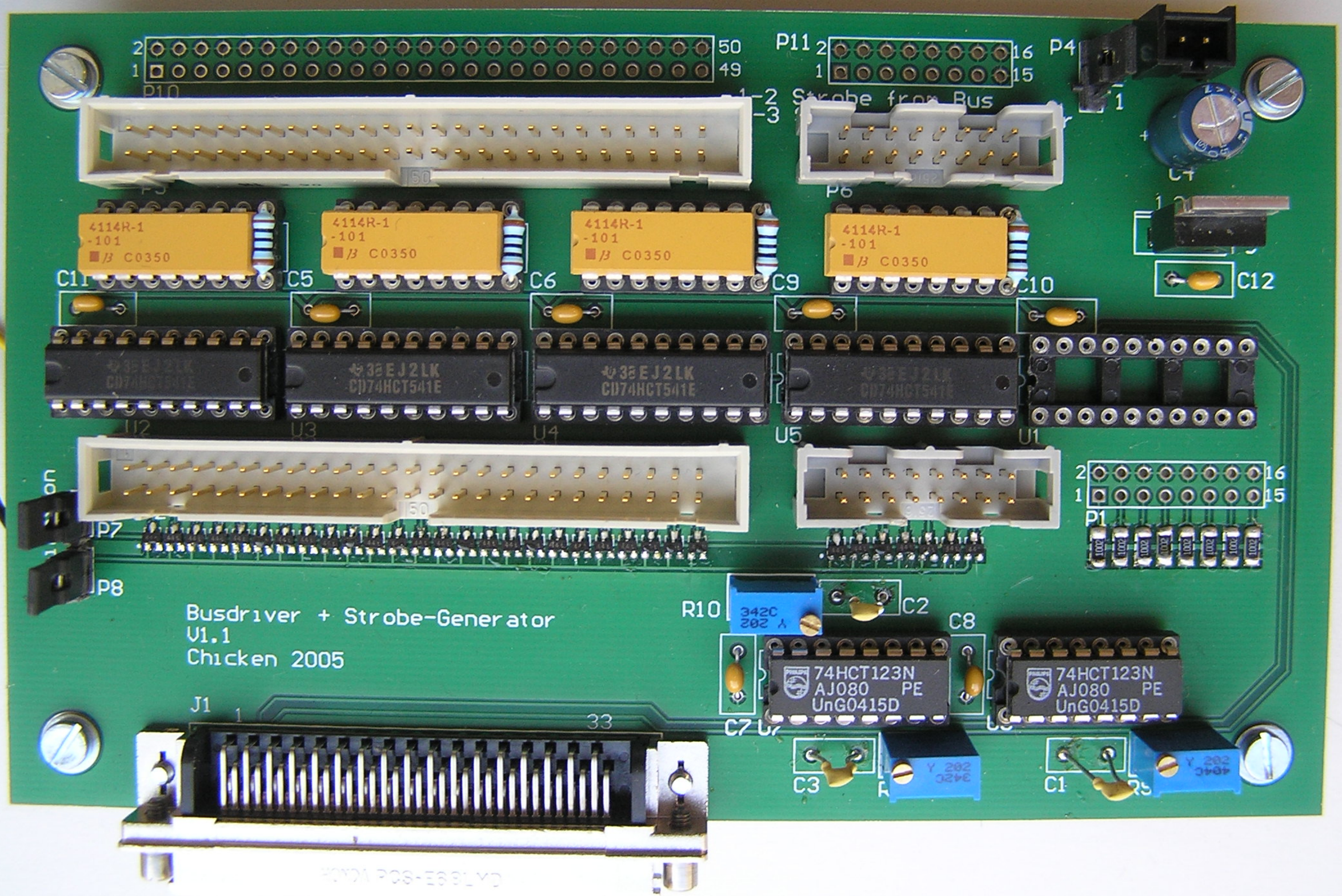
Altium Limited 12a Rodborough Rd Frenchs Forest NSW 2086	ENGINEER:	TITLE: Adapterkarte 68-50 polig mit Strobegenerator Bottom Layer	
	PCB DESIGNER:		
	DATE: 15.07.2005	PART NO.:	REV:
	FILE NAME: Strobe 68-50 V3GNDplane.PcbDoc	DWG NO:	SCALE:



Altium Limited 12a Rodborough Rd Frenchs Forest NSW 2086	ENGINEER:	TITLE: Adapterkarte 68-50 polig mit Strobegenerator Top Silkscreen Overlay	
	PCB DESIGNER:		
	DATE: 15.07.2005	PART NO.:	REV:
	FILE NAME: Strobe 68-50 V3GNDplane.PcbDoc	DWG NO:	SCALE:

Designator	Description	Value	LibRef	Footprint
C1	Capacitor	100pF	Cap	RAD-0.2
C2	Capacitor	470pF	Cap	RAD-0.2
C3	Capacitor	470pF	Cap	RAD-0.2
C4	Polarized Capacitor (Radial)	220uF	Cap Pol1	CAPPR5-5x5
C5	Capacitor	0.1uF	Cap	RAD-0.2
C6	Capacitor	0.1uF	Cap	RAD-0.2
C7	Capacitor	0.1uF	Cap	RAD-0.2
C8	Capacitor	0.1uF	Cap	RAD-0.2
C9	Capacitor	0.1uF	Cap	RAD-0.2
C10	Capacitor	0.1uF	Cap	RAD-0.2
C11	Capacitor	0.1uF	Cap	RAD-0.2
C12	Capacitor	0.1uF	Cap	RAD-0.2
D1	Schottky Barrier Double Diode		1PS70SB14	SOT323
D2	Schottky Barrier Double Diode		1PS70SB14	SOT323
D3	Schottky Barrier Double Diode		1PS70SB14	SOT323
D4	Schottky Barrier Double Diode		1PS70SB14	SOT323
D5	Schottky Barrier Double Diode		1PS70SB14	SOT323
D6	Schottky Barrier Double Diode		1PS70SB14	SOT323
D7	Schottky Barrier Double Diode		1PS70SB14	SOT323
D8	Schottky Barrier Double Diode		1PS70SB14	SOT323
D9	Schottky Barrier Double Diode		1PS70SB14	SOT323
D10	Schottky Barrier Double Diode		1PS70SB14	SOT323
D11	Schottky Barrier Double Diode		1PS70SB14	SOT323
D12	Schottky Barrier Double Diode		1PS70SB14	SOT323
D13	Schottky Barrier Double Diode		1PS70SB14	SOT323
D14	Schottky Barrier Double Diode		1PS70SB14	SOT323
D15	Schottky Barrier Double Diode		1PS70SB14	SOT323
D16	Schottky Barrier Double Diode		1PS70SB14	SOT323
D17	Schottky Barrier Double Diode		1PS70SB14	SOT323
D18	Schottky Barrier Double Diode		1PS70SB14	SOT323
D19	Schottky Barrier Double Diode		1PS70SB14	SOT323
D20	Schottky Barrier Double Diode		1PS70SB14	SOT323
D21	Schottky Barrier Double Diode		1PS70SB14	SOT323
D22	Schottky Barrier Double Diode		1PS70SB14	SOT323
D23	Schottky Barrier Double Diode		1PS70SB14	SOT323
D24	Schottky Barrier Double Diode		1PS70SB14	SOT323
D25	Schottky Barrier Double Diode		1PS70SB14	SOT323
D26	Schottky Barrier Double Diode		1PS70SB14	SOT323
D27	Schottky Barrier Double Diode		1PS70SB14	SOT323
D28	Schottky Barrier Double Diode		1PS70SB14	SOT323
D29	Schottky Barrier Double Diode		1PS70SB14	SOT323
D30	Schottky Barrier Double Diode		1PS70SB14	SOT323
D31	Schottky Barrier Double Diode		1PS70SB14	SOT323
D32	Schottky Barrier Double Diode		1PS70SB14	SOT323
J1	Plug Assembly, Horizontal with Kink		3-174682-7	3-174682-7
P1	Header, 8-Pin, Dual row		Header 8X2	HDR2X8
P2	Header, 25-Pin, Dual row		Header 25X2	HDR2X25
P3	Header, 8-Pin, Dual row		Header 8X2	HDR2X8
P4	Header, 3-Pin		Header 3	HDR1X3
P5	Header, 25-Pin, Dual row		Header 25X2	HDR2X25
P6	Header, 8-Pin, Dual row		Header 8X2	HDR2X8
P7	Header, 2-Pin		Header 2	HDR1X2
P8	Header, 2-Pin		Header 2	HDR1X2
P9	Header, 2-Pin		Header 2	HDR1X2

P10	Header, 25-Pin, Dual row		Header 25X2	HDR2X25
P11	Header, 8-Pin, Dual row		Header 8X2	HDR2X8
R1	Resistor	10K	Res2	cr3216-1206
R2	Resistor	10K	Res2	cr3216-1206
R3	Resistor	10K	Res2	cr3216-1206
R4	Resistor	10K	Res2	cr3216-1206
R5	Resistor	10K	Res2	cr3216-1206
R6	Resistor	10K	Res2	cr3216-1206
R7	Resistor	10K	Res2	cr3216-1206
R8	Resistor	10K	Res2	cr3216-1206
R9	Potentiometer	2k	RPot	rpot3
R10	Potentiometer	2k	RPot	rpot3
R11	Potentiometer	2k	RPot	rpot3
R12	Isolated Resistor Network - Parts	1K	Res Pack2	DIP-16
R13	Isolated Resistor Network - Parts	1K	Res Pack2	DIP-16
R14	Isolated Resistor Network - Parts	1K	Res Pack2	DIP-16
R15	Isolated Resistor Network - Parts	1K	Res Pack2	DIP-16
U1	Octal Bus Buffer with 3 State Outputs		M74HCT541B1R	DIP20
U2	Octal Bus Buffer with 3 State Outputs		M74HCT541B1R	DIP20
U3	Octal Bus Buffer with 3 State Outputs		M74HCT541B1R	DIP20
U4	Octal Bus Buffer with 3 State Outputs		M74HCT541B1R	DIP20
U5	Octal Bus Buffer with 3 State Outputs		M74HCT541B1R	DIP20
U6	Dual Retriggerable Monostable Multivibrator		M74HC123AB1R	DIP16
U7	Dual Retriggerable Monostable Multivibrator		M74HC123AB1R	DIP16
U8	Precision 1A Regulator		L7805AB-V	TO220ABN


P10
P11
P4
P3
P6
P7
P8
P1
J1
U2
U3
U4
U5
U1
C11
C5
C6
C9
C10
C12
C7
C8
C3
C1
R10
4114R-1
-101
C0350
CD74HCT541E
74HCT123N
AJ080 PE
UnG0415D
Busdriver + Strobe-Generator
V1.1
Chicken 2005