



UNIVERSIDAD
DE GRANADA



Sistemas con Microprocesadores

Microcontroladores avanzados:

ATmega2560

Familia:

ATmega640/V-1280/V-1281/V-2560/V-2561/V

- Arquitectura del procesador: AVR de 8 bits

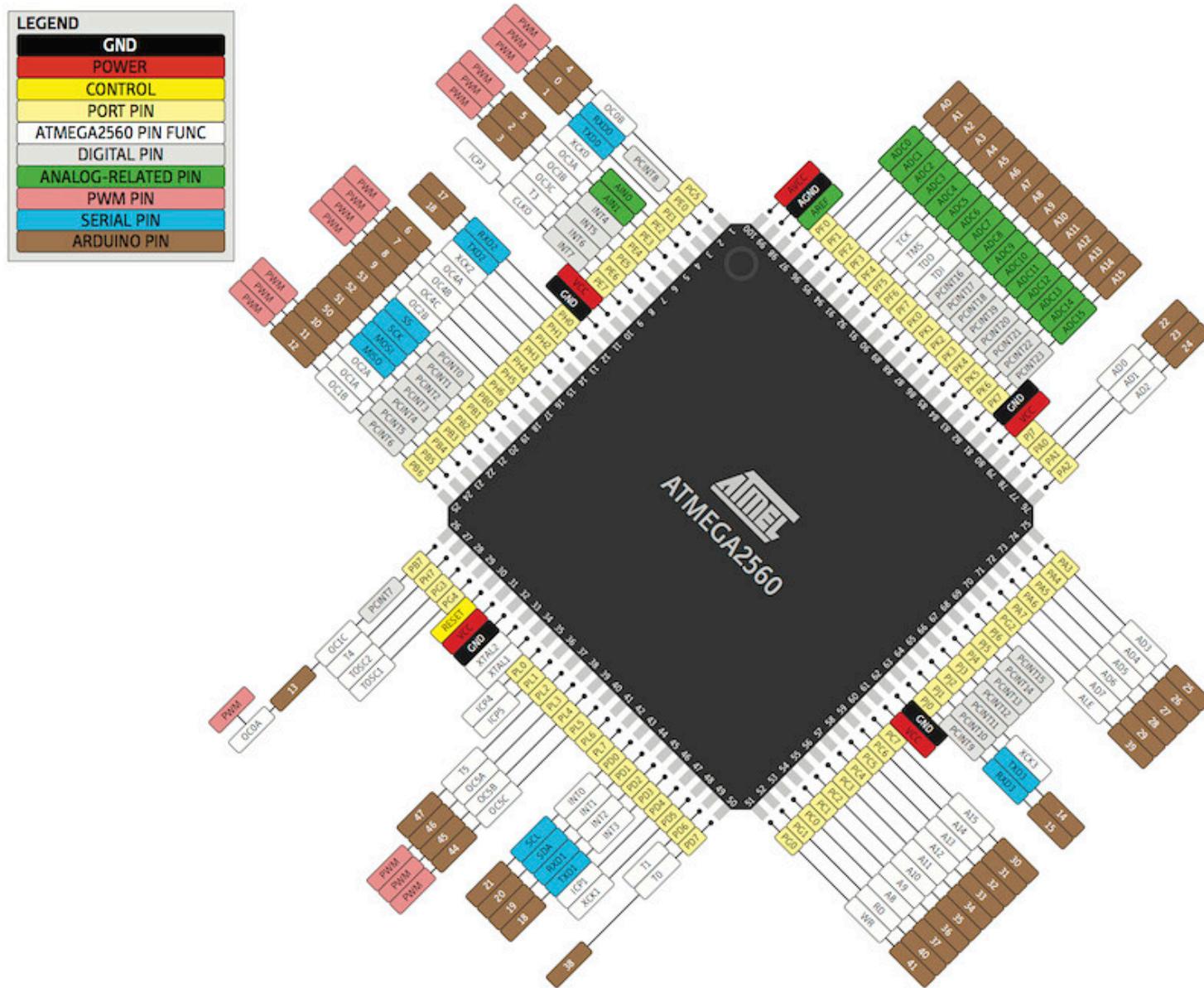
Comparison Between ATmega1281/2561 and ATmega640/1280/2560

Each device in the ATmega640/1280/1281/2560/2561 family differs only in memory size and number of pins. [Table 2-1](#) summarizes the different configurations for the six devices.

Table 2-1. Configuration Summary

Device	Flash	EEPROM	RAM	General Purpose I/O pins	16 bits resolution PWM channels	Serial USARTs	ADC Channels
ATmega640	64KB	4KB	8KB	86	12	4	16
ATmega1280	128KB	4KB	8KB	86	12	4	16
ATmega1281	128KB	4KB	8KB	54	6	2	8
ATmega2560	256KB	4KB	8KB	86	12	4	16
ATmega2561	256KB	4KB	8KB	54	6	2	8

ATmega2560 pinout



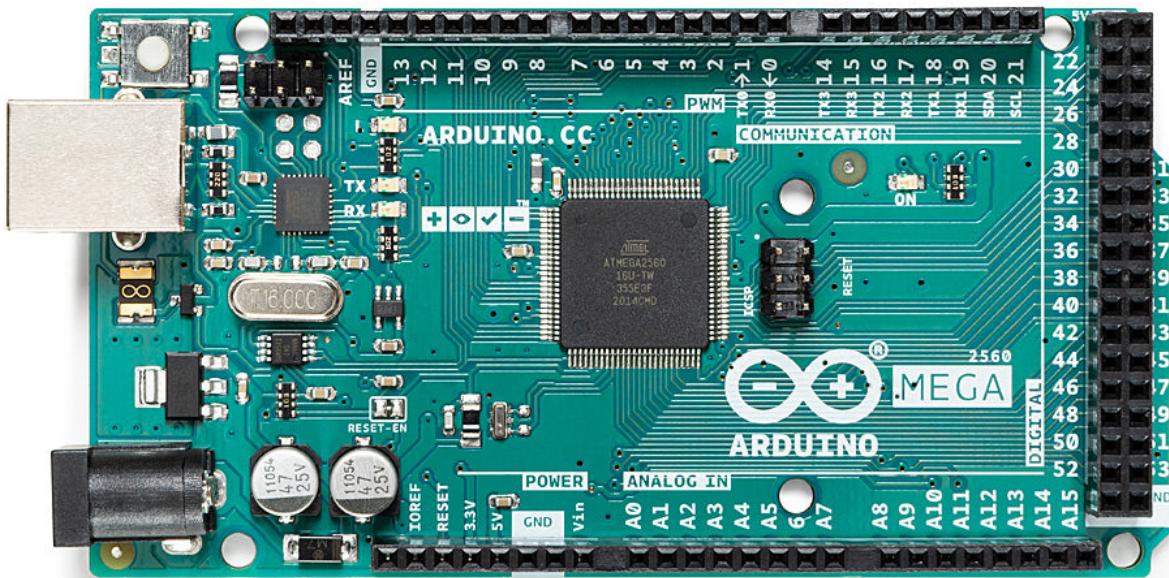
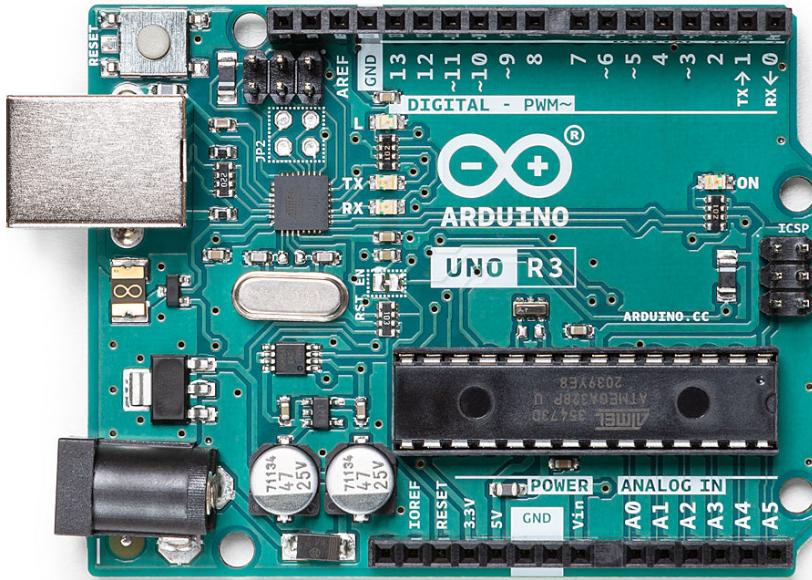
Características ATmega2560

Parámetro	Atmega2560	ATmega328P
Tipo de procesador	AVR de 8 bits	AVR de 8 bits
Rendimiento	16 MIPS a 16 MHz	20 MIPS a 20 MHz
Memoria Flash	256 KB	32 KB
SRAM	8 KB	2 KB
EEPROM	4 KB	1 KB
Encapsulado	100 TQFP (64 en otro)	28 PDIP (32 en otro)
Máxima frecuencia	16 MHz	20 MHz
Número de canales táctiles	64	16
Circuitería QTouch Acquisition	Yes	No
Máximo núm. de patillas de E/S	86	23
Fuentes de interrup. (externas)	57 (8)	25 (2)
Interfaz USB	No	No
Velocidad USB	—	—

Data Retention

Reliability Qualification results show that the projected data retention failure rate is much less than 1 PPM over 20 years at 85°C or 100 years at 25°C.

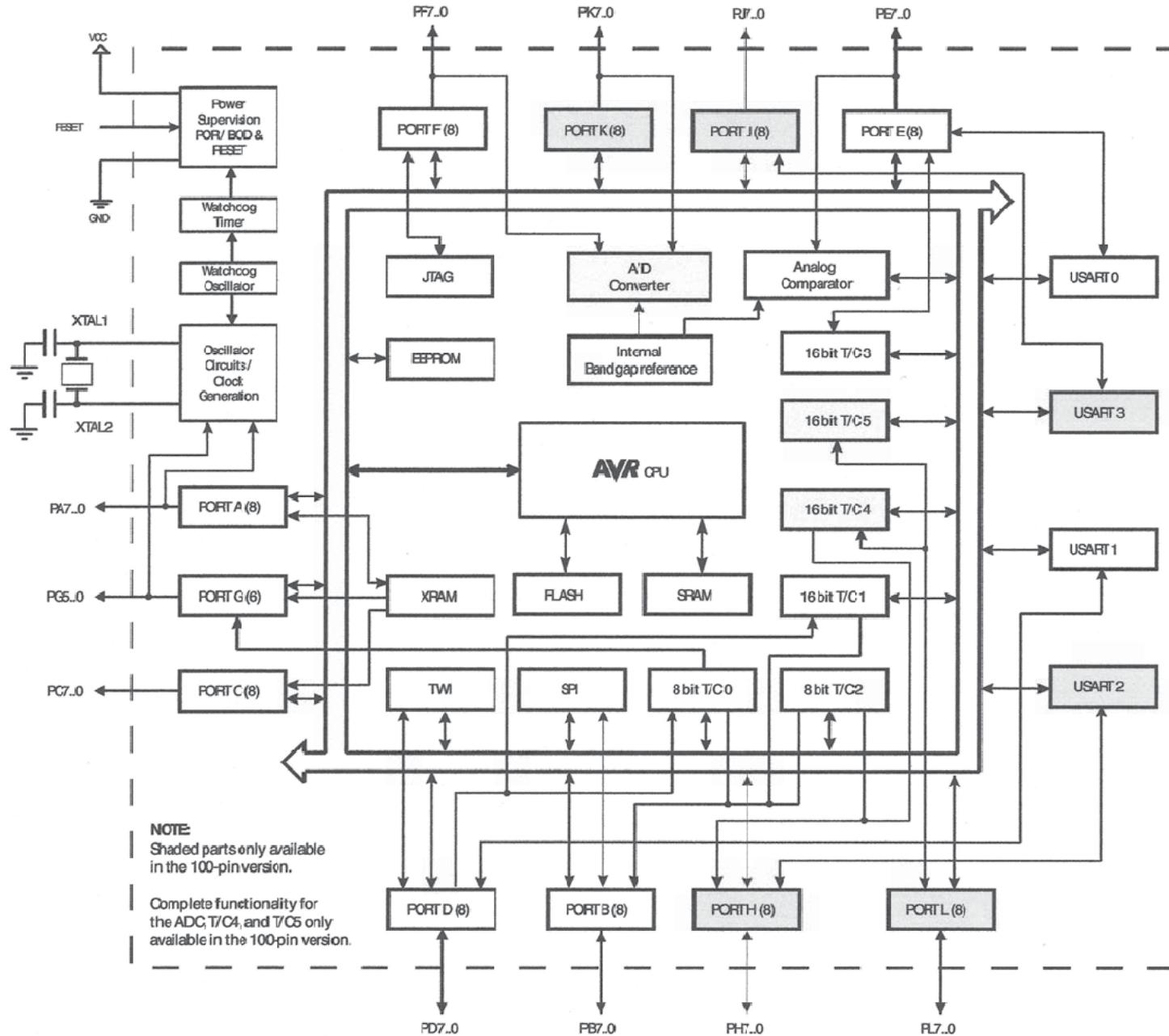
ATmega en placas Arduino



Encapsulados

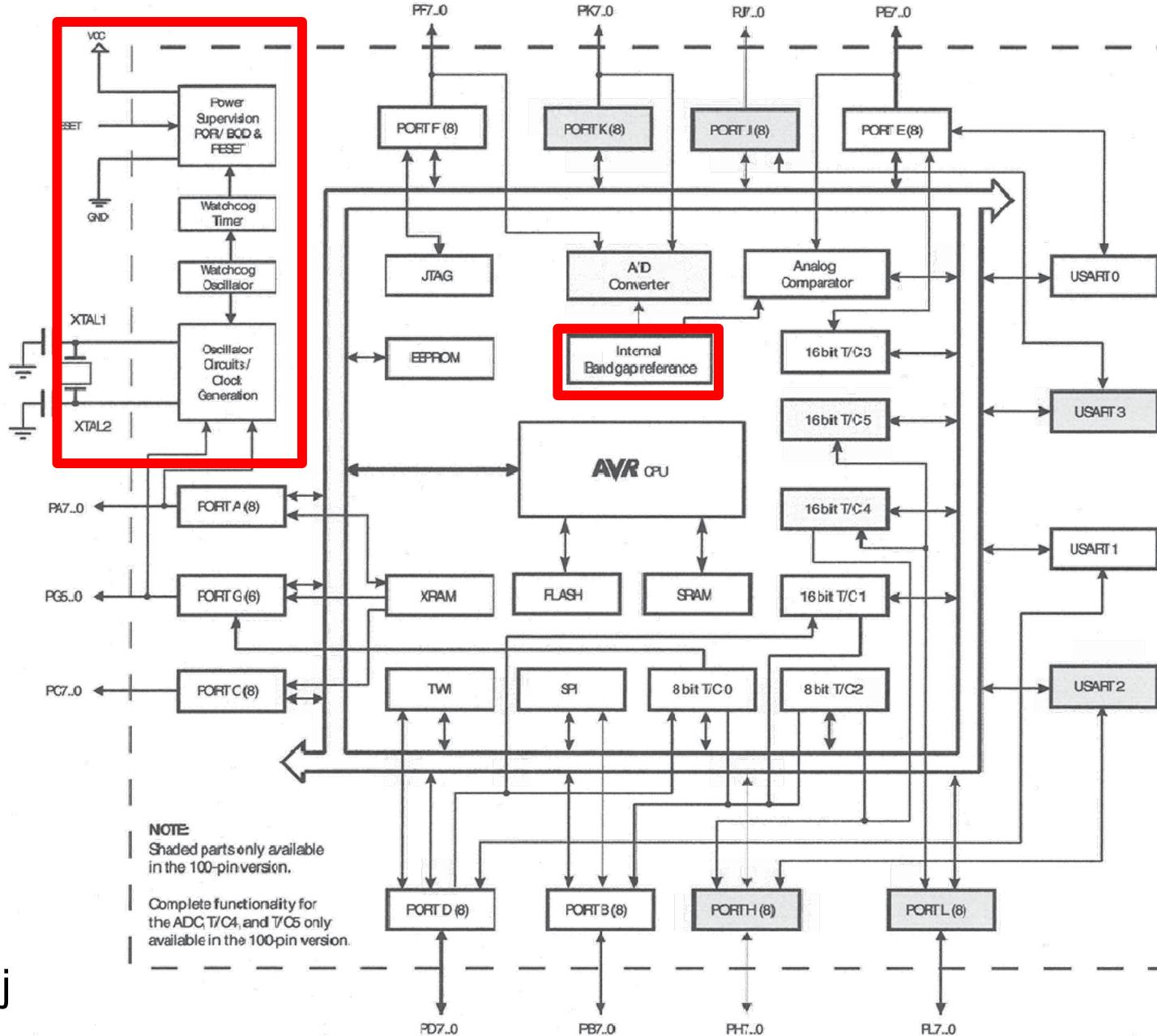
- Arduino UNO:
 - Atmega328P -> PDIP (*Plastic Dual In-Line Package*)
- Arduino MEGA:
 - Atmega2560 -> TQFP (*Thin profile Quad Flat Package*)

Arquitectura ATmega2560



Arquitectura ATmega2560

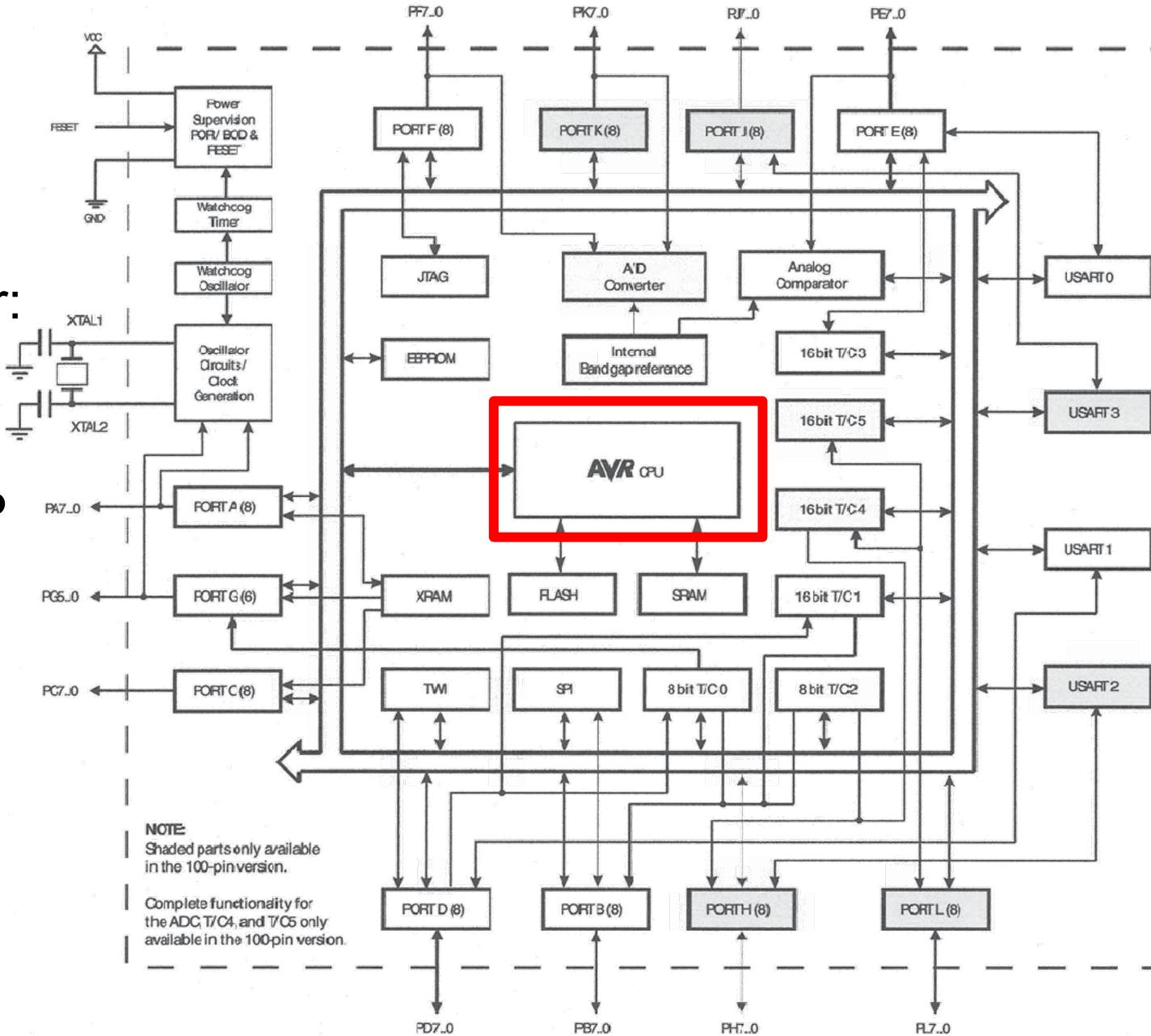
- Alimentación:
 - POR:
Power-on Reset
 - BOD:
Brown-out detector
 - Reset
 - Referencia de voltaje interna:
Bandgap
- Perro guardián (*watch dog*)
- Oscilador y generador de señales de reloj



Arquitectura ATmega2560

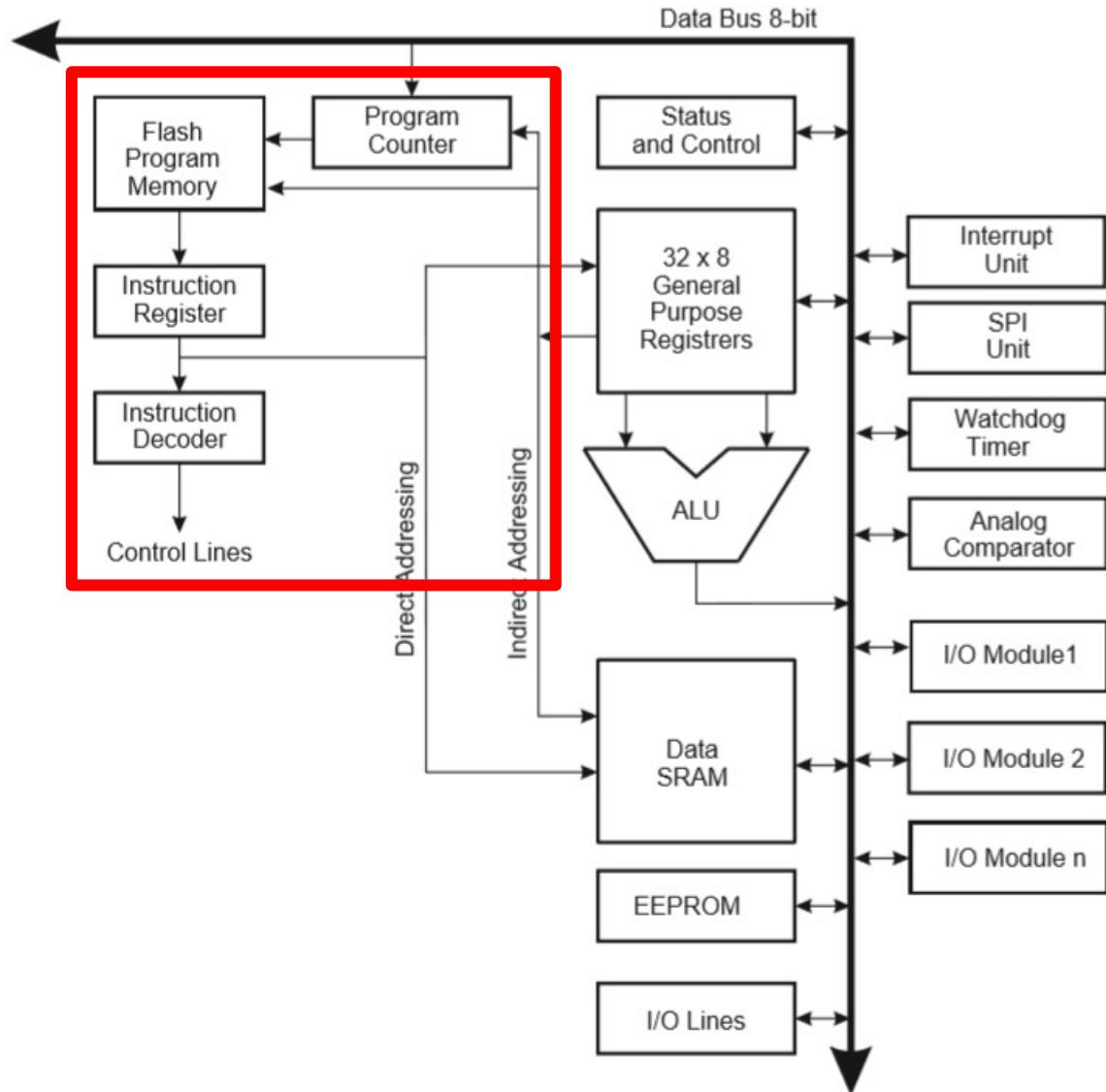
- Núcleo del procesador:

Igual que en ATmega328P



AVR CPU

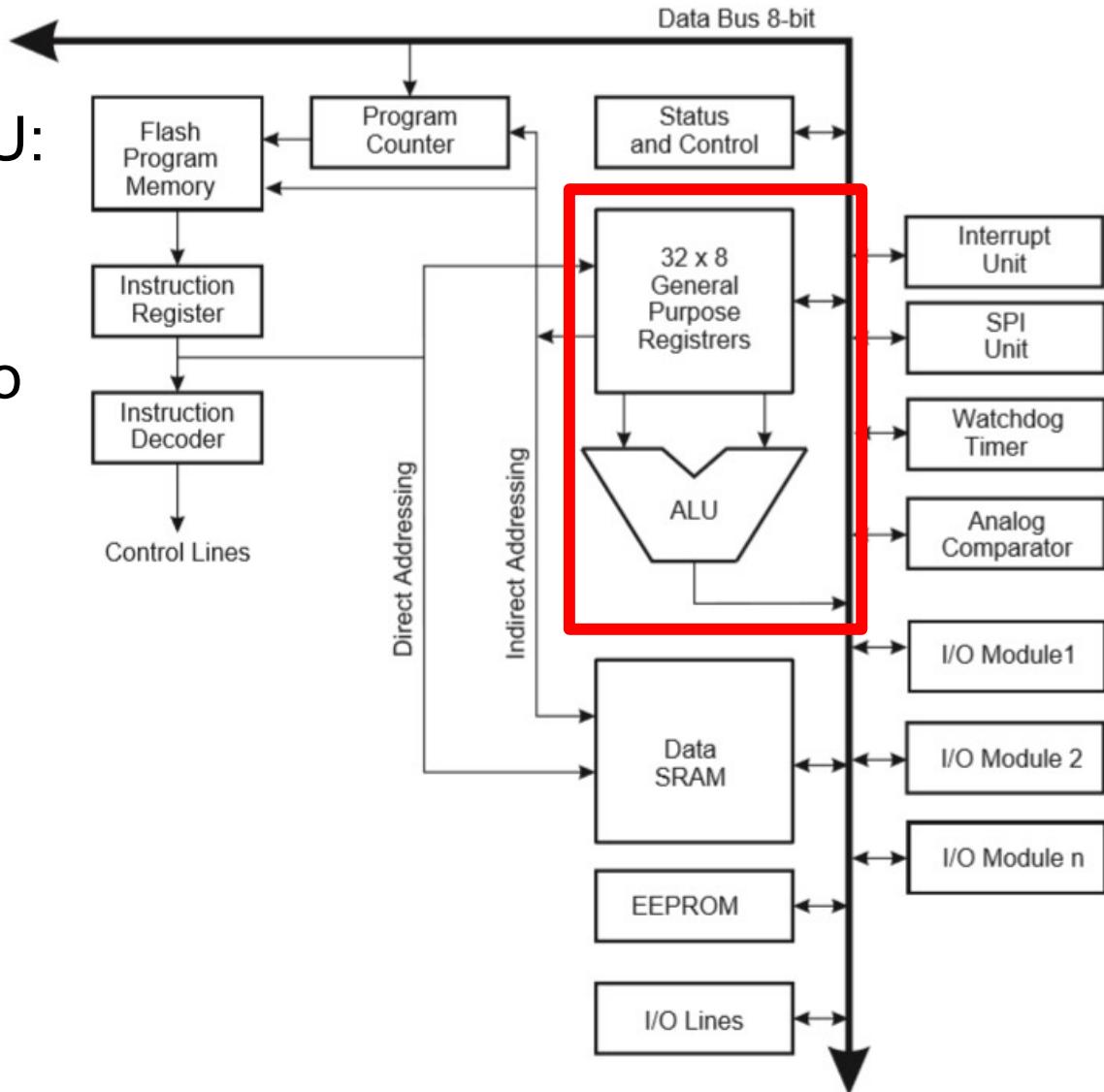
- Captación y decodificación de instrucción



AVR CPU

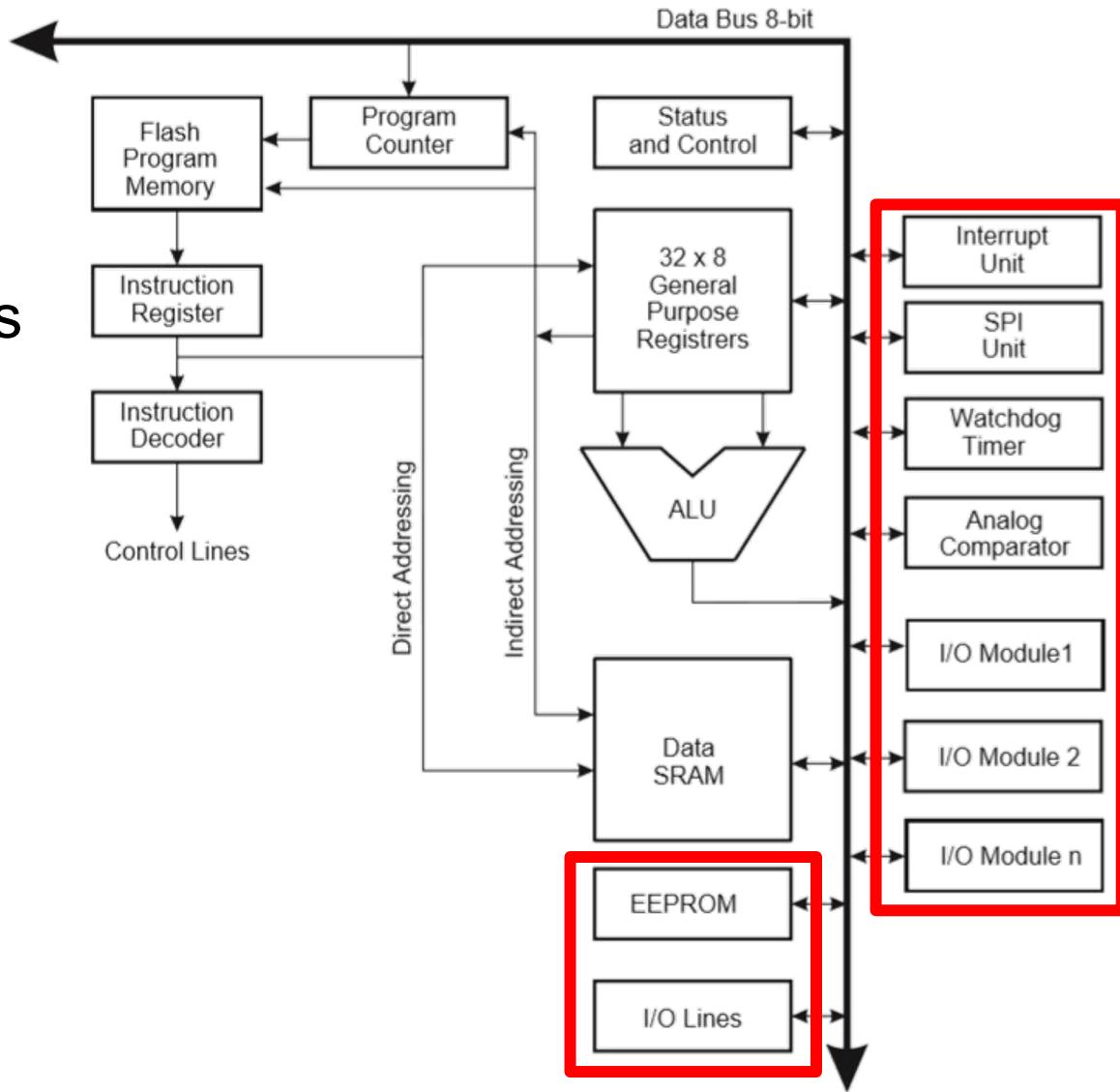
Operaciones con la ALU:

- Generalmente los operandos están en registros de propósito general (GPR)



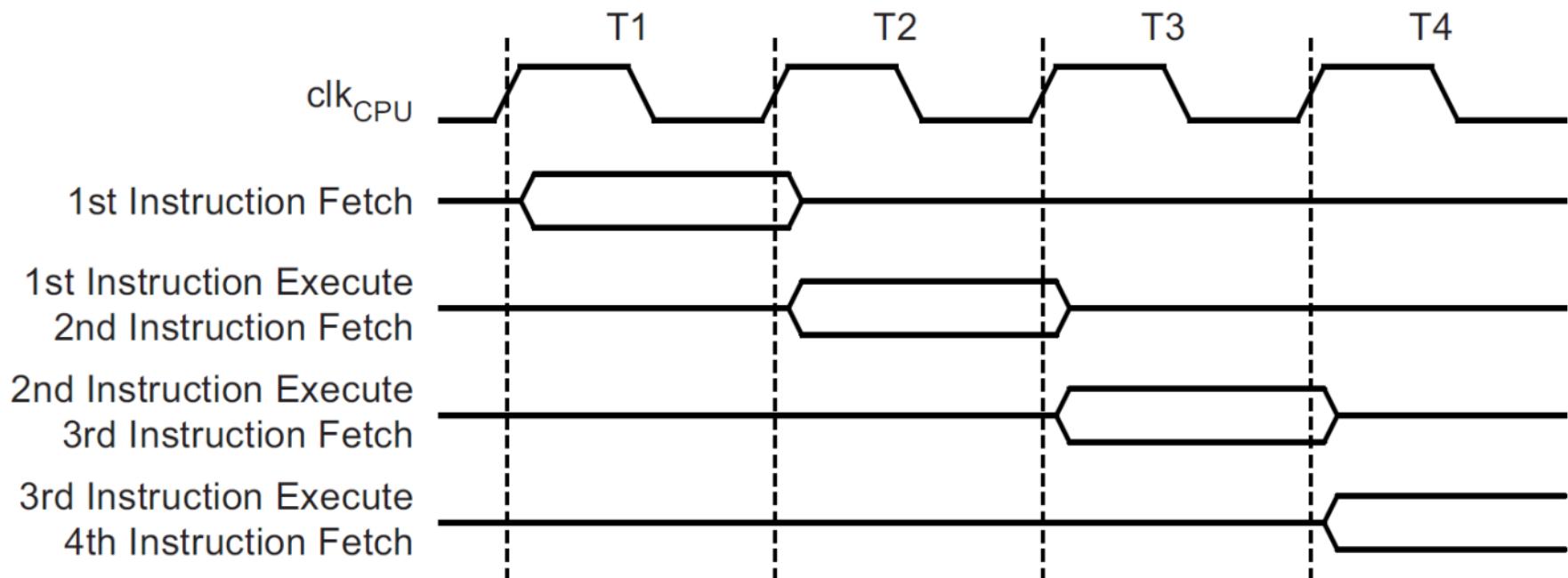
AVR CPU

- Entradas/Salidas
- Funciones especiales



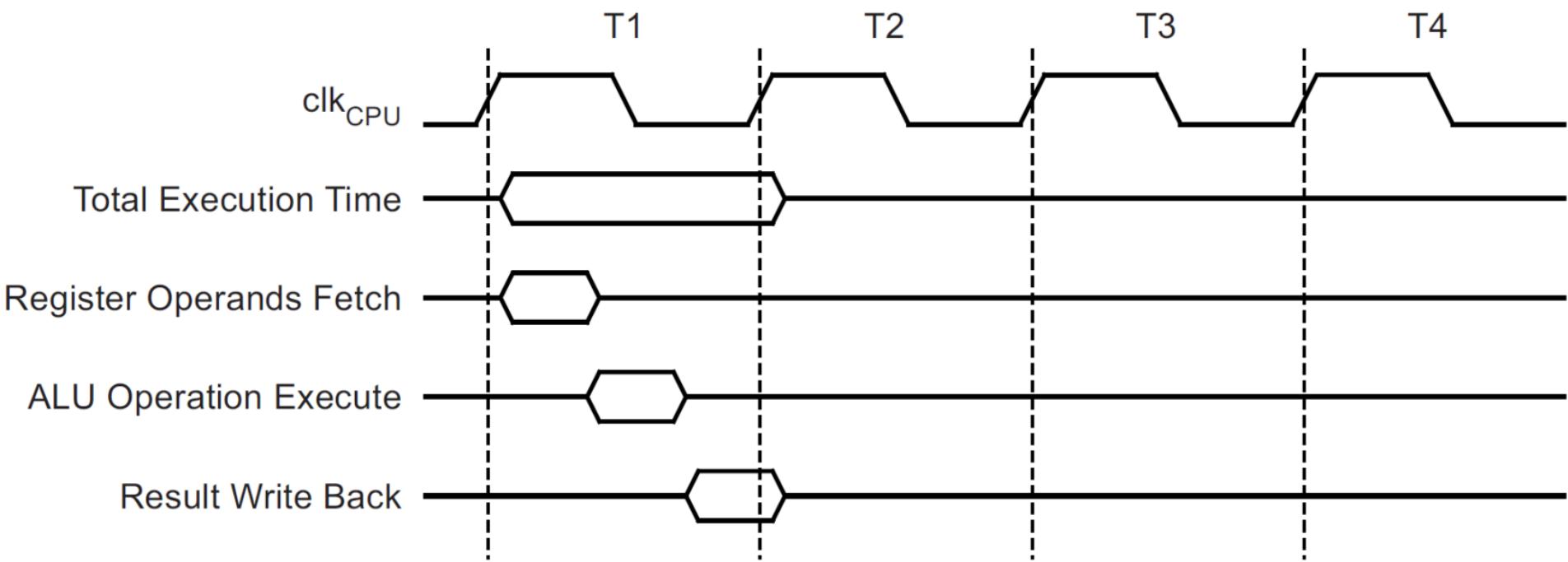
Segmentación de cauce

- 2 etapas



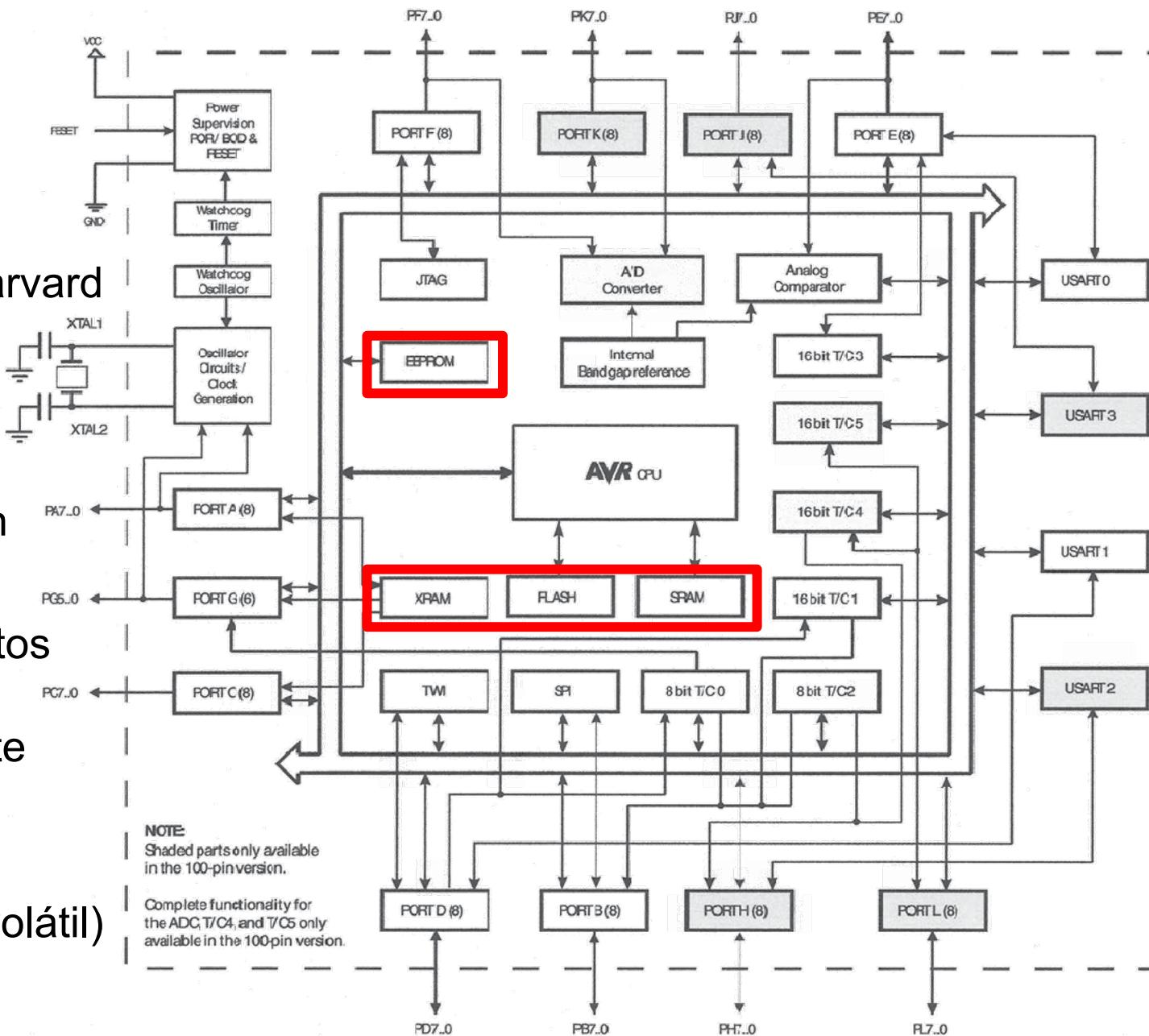
Ciclo de instrucción

- CPI (ciclos por instrucción) = 1 \rightarrow MHz \equiv MIPS



Arquitectura ATmega2560

- Arquitectura Harvard



- Memoria de programa Flash

- Memoria de datos
SRAM
(+opcionalmente eXternal RAM)

- EEPROM (no volátil)

Organización de las memorias

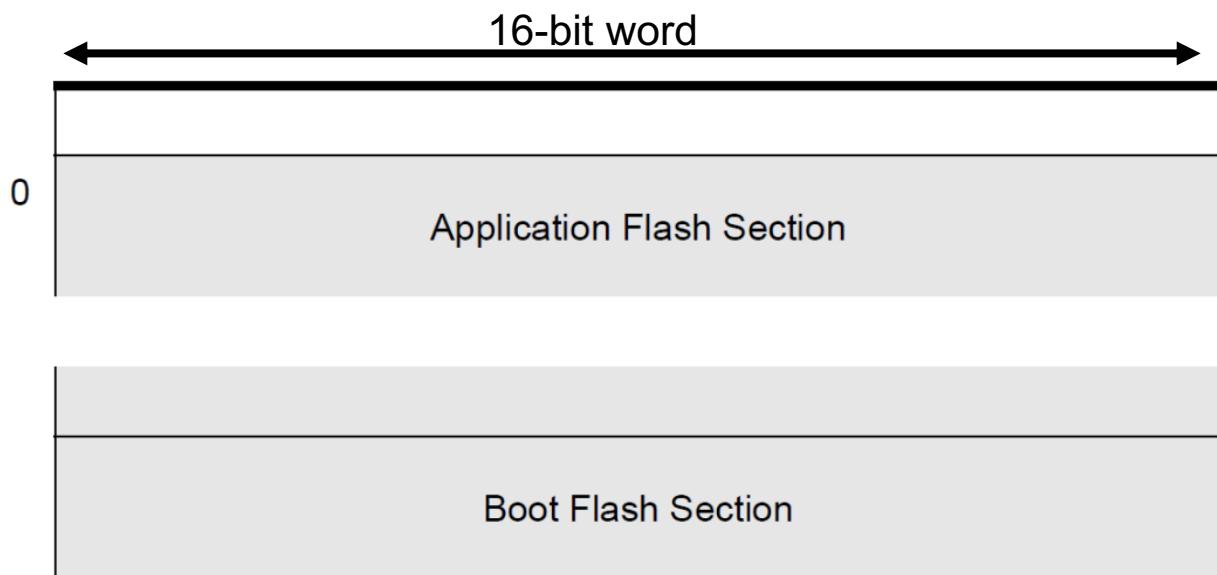
- Memoria de programa
- Al menos 10.000 ciclos R/W

Program Flash Memory Map

Address (HEX)

17-bit
word
address
(PC)

0x1FFF



Organización de las memorias

□ Direcciones especiales: vectores de *reset* e interrupciones

Vector No.	Program Address ⁽²⁾	Source	Interrupt Definition
1	\$0000 ⁽¹⁾	RESET	External Pin, Power-on Reset, Brown-out Reset, Watchdog Reset, and JTAG AVR Reset
2	\$0002	INT0	External Interrupt Request 0
3	\$0004	INT1	External Interrupt Request 1
4	\$0006	INT2	External Interrupt Request 2
5	\$0008	INT3	External Interrupt Request 3
6	\$000A	INT4	External Interrupt Request 4
7	\$000C	INT5	External Interrupt Request 5
8	\$000E	INT6	External Interrupt Request 6
9	\$0010	INT7	External Interrupt Request 7
10	\$0012	PCINT0	Pin Change Interrupt Request 0
11	\$0014	PCINT1	Pin Change Interrupt Request 1
12	\$0016 ⁽³⁾	PCINT2	Pin Change Interrupt Request 2
13	\$0018	WDT	Watchdog Time-out Interrupt
14	\$001A	TIMER2 COMPA	Timer/Counter2 Compare Match A
15	\$001C	TIMER2 COMPB	Timer/Counter2 Compare Match B
16	\$001E	TIMER2 OVF	Timer/Counter2 Overflow
17	\$0020	TIMER1 CAPT	Timer/Counter1 Capture Event
18	\$0022	TIMER1 COMPA	Timer/Counter1 Compare Match A
19	\$0024	TIMER1 COMPB	Timer/Counter1 Compare Match B
20	\$0026	TIMER1 COMPC	Timer/Counter1 Compare Match C
21	\$0028	TIMER1 OVF	Timer/Counter1 Overflow
22	\$002A	TIMER0 COMPA	Timer/Counter0 Compare Match A
23	\$002C	TIMER0 COMPB	Timer/Counter0 Compare match B
24	\$002E	TIMER0 OVF	Timer/Counter0 Overflow
25	\$0030	SPI, STC	SPI Serial Transfer Complete
26	\$0032	USART0 RX	USART0 Rx Complete
27	\$0034	USART0 UDRE	USART0 Data Register Empty
28	\$0036	USART0 TX	USART0 Tx Complete
29	\$0038	ANALOG COMP	Analog Comparator
30	\$003A	ADC	ADC Conversion Complete

Vector No.	Program Address ⁽²⁾	Source	Interrupt Definition
31	\$003C	EE READY	EEPROM Ready
32	\$003E	TIMER3 CAPT	Timer/Counter3 Capture Event
33	\$0040	TIMER3 COMPA	Timer/Counter3 Compare Match A
34	\$0042	TIMER3 COMPB	Timer/Counter3 Compare Match B
35	\$0044	TIMER3 COMPC	Timer/Counter3 Compare Match C
36	\$0046	TIMER3 OVF	Timer/Counter3 Overflow
37	\$0048	USART1 RX	USART1 Rx Complete
38	\$004A	USART1 UDRE	USART1 Data Register Empty
39	\$004C	USART1 TX	USART1 Tx Complete
40	\$004E	TWI	2-wire Serial Interface
41	\$0050	SPM READY	Store Program Memory Ready
42	\$0052 ⁽³⁾	TIMER4 CAPT	Timer/Counter4 Capture Event
43	\$0054	TIMER4 COMPA	Timer/Counter4 Compare Match A
44	\$0056	TIMER4 COMPB	Timer/Counter4 Compare Match B
45	\$0058	TIMER4 COMPC	Timer/Counter4 Compare Match C
46	\$005A	TIMER4 OVF	Timer/Counter4 Overflow
47	\$005C ⁽³⁾	TIMER5 CAPT	Timer/Counter5 Capture Event
48	\$005E	TIMER5 COMPA	Timer/Counter5 Compare Match A
49	\$0060	TIMER5 COMPB	Timer/Counter5 Compare Match B
50	\$0062	TIMER5 COMPC	Timer/Counter5 Compare Match C
51	\$0064	TIMER5 OVF	Timer/Counter5 Overflow
52	\$0066 ⁽³⁾	USART2 RX	USART2 Rx Complete
53	\$0068 ⁽³⁾	USART2 UDRE	USART2 Data Register Empty
54	\$006A ⁽³⁾	USART2 TX	USART2 Tx Complete
55	\$006C ⁽³⁾	USART3 RX	USART3 Rx Complete
56	\$006E ⁽³⁾	USART3 UDRE	USART3 Data Register Empty
57	\$0070 ⁽³⁾	USART3 TX	USART3 Tx Complete

Organización de las memorias

- Memoria de datos: 8192 posiciones de memoria interna
 - Incluye espacio de pila
- Recursos mapeados en el espacio de direcciones de memoria:

Address (HEX)

0 - 1F

32 Registers

20 - 5F

64 I/O Registers

60 - 1FF

416 External I/O Registers

200

Internal SRAM
(8192 × 8)

21FF

2200

External SRAM
(0 - 64K × 8)

FFFF

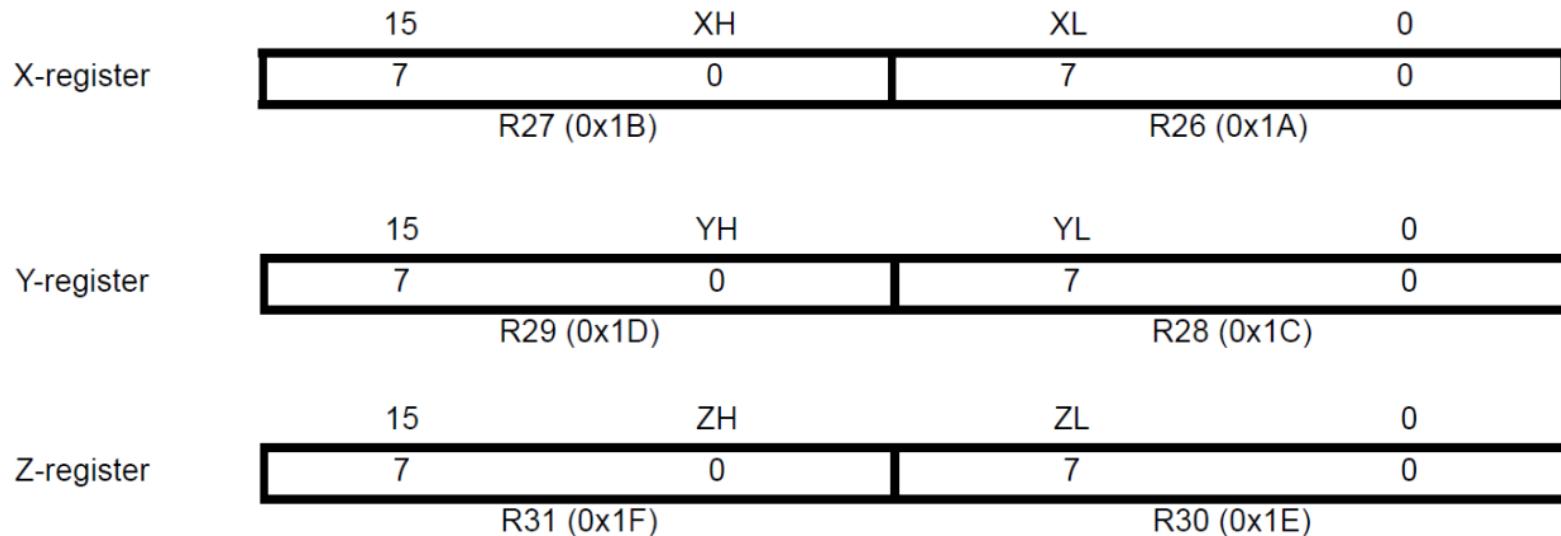
Registros de propósito general

- Optimizados para ser usados con datos de 8 y 16 bits

7	0	Addr.	
	R0	0x00	
	R1	0x01	
	R2	0x02	
	...		
	R13	0x0D	
	R14	0x0E	
	R15	0x0F	
	R16	0x10	
	R17	0x11	
	...		
	R26	0x1A	X-register Low Byte
	R27	0x1B	X-register High Byte
	R28	0x1C	Y-register Low Byte
	R29	0x1D	Y-register High Byte
	R30	0x1E	Z-register Low Byte
	R31	0x1F	Z-register High Byte

Registros de propósito general

□ Registros X, Y, Z

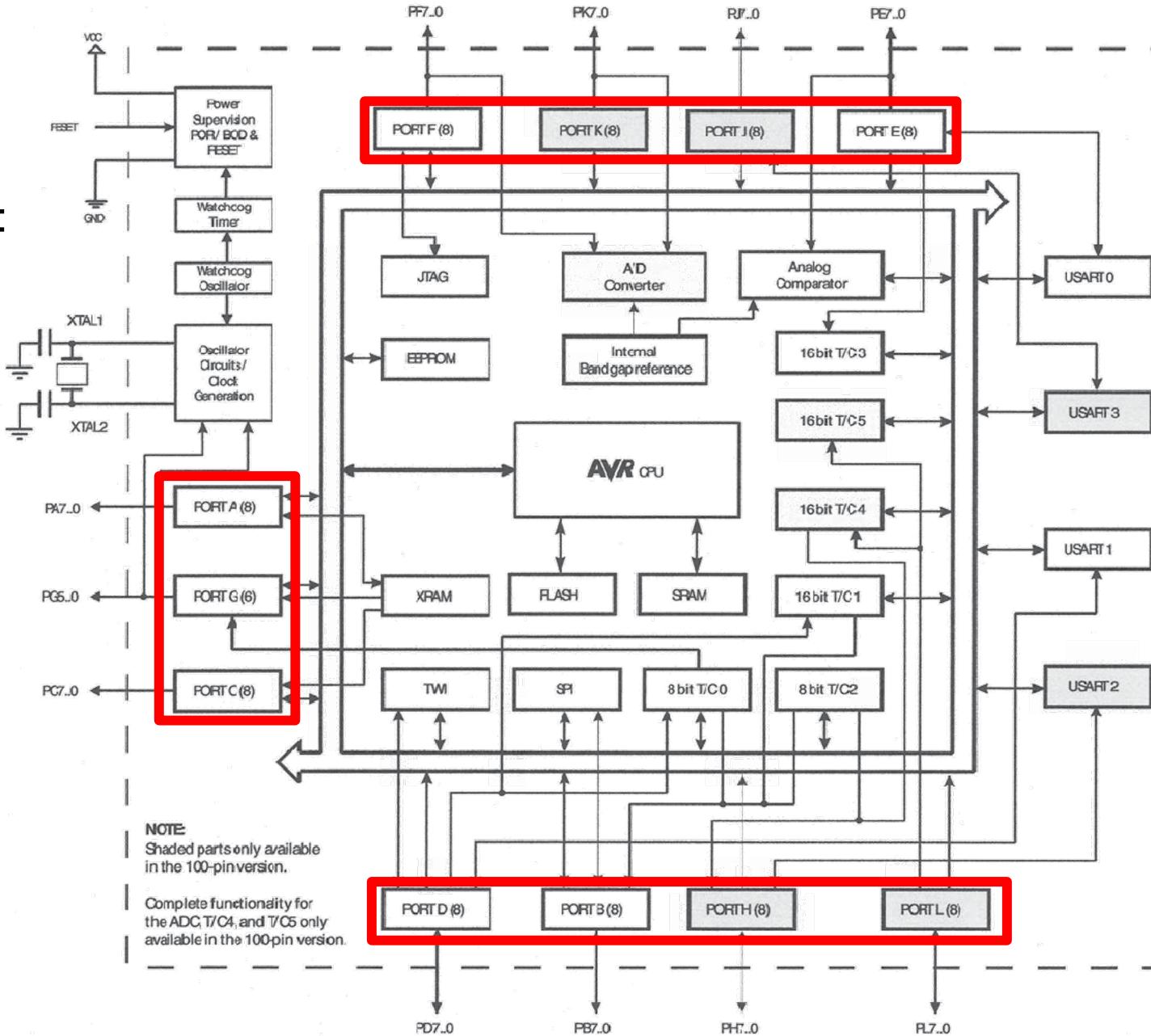


In the different addressing modes these address registers have functions as fixed displacement, automatic increment, and automatic decrement (see the instruction set reference for details).

Arquitectura ATmega2560

□ Puertos de E/S:

PORTA
PORTB
PORTC
PORTD
PORTE
PORTF
PORTG
PORTH
PORTK
PORTL



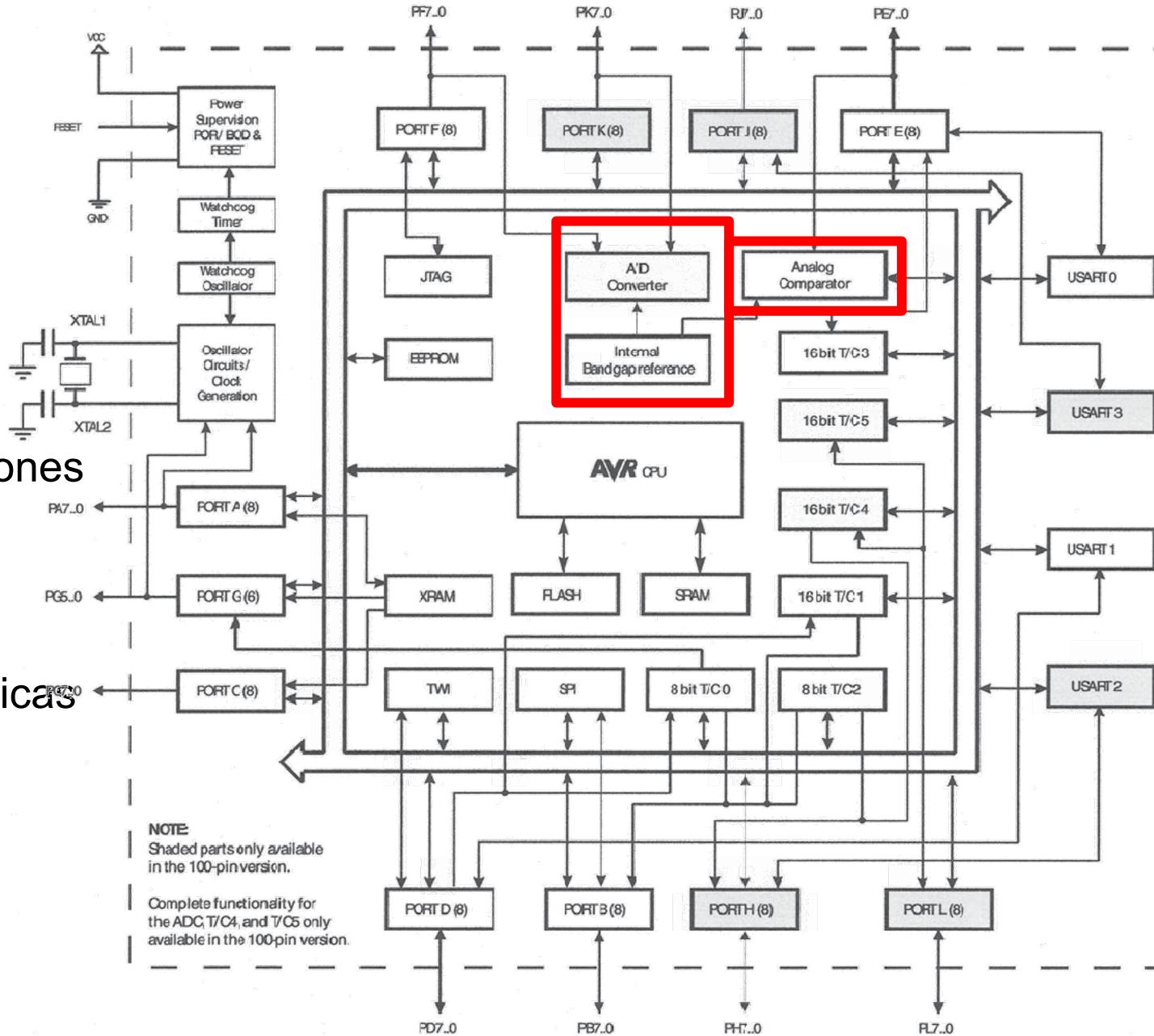
Arquitectura ATmega2560

- Conversor A/D

- 16 canales

- Aproximaciones sucesivas

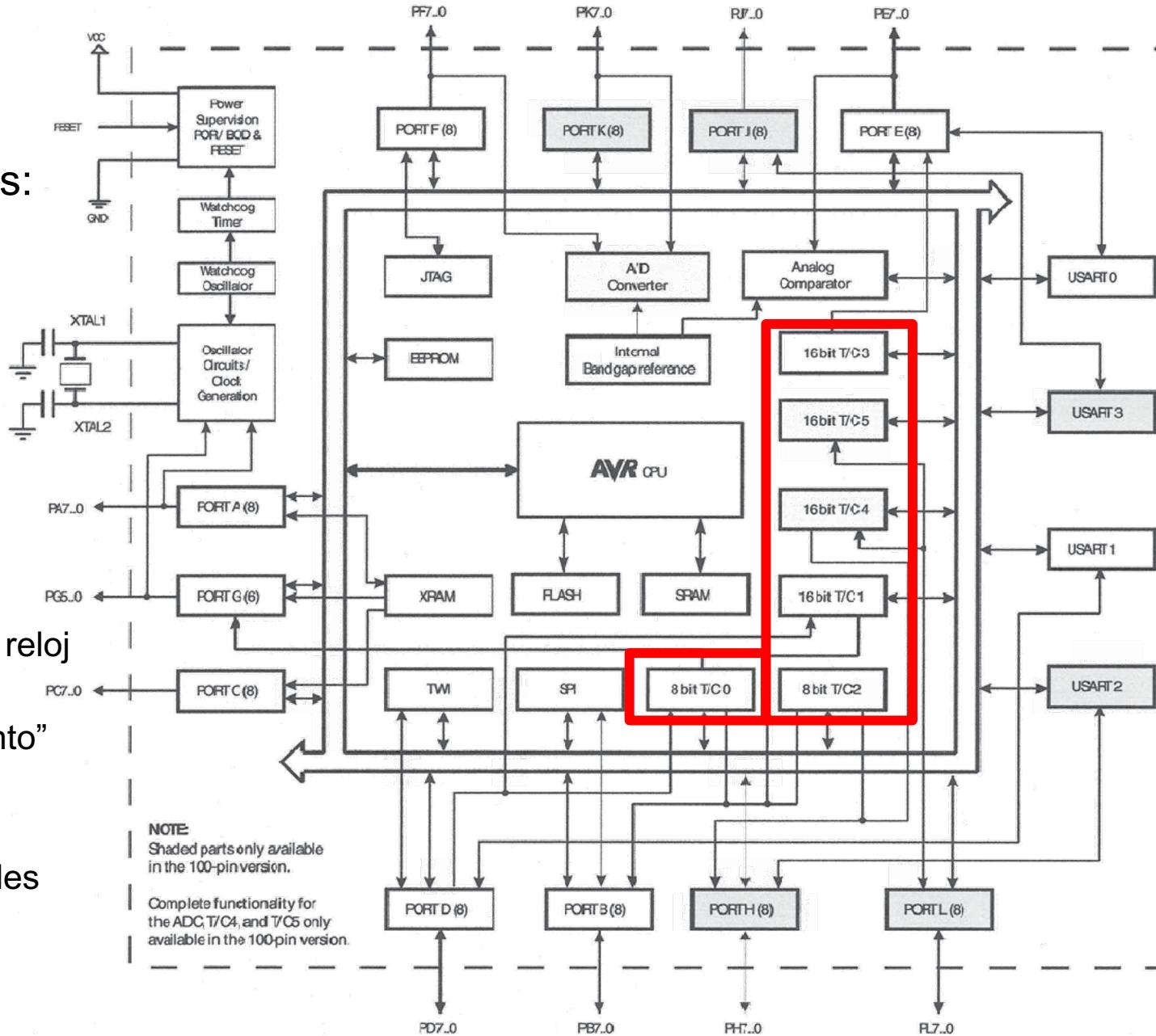
- Comparador señales analógicas



Arquitectura ATmega2560

□ Temporizadores:

- 2 de 8 bits
- 4 de 16 bits



Arquitectura ATmega2560

Comunicación serie:

- 4 USART (*Universal Synchronous and Asynchronous serial Receiver and Transmitter*)
- I²C (*Inter-Integrated Circuit*)
- SPI (*Serial Peripheral Interface*)

