ALU Instruction Set Break Down

Instruction	COND	Op Code	S bit	Dest Register	Immediate Value				Shift/ROR Cmd
					Source-1	Source-2	Shift/ROR bits	Part of Immediate	
MOV R3,#4	0000	0110	0	0011	0000000000000100				000
MOV R8,#4	0000	0110	0	1000	0000000000000100				000
CMP R3,R8	0000	1000	0	0000	0011	1000	00000	000	000
ADDGT R1,R3,R8	0010	0000	0	0001	0011	1000	00000	000	000
MULEQ R2, R3,R8 LSR#1	0001	0010	0	0010	0011	1000	00001	000	001
SUBS R7,R8,R2	0000	0001	1	0111	1000	0010	00000	000	000

Result:

R3=4
R8=4
R2=8
R7=-4
Flags (NZCV): 1000

Notes:

1. The purpose of the CMP is to set the flags. The destination register is a don't care.
2. ADDGT R1,R3,R8 should not execute since the condition (GT) is not satisfied.
3. The number -4 represented in two's complement is 32'b11111111111111111111111111111100, if you are displaying your register values in binary, the answer should be 4294967292.

STR Instruction Set Break Down

Instruction	COND	Op Code	S bit	Dest Register	Immediate Value				Shift/ROR Cmd
					Source-1	Source-2	Shift/ROR bits	Part of Immediate	
MOV R11, #0	0000	0110	0	1011	0000000000000000				000
MOV R6, #26947	0000	0110	0	**0110**	0110100101000011				000
STR R6, [R11]	0000	1010	0	0000	1011	0110	00000	000	000

Result:

R11=0
R6=26947
Flags (NZCV): 0000
Output data file with 16'b0110100101000011 stored in the first memory location

Note:

1. Source 1 (R11) points to the address and source 2 (R6) points to the register containing the data to be written in the RAM

LDR Instruction Set Break Down

					Immediate Value				
Instruction	**COND**	**Op Code**	**S bit**	**Dest Register**	**Source-1**	**Source-2**	**Shift/ROR bits**	**Part of Immediate**	**Shift/ROR Cmd**
MOV R9, #0	0000	0110	0	1001	0000000000000000				000
LDR R10, [R9]	0000	1001	0	1010	1001	0000	00000	000	000

Result:

R9=0
R10=26947
Flags (NZCV): 0000

Notes:

1. Use the data file outputted from the STR execution
2. Source 1 (R9) points to the address of the data in the RAM