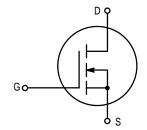
The RF MOSFET Line **RF Power Field Effect Transistor**N-Channel Enhancement-Mode

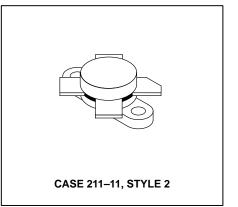
 \dots designed primarily for wideband large—signal output and driver stages up to 200 MHz frequency range.

- Guaranteed Performance at 150 MHz, 28 Vdc Output Power = 125 Watts Minimum Gain = 9.0 dB Efficiency = 50% (Min)
- Excellent Thermal Stability, Ideally Suited For Class A Operation
- Facilitates Manual Gain Control, ALC and Modulation Techniques
- 100% Tested For Load Mismatch At All Phase Angles With 30:1 VSWR
- Low Noise Figure 3.0 dB Typ at 2.0 A, 150 MHz



MRF174

125 W, to 200 MHz N-CHANNEL MOS BROADBAND RF POWER FET



MAXIMUM RATINGS

Rating	Symbo	ol Value	Unit
Drain-Source Voltage	VDSS	65	Vdc
Drain–Gate Voltage (RGS = 1.0 M Ω)	V _{DGR}	65	Vdc
Gate–Source Voltage	V _{GS}	±40	Vdc
Drain Current — Continuous	ID	13	Adc
Total Device Dissipation @ T _C = 25°C Derate above 25°C	P _D	270 1.54	Watts W/°C
Storage Temperature Range	T _{stg}	-65 to +150	°C
Operating Junction Temperature	TJ	200	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	0.65	°C/W

Handling and Packaging — MOS devices are susceptible to damage from electrostatic charge. Reasonable precautions in handling and packaging MOS devices should be observed.

Characteristic	Symbol	Min	Тур	Max	Unit
OFF CHARACTERISTICS			•	•	•
Drain–Source Breakdown Voltage (V _{GS} = 0, I _D = 50 mA)	V(BR)DSS	65	_	_	Vdc
Zero Gate Voltage Drain Current (V _{DS} = 28 V, V _{GS} = 0)	IDSS	_	_	10	mAdc
Gate–Source Leakage Current (V _{GS} = 20 V, V _{DS} = 0)	IGSS	_	_	1.0	μAdc
ON CHARACTERISTICS					
Gate Threshold Voltage (V _{DS} = 10 V, I _D = 100 mA)	VGS(th)	1.0	3.0	6.0	Vdc
Forward Transconductance (V _{DS} = 10 V, I _D = 3.0 A)	9fs	1.75	2.5	_	mhos
DYNAMIC CHARACTERISTICS			•		
Input Capacitance ($V_{DS} = 28 \text{ V}, V_{GS} = 0, f = 1.0 \text{ MHz}$)	C _{iss}	_	175	_	pF
Output Capacitance (V _{DS} = 28 V, V _{GS} = 0, f = 1.0 MHz)	C _{oss}	_	190	_	pF
Reverse Transfer Capacitance (V _{DS} = 28 V, V _{GS} = 0, f = 1.0 MHz)	C _{rss}	_	40	_	pF
FUNCTIONAL CHARACTERISTICS (Figure 1)					
Noise Figure (V _{DD} = 28 Vdc, I _D = 2.0 A, f = 150 MHz)	NF	_	3.0	_	dB
Common Source Power Gain (V _{DD} = 28 Vdc, P _{Out} = 125 W, f = 150 MHz, I _{DQ} = 100 mA)	G _{ps}	9.0	11.8	_	dB
Drain Efficiency (V _{DD} = 28 Vdc, P _{Out} = 125 W, f = 150 MHz, I _{DQ} = 100 mA)	η	50	60	_	%
Electrical Ruggedness (V _{DD} = 28 Vdc, P _{out} = 125 W, f = 150 MHz, I _{DQ} = 100 mA, VSWR 30:1 at all Phase Angles)	Ψ	No Degradation in Output Power			

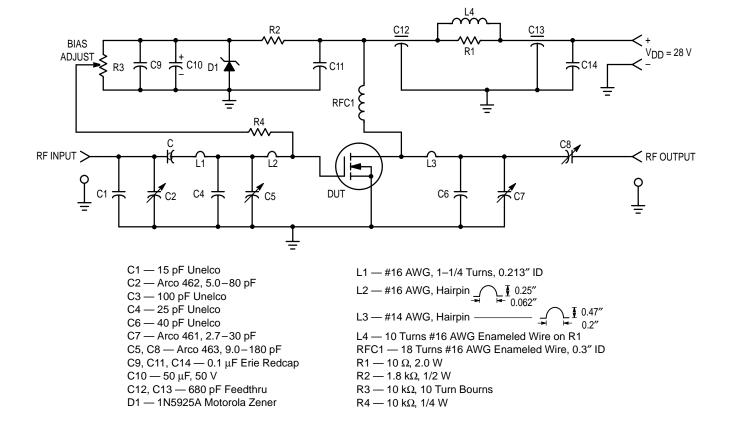


Figure 1. 150 MHz Test Circuit

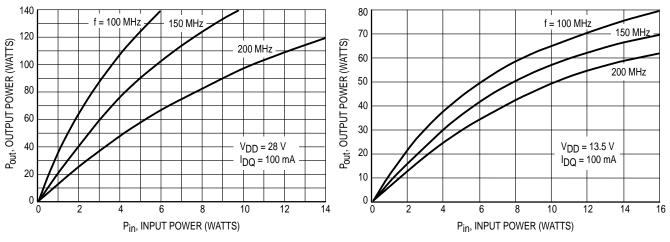


Figure 2. Output Power versus Input Power

Figure 3. Output Power versus Input Power

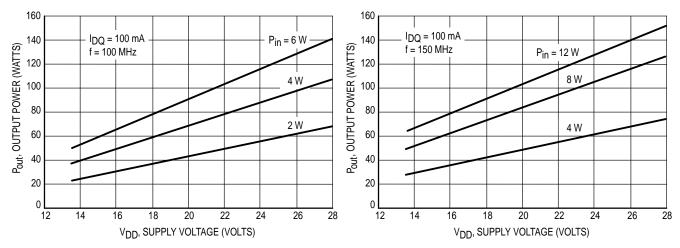


Figure 4. Output Power versus Supply Voltage

Figure 5. Output Power versus Supply Voltage

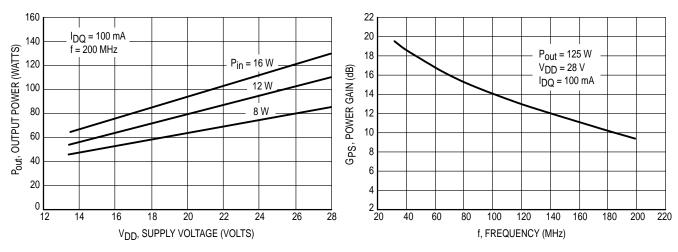


Figure 6. Output Power versus Supply Voltage

Figure 7. Power Gain versus Frequency

MOTOROLA RF DEVICE DATA **MRF174**

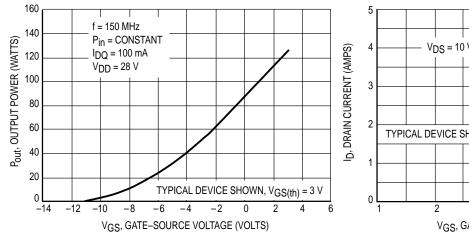


Figure 8. Output Power versus Gate Voltage

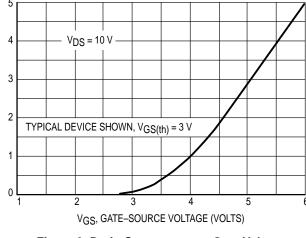


Figure 9. Drain Current versus Gate Voltage (Transfer Characteristics)

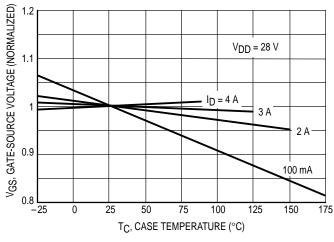


Figure 10. Gate—Source Voltage versus Case Temperature

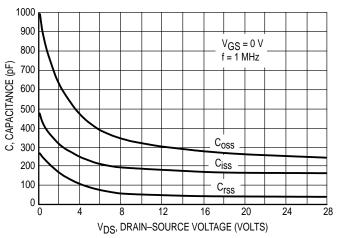


Figure 11. Capacitance versus Drain Voltage

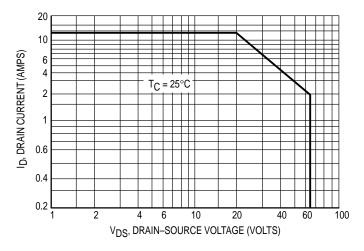


Figure 12. DC Safe Operating Area

f	S ₁₁		s ₂₁		s ₁₂		S ₂₂	
(MHz)	S ₁₁	∠ ф	S ₂₁	∠¢	S ₁₂	∠¢	S ₂₂	∠ ф
2.0	0.932	-133	74.0	112	0.011	23	0.835	-151
5.0	0.923	-160	31.6	98	0.011	12	0.886	-168
10	0.921	-170	16.0	93	0.011	10	0.896	-174
20	0.921	-175	8.00	88	0.011	12	0.899	-177
30	0.921	-177	5.32	86	0.011	16	0.900	-178
40	0.921	-177	3.98	83	0.012	21	0.901	-178
50	0.922	-178	3.17	81	0.012	26	0.902	-178
60	0.923	-178	2.63	79	0.012	30	0.903	-178
70	0.924	-178	2.24	77	0.013	34	0.904	-178
80	0.925	-178	1.95	75	0.013	39	0.906	-178
90	0.927	-178	1.72	73	0.014	43	0.907	-178
100	0.930	-178	1.50	71	0.016	45	0.910	-178
110	0.930	-178	1.31	70	0.018	46	0.912	-178
120	0.931	-178	1.19	68	0.019	47	0.914	-178
130	0.942	-178	1.10	67	0.019	49	0.919	-178
140	0.936	-178	1.01	66	0.021	50	0.921	-178
150	0.938	-178	0.936	65	0.021	53	0.922	-178
160	0.938	-178	0.879	64	0.022	53	0.923	-178
170	0.940	-178	0.830	63	0.023	54	0.923	-177
180	0.942	-178	0.780	61	0.024	56	0.924	-177
190	0.942	-178	0.737	60	0.026	59	0.928	-177
200	0.952	-178	0.705	59	0.027	58	0.929	-177
210	0.950	-178	0.668	57	0.029	61	0.934	-177
220	0.942	-178	0.626	56	0.030	61	0.933	-177
230	0.943	-178	0.592	56	0.032	62	0.939	-177
240	0.946	-177	0.566	55	0.033	64	0.941	-177
250	0.952	-177	0.545	54	0.035	64	0.943	-177
260	0.958	-177	0.523	53	0.036	65	0.946	-177
270	0.956	-177	0.500	52	0.038	67	0.943	-177
280	0.960	-177	0.481	52	0.039	68	0.946	-177
290	0.956	-178	0.460	51	0.042	68	0.944	-177
300	0.955	-178	0.443	50	0.043	68	0.947	-177

Table 1. Common Source Scattering Parameters V_{DS} = 28 V, I_{D} = 3.0 A

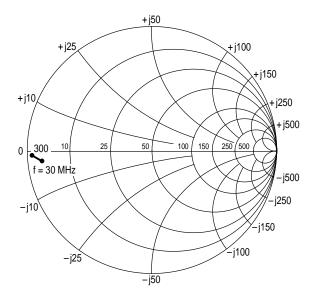


Figure 13. S₁₁, Input Reflection Coefficient versus Frequency V_{DS} = 28 V, I_D = 3.0 A

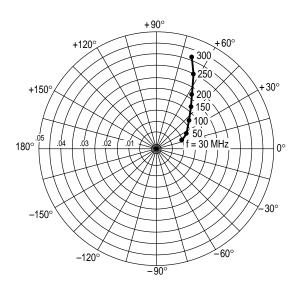


Figure 14. S_{12} , Reverse Transmission Coefficient versus Frequency $V_{DS} = 28 \text{ V}$, $I_D = 3.0 \text{ A}$

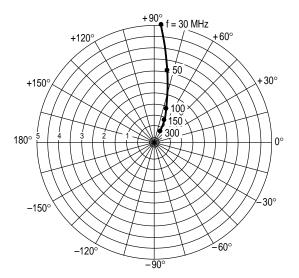


Figure 15. S₂₁, Forward Transmission Coefficient versus Frequency V_{DS} = 28 V, I_D = 3.0 A

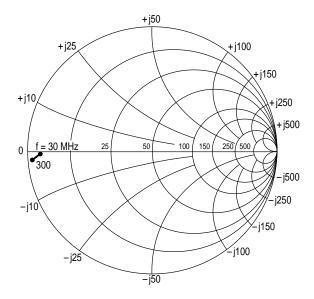


Figure 16. S₂₂, Output Reflection Coefficient versus Frequency V_{DS} = 28 V, I_D = 3.0 A

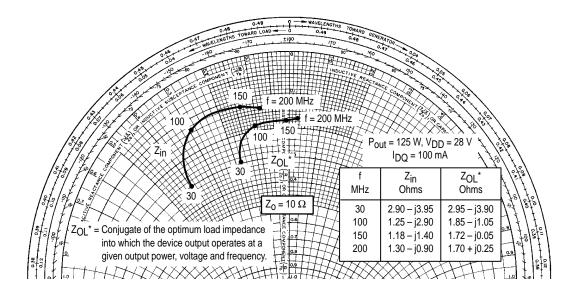


Figure 17. Series Equivalent Input/Output Impedance, Z_{in} , Z_{OL}^*

DESIGN CONSIDERATIONS

The MRF174 is a RF power N-Channel enhancement mode field-effect transistor (FET) designed especially for UHF power amplifier and oscillator applications. Motorola RF MOSFETs feature a vertical structure with a planar design, thus avoiding the processing difficulties associated with V-groove vertical power FETs.

Motorola Application Note AN211A, FETs in Theory and Practice, is suggested reading for those not familiar with the construction and characteristics of FETs.

The major advantages of RF power FETs include high gain, low noise, simple bias systems, relative immunity from thermal runaway, and the ability to withstand severely mismatched loads without suffering damage. Power output can be varied over a wide range with a low power dc control signal, thus facilitating manual gain control, ALC and modulation.

DC BIAS

The MRF174 is an enhancement mode FET and, therefore, does not conduct when drain voltage is applied. Drain current flows when a positive voltage is applied to the gate. See Figure 9 for a typical plot of drain current versus gate voltage. RF power FETs require forward bias for optimum performance. The value of quiescent drain current (IDQ) is not critical for many applications. The MRF174 was charac-

terized at I_{DQ} = 100 mA, which is the suggested minimum value of I_{DQ} . For special applications such as linear amplification, I_{DQ} may have to be selected to optimize the critical parameters.

The gate is a dc open circuit and draws no current. Therefore, the gate bias circuit may generally be just a simple resistive divider network. Some special applications may require a more elaborate bias system.

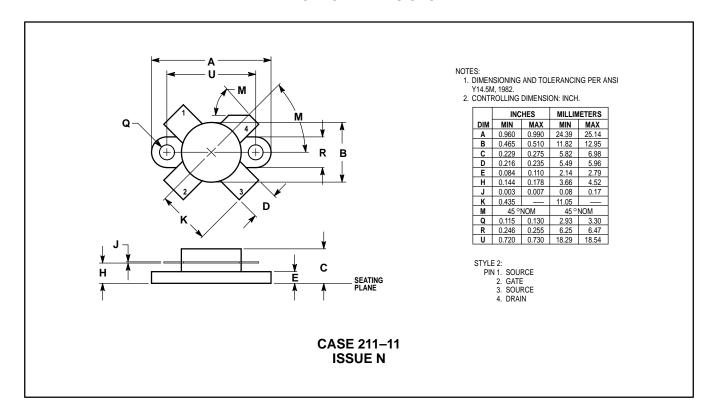
GAIN CONTROL

Power output of the MRF174 may be controlled from its rated value down to zero (negative gain) by varying the dc gate voltage. This feature facilitates the design of manual gain control, AGC/ALC and modulation systems. (See Figure 8.)

AMPLIFIER DESIGN

Impedance matching networks similar to those used with bipolar UHF transistors are suitable for MRF174. See Motorola Application Note AN721, Impedance Matching Networks Applied to RF Power Transistors. The higher input impedance of RF MOSFETs helps ease the task of broadband network design. Both small signal scattering parameters and large signal impedances are provided. While the s-parameters will not produce an exact design solution for high power operation, they do yield a good first approximation. This is an additional advantage of RF MOS power FETs.

PACKAGE DIMENSIONS



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