N-Channel JFETs

2N5484	SST5484
2N5485	SST5485
2N5486	SST5486

PRODUCT SUMMARY				
Part Number	$V_{GS(off)}$ (V)	$V_{(BR)GSS}$ Min (V)	g_{fs} Min (mS)	I_{DSS} Min (mA)
2N/SST5484	−0.3 to −3	−25	3	1
2N/SST5485	−0.5 to −4	−25	3.5	4
2N/SST5486	−2 to −6	−25	4	8

FEATURES

- Excellent High-Frequency Gain: Gps 13 dB (typ) @ 400 MHz – 5485/6
- Very Low Noise: 2.5 dB (typ) @ 400 MHz – 5485/6
- Very Low Distortion
- High AC/DC Switch Off-Isolation

BENEFITS

- Wideband High Gain
- Very High System Sensitivity
- High Quality of Amplification
- High-Speed Switching Capability
- High Low-Level Signal Amplification

APPLICATIONS

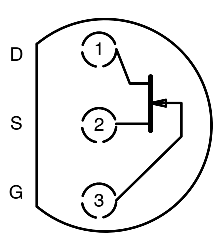
- High-Frequency Amplifier/Mixer
- Oscillator
- Sample-and-Hold
- Very Low Capacitance Switches

DESCRIPTION

The 2N/SST5484 series consists of n-channel JFETs designed to provide high-performance amplification, especially at high frequencies up to and beyond 400 MHz.

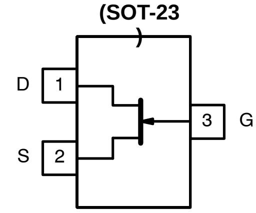
The 2N series, TO-226AA (TO-92), and SST series, TO-236 (SOT-23), packages provide low-cost options and are available with tape-and-reel to support automated assembly (see Packaging Information).

TO-226AA (TO-92)



Top View
2N5484
2N5485
2N5486

TO-236 (SOT-23)



Top View
SST5484 (H4)*
SST5485 (H5)*
SST5486 (H6)*

*Marking Code for TO-236

For applications information see AN102 and AN105.

ABSOLUTE MAXIMUM RATINGS

Gate-Drain, Gate-Source Voltage . . . . −25 V
Gate Current . . . . 10 mA
Lead Temperature . . . . 300°C
Storage Temperature . . . . −65 to 150°C

Operating Junction Temperature . . . . −55 to 150°C
Power Dissipation[a] . . . . 350 mW

Notes
a. Derate 2.8 mW/°C above 25°C

SPECIFICATIONS FOR 2N SERIES (T_A = 25°C UNLESS OTHERWISE NOTED)

Parameter	Symbol	Test Conditions		Typ[a]	Limits 2N5484 Min	2N5484 Max	2N5485 Min	2N5485 Max	2N5486 Min	2N5486 Max	Unit
Static											
Gate-Source Breakdown Voltage	$V_{(BR)GSS}$	I_G = −1 µA , V_{DS} = 0 V		−35	−25		−25		−25		V
Gate-Source Cutoff Voltage	$V_{GS(off)}$	V_{DS} = 15 V, I_D = 10 nA			−0.3	−3	−0.5	−4	−2	−6	V
Saturation Drain Current[b]	I_{DSS}	V_{DS} = 15 V, V_{GS} = 0 V			1	5	4	10	8	20	mA
Gate Reverse Current	I_{GSS}	V_{GS} = −20 V, V_{DS} = 0 V		−0.002		−1		−1		−1	nA
			T_A = 100°C	−0.2		−200		−200		−200	nA
Gate Operating Current[c]	I_G	V_{DG} = 10 V, I_D = 1 mA		−20							pA
Gate-Source Forward Voltage[c]	$V_{GS(F)}$	I_G = 10 mA , V_{DS} = 0 V		0.8							V
Dynamic											
Common-Source Forward Transconductance[NO TAG]	g_{fs}	V_{DS} = 15 V, V_{GS} = 0 V f = 1 kHz			3	6	3.5	7	4	8	mS
Common-Source Output Conductance[NO TAG]	g_{os}	V_{DS} = 15 V, V_{GS} = 0 V f = 1 kHz				50		60		75	µS
Common-Source Input Capacitance	C_{iss}	V_{DS} = 15 V, V_{GS} = 0 V f = 1 MHz		2.2		5		5		5	pF
Common-Source Reverse Transfer Capacitance	C_{rss}	V_{DS} = 15 V, V_{GS} = 0 V f = 1 MHz		0.7		1		1		1	pF
Common-Source Output Capacitance	C_{oss}	V_{DS} = 15 V, V_{GS} = 0 V f = 1 MHz		1		2		2		2	pF
Equivalent Input Noise Voltage[c]	$\bar{e}_n$	V_{DS} = 15 V, V_{GS} = 0 V f = 100 Hz		10							nV/√Hz
High-Frequency											
Common-Source Transconductance[d]	$Y_{fs(RE)}$	V_{DS} = 15 V V_{GS} = 0 V	f = 100 MHz	5.5	2.5						mS
			f = 400 MHz	5.5			3		3.5		mS
Common-Source Output Conductance[d]	$Y_{os(RE)}$	V_{DS} = 15 V V_{GS} = 0 V	f = 100 MHz	45		75					µS
			f = 400 MHz	65				100		100	µS
Common-Source Input Conductance[d]	$Y_{is(RE)}$	V_{DS} = 15 V V_{GS} = 0 V	f = 100 MHz	0.05		0.1					mS
			f = 400 MHz	0.8				1		1	mS
Common-Source Power Gain[d]	G_{ps}	V_{DS} = 15 V, I_D = 1 mA f = 100 MHz		20	16	25					dB
		V_{DS} = 15 V I_D = 4 mA	f = 100 MHz	21			18	30	18	30	dB
			f = 400 MHz	13			10	20	10	20	dB
Noise Figure[d]	NF	V_{DS} = 15 V, V_{GS} = 0 V R_G = 1 MΩ, f = 1 kHz		0.3		2.5		2.5		2.5	dB
		V_{DS} = 15 V, I_D = 1 mA R_G = 1 kΩ, f = 100 MHz		2		3					dB
		V_{DS} = 15 V I_D = 4 mA R_G = 1 kΩ	f = 100 MHz	1				2		2	dB
			f = 400 MHz	2.5				4		4	dB

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SPECIFICATIONS FOR SST SERIES (T_A = 25°C UNLESS OTHERWISE NOTED)

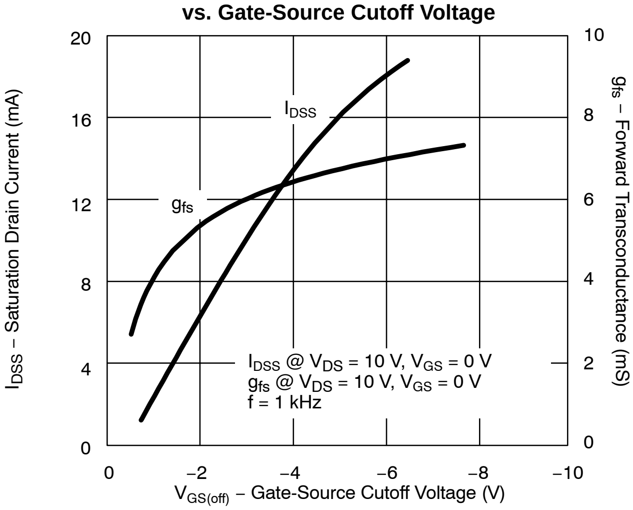
Parameter	Symbol	Test Conditions	Typ[b]	Limits SST5484 Min	SST5484 Max	SST5485 Min	SST5485 Max	SST5486 Min	SST5486 Max	Unit
Static										
Gate-Source Breakdown Voltage	$V_{(BR)GSS}$	I_G = –1 μA , V_{DS} = 0 V	–35	–25		–25		–25		V
Gate-Source Cutoff Voltage	$V_{GS(off)}$	V_{DS} = 15 V, I_D = 10 nA		–0.3	–3	–0.5	–4	–2	–6	V
Saturation Drain Current[b]	I_{DSS}	V_{DS} = 15 V, V_{GS} = 0 V		1	5	4	10	8	20	mA
Gate Reverse Current	I_{GSS}	V_{GS} = –20 V, V_{DS} = 0 V	–0.002		–1		–1		–1	nA
		T_A = 100°C	–0.2		–200		–200		–200	nA
Gate Operating Current[c]	I_G	V_{DG} = 10 V, I_D = 1 mA	–20							pA
Gate-Source Forward Voltage[c]	$V_{GS(F)}$	I_G = 10 mA , V_{DS} = 0 V	0.8							V
Dynamic										
Common-Source Forward Transconductance[NO TAG]	g_{fs}	V_{DS} = 15 V, V_{GS} = 0 V, f = 1 kHz		3	6	3.5	7	4	8	mS
Common-Source Output Conductance[NO TAG]	g_{os}	V_{DS} = 15 V, V_{GS} = 0 V, f = 1 kHz			50		60		75	μS
Common-Source Input Capacitance	C_{iss}	V_{DS} = 15 V, V_{GS} = 0 V, f = 1 MHz	2.2							pF
Common-Source Reverse Transfer Capacitance	C_{rss}	V_{DS} = 15 V, V_{GS} = 0 V, f = 1 MHz	0.7							pF
Common-Source Output Capacitance	C_{oss}	V_{DS} = 15 V, V_{GS} = 0 V, f = 1 MHz	1							pF
Equivalent Input Noise Voltage[c]	$\bar{e}_n$	V_{DS} = 15 V, V_{GS} = 0 V, f = 100 Hz	10							nV⁄√Hz
High-Frequency										
Common-Source Transconductance	Y_{fs}	V_{DS} = 15 V, V_{GS} = 0 V; f = 100 MHz	5.5							mS
		f = 400 MHz	5.5							mS
Common-Source Output Conductance	Y_{os}	V_{DS} = 15 V, V_{GS} = 0 V; f = 100 MHz	45							μS
		f = 400 MHz	65							μS
Common-Source Input Conductance	Y_{is}	V_{DS} = 15 V, V_{GS} = 0 V; f = 100 MHz	0.05							mS
		f = 400 MHz	0.8							mS
Common-Source Power Gain	G_{ps}	V_{DS} = 15 V, I_D = 1 mA, f = 100 MHz	20							dB
		V_{DS} = 15 V, I_D = 4 mA; f = 100 MHz	21							dB
		f = 400 MHz	13							dB
Noise Figure	NF	V_{DS} = 15 V, V_{GS} = 0 V, R_G = 1 MΩ, f = 1 kHz	0.3							dB
		V_{DS} = 15 V, I_D = 1 mA, R_G = 1 kΩ, f = 100 MHz	2							dB
		V_{DS} = 15 V, I_D = 4 mA, R_G = 1 kΩ; f = 100 MHz	1							dB
		f = 400 MHz	2.5							dB

Notes
a. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing. NH
b. Pulse test: PW ≤300 μs duty cycle ≤3%.
c. This parameter not registered with JEDEC.
d. Not a production test.

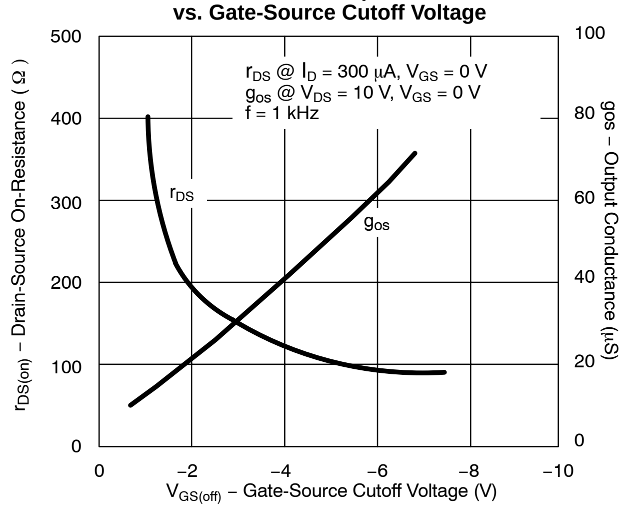
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

TYPICAL CHARACTERISTICS (T_A = 25°C UNLESS OTHERWISE NOTED)

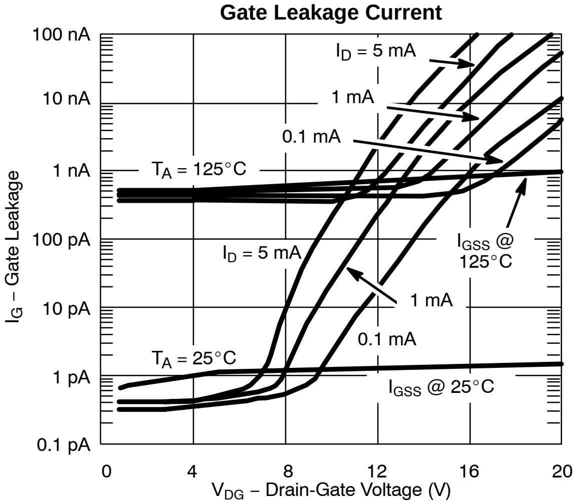
Drain Current and Transconductance vs. Gate-Source Cutoff Voltage



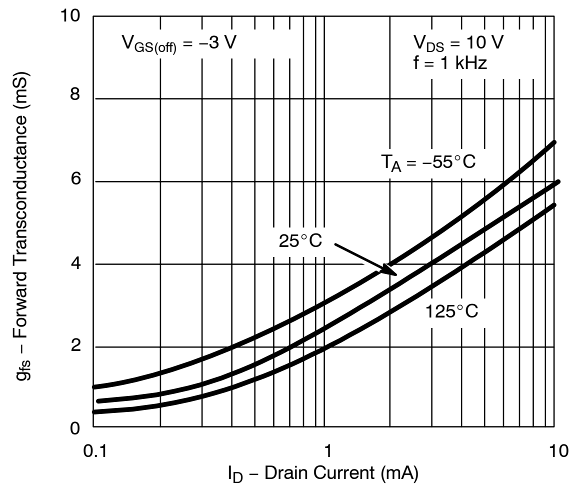
On-Resistance and Output Conductance vs. Gate-Source Cutoff Voltage



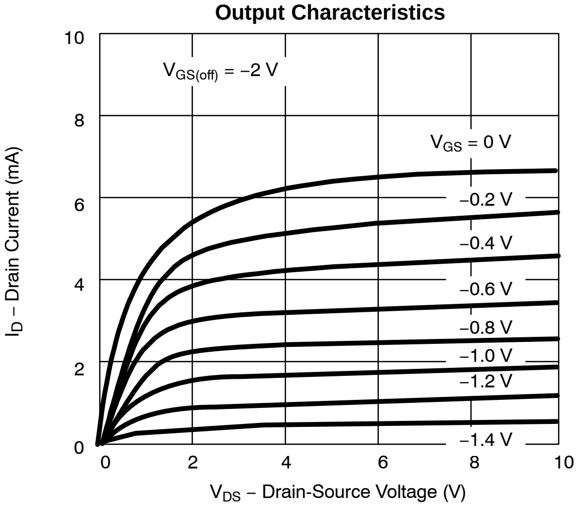
Gate Leakage Current



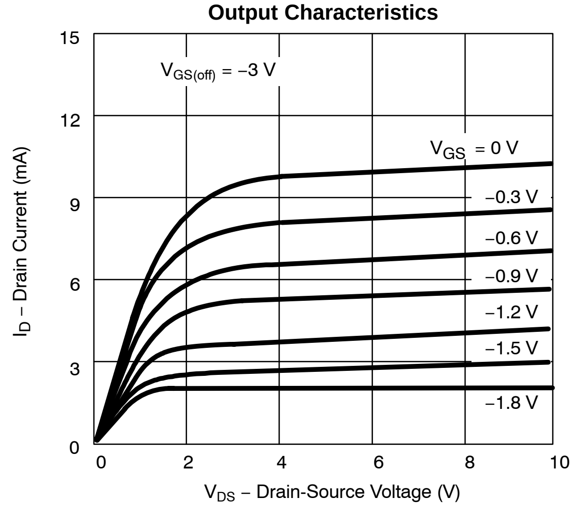
Common-Source Forward Transconductance vs. Drain Current



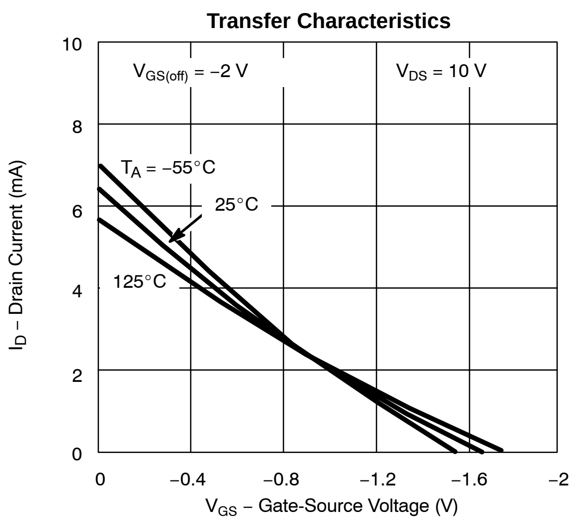
Output Characteristics

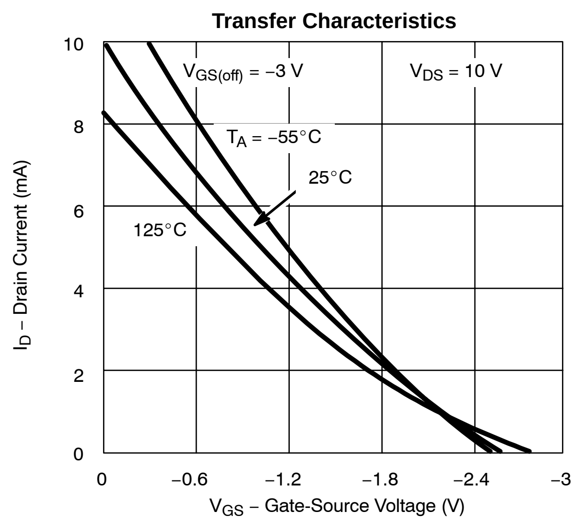


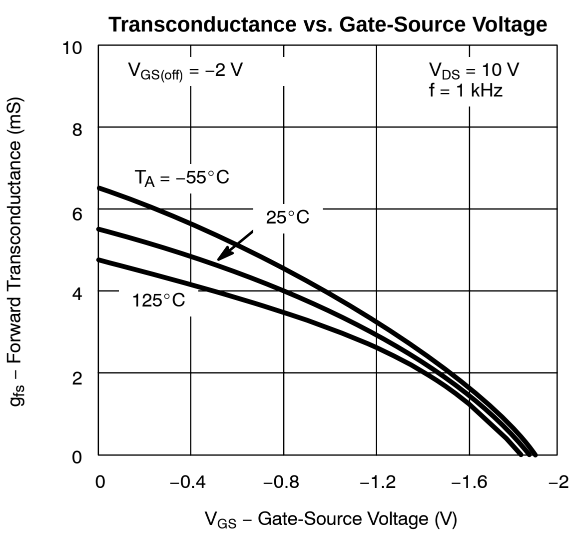
Output Characteristics

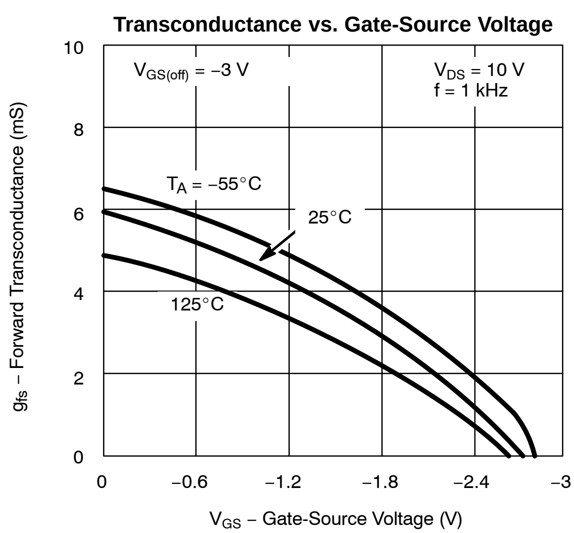


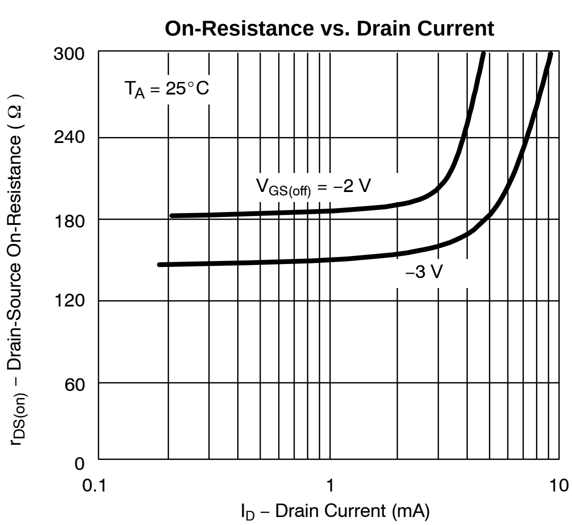
TYPICAL CHARACTERISTICS (T_A = 25°C UNLESS OTHERWISE NOTED)

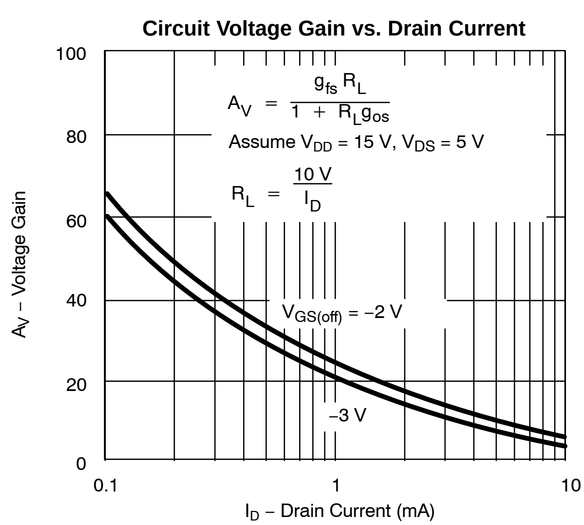












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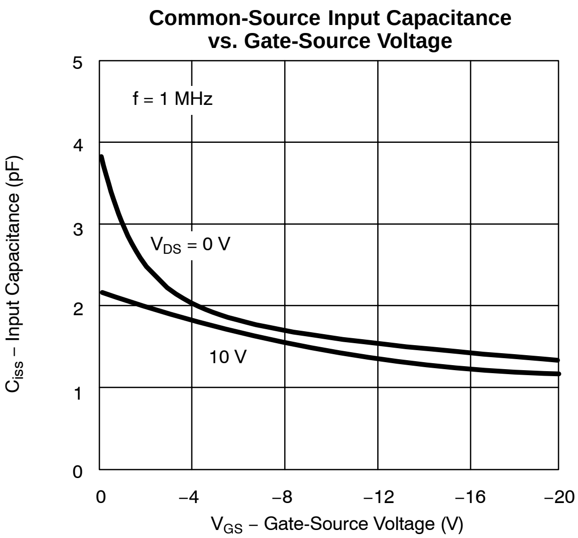

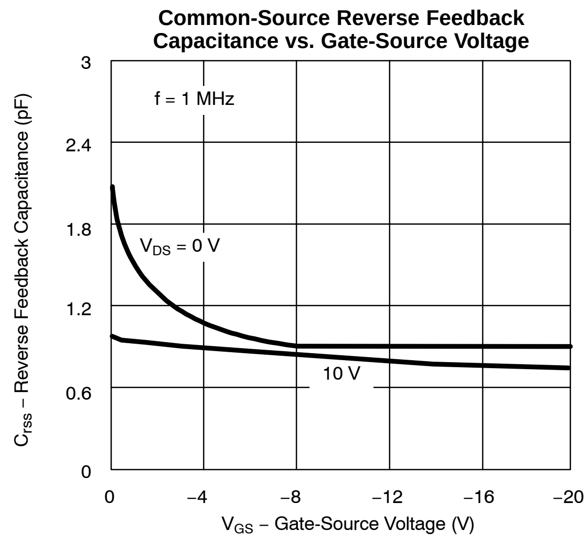

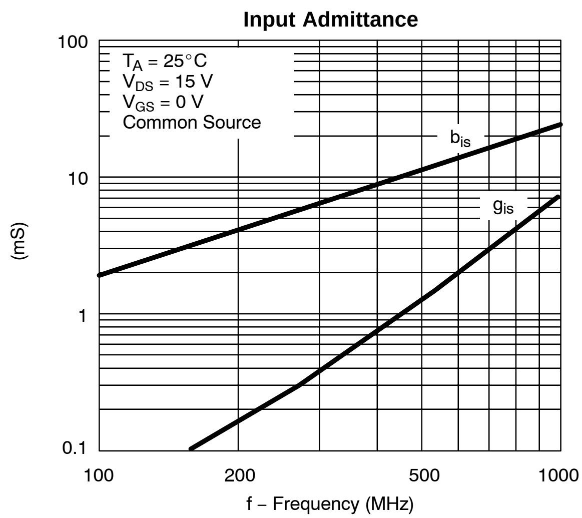

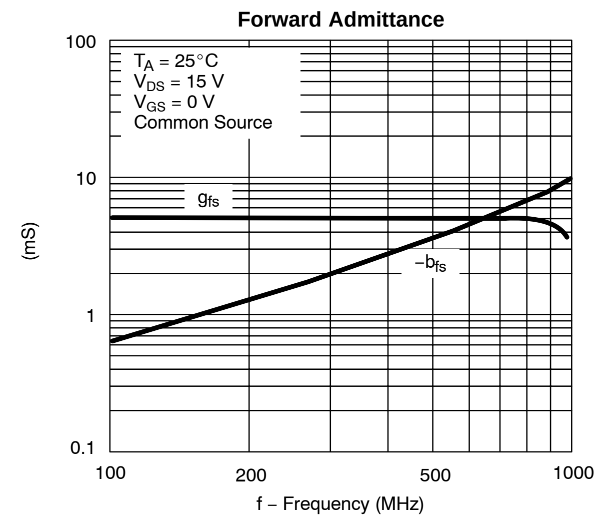

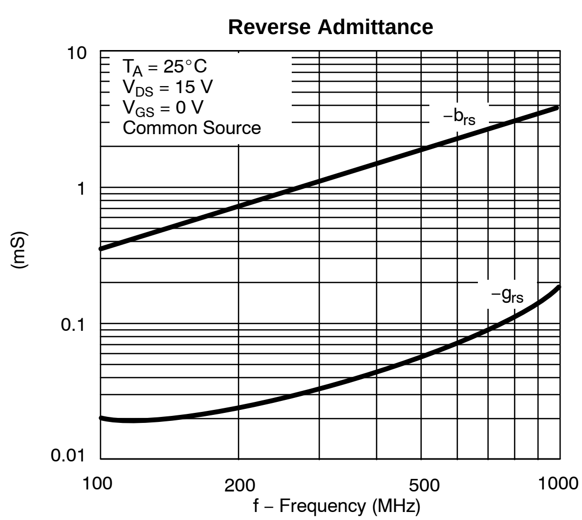

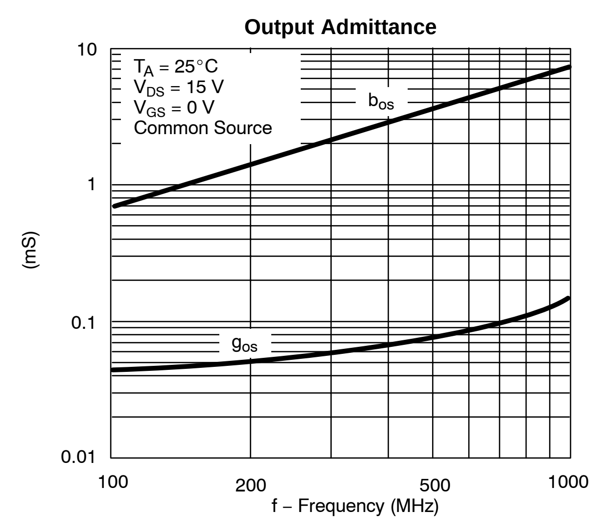

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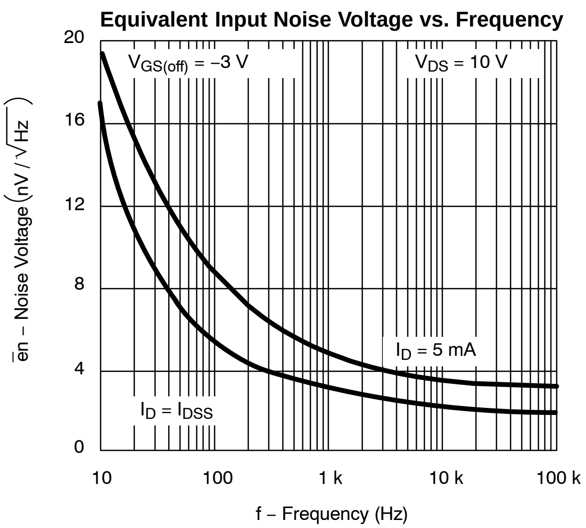

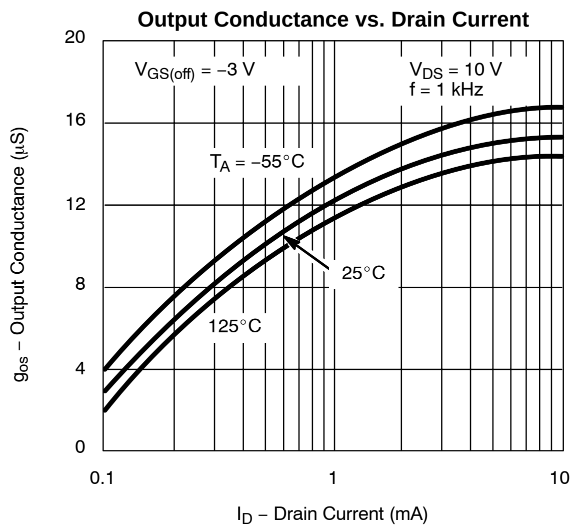

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