

A

A

MEMORY

- WRITE
- ENABLE
- BUS[0..15]
- ADDR[0..18]
- UB
- LB

MEMORY

MEMORY

MEM_BUS_JUMPER

I MEMORY.BUS0	1	2	MEMORY.BUS0
I MEMORY.BUS1	3	4	MEMORY.BUS1
I MEMORY.BUS2	5	6	MEMORY.BUS2
I MEMORY.BUS3	7	8	MEMORY.BUS3
I MEMORY.BUS4	9	10	MEMORY.BUS4
I MEMORY.BUS5	11	12	MEMORY.BUS5
I MEMORY.BUS6	13	14	MEMORY.BUS6
I MEMORY.BUS7	15	16	MEMORY.BUS7
I MEMORY.BUS8	17	18	MEMORY.BUS8
I MEMORY.BUS9	19	20	MEMORY.BUS9
I MEMORY.BUS10	21	22	MEMORY.BUS10
I MEMORY.BUS11	23	24	MEMORY.BUS11
I MEMORY.BUS12	25	26	MEMORY.BUS12
I MEMORY.BUS13	27	28	MEMORY.BUS13
I MEMORY.BUS14	29	30	MEMORY.BUS14
I MEMORY.BUS15	31	32	MEMORY.BUS15

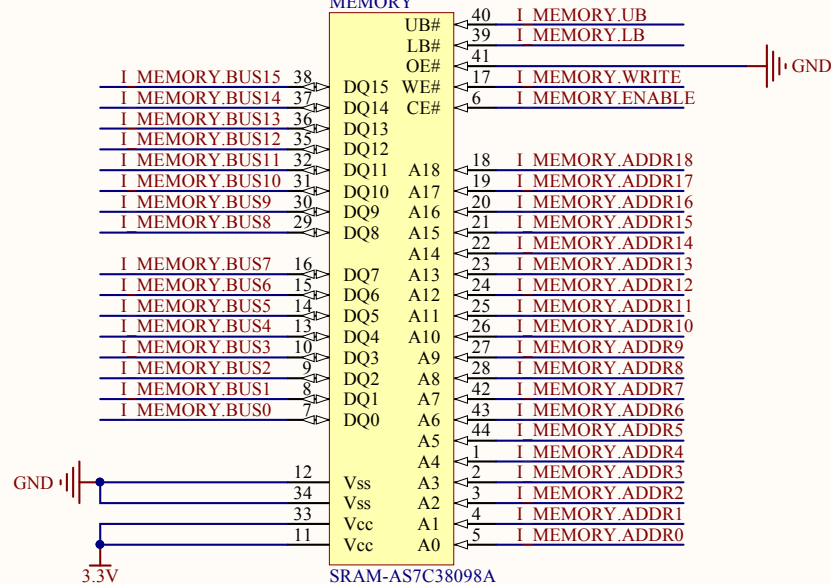
Header 16X2

B

B

2103743

MEMORY



SRAM-AS7C38098A

MEM_ADDR_JUMPER

I MEMORY.ADDR0	1	2	MEMORY.ADDR0
I MEMORY.ADDR1	3	4	MEMORY.ADDR1
I MEMORY.ADDR2	5	6	MEMORY.ADDR2
I MEMORY.ADDR3	7	8	MEMORY.ADDR3
I MEMORY.ADDR4	9	10	MEMORY.ADDR4
I MEMORY.ADDR5	11	12	MEMORY.ADDR5
I MEMORY.ADDR6	13	14	MEMORY.ADDR6
I MEMORY.ADDR7	15	16	MEMORY.ADDR7
I MEMORY.ADDR8	17	18	MEMORY.ADDR8
I MEMORY.ADDR9	19	20	MEMORY.ADDR9
I MEMORY.ADDR10	21	22	MEMORY.ADDR10
I MEMORY.ADDR11	23	24	MEMORY.ADDR11
I MEMORY.ADDR12	25	26	MEMORY.ADDR12
I MEMORY.ADDR13	27	28	MEMORY.ADDR13
I MEMORY.ADDR14	29	30	MEMORY.ADDR14
I MEMORY.ADDR15	31	32	MEMORY.ADDR15
I MEMORY.ADDR16	33	34	MEMORY.ADDR16
I MEMORY.ADDR17	35	36	MEMORY.ADDR17
I MEMORY.ADDR18	37	38	MEMORY.ADDR18

Header 19X2

C

C

MEM_CONTROL_JUMPER

I MEMORY.UB	1	2	MEMORY.UB
I MEMORY.LB	3	4	MEMORY.LB
I MEMORY.WRITE	5	6	MEMORY.WRITE
I MEMORY.ENABLE	7	8	MEMORY.ENABLE

Header 4X2

D

D

Title Memory (all alone in the moonlight?)		
Size A	Number	Revision version 1
Date: 11/4/2014	Sheet of	
File: C:\Users\...\SRAM.SchDoc	Drawn By:	