Exam 2: Floorplanner (Due 4/27/15)

1. Introduction

The physical placement of a circuit can significantly affect the power, performance and cost of a circuit. A poor placement can lead to unnecessarily long interconnects, resulting in additional delay and power consumption, and can even increase area due to interconnect routing congestion. Although interconnect length can sometimes be reduced at the expense of additional area (i.e. leaving some of the chip area uninhabited by transistors), this increases the cost of the chip.

Physical placement can be done at different levels of abstraction. The final physical layout of a circuit must be decided at the gate or even transistor level, but often the physical placement is determined early on at the module or subcircuit level. We call such abstract physical placement floorplanning.

In this exam you are asked to write a floorplanning program. The inputs, outputs, and evaluation metrics for your floorplanner will be explained in the rest of this document. You will evaluate your program using a set of floorplanning benchmarks we will provide to you.

2. Problem Description

For this exam we will consider the hard block floorplanning problem. A hard block is a module that has a fixed size and shape. We will assume that all blocks are rectangles, so this means each block has a fixed width and height. We will assume that the interconnection netlist consists of I/O pins (called terminals) and blocks, and the connection to each block is made at its center. The goal of this floorplanning problem is to fix the location of each block and each terminal so as to minimize the total wirelength and the total area of the floorplan. The formal problem description is given below.

Let $\mathcal{P}$ be a set of *m* terminals and let $\mathcal{B}$ be a set of *n* blocks. Let **w** and **h** be the block width and height vector respectively, each containing *n* elements such that w_i and h_i are the width and height of block *i*. Terminals and blocks are connected together by nets. Let a net be a set of two or more elements from $\mathcal{P}$ and $\mathcal{B}$. The number of elements in a net defines the degree of that net. The wirelength of a net is defined as the half perimeter (i.e. width plus height) of the smallest rectangle that encloses the center point of all members of the net. Let $\mathcal{L}$ be a netlist, which is a set of nets. The total wirelength of a netlist is the sum of the wirelengths of all nets contained in a netlist.

The objective of the floorplanning problem is to determine the position vectors for terminals $\mathbf{x}_p$, $\mathbf{y}_p$ and the position vectors for blocks $\mathbf{x}_b$, $\mathbf{y}_b$ such that total wirelength and chip area are minimized and no overlap exists between blocks. Additionally a minimum distance *s* between terminals must be enforced. Distance between two pins is defined as the half perimeter of the smallest rectangle enclosing both pins (i.e. the Manhattan distance). Position vectors represent the position of the lower left corner of each block, or the position of each terminal. The chip area is defined as the area of the smallest rectangle that encloses all blocks in $\mathcal{B}$. Terminals are considered as points, and thus have no area, but are constrained to be placed along the edge of the smallest rectangle that encloses all the blocks (i.e. along the edge of the chip).

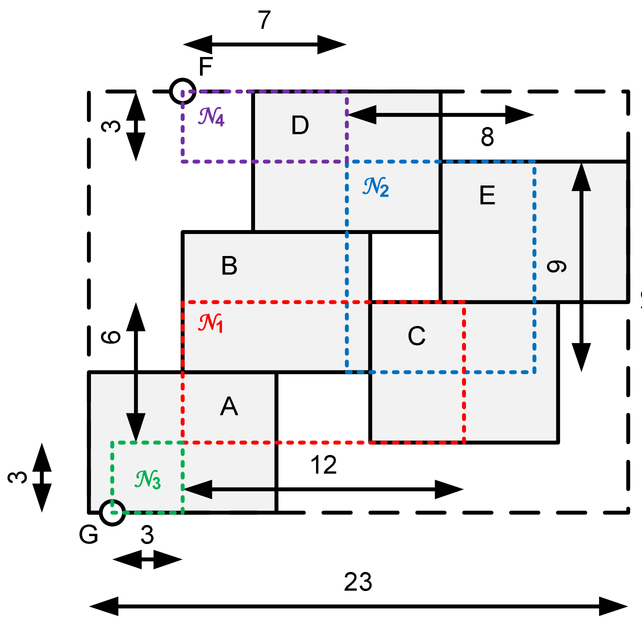
To re-emphasize the problem, the following three constraints must be enforced:

- No overlap between blocks
- Minimum distance *s* between pins
- Pins must all be located along the edge of the chip

The metrics used to evaluate a floorplans quality are:

- The area of the smallest rectangle that encloses all blocks
- The sum of the half perimeter wire length of each net

An example floorplan with the respective floorplan data is shown in Figure 1.



$\mathcal{B}$={A B C D E}
$\mathcal{P}$={F G}
$\mathcal{L}=\{\mathcal{N}_1\ \mathcal{N}_2\ \mathcal{N}_3\ \mathcal{N}_4\}$
$\mathcal{N}_1$={A B C}
$\mathcal{N}_2$={C D E}
$\mathcal{N}_3$={A G}
$\mathcal{N}_4$={D F}
w=[8 8 8 8 8]
h=[6 6 6 6 6]
$\mathbf{x_b}$=[0 4 12 7 15]
$\mathbf{y_b}$=[0 6 3 12 9]
$\mathbf{x_p}$=[4 1]
$\mathbf{y_p}$=[18 0]
$WL(\mathcal{N}_1)=6+12=18$
$WL(\mathcal{N}_2)=8+9=17$
$WL(\mathcal{N}_3)=3+3=6$
$WL(\mathcal{N}_4)=3+7=10$
$WL(\mathcal{L})=18+17+6+10=51$
$A=23*18=414$

Figure 1 - Example Floorplan

3. Input Format

The input to the floorplanner will be two text files. The first is a `*.blocks` file which defines the number of blocks and terminals, the names of blocks and terminals, and the size of blocks. The second file is a `*.nets` file which defines the number of nets, the degree of each net, and the members (blocks and/or pins) of each net. Additionally it defines the number of pins, which is the sum of degree across all nets. Below an example `*.blocks` and `*.nets` file is given for the example from Figure 1.

```
NumSoftRectangularBlocks : 0
NumHardRectilinearBlocks : 5
NumTerminals : 2

A hardrectilinear 4 (0, 0) (0, 6) (8, 6) (8, 0)
B hardrectilinear 4 (0, 0) (0, 6) (8, 6) (8, 0)
C hardrectilinear 4 (0, 0) (0, 6) (8, 6) (8, 0)
D hardrectilinear 4 (0, 0) (0, 6) (8, 6) (8, 0)
E hardrectilinear 4 (0, 0) (0, 6) (8, 6) (8, 0)

F terminal
G terminal
```

Figure 2 - example.blocks

```
NumNets : 4
NumPins : 10
NetDegree : 3
A B
B B
C B
NetDegree : 3
C B
D B
E B
NetDegree : 2
A B
G B
NetDegree : 2
D B
F B
```

Figure 3 - example.nets

Figure 2 defines the number of soft and hard blocks (we only use hard blocks in this exam) and the number of terminals. The shape of each block is defined as a set of points. Since we only consider blocks that are rectangles, each block will have type "rectilinear 4" meaning a rectilinear shape defined by four points (i.e. a rectangle). The size of each hard block is given as a set of (*x*,*y*) points defining the lower left, upper left, upper right, and lower right corner of each block when it is positioned at the origin. The upper right corner of each block defines its width and height. Finally the terminals are declared.

Figure 3 defines the number of nets, the number of pins (the sum of degree across all nets), and then describes each net. Each net has a defined degree, followed by a list of member blocks and terminals. Each block or terminal name is followed by the letter "B" which can be ignored for this exam.

4. Output Format

The output of the floorplanner should be a `*.pl` text file which lists each block followed by the (*x*,*y*) value of the lower left corner, and each terminal followed by its (*x*,*y*) value. An example is shown below.

```
A      0      0
B      4      6
C      12     3
D      7      12
E      15     9

F      4      18
G      1      0
```

Figure 4 - example.pl

5. Metrics

The metrics used to evaluate the quality of a floorplan will be total wire length (WL) and area (A). Furthermore we will include program runtime as a metric to evaluate the quality of the software. A MATLAB script and the corresponding functions have been uploaded to help you check your floorplan to see if it violates any constraints, and to report the area and wirelength. You will need to measure the runtime of your code on your own using the appropriate function calls in whatever language and/or operating system you decided to code with.

6. Benchmarks

A set of six benchmarks (i.e. pairs of `*.blocks` and `*.nets` files) have been posted on ELMS. They range in size from 10 to 300 blocks. The metrics generated by running your floorplanner on these benchmarks will be used to determine your Exam 2 grades. You must enforce a minimum distance between terminals *s*=2.

7. Deliverables

- **Source code** of your floorplanner. If written in a language that must be compiled, make sure it compiles on `glue`. Please include a README file describing how to compile if there is anything unusual about the way you compile.
- **Report** explaining how your floorplanner works including algorithms and data structures. Please include figures when helpful to explain. Include a table showing the three metrics for each benchmark in the results section, and try to offer some constructive discussion about the results, and how you think they could be improved. Please include a figure of each floorplan you generate using the provided MATLAB script for plotting your floorplan.
- **Floorplan Results** (i.e. `*.pl` files for each benchmark)