Zadaća 1 LD - Daris Mujkić 19413

Zadatak 1.

1.Identifikacija I imenovanje ulaznih i izlaznih promjenjivih:

Kolo ima dva trobitna ulaza A i B, te četverobitni izlaz R.

2.Definisanje tabele istine:

A[2..0] B[2..0] | R[3..0]

~~~~~~~~~~~~~~~~~~~~~~~~~

000 000 | ----

000 001 | 0000

000 010 | ----

000 011 | ----

000 100 | ----

000 101 | ----

000 110 | ----

000 111 | ----

001 000 | 0000

001 001 | ----

001 010 | ----

001 011 | ----

001 100 | ----

001 101 | ----

001 110 | ----

001 111 | ----

010 000 | ----

010 001 | ----

010 010 | ----

010 011 | ----

010 100 | ----

010 101 | ----

010 110 | ----

010 111 | 1110
~~~~~~~~~~~~~~~~~~~~~~~~~

011 000 | ----
011 001 | ----
011 010 | ----
011 011 | ----
011 100 | ----
011 101 | ----
011 110 | 1010
011 111 | ----
100 000 | ----
100 001 | ----
100 010 | ----
100 011 | ----
100 100 | ----
100 101 | ----
100 110 | ----
100 111 | ----
101 000 | ----
101 001 | ----
101 010 | ----
101 011 | ----
101 100 | ----
101 101 | ----
101 110 | ----
101 111 | ----
110 000 | ----
110 001 | ----
110 010 | ----
110 011 | 1010
110 100 | ----
110 101 | ----
110 110 | ----
110 111 | ----
111 000 | ----

111 001 | ----

111 010 | 1110

111 011 | ----

111 100 | ----

111 101 | ----

111 110 | ----

111 111 | ----

3.Minimizacije logičkih izraza:

Output Expressions (double-click to edit):

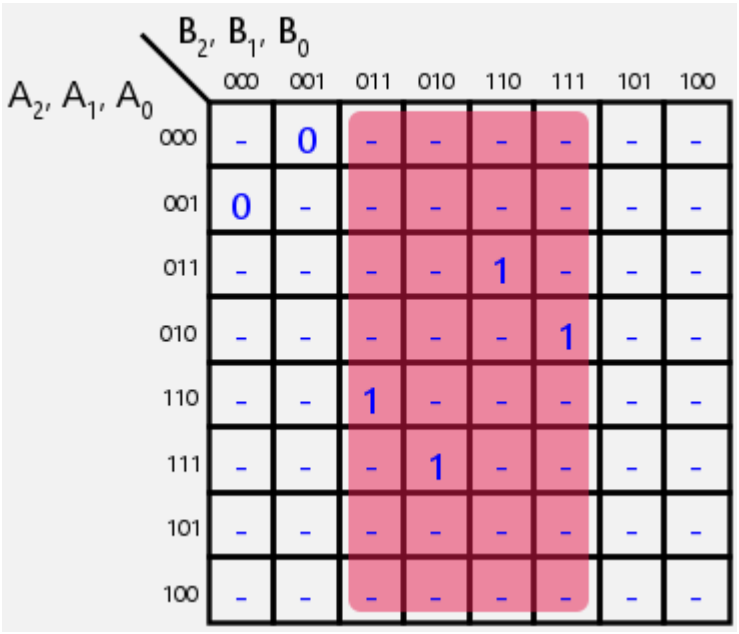
$$R_3 = B_1$$

$$R_2 = \overline{B_2}\cdot B_1\cdot\overline{B_0}+\overline{A_2}\cdot\overline{A_0}\cdot B_1$$

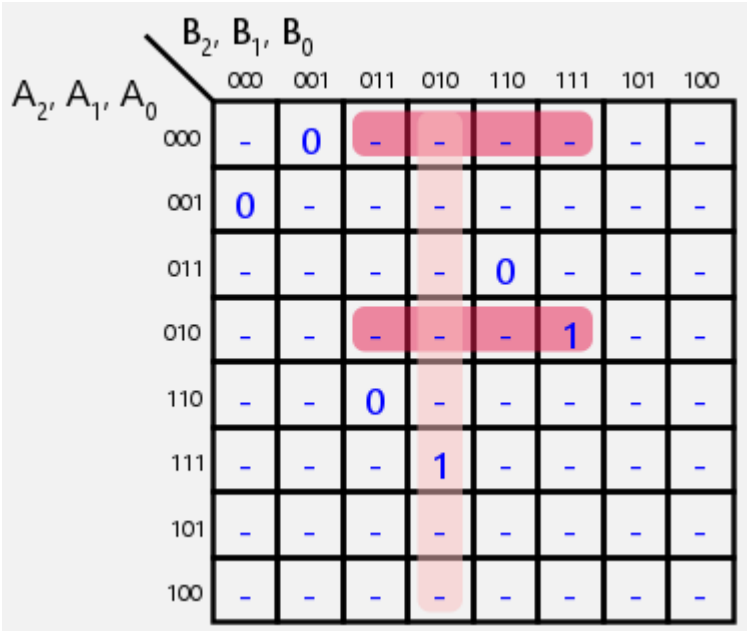
$$R_1 = B_1$$

$$R_0 = 0$$

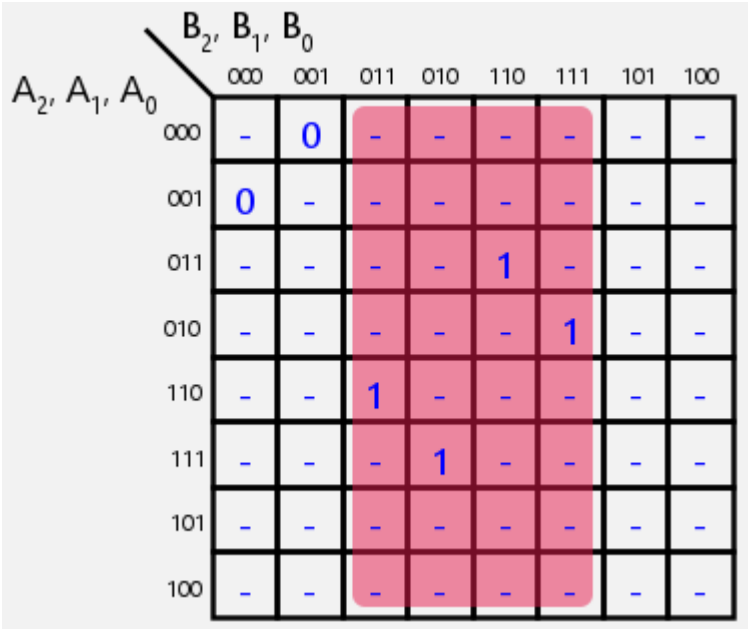
R3:



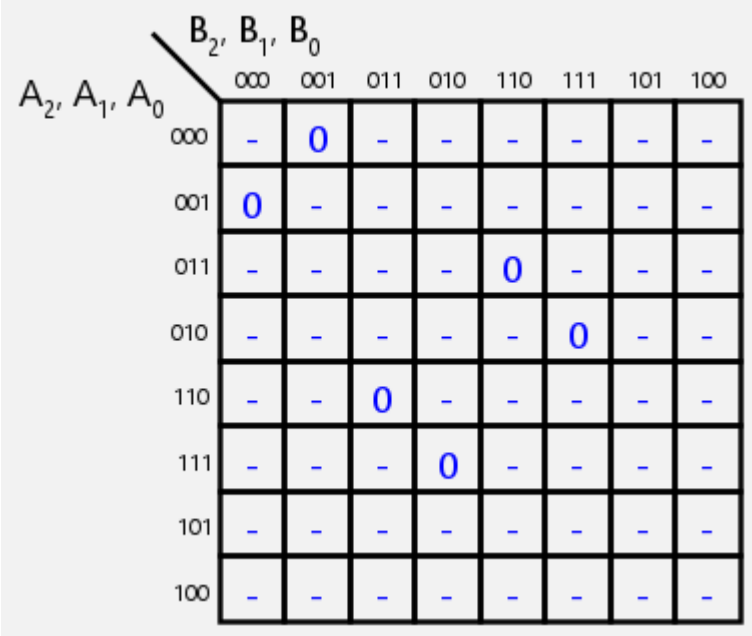
R2:


B2, B1, B0
A2, A1, A0
000 001 011 010 110 111 101 100
000 - 0 - - - - - -
001 0 - - - - - - -
011 - - - - 0 - - -
010 - - - - - 1 - -
110 - - 0 - - - - -
111 - - - 1 - - - -
101 - - - - - - - -
100 - - - - - - - -

R1:


B2, B1, B0
A2, A1, A0
000 001 011 010 110 111 101 100
000 - 0 - - - - - -
001 0 - - - - - - -
011 - - - - 1 - - -
010 - - - - - 1 - -
110 - - 1 - - - - -
111 - - - 1 - - - -
101 - - - - - - - -
100 - - - - - - - -

R0:



4.Crtanje sheme (Logisim)

Zadatak 2.

1.Identifikacija I imenovanje ulaznih i izlaznih promjenjivih:

Kolo ima jedan četverobitni ulaz U u EXCESS-3 BCD format i sedmosegmentni displej (izlazi A, B, C, D, E, F, G), diode se pale visokim naponskim nivoom.

2.Definisanje tabele istine:

Ulaz[3..0] | A B C D E F G

~~~~~~~~~~~~~~~~~~~~~~~~~~~~

0000 | - - - - - - -

0001 | - - - - - - -

0010 | - - - - - - -

0011 | 1 1 1 1 1 1 0

0100 | 0 1 1 0 0 0 0

0101 | 1 1 0 1 1 0 1

0110 | 1 1 1 1 0 0 1

0111 | 0 1 1 0 0 1 1

1000 | 1 0 1 1 0 1 1
~~~~~~~~~~~~~~~~~~~~~~~~~~~~

1001 | 1 0 1 1 1 1 1

1010 | 1 1 1 0 0 0 0

1011 | 1 1 1 1 1 1 1

1100 | 1 1 1 1 0 1 1

1101 | - - - - - - -

1110 | - - - - - - -

1111 | - - - - - - -

3.Minimizacije logičkih izraza:

Output Expressions (double-click to edit):

$A = \overline{Ulaz_2}+\overline{Ulaz_1}\cdot Ulaz_0+Ulaz_1\cdot\overline{Ulaz_0}+Ulaz_3$

$B = \overline{Ulaz_2}\cdot Ulaz_1+Ulaz_2\cdot\overline{Ulaz_1}+\overline{Ulaz_3}\cdot Ulaz_1$

$C = \overline{Ulaz_2}+\overline{Ulaz_0}+Ulaz_1$

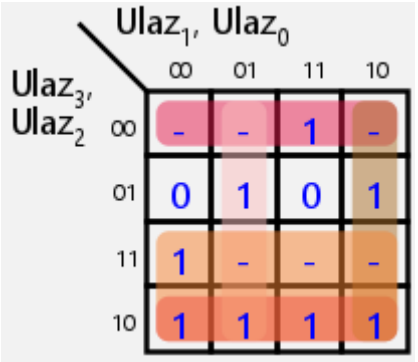
$D = \overline{Ulaz_1}\cdot Ulaz_0+\overline{Ulaz_3}\cdot Ulaz_1\cdot\overline{Ulaz_0}+Ulaz_3\cdot\overline{Ulaz_1}+\overline{Ulaz_2}\cdot Ulaz_0$

$E = \overline{Ulaz_2}\cdot Ulaz_0+\overline{Ulaz_1}\cdot Ulaz_0$

$F = Ulaz_1\cdot Ulaz_0+Ulaz_3\cdot\overline{Ulaz_1}$

$G = Ulaz_2\cdot Ulaz_0+Ulaz_2\cdot Ulaz_1+Ulaz_3\cdot Ulaz_0+Ulaz_3\cdot\overline{Ulaz_1}$

a) A preko 2u1 MUX, A:

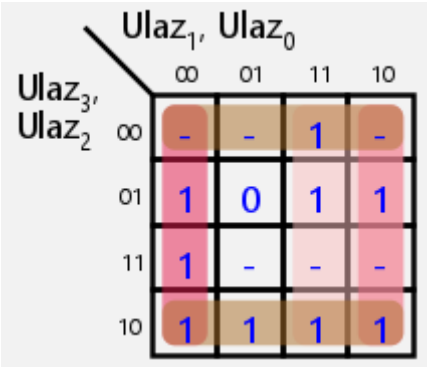


b) B sa 8u1 MUX

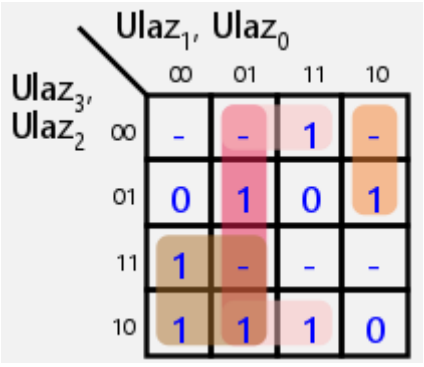
Za kontrolne uzimamo U3, U2, U1:

Ulaz[3..0]	A	B	C	D	E	F	G	
0 0 0 0	-	-	-	-	-	-	-	B_0
0 0 0 1	-	-	-	-	-	-	-	
0 0 1 0	-	-	-	-	-	-	-	B_1
0 0 1 1	1	1	1	1	1	1	0	
0 1 0 0	0	1	1	0	0	0	0	B_2
0 1 0 1	1	1	0	1	1	0	1	
0 1 1 0	1	1	1	1	0	0	1	B_3
0 1 1 1	0	1	1	0	0	1	1	
1 0 0 0	1	0	1	1	0	1	1	B_4
1 0 0 1	1	0	1	1	1	1	1	
1 0 1 0	1	1	1	0	0	0	0	B_5
1 0 1 1	1	1	1	1	1	1	1	
1 1 0 0	1	1	1	1	0	1	1	B_6
1 1 0 1	-	-	-	-	-	-	-	
1 1 1 0	-	-	-	-	-	-	-	B_7
1 1 1 1	-	-	-	-	-	-	-	

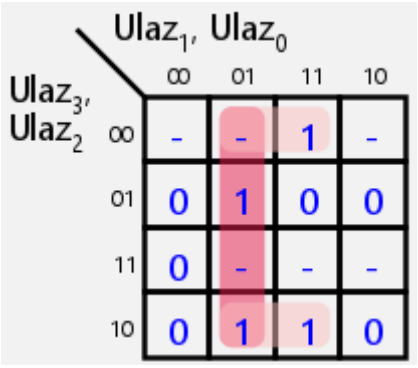
c) C preko minimalnih logičkih kola



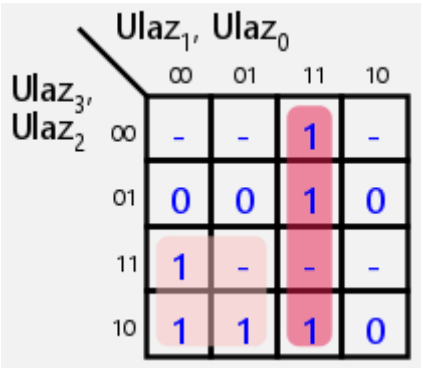
d) D koristeći minimalan broj NILI kola



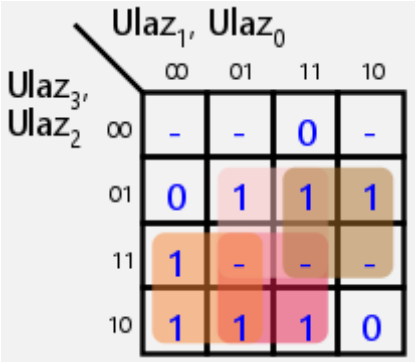
e) E koristeći minimalan broj NI kola



f) F koristeći minimalan broj osnovnih kola



g) G koristeći minimalan broj 4u1 MUX



4.Crtanje sheme (Logisim)

Zadatak 3.

1.Identifikacija I imenovanje ulaznih i izlaznih promjenjivih:

Kolo ima ulaze A i B, te Cin za oduzimanje. Izlazi su Izlaz i Cout.

2.Definisanje tabele istine:

A B Cin | Cout Izlaz

~~~~~~~~~~~~~~~~~~~~

0 0 0 | 0 0

0 0 1 | 1 1
~~~~~~~~~~~~~~~~~~~~

0 1 0 | 1 1

0 1 1 | 1 0

1 0 0 | 0 1

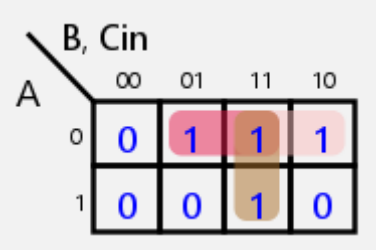
1 0 1 | 0 0

1 1 0 | 0 0

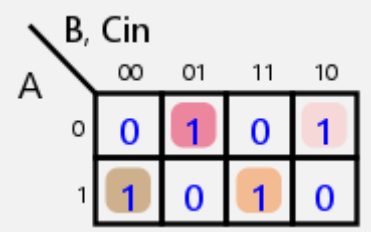
1 1 1 | 1 1

3.Minimizacije logičkih izraza:

Cout:



Izlaz:



Output Expressions (double-click to edit):

$Cout = \overline{A}\cdot Cin+\overline{A}\cdot B+B\cdot Cin$

$Izlaz = \overline{A}\cdot\overline{B}\cdot Cin+\overline{A}\cdot B\cdot\overline{Cin}+A\cdot\overline{B}\cdot\overline{Cin}+A\cdot B\cdot Cin$

4.Crtanje sheme (Logisim)

Zadatak 4.

1.Identifikacija I imenovanje ulaznih i izlaznih promjenjivih:

Kolo ima ulaze A i B, V i M, te izlaze V1 i M1.

2.Definisanje tabele istine:

A B V M | V1 M1

~~~~~~~~~~~~~~~~

0 0 0 0 | 0 0

0 0 0 1 | 0 1

0 0 1 0 | 1 0

0 0 1 1 | - -

0 1 0 0 | 0 1

0 1 0 1 | 0 1

0 1 1 0 | 0 1

0 1 1 1 | - -

1 0 0 0 | 1 0

1 0 0 1 | 1 0

1 0 1 0 | 1 0

1 0 1 1 | - -

1 1 0 0 | 0 0

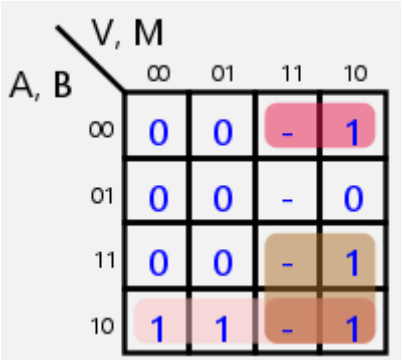
1 1 0 1 | 0 1

1 1 1 0 | 1 0

1 1 1 1 | - -

3.Minimizacije logičkih izraza:

V1:


~~~~~~~~~~~~~~~~

M1:

A, B \ V, M	00	01	11	10
00	0	1	-	0
01	1	1	-	1
11	0	1	-	0
10	0	0	-	0

Output Expressions (double-click to edit):

V1 = B+V+A+B+A+V+B+V+A+B+A+V

M1 = A+M+A+B+B+M+A+M+A+B+B+M

4.Crtanje sheme (Logisim)