CPSC 3300 Section 2 Tentative Schedule

Date	Topics	Reading	Assignment
1/9	Introduction / Overview	5th ed: Chp. 1.1-3	
1/14	Technologies, Performance and Power	Chp. 1.4-6	
1/16	Technologies, Performance and Power (Continued)	Chp. 1.6-7	HW1 assigned, due 1/30 before class
1/21	**Martin Luther King Jr. Day**		
1/23	Benchmarking	Chp. 1.8-11	
1/28	Combinational Logic	B. 1-4	
1/30	Adders	B. 5-6	**HW1 due** HW2 assigned, due 2/11 before class
2/4	Sequential Logic	B. 7-8	Project 1 available
2/6	Example devices and finite state machines	B. 10-11	
2/11	Review for Exam I		**HW2 due**
2/13	**Exam I**		
2/18	MIPS Instructions and Datapath	Chp. 4.1-3	
2/20	Datapath (Continued)		
2/25	Pipeline	Chp. 4.5-6	HW3 assigned, due 3/6 before class
2/27	Pipeline Hazards	Chp. 4.7-8	**Project 1 due (11:59 PM)**
3/4	Datapath with Branch Prediction	Chp. 4.8	Project 2 available
3/6	Datapath with Floating Point & Instruction Level Parallelism	Chp. 4.10	**HW3 due**, HW4 assigned (due 3/25 before class)
3/11	Instruction Level Parallelism (continued), Real Examples	Chp. 4.11-14	
3/13	Memory overview	Chp. 5.1-3	
3/16 – 3/24	**Spring Break**		
3/25	Basics of Caches		**HW4 due**
3/27	Review for Exam II		
4/1	**Exam II**		
4/3	Cache Performance	Chp. 5.4	**Project 2 due (11:59 PM)**, HW5 assigned (due 4/15 before class)
4/8	Cache Performance (Continued)		Project 3 available
4/10	Virtual Memory	Chp. 5.7	
4/15	Virtual Memory and replacement policy		**HW5 due**, HW6 assigned (due 4/24 before class)
4/17	Parallel Processing	Chp. 6.1-6.3	
4/22	Parallel Processing (Continued)		
4/24	Review for Final		**HW6 due**, **Project 3 due**
4/30	**Final Exam** Tuesday, April 30 7:00pm – 9:30pm		