GAPD HV System V02

V.Commichau[1]
Hp. von Gunten[2]

IPP/ETHZ

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[1] vcommichau@phys.ethz.ch
[2] vgunten@phys,ethz.ch

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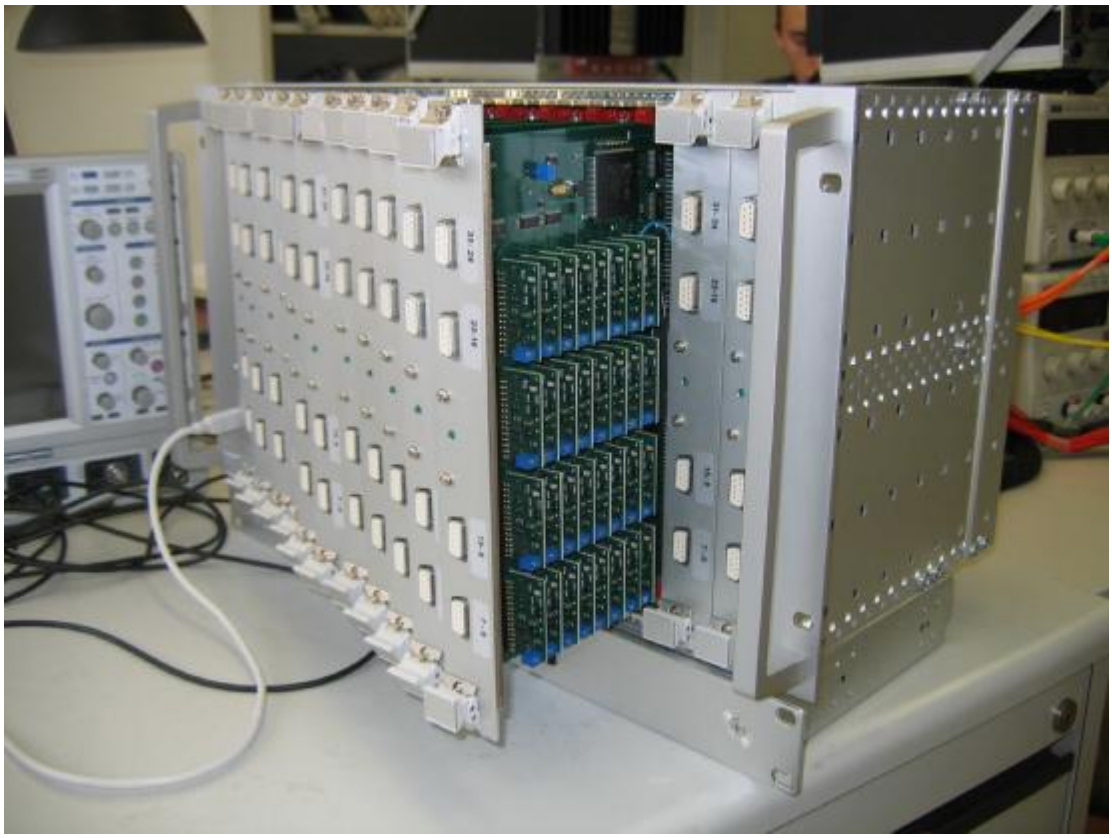
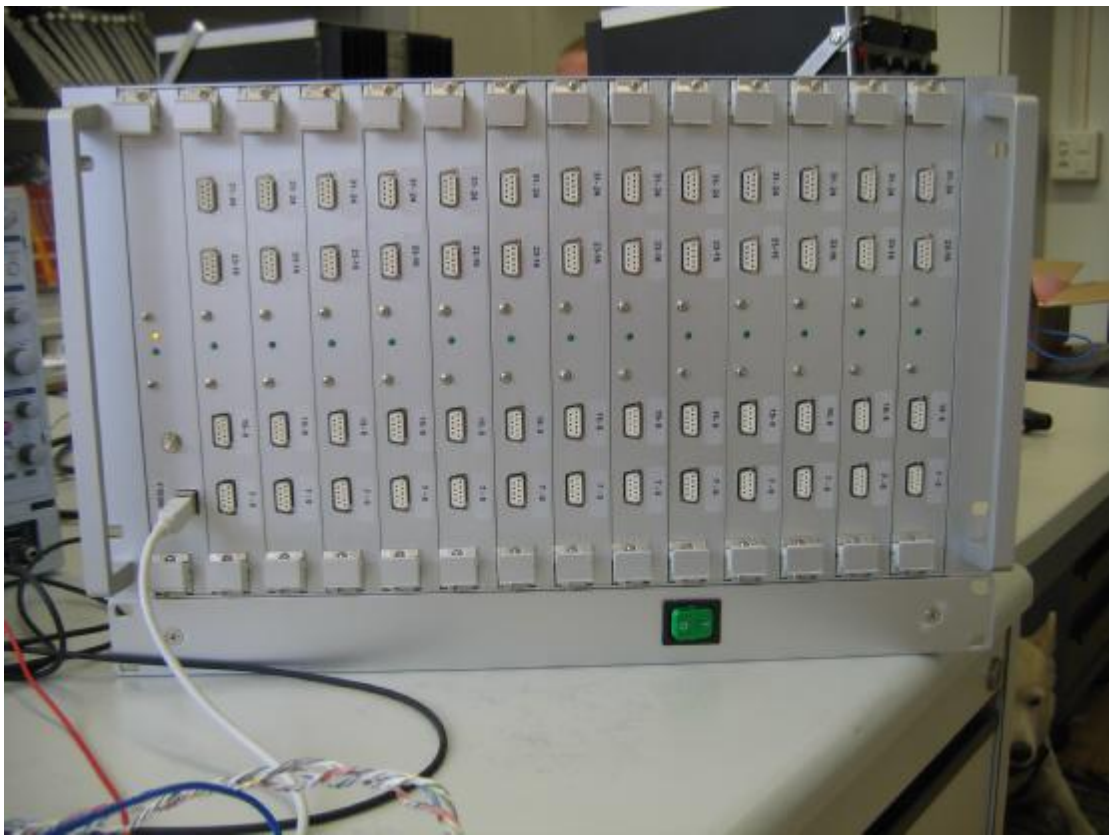
System Overview

The GAPD Bias Supply Unit Version 2 delivers 416 high voltage channels with an individual programmable output voltage between 5 to 90 VDC with a 12 bit digital resolution (~20mV step width). The maximal output current of each channel is limited to 4mA for the external circuit connected, 1mA is consumed by the single HV module itself, e.g. Imax = 5mA/channel. An individual current measurement is implemented for each single channel with a 12-bit resolution, which practically results in a 1% accuracy due to the channel regulation noise effects. The complete system is built in a double height VME like crate with 14 subunits (one system controller, thirteen 32 channel motherboard units). Below the crate a fan unit is mounted and delivers the necessary air flow for cooling. As separate part a HV power supply (Umin 95VDC, Imax 2Amp) has to be connected to the GAPD Bias Supply crate.

The programming of the device is done via one USB port connected to a PC. At the very beginning the PC software has to synchronize the USB port. Depending on the unknown number of dummy data transfers, which happens during the connecting and powering up the system between the PC and the bias supply system, one or two bytes may be send and not processed by the system controller, because of the fact, that the controller becomes active only after the third byte received.

A two times three bytes protocol serves for all different modes. A special feature are global commands, e.g. with only a three bytes data set one may make a system reset or loading all 416 channels to a specific output voltage. This way a smooth ramping, during start-up of the consumers connected is possible. Because of the load current for the filter capacitors, part of every GAPD preamplifier circuit, ramping is necessary. After ramping up close to a general set point, every channel may be adjusted to its own exact output voltage. On every access from the control program (three bytes send) the bias supply system responds with a three bytes output. Depending of the command, the data sent back deliver information of the system status. An incrementing wrap counter flags the correct basic device functionality. In case of a voltage write or status read of a single channel, further information of the actual current is sending back. In case of a single channel over current switch off an additional bit will be set, also in case of a manual activated system reset request (emergency shut down all output voltages) a separate data bit is set. The cycle time for a 3 bytes command and the 3 bytes send back from the device is ~50μs. Part of the final application software should be a permanent check of the manual reset/shut down request generated by one simple push button on the system controller front panel. This will be the only chance for an emergency shut down of all HV voltage outputs.





New gAPD HV Supply V02 USB Data Format

19.01.2010 V.Commichau IPP/ETHZ

Data to HV System

Byte 1	Byte 2	Byte 3

Output

D23	D22	D21	D20	D19	D18	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Function			Board					Channel				Voltage											

Input

D23	D22	D21	D20	D19	D18	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
S	W	W	W	D	D	D	D	D	D	D	D	D	D	D	D			Error			Board		

System Reset

D23	D22	D21	D20	D19	D18	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
0	**0**	**0**	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X

Data from Controller

Status S = 0 **Wrap Counter = WWW (n+1)**

D23	D22	D21	D20	D19	D18	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
0	W	W	W	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Read Channel Status & Current

D23	D22	D21	D20	D19	D18	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
0	**0**	**1**	A	A	A	A	C	C	C	C	C	X	X	X	X	X	X	X	X	X	X	X	X

Data from Controller **Status S = 0/1 OK/ Over Current @ Channel adressed**
Wrap Counter = WWW **Current = DDDDDDDDDDDD** **Board adressed = 0...12**

Case: no device **Wrap Counter = WWW (n+1)** **Status S = 0** **D=0** **Board adressed = 0...12**

D23	D22	D21	D20	D19	D18	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
0	W	W	W	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1		Board #		

Global Set **Voltage = DDDDDDDDDDDD**

D23	D22	D21	D20	D19	D18	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
0	**1**	**0**	X	X	X	X	X	X	X	X	X	D	D	D	D	D	D	D	D	D	D	D	D

Data from Controller

Status S = 0 **Wrap Counter = WWW (n+1)**

D23	D22	D21	D20	D19	D18	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
0	W	W	W	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Channel set to Voltage DDDD **Bord # = AAAA** **Channel # = CCCCC** **Voltage = DDDDDDDDDDDD**

D23	D22	D21	D20	D19	D18	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
0	**1**	**1**	A	A	A	A	C	C	C	C	C	D	D	D	D	D	D	D	D	D	D	D	D

Data from Controller

Status S = 0/1 OK/ Over Current @ Channel **Wrap Counter = WWW** **Current = DDDDDDDDDDDD** **Board adressed = 0...12**

D23	D22	D21	D20	D19	D18	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
S	W	W	W	D	D	D	D	D	D	D	D	D	D	D	D	0	0	0	0		Board #		

Case: no device **Wrap Counter = WWW (n+1)** **Status S = 0** **D=0** **Board adressed = 0...12**

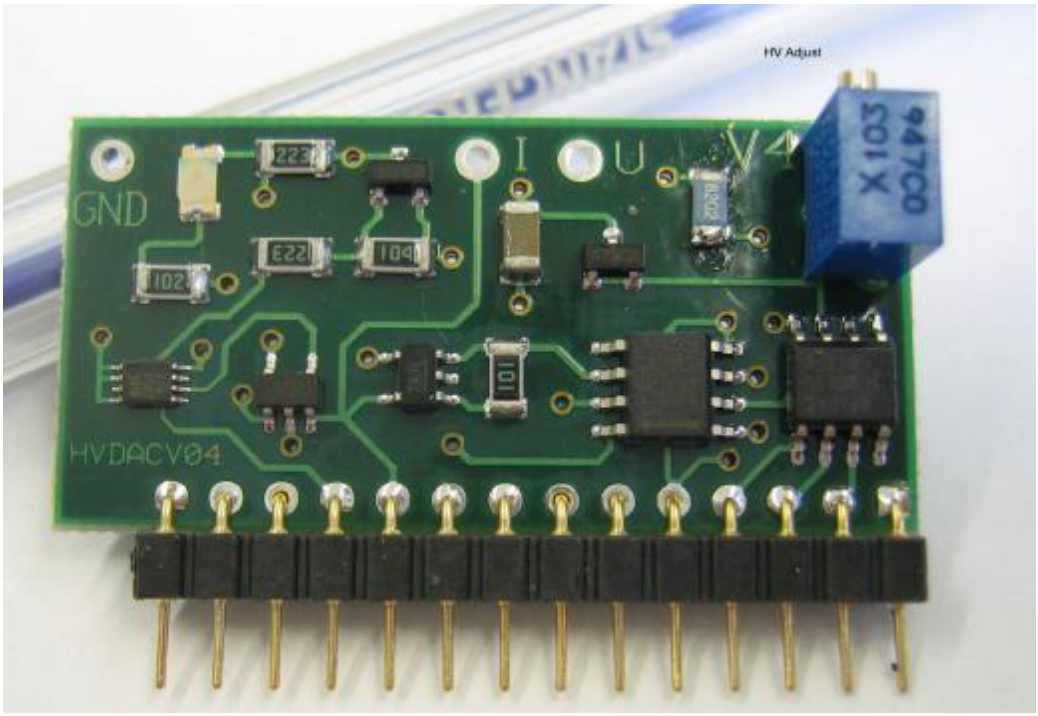
D23	D22	D21	D20	D19	D18	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
0	W	W	W	0	0	0	0	0	0	0	0	0	0	0	0	0	**1**	**1**	**1**		Board #		

Case: HV down request **Wrap Counter = WWW (n+1)** **Status S = 0** **D=0** **Board adressed = 0...12**

D23	D22	D21	D20	D19	D18	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
0	W	W	W	0	0	0	0	0	0	0	0	0	0	0	0	**1**	0	0	0		Board #		

HV down request generated by manual reset push button at controller frontpanel.

Basic HV Module



A high voltage opamp (OPA454) is controlled via a 12-bit Digital Analogue Converter (DAC8043U). The DAC is controlled via a 12-bit serial data protocol. An external precise –10VDC source is connected to the DAC reference voltage input. The DAC delivers, depending on the data loaded, an output current to the inverting input of the opamp. The opamp compensates the input current by raising it output voltage to the corresponding value. The output current of the opamp (sum of internal and consumer depending load current) is measurement by a high side current monitor (HV7800). The output voltage of this current monitor is compared with an external adjustable voltage (0.1 – 0.5VDC ≅ 1 – 5mA) by a comparator circuit (MAX4480). The comparator activates, in case of an over current situation, a single flip flop (74LVCG74). The output of this flip-flop is connected to the en/disable input of the opamp. This way the high voltage opamp may be deactivated, e.g. the output voltage is set to zero, independent of the DAC output current. In case the over current situation has gone, an external reset command (by software, no manual reset push button!) to the flip flop reactivates the opamp and the original high voltage value will be recovered. The calibration of a single HV module may be done by loading the full scale value to the DAC, measuring the output voltage with a precise DVM and adjusting the output voltage to the exact value of 90.00VDC.

The HV module requires five external supply voltages. +5VDC, -5VDC, -10VDC, +0.1 – 0.5VDC and +95VDC. The HV output may be short circuited for an unlimited time. For maintenance time a SMD LED display on every single HV module a over current event. The HV opamps have their own over temperature monitoring and shut down capability.

32 Channel Motherboard

The 32 channel motherboard is connected via a special defined bus system to the system controller. On the motherboard 32 HV modules are mounted via separate 14 pin single line connectors. All potentiometers for the final adjustment are easily accessible using a bus extender card for this procedure. A PLD (Xilinx XC95108-10-PC84) serves for the local data decoding, serial data transfer, status reading&writing and the ADC control for the current measurement. Every motherboard has its own unique address, set by a 4 bit DIP switch. A specific bus line is activated by the board addressed as an acknowledge to the system controller. This way the correct basic function of a motherboard may be checked. A local xtal oscillator of 10Mhz delivers the clock for the PLD.
The PLD decodes the function control bits sent by the system controller and depending on their settings it will send the serial data to one specific HV module. After the transfer to the DAC the over current status and the actual current of the HV channel addressed, converted by a local 12 bit ADC (AD7476ARTZ), are sent back to the system controller. In case of a global write command the PLD addresses all 32 HV modules and loads all DAC with the same data and does not sent back any data. A system reset command sent by the controller will reset the PLD and clears all over current flip flops of the HV modules. A LED on the font panel displays a board activity (write&read).
The motherboard is fed via a second 96 pin connector with the supply voltages +5VDC, +12VDC and –12VDC. A local voltage regulator produces from the primary negative 12V source the –5V required. The precise –10VDC reference voltage for all 32 HV modules is built around a precision voltage reference circuit (ADR01AR) in addition with a power stage to have low impedance reference voltage source for 32 HV modules. All 32 HV outputs are accessible via this 96 pin connector.

System Controller

The system controller links the USB port to the 13 motherboards. A local oscillator of 10Mhz drives the PLD (XILINX XC95-216 -10-PQ160I). The USB port is used as separate commercial unit UM245R built around the FT245R. On a three byte data transfer via USB the controller reads and stores the bytes. Then a decoding phase is started and depending on the command type the relevant action is started. The special function bits, the motherboard and the HV channel address are set on the bus system. Now the HV data send by the PC program are send as serial data stream to the bus system. Depending on the command, global or single channel, the mother board reacts by sending the data to all or one specific HV channel. In case of a global command the controller does not expect data returned from any board addressed, therefore a local data set is generated, e.g. over current equal zero, wrap counter incremented, manual reset request copied and all other data set to zero. In case of a single channel access, there are two different modes. For a single channel write, the output of the controller delivers information on the over current status, wrap counter increment, actual current, manual reset request, a flag for a non existent board and the board address used. In case of a relevant voltage change, one should keep in mind, the measured current will not be the real final value, because of some time constants in the supply and signal filtering path. For a precise current reading one should use the read single channel command.

All bus signals from and to the controller are isolated via fast opto couplers. This way all 416 HV outputs are floating.

The controller has a single +5VDC supply. One LED at its front panel show a USB/bus activity. A second LED is driven by a special logic, which checks the presence of all low voltages for the 32 channel mother boards. In case one voltage fails, the high voltage output will not be enabled. This function was implemented, because of a possible damage of the HV modules.

Connectors for a mezzanine board to be mounted on the system controller are foreseen. This mezzanine board may have a MCU to handle a different serial protocol (RS485, RS422), which will be used instead of the UM245R USB link. The serial I/O then may be done via a 4 pin rear connector.

Part of the final application software should be a permanent check of the manual reset/shut down request generated by one simple push button on the system controller front panel. This activity could not be implemented in the controller PLD software, because of the absolutely asynchronous data transfer between the controlling PC and the system controller.

Crate Controller
Bus Signals

Pin	Signal	Source	Function	Destination
C1	CTR_CK	Crate Controller	DAC CLK	HV Boards
C2	CTRL_DATA	Crate Controller	DAC DATA	HV Boards
C3	CTRL_LOAD	Crate Controller	DAC Select	HV Boards
C4	CTRL_A0	Crate Controller	Chann. Adr. A0	HV Boards
C5	CTRL_A1	Crate Controller	Chann. Adr. A1	HV Boards
C6	CTRL_A2	Crate Controller	Chann. Adr. A2	HV Boards
C7	CTRL_A3	Crate Controller	Chann. Adr. A3	HV Boards
C8	CTRL_A4	Crate Controller	Chann. Adr. A4	HV Boards
C9	CTRL_BD0	Crate Controller	Board Adr. B0	HV Boards
C10	CTRL_BD1	Crate Controller	Board Adr. B1	HV Boards
C11	CTRL_BD2	Crate Controller	Board Adr. B2	HV Boards
C12	CTRL_BD3	Crate Controller	Board Adr. B3	HV Boards
C13	CTRL_SPB0	Crate Controller	Spec. Bit 0	HV Boards
C14	CTRL_SPB1	Crate Controller	Spec. Bit 1	HV Boards
C15	CTRL_SPB2	Crate Controller	Spec. Bit 2	HV Boards
C16	CTRL_RESET	Crate Controller	Reset	HV Boards
C17	OUT_LOAD	Active Board	Select	Crate Controller
C18	OUT_CLK	Active Board	Clock	Crate Controller
C19	OUT_DATA	Active Board	Data	Crate Controller
C20	BDACTIVE	Active Board	Board Ackn.	Crate Controller
C21	BDACTIVE_0	Active Board	TBD	Crate Controller
C22	BDACTIVE_1	Active Board	TBD	Crate Controller
C23	BDACTIVE_2	Active Board	TBD	Crate Controller
C24	BDACTIVE_3	Active Board	TBD	Crate Controller
C25	AGND	SLAVE PS	SLAVE GND	HV Boards
C26 - 27	+12V	SLAVE PS	SLAVE +12V	HV Boards
C28 - 29	-12V	SLAVE PS	SLAVE –12V	HV Boards
C30 – 32	+90V	SLAVE PS	SLAVE HV	HV Boards
A1 – 2	AGND	SLAVE PS	SLAVE GND	HV Boards
A3 – 16	+5V	SLAVE PS	SLAVE +5V	HV Boards
A17 – 25	AGND	SLAVE PS	SLAVE GND	HV Boards
A26 –27	+12V	SLAVE PS	SLAVE +12V	HV Boards
A28 - 29	-12V	SLAVE PS	SLAVE –12V	HV Boards
A30 – 32	+90V	SLAVE PS	SLAVE HV	HV Boards

Crate Controller
Power Connector

Pin	Voltage	Pin	Voltage	Pin	Voltage
A1	VCC	B1	+5V	C1	VCC
A2	VCC	B2	+5V	C2	VCC
A3	VCC	B3	+5V	C3	VCC
A4	GND	B4	+5V	C4	GND
A5	GND	B5	+5V	C5	GND
A6	GND	B6	+5V	C6	GND
A7	+5V	B7	+5V	C7	+5V
A8	+5V	B8	+5V	C8	+5V
A9	+5V	B9	+5V	C9	+5V
A10	+5V	B10	+5V	C10	+5V
A11	+5V	B11	+5V	C11	+5V
A12	+5V	B12	+5V	C12	+5V
A13	+5V	B13	+5V	C13	+5V
A14	-12V	B14	-12V	C14	-12V
A15	-12V	B15	-12V	C15	-12V
A16	+12V	B16	+12V	C16	+12V
A17	+12V	B17	+12V	C17	+12V
A18	AGND	B18	AGND	C18	AGND
A19	AGND	B19	AGND	C19	AGND
A20	AGND	B20	AGND	C20	AGND
A21	AGND	B21	AGND	C21	AGND
A22	AGND	B22	AGND	C22	AGND
A23	AGND	B23	AGND	C23	AGND
A24	AGND	B24	AGND	C24	AGND
A25	AGND	B25	AGND	C25	AGND
A26	AGND	B26	AGND	C26	AGND
A27	+90VIN	B27	+90VIN	C27	+90VIN
A28	+90VIN	B28	+90VIN	C28	+90VIN
A29	+90VIN	B29	+90VIN	C29	+90VIN
A30	+90VIN	B30	+90VIN	C30	+90VIN
A31	USB_+5	B31	+90VIN	C31	USB_D+
A32	USB_D-	B32	+90VIN	C32	USB_GND

Crate Controller
Signal Functions

Signal	Function	Source/Destination
A0	Slave DAC Adr. A0	To Bus
A1	Slave DAC Adr. A1	To Bus
A2	Slave DAC Adr. A2	To Bus
A3	Slave DAC Adr. A3	To Bus
A4	Slave DAC Adr. A4	To Bus
Load	Slave DAC load	To Bus
Data	Slave DAC Data	To Bus
CK	Slave DAC Clock	To Bus
MAN Res	Manuel Reset	=> PLD
BUSY	Activity Display	PLD =>Timer & LED
CLOCK	Main Oscillator	=> PLD
RES	Reset	=> PLD
WR#	USB Write	UM245R
RST#	NC	UM245R
TXE#	USB Empty Flag	UM245R
RXF#	USB Data Flag	UM245R
RD#	USB Read	UM245R
PWE#	NC	UM245R
DB0 – DB7	USB Data I/O	PLD **ó** UM245R
BDACTIVE 0	From active Slave	=> PLD
BDACTIVE 1	From Slave (TBD)	=> PLD
BDACTIVE 2	From Slave (TBD)	=> PLD
BDACTIVE 3	From Slave (TBD)	=> PLD
BDACTIVE LOW	Slave Acknowledge	=> PLD
SL_LOAD	From active Slave	LOAD to PLD
SL_CLK	From active Slave	CLOCK to PLD
SL_DATA	From active Slave	DATA to PLD
RESET	To all Slaves	Bus
SPB 0	To all Slaves	Bus
SPB 1	To all Slaves	Bus
SPB 2	To all Slaves	Bus
BD 0	Slave Board Adr. 0	Bus
BD 1	Slave Board Adr. 1	Bus
BD 2	Slave Board Adr. 2	Bus
BD 3	Slave Board Adr. 3	Bus

Crate Controller link to optional MCU

J4

Pin	Signal
1	RESET, low active
2	GND
3	VCC
4	VCC
5	VCC
6	GND
7	GND
8	GND

J5

Signal	Function	Source/Destination
MCU_0	TBD	PLD **ó** MCU
MCU_1	TBD	PLD **ó** MCU
MCU_2	TBD	PLD **ó** MCU
MCU_3	TBD	PLD **ó** MCU
MCU_4	TBD	PLD **ó** MCU
MCU_5	TBD	PLD **ó** MCU
MCU_6	TBD	PLD **ó** MCU
MCU_7	TBD	PLD **ó** MCU
MCU_8	TBD	PLD **ó** MCU
MCU_9	TBD	PLD **ó** MCU
MCU_10	TBD	PLD **ó** MCU
MCU_11	TBD	PLD **ó** MCU
MCU_12	TBD	PLD **ó** MCU
MCU_13	TBD	PLD **ó** MCU
MCU_14	TBD	PLD **ó** MCU
MCU_15	TBD	PLD **ó** MCU

J6

Pin	Signal
1	USB_+5
2	USB_D-
3	USB_D+
4	USB_GND

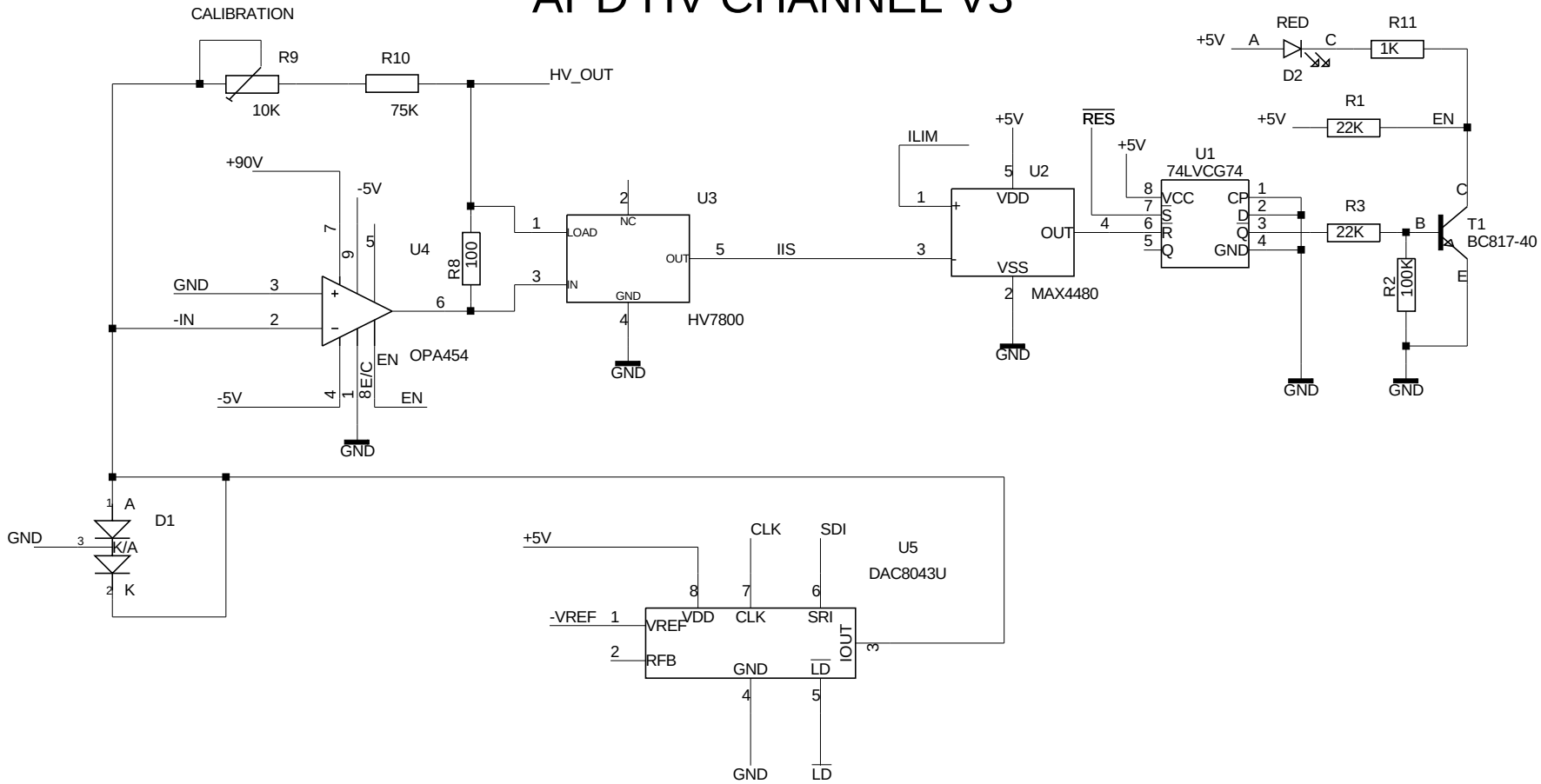
HV Board
Bus Signals

Pin	Signal	Source	Function	Destination
C1	CTR_CK	Crate Controller	DAC CLK	HV Boards
C2	CTRL_DATA	Crate Controller	DAC DATA	HV Boards
C3	CTRL_LOAD	Crate Controller	DAC Select	HV Boards
C4	CTRL_A0	Crate Controller	Chann. Adr. A0	HV Boards
C5	CTRL_A1	Crate Controller	Chann. Adr. A1	HV Boards
C6	CTRL_A2	Crate Controller	Chann. Adr. A2	HV Boards
C7	CTRL_A3	Crate Controller	Chann. Adr. A3	HV Boards
C8	CTRL_A4	Crate Controller	Chann. Adr. A4	HV Boards
C9	CTRL_BD0	Crate Controller	Board Adr. B0	HV Boards
C10	CTRL_BD1	Crate Controller	Board Adr. B1	HV Boards
C11	CTRL_BD2	Crate Controller	Board Adr. B2	HV Boards
C12	CTRL_BD3	Crate Controller	Board Adr. B3	HV Boards
C13	CTRL_SPB0	Crate Controller	Spec. Bit 0	HV Boards
C14	CTRL_SPB1	Crate Controller	Spec. Bit 1	HV Boards
C15	CTRL_SPB2	Crate Controller	Spec. Bit 2	HV Boards
C16	CTRL_RESET	Crate Controller	Reset	HV Boards
C17	OUT_LOAD	Active Board	Select	Crate Controller
C18	OUT_CLK	Active Board	Clock	Crate Controller
C19	OUT_DATA	Active Board	Data	Crate Controller
C20	BDACTIVE	Active Board	Board Ackn.	Crate Controller
C21	BDACTIVE_0	Active Board	TBD	Crate Controller
C22	BDACTIVE_1	Active Board	TBD	Crate Controller
C23	BDACTIVE_2	Active Board	TBD	Crate Controller
C24	OUT Status	Active Board	HV Status	Crate Controller
C25	AGND	SLAVE PS	SLAVE GND	HV Boards
C26 – 27	+12V	SLAVE PS	SLAVE +12V	HV Boards
C28 – 29	-12V	SLAVE PS	SLAVE –12V	HV Boards
C30 – 32	+90V	SLAVE PS	SLAVE HV	HV Boards
A1 – 2	AGND	SLAVE PS	SLAVE GND	HV Boards
A3 – 16	+5V	SLAVE PS	SLAVE +5V	HV Boards
A17 – 25	AGND	SLAVE PS	SLAVE GND	HV Boards
A26 – 27	+12V	SLAVE PS	SLAVE +12V	HV Boards
A28 – 29	-12V	SLAVE PS	SLAVE –12V	HV Boards
A30 – 32	+90V	SLAVE PS	SLAVE HV	HV Boards

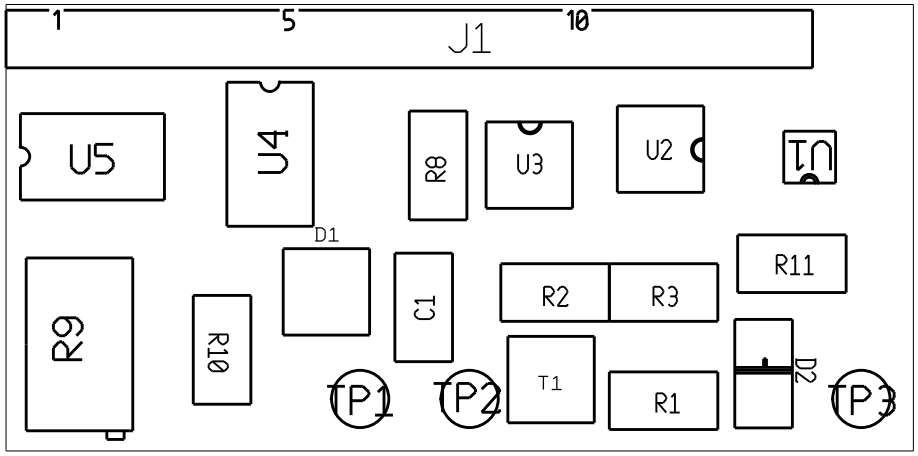
HV Board
Power Connector

Pin	Voltage	Pin	Voltage	Pin	Voltage
A1	+5V	B1	+5V	C1	HVOUT_31
A2	+5V	B2	+5V	C2	HVOUT_30
A3	+5V	B3	+5V	C3	HVOUT_29
A4	+5V	B4	+5V	C4	HVOUT_28
A5	+5V	B5	+5V	C5	HVOUT_27
A6	+5V	B6	+5V	C6	HVOUT_26
A7	+5V	B7	+5V	C7	HVOUT_25
A8	+5V	B8	+5V	C8	HVOUT_24
A9	+5V	B9	+5V	C9	HVOUT_23
A10	+5V	B10	+5V	C10	HVOUT_22
A11	+5V	B11	+5V	C11	HVOUT_21
A12	+5V	B12	+5V	C12	HVOUT_20
A13	AGND	B13	AGND	C13	HVOUT_19
A14	AGND	B14	AGND	C14	HVOUT_18
A15	AGND	B15	AGND	C15	HVOUT_17
A16	AGND	B16	AGND	C16	HVOUT_16
A17	AGND	B17	AGND	C17	HVOUT_15
A18	AGND	B18	AGND	C18	HVOUT_14
A19	AGND	B19	AGND	C19	HVOUT_13
A20	AGND	B20	AGND	C20	HVOUT_12
A21	AGND	B21	AGND	C21	HVOUT_11
A22	AGND	B22	AGND	C22	HVOUT_10
A23	AGND	B23	AGND	C23	HVOUT_9
A24	AGND	B24	AGND	C24	HVOUT_8
A25	+12V	B25	+12V	C25	HVOUT_7
A26	+12V	B26	+12V	C26	HVOUT_6
A27	-12V	B27	-12V	C27	HVOUT_5
A28	-12V	B28	-12V	C28	HVOUT_4
A29	AGND	B29	AGND	C29	HVOUT_3
A30	AGND	B30	AGND	C30	HVOUT_2
A31	AGND	B31	AGND	C31	HVOUT_1
A32	AGND	B32	AGND	C32	HVOUT_0

APD HV CHANNEL V3



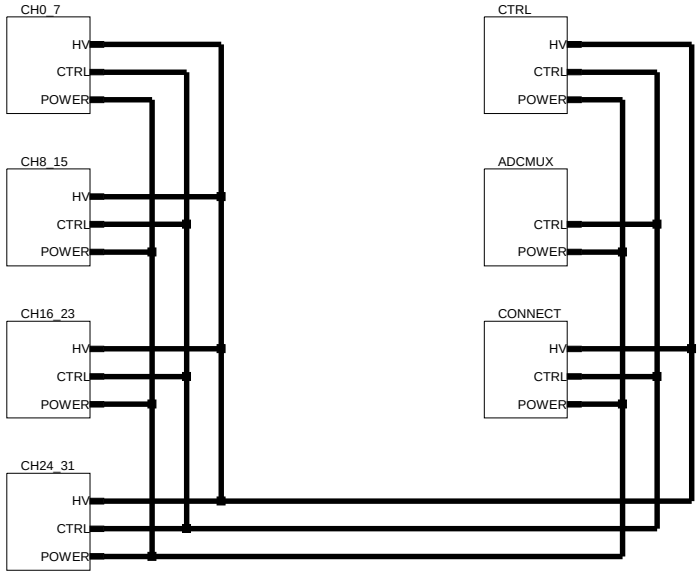
REV: A	DATE: 19.10.2009	ENG: V.COMMICHAU
PROJECT: SINGLE APD HV CHANNEL VERSION 3		
COMPANY: IPP ETHZ ADDRESS: SCHAFMATTSTR.20 CITY CH-8093 ZUERICH COUNTRY: SWITZERLAND#	FILE:APDHVNEW.SCH	
INITIAL 01.03.2009	PAGE: 1	OF: 1


1
5
10
J1
U5
U4
R8
U3
U2
U1
D1
R9
R10
C1
R2
R3
R11
T1
R1
D2
TP1
TP2
TP3

GAPDHV02

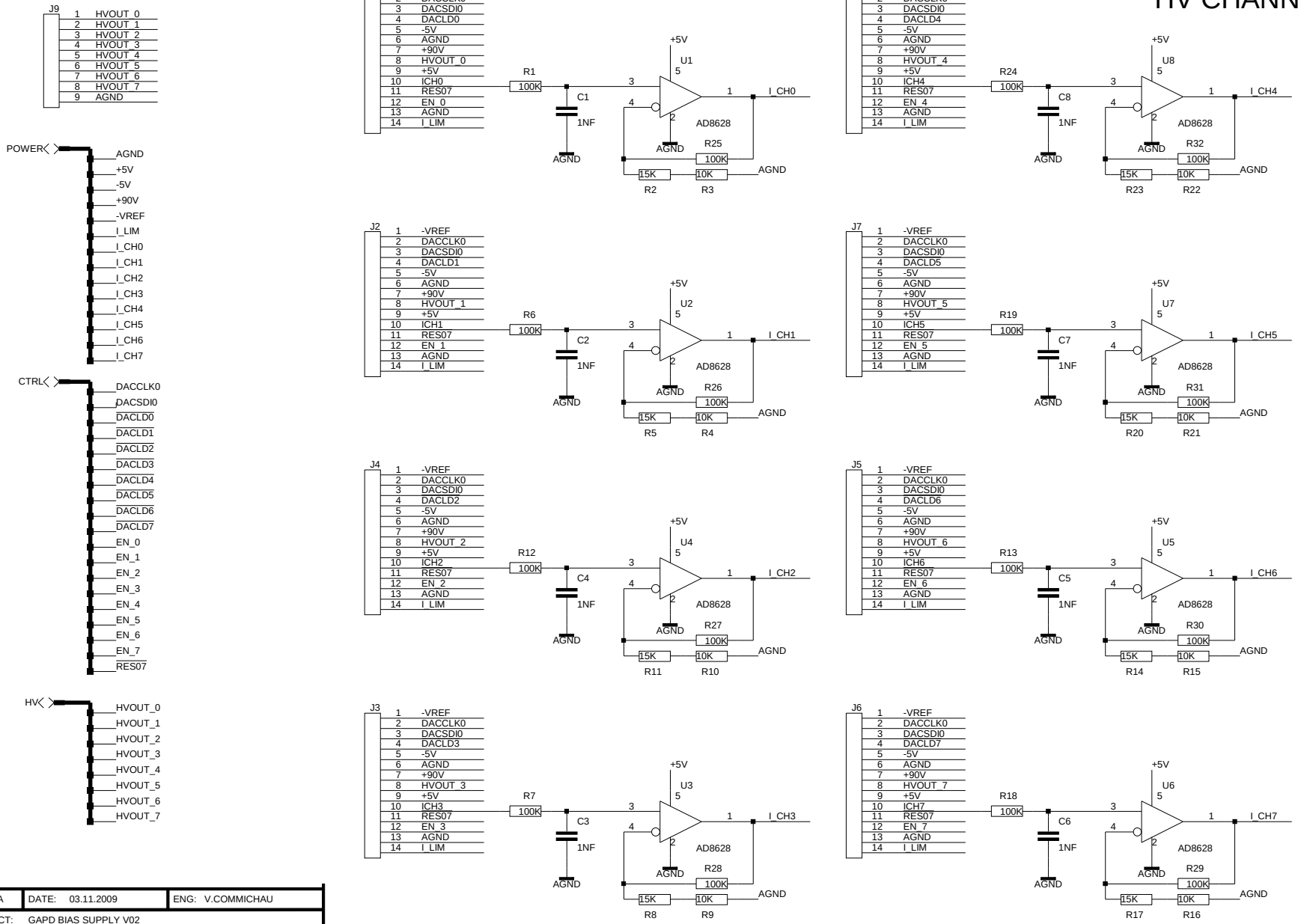
32 CHANNEL HV SUPPLY

09.11.2009



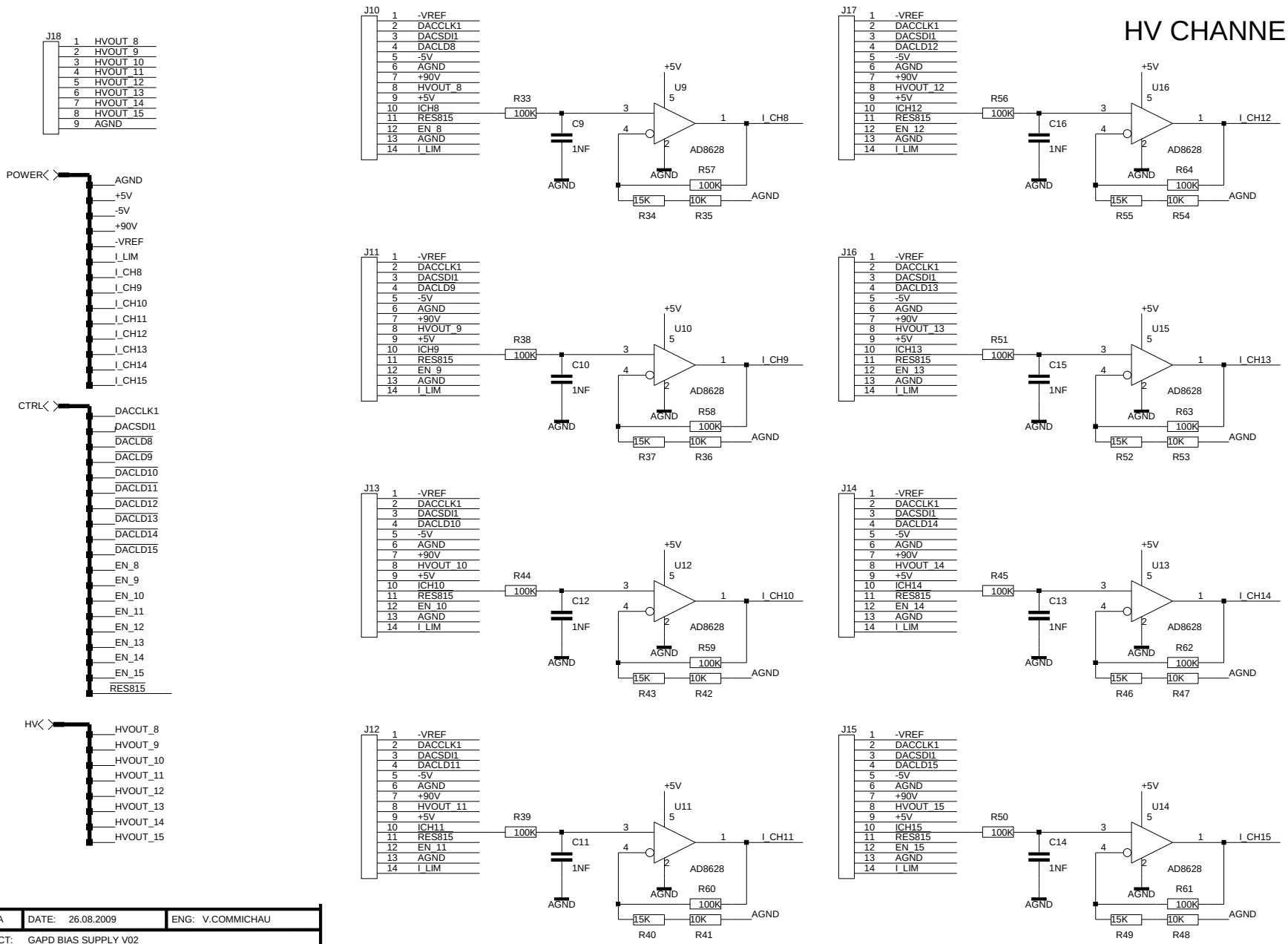
REV: A	DATE: 09.09.2009	ENG: V.COMMICHAU
PROJECT: GAPD BIAS SUPPLY V02		
COMPANY: IPP ETHZ ADDRESS: SCHAFMATTSTR.20 CITY CH-8093 ZUERICH COUNTRY: SWITZERLAND#	FILE:GAPDHV02.SCH	
INITIAL 22.06.2009	PAGE: 1	OF: 8

HV CHANNELS 0-7



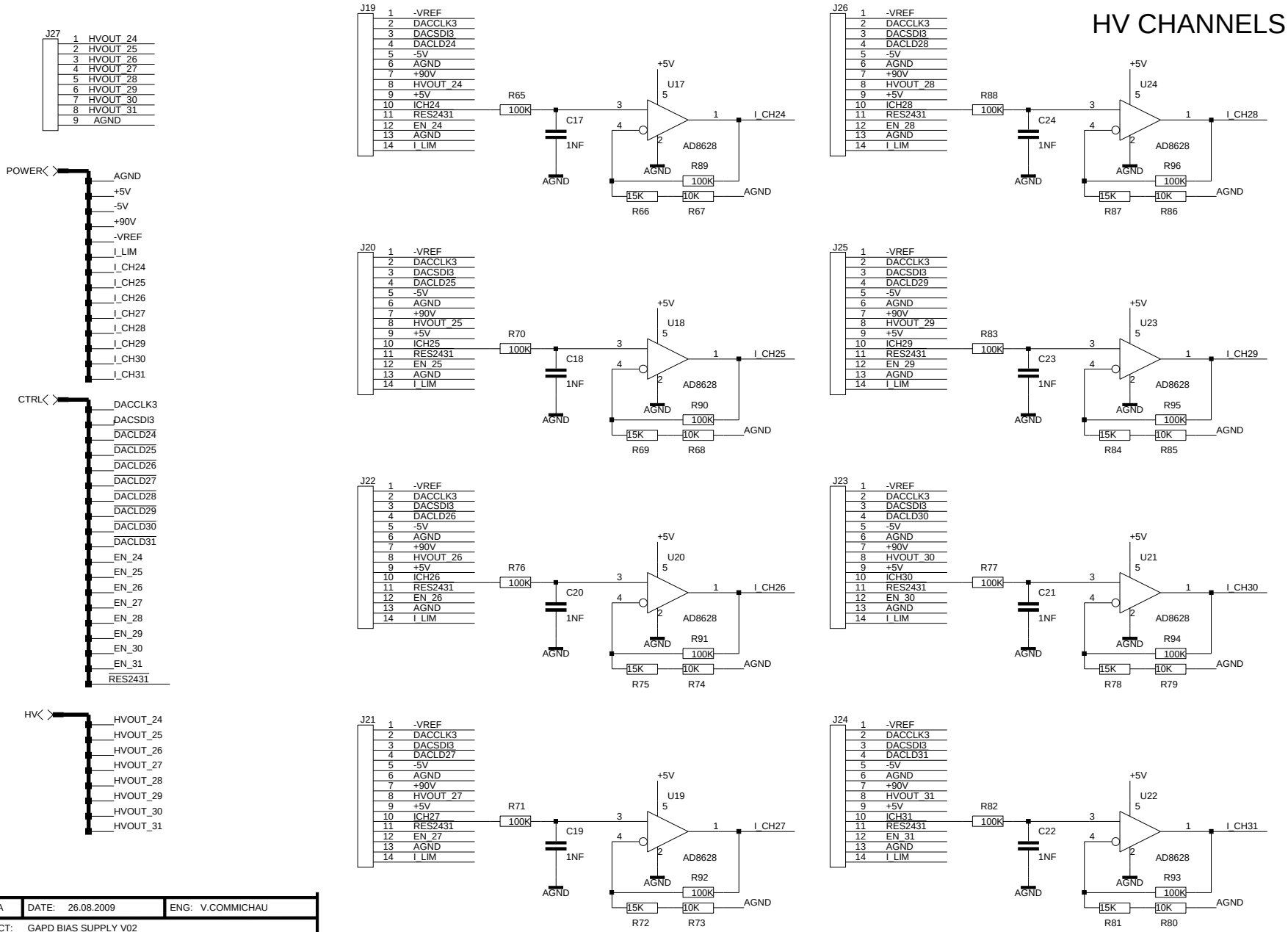
REV: A	DATE: 03.11.2009	ENG: V.COMMICHAU
PROJECT: GAPD BIAS SUPPLY V02		
COMPANY: IPP ETHZ ADDRESS: SCHAFMATTSTR.20 CITY CH-8093 ZUERICH COUNTRY: SWITZERLAND#	FILE:CH0_7.SCH	
INITIAL 22.06.2009	PAGE: 2	OF: 8

HV CHANNELS 8-15



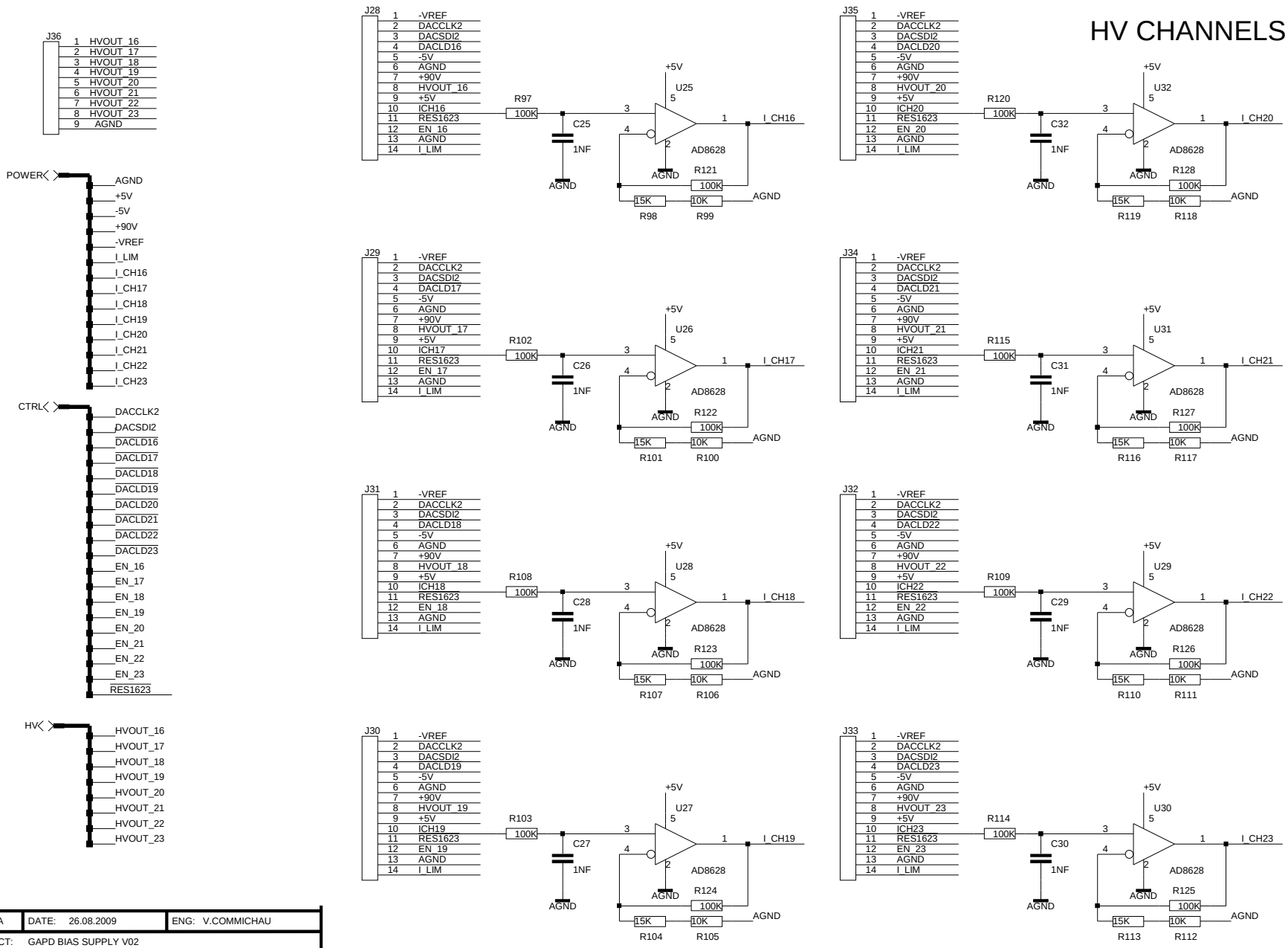
REV: A	DATE: 26.08.2009	ENG: V.COMMICHAU
PROJECT: GAPD BIAS SUPPLY V02		
COMPANY: IPP ETHZ ADDRESS: SCHAFMATTSTR.20 CITY CH-8093 ZUERICH COUNTRY: SWITZERLAND#	FILE:CH8_15.SCH	
INITIAL 22.06.2009	PAGE: 3	OF: 8

HV CHANNELS 24-31



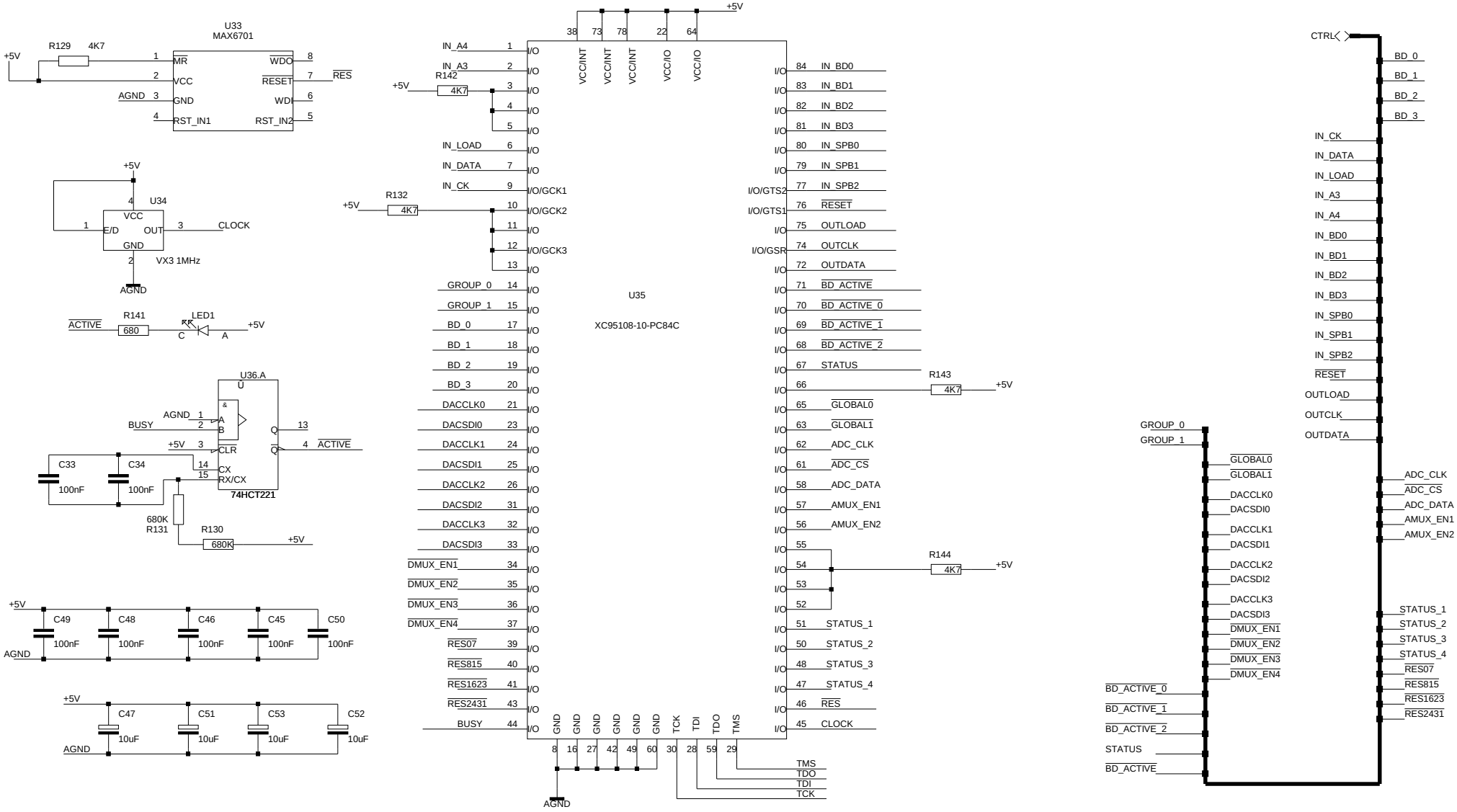
REV: A	DATE: 26.08.2009	ENG: V.COMMICHAU
PROJECT: GAPD BIAS SUPPLY V02		
COMPANY: IPP ETHZ ADDRESS: SCHAFMATTSTR.20 CITY CH-8093 ZUERICH COUNTRY: SWITZERLAND#	FILE:CH24_31.SCH	
INITIAL 22.06.2009	PAGE: 5	OF: 8

HV CHANNELS 16-23

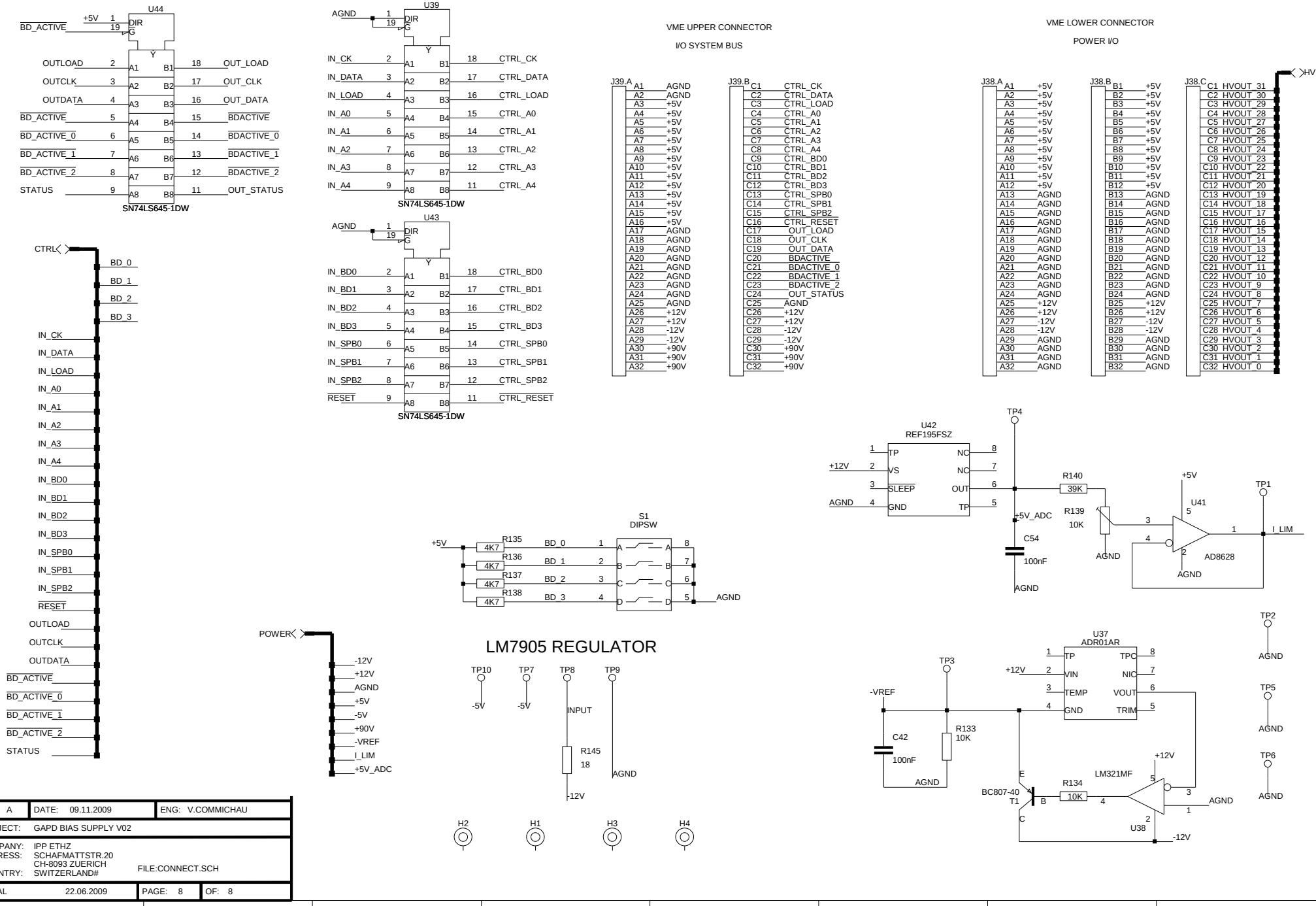


REV: A	DATE: 26.08.2009	ENG: V.COMMICHAU
PROJECT: GAPD BIAS SUPPLY V02		
COMPANY: IPP ETHZ ADDRESS: SCHAFMATTSTR.20 CITY CH-8093 ZUERICH COUNTRY: SWITZERLAND#	FILE:CH16_23.SCH	
INITIAL 22.06.2009	PAGE: 4	OF: 8

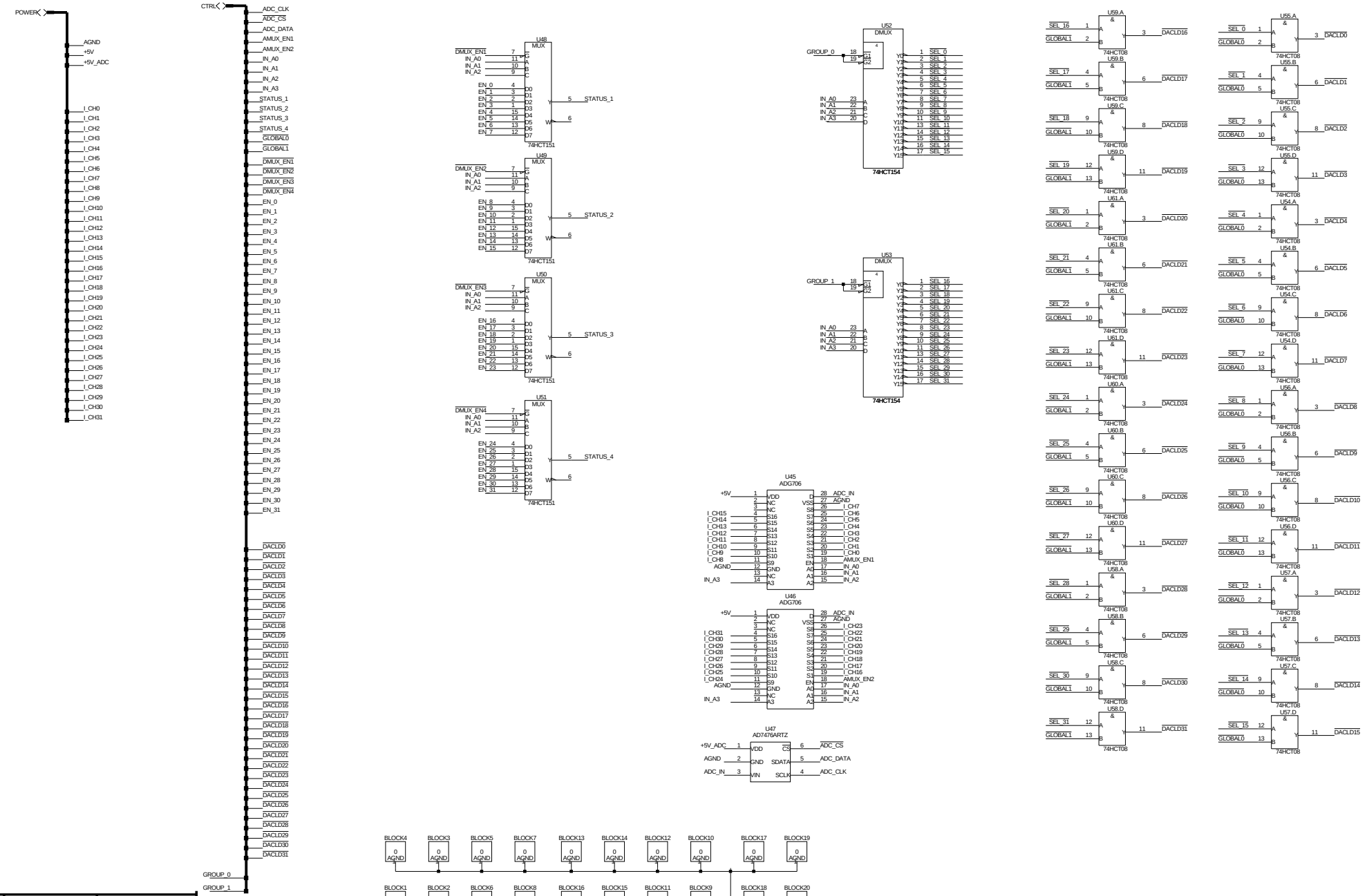
BOARD CONTROLLER



REV: A	DATE: 21.09.2009	ENG: V.COMMICHAU
PROJECT: GAPD BIAS SUPPLY V02		
COMPANY: IPP ETHZ ADDRESS: SCHAFMATTSTR.20 CITY CH-8093 ZUERICH COUNTRY: SWITZERLAND#	FILE:CTRL.SCH	
INITIAL 22.06.2009	PAGE: 6	OF: 8

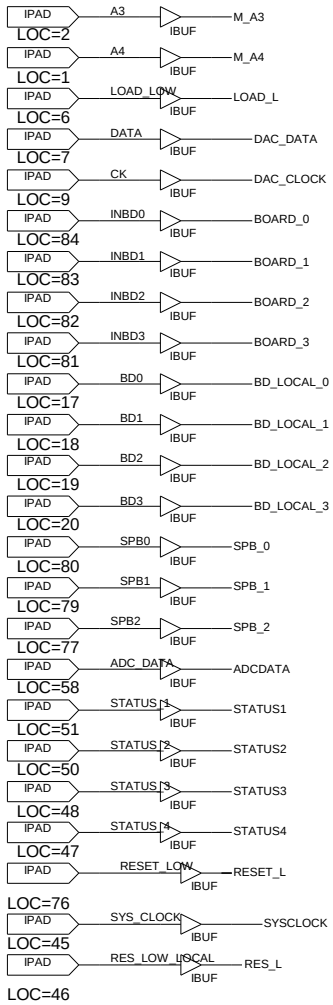


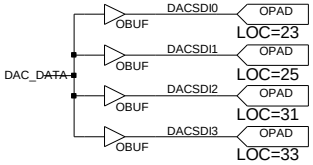
REV: A	DATE: 09.11.2009	ENG: V.COMMICHAU
PROJECT: GAPD BIAS SUPPLY V02		
COMPANY: IPP ETHZ ADDRESS: SCHAFMATTSTR.20 CITY CH-8093 ZUERICH COUNTRY: SWITZERLAND#	FILE:CONNECT.SCH	
INITIAL 22.06.2009	PAGE: 8	OF: 8

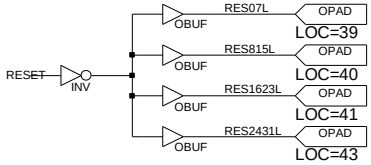


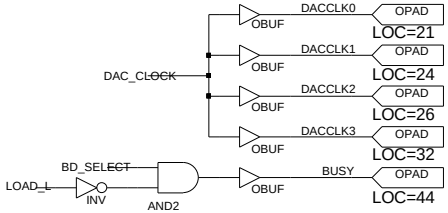
REV: A	DATE: 26.08.2009	ENG: V.COMMICHAU
PROJECT: GAPD BIAS SUPPLY V02		
COMPANY: IPP ETHZ ADDRESS: SCHAFMATTSTR.20 CITY CH-8093 ZUERICH COUNTRY: SWITZERLAND#	FILE:ADCMUX.SCH	
INITIAL 22.06.2009	PAGE: 7	OF: 8

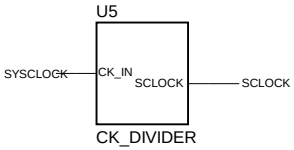
APDHV V2 19.01.2010

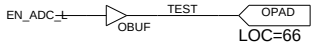


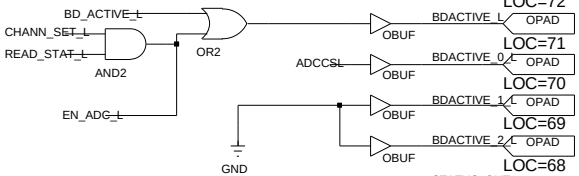


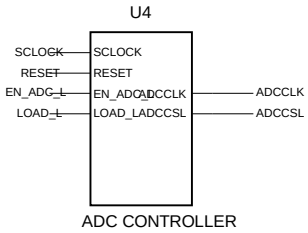


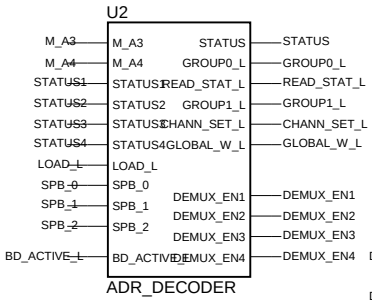


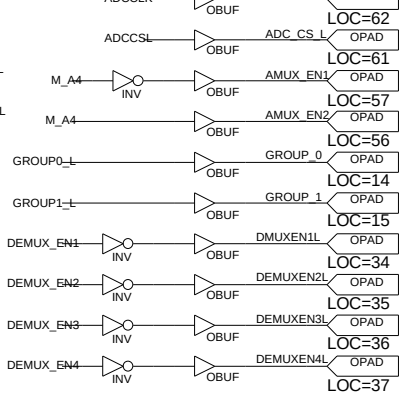


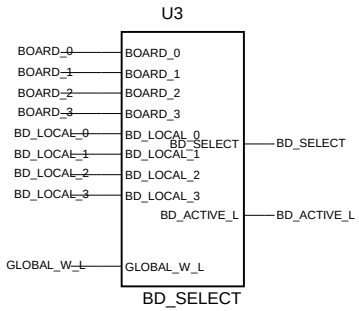


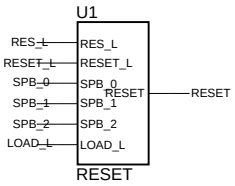






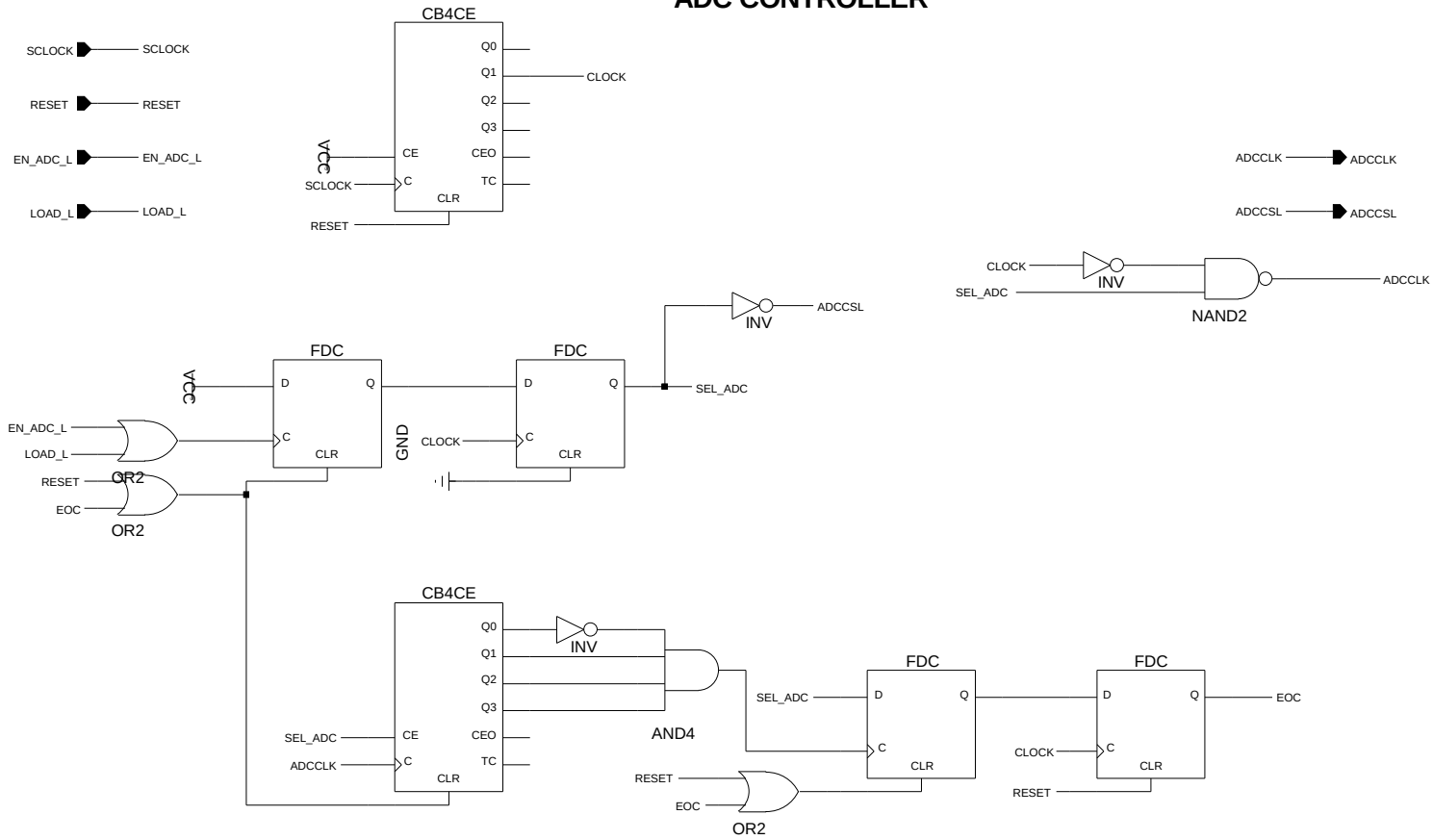






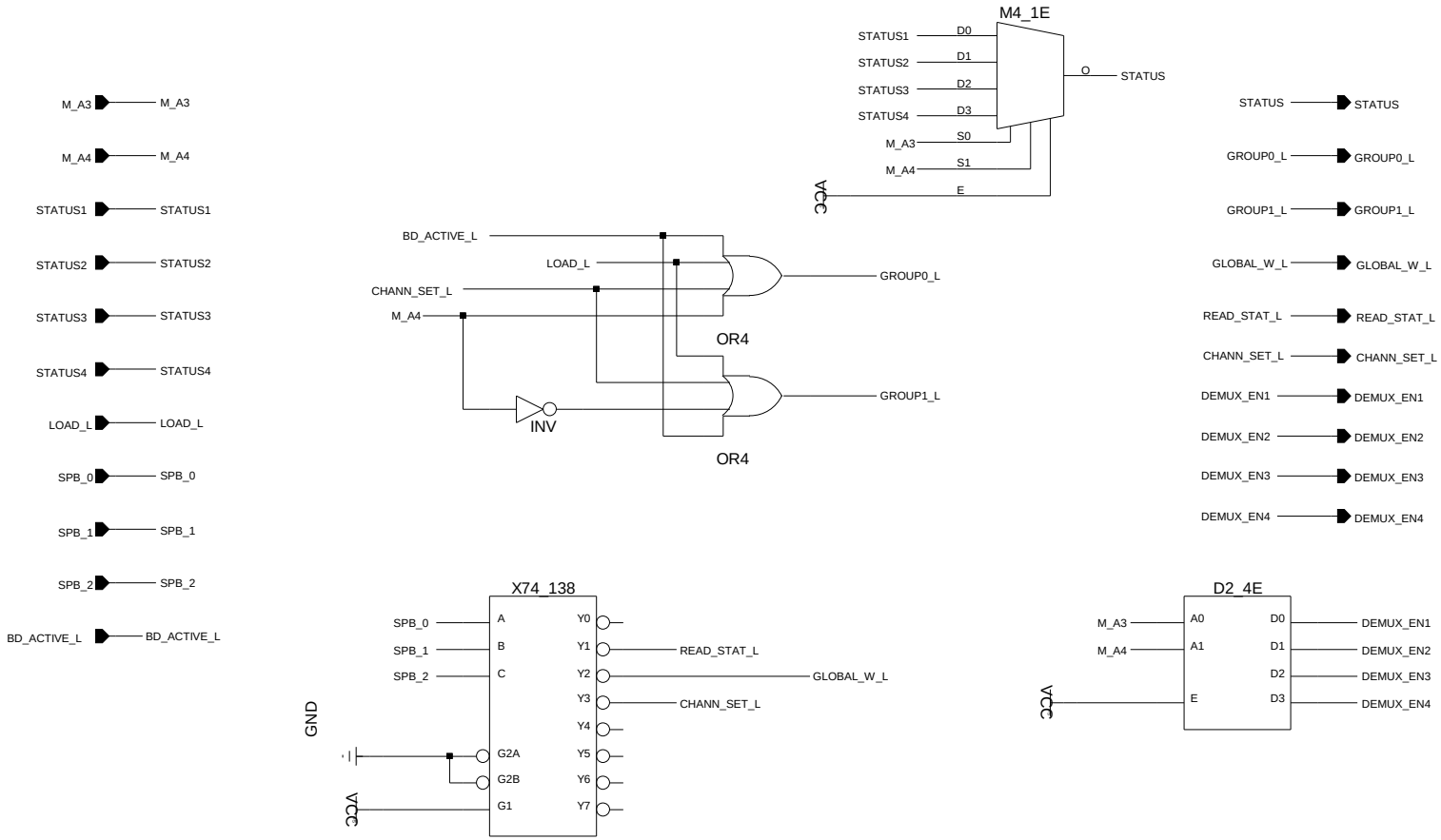
APDHV V2	Project: APDHV_V2
V.Commichau IPP/ETHZ	Macro: APDHV_V1
CH 8093 ZUERICH	Date: 8/25/09
Date Last Modified: 1/19/10	

ADC CONTROLLER



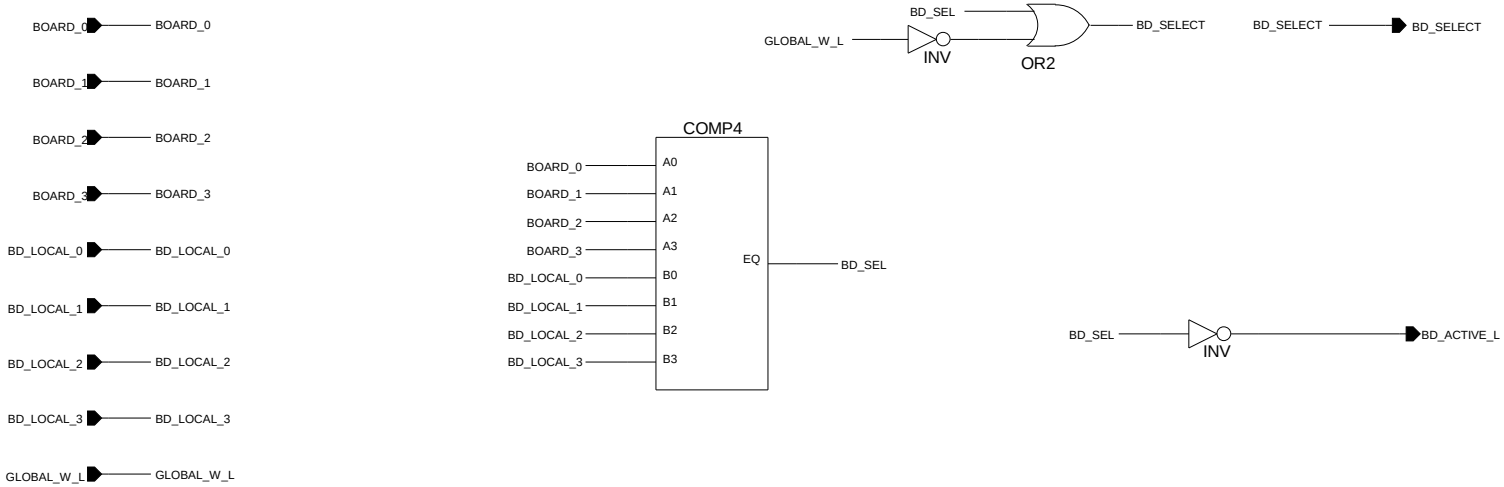
APDHV V2	Project: APDHV_V2
V.Commichau IPP/ETHZ	Macro: ADC_CTRL
CH 8093 ZUERICH	Date: 8/25/09
Date Last Modified: 11/23/09	

ADR & SELECT Logic

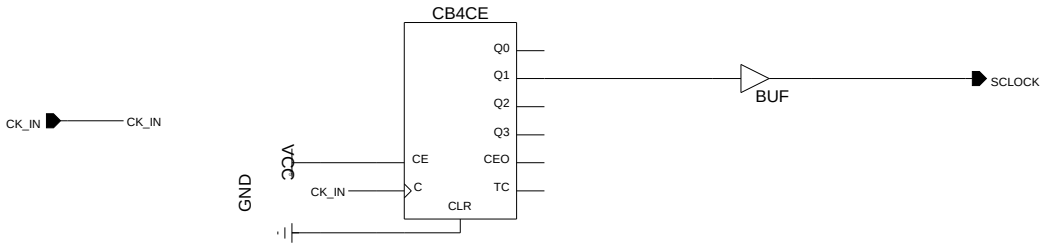


APDHV V2	Project: APDHV_V2
V.Commichau IPP/ETHZ	Macro: ADR_DECODER
CH 8093 ZUERICH	Date: 8/25/09
Date Last Modified: 11/9/09	

Board Selector

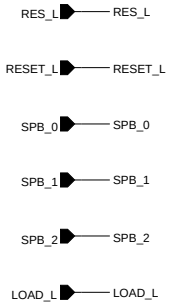


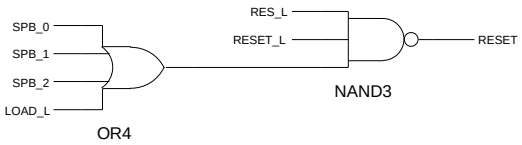
APDHV V2	Project: APDHV_V2
V.Commichau IPP/ETHZ	Macro: BD_SELECT
CH 8093 ZUERICH	Date: 8/25/09
Date Last Modified: 1/19/10	



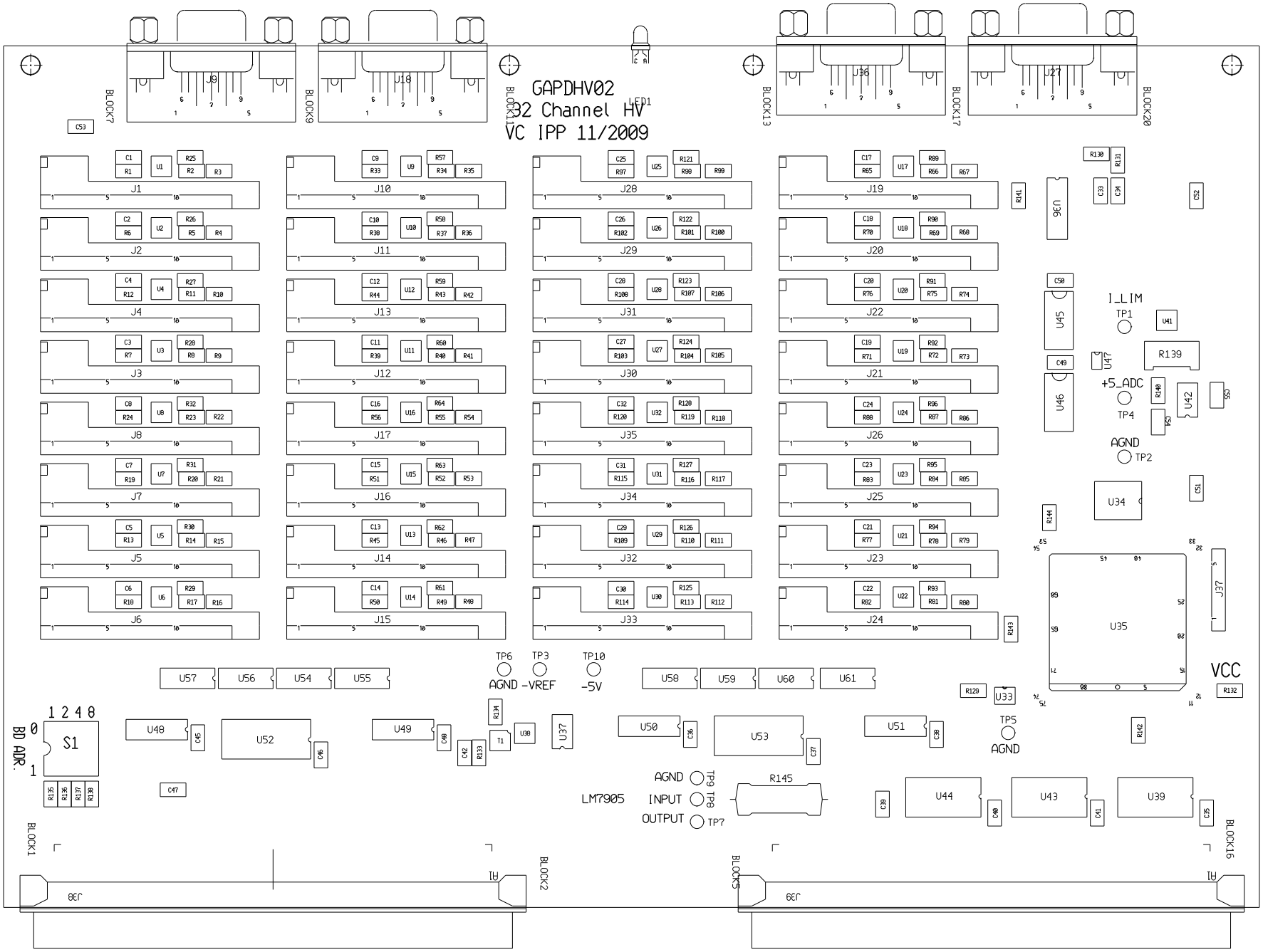
APDHV V2	Project: APDHV_V2
V.Commichau IPP/ETHZ	Macro: CK_DIVIDER
CH 8093 ZUERICH	Date: 8/25/09
Date Last Modified: 11/17/09	

RESET LOGIC



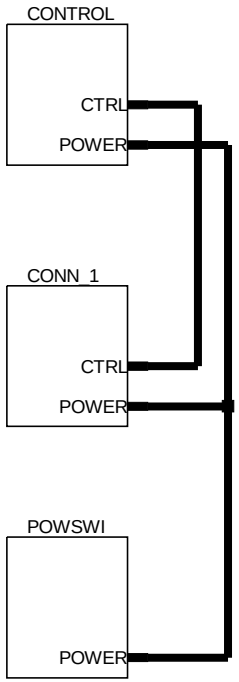


APDHV V2	Project: APDHV_V2
V.Commichau IPP/ETHZ	Macro: RESET
CH 8093 ZUERICH	Date: 8/25/09
Date Last Modified: 8/25/09	


GAPDHV02
32 Channel HV
VC IPP 11/2009
LED1
BLOCK7
BLOCK9
BLOCK11
BLOCK13
BLOCK17
BLOCK20
J9
J18
J36
J27
C53
J1
J10
J28
J19
J2
J11
J29
J20
J4
J13
J31
J22
J3
J12
J30
J21
J8
J17
J35
J26
J7
J16
J34
J25
J5
J14
J32
J23
J6
J15
J33
J24
U45
U46
U47
U41
R139
U42
U34
U35
U37
U33
I_LIM
TP1
+5_ADC
TP4
AGND
TP2
VCC
R130
R131
C33
C34
C52
R141
C50
C49
C54
C55
C51
R144
R143
R129
R132
R142
TP6
AGND
TP3
-VREF
TP10
-5V
U57
U56
U54
U55
U58
U59
U60
U61
1 2 4 8
BD ADR.
0
1
S1
R135
R136
R137
R138
U48
C45
U52
C46
C47
U49
C48
C42
R133
R134
T1
U38
U37
U50
C36
U53
C37
U51
C38
TP5
AGND
R145
LM7905
AGND
INPUT
OUTPUT
TP9
TP8
TP7
C39
U44
C40
U43
C41
U39
C35
BLOCK1
BLOCK2
BLOCK5
BLOCK16
J38
J39
A1

GAPD HV SYSTEM CONTROLLER

23.09.2009



REV: A	DATE: 23.09.2009	ENG: V.COMMICHAU
PROJECT:	GAPD BIAS SUPPLY V02 CONTROLLER	
COMPANY: IPP ETHZ ADDRESS: SCHAFMATTSTR.20 CITY CH-8093 ZUERICH COUNTRY: SWITZERLAND#	FILE:HV__CTRL.SCH	
INITIAL 30.06.2009	PAGE: 1	OF: 4

VME LOWER CONNECTOR
TO POWER SUPPLIES

VME UPPER CONNECTOR
I/O SYSTEM BUS

J2.C
C1 VCC
C2 VCC
C3 VCC
C4 GND
C5 GND
C6 GND
C7 +5V
C8 +5V
C9 +5V
C10 +5V
C11 +5V
C12 +5V
C13 +5V
C14 -12V
C15 -12V
C16 +12V
C17 +12V
C18 AGND
C19 AGND
C20 AGND
C21 AGND
C22 AGND
C23 AGND
C24 AGND
C25 AGND
C26 AGND
C27 +90VIN
C28 +90VIN
C29 +90VIN
C30 +90VIN
C31 USB_+5
C32 USB_D-

J2.B
B1 +5V
B2 +5V
B3 +5V
B4 +5V
B5 +5V
B6 +5V
B7 +5V
B8 +5V
B9 +5V
B10 +5V
B11 +5V
B12 +5V
B13 +5V
B14 -12V
B15 -12V
B16 +12V
B17 +12V
B18 AGND
B19 AGND
B20 AGND
B21 AGND
B22 AGND
B23 AGND
B24 AGND
B25 AGND
B26 AGND
B27 +90VIN
B28 +90VIN
B29 +90VIN
B30 +90VIN
B31 +90VIN
B32 +90VIN

J2.A
A1 VCC
A2 VCC
A3 VCC
A4 GND
A5 GND
A6 GND
A7 +5V
A8 +5V
A9 +5V
A10 +5V
A11 +5V
A12 +5V
A13 +5V
A14 -12V
A15 -12V
A16 +12V
A17 +12V
A18 AGND
A19 AGND
A20 AGND
A21 AGND
A22 AGND
A23 AGND
A24 AGND
A25 AGND
A26 AGND
A27 +90VIN
A28 +90VIN
A29 +90VIN
A30 +90VIN
A31 USB_D+
A32 USB_GND

J1.A
A1 AGND
A2 AGND
A3 +5V
A4 +5V
A5 +5V
A6 +5V
A7 +5V
A8 +5V
A9 +5V
A10 +5V
A11 +5V
A12 +5V
A13 +5V
A14 +5V
A15 +5V
A16 +5V
A17 AGND
A18 AGND
A19 AGND
A20 AGND
A21 AGND
A22 AGND
A23 AGND
A24 AGND
A25 AGND
A26 +12V
A27 +12V
A28 -12V
A29 -12V
A30 +90V
A31 +90V
A32 +90V

J1.B
C1 CTRL_CK
C2 CTRL_DATA
C3 CTRL_LOAD
C4 CTRL_A0
C5 CTRL_A1
C6 CTRL_A2
C7 CTRL_A3
C8 CTRL_A4
C9 CTRL_BD0
C10 CTRL_BD1
C11 CTRL_BD2
C12 CTRL_BD3
C13 CTRL_SPB0
C14 CTRL_SPB1
C15 CTRL_SPB2
C16 CTRL_RESET
C17 OUT_LOAD
C18 OUT_CLK
C19 OUT_DATA
C20 BDACTIVE
C21 BDACTIVE_0
C22 BDACTIVE_1
C23 BDACTIVE_2
C24 STATUS_IN
C25 AGND
C26 +12V
C27 +12V
C28 -12V
C29 -12V
C30 +90V
C31 +90V
C32 +90V

CTRL
USB_+5
USB_D-
USB_D+
USB_GND
CK
DATA
LOAD
A0
A1
A2
A3
A4
BD0
BD1
BD2
BD3
SPB0
SPB1
SPB2
RESET
SL_LOAD
SL_CLK
SL_DATA
BD_ACTIVE
BD_ACTIVE_0
BD_ACTIVE_1
BD_ACTIVE_2
STATUSIN

+5V
C24 100nF
C23 100nF
C25 100nF
AGND

U8
HCPL-090J
VCC 16 VDD2 VDD1 1 +5V
GND 15 GND2 GND1 2 AGND
SL_LOAD 14 OUT1 IN1 3 SD_0
SL_CLK 13 OUT2 IN2 4 SD_1
SL_DATA 12 OUT3 IN3 5 SD_2
BD_ACTIVE 11 OUT4 IN4 6 SD_3
10 NC NC 7
GND 9 GND2 GND1 8 AGND

U9
HCPL-090J
VCC 16 VDD2 VDD1 1 +5V
GND 15 GND2 GND1 2 AGND
BD_ACTIVE_0 14 OUT1 IN1 3 SD_4
BD_ACTIVE_1 13 OUT2 IN2 4 SD_5
BD_ACTIVE_2 12 OUT3 IN3 5 SD_6
STATUSIN 11 OUT4 IN4 6 SD_7
10 NC NC 7
GND 9 GND2 GND1 8 AGND

U7
AGND 1 DIR
19 G
Y
SD_0 2 A1 B1 18 OUT_LOAD
SD_1 3 A2 B2 17 OUT_CLK
SD_2 4 A3 B3 16 OUT_DATA
SD_3 5 A4 B4 15 BDACTIVE
SD_4 6 A5 B5 14 BDACTIVE_0
SD_5 7 A6 B6 13 BDACTIVE_1
SD_6 8 A7 B7 12 BDACTIVE_2
SD_7 9 A8 B8 11 STATUS_IN
SN74LS645-1DW

R25 +5V 1K BDACTIVE
R24 +5V 1K BDACTIVE_0
R23 +5V 1K BDACTIVE_1
R22 +5V 1K BDACTIVE_2

U5
HCPL-090J
VCC 1 VDD1 VDD2 16 +5V
GND 2 GND1 GND2 15 AGND
CK 3 IN1 OUT1 14 CTRL_0
DATA 4 IN2 OUT2 13 CTRL_1
LOAD 5 IN3 OUT3 12 CTRL_2
A0 6 IN4 OUT4 11 CTRL_3
7 NC NC 10
GND 8 GND1 GND2 9 AGND

U6
HCPL-090J
VCC 1 VDD1 VDD2 16 +5V
GND 2 GND1 GND2 15 AGND
A1 3 IN1 OUT1 14 CTRL_4
A2 4 IN2 OUT2 13 CTRL_5
A3 5 IN3 OUT3 12 CTRL_6
A4 6 IN4 OUT4 11 CTRL_7
7 NC NC 10
GND 8 GND1 GND2 9 AGND

U4
+5V 1 DIR
AGND 19 G
Y
CTRL_0 2 A1 B1 18 CTRL_CK
CTRL_1 3 A2 B2 17 CTRL_DATA
CTRL_2 4 A3 B3 16 CTRL_LOAD
CTRL_3 5 A4 B4 15 CTRL_A0
CTRL_4 6 A5 B5 14 CTRL_A1
CTRL_5 7 A6 B6 13 CTRL_A2
CTRL_6 8 A7 B7 12 CTRL_A3
CTRL_7 9 A8 B8 11 CTRL_A4
SN74LS645-1DW

U3
HCPL-090J
VCC 1 VDD1 VDD2 16 +5V
GND 2 GND1 GND2 15 AGND
BD0 3 IN1 OUT1 14 CTRL_8
BD1 4 IN2 OUT2 13 CTRL_9
BD2 5 IN3 OUT3 12 CTRL_10
BD3 6 IN4 OUT4 11 CTRL_11
7 NC NC 10
GND 8 GND1 GND2 9 AGND

U2
HCPL-090J
VCC 1 VDD1 VDD2 16 +5V
GND 2 GND1 GND2 15 AGND
SPB0 3 IN1 OUT1 14 CTRL_12
SPB1 4 IN2 OUT2 13 CTRL_13
SPB2 5 IN3 OUT3 12 CTRL_14
RESET 6 IN4 OUT4 11 CTRL_15
7 NC NC 10
GND 8 GND1 GND2 9 AGND

U1
+5V 1 DIR
AGND 19 G
Y
CTRL_8 2 A1 B1 18 CTRL_BD0
CTRL_9 3 A2 B2 17 CTRL_BD1
CTRL_10 4 A3 B3 16 CTRL_BD2
CTRL_11 5 A4 B4 15 CTRL_BD3
CTRL_12 6 A5 B5 14 CTRL_SPB0
CTRL_13 7 A6 B6 13 CTRL_SPB1
CTRL_14 8 A7 B7 12 CTRL_SPB2
CTRL_15 9 A8 B8 11 CTRL_RESET
SN74LS645-1DW

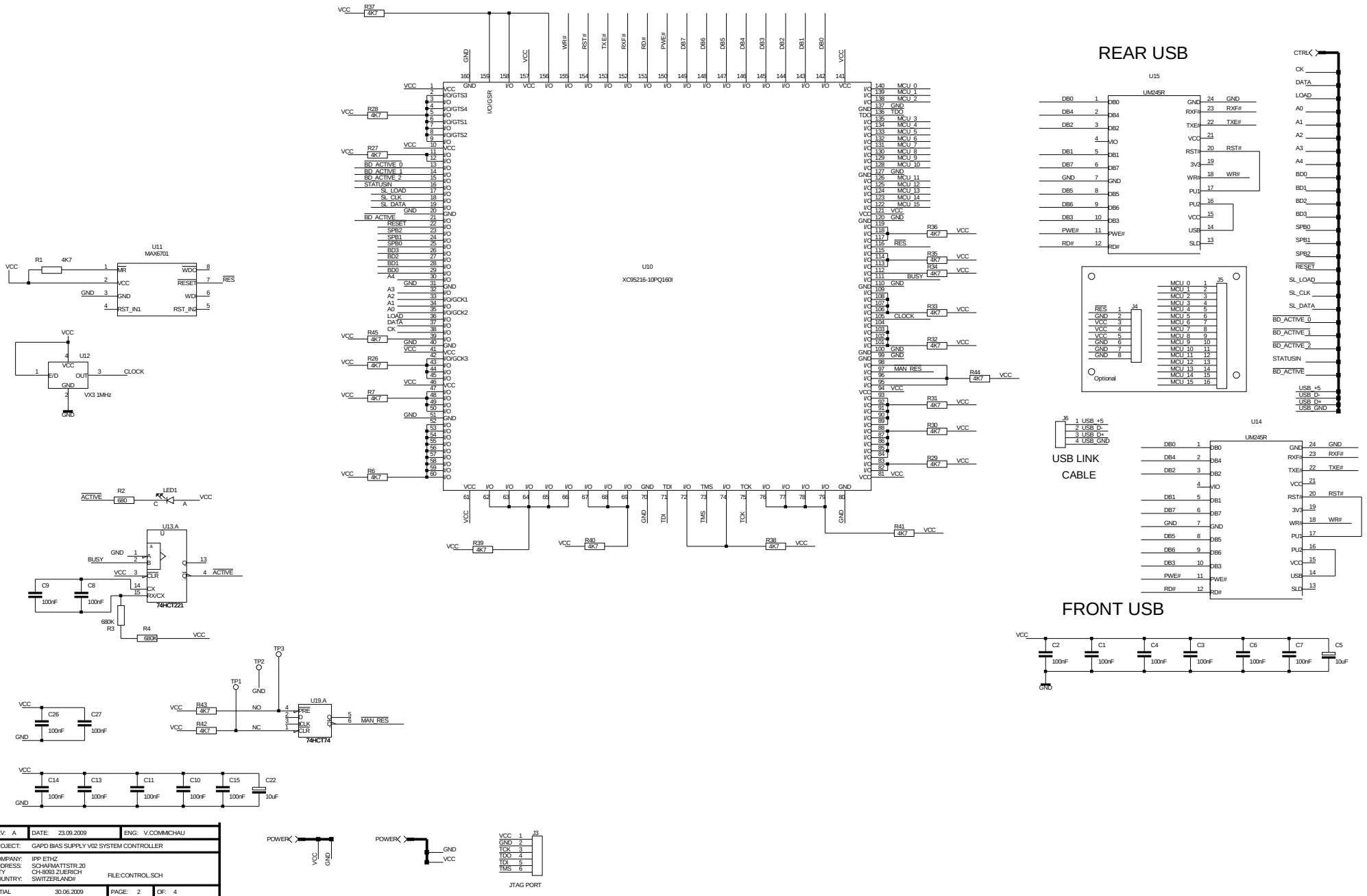
POWER
VCC
GND
+90VIN
+90V
+5V
+12V
-12V
AGND

+5V
C16 100nF
C28 100nF
C12 100nF
C18 100nF
C17 100nF
C20 100nF
C21 100nF
C19 10uF
AGND

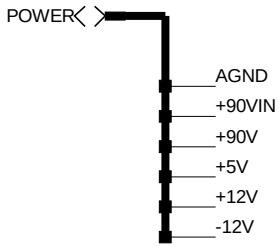
GND
H3 H4 H2 H1
H6 H5 H7 H8

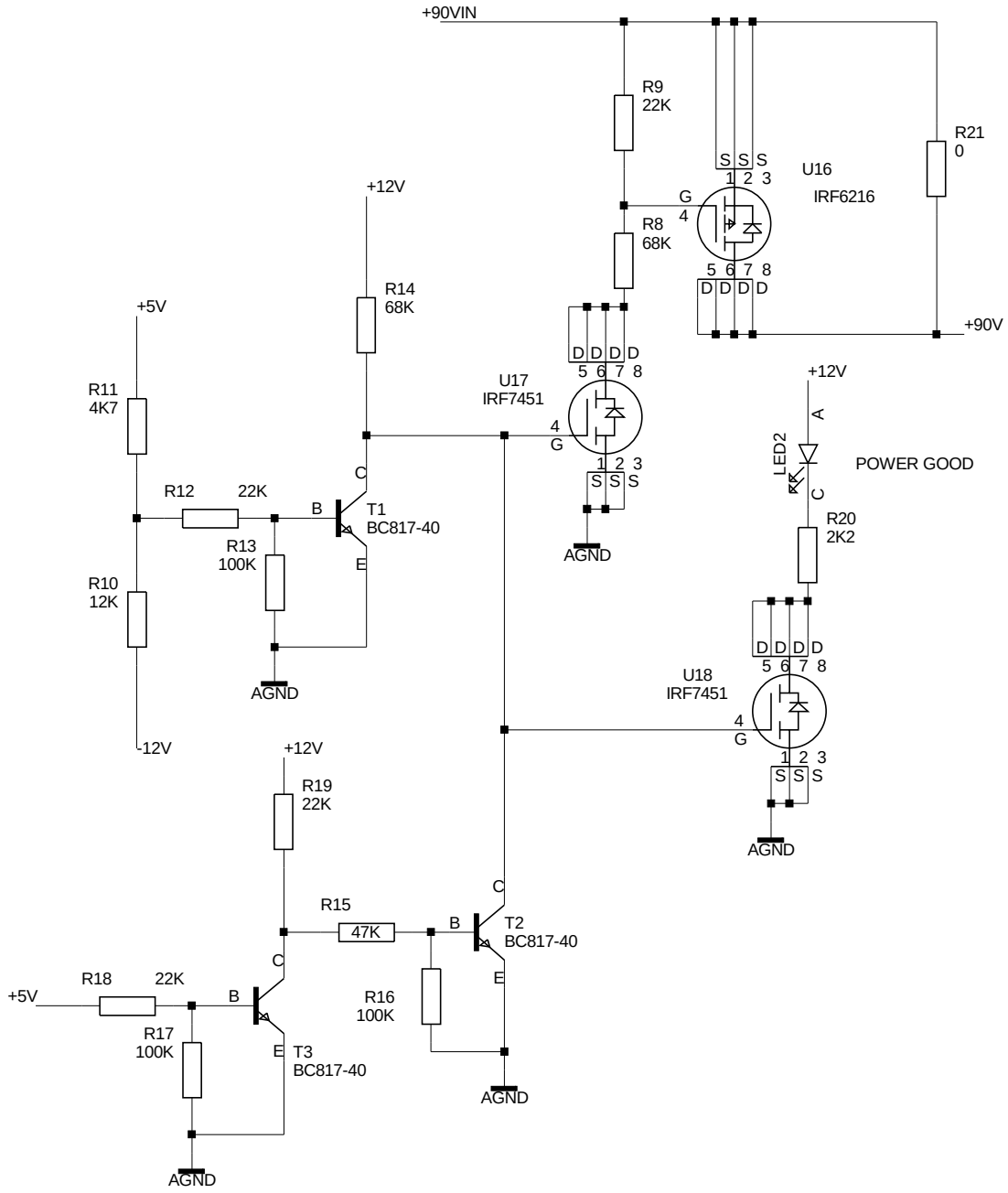
REV: A	DATE: 15.09.2009	ENG: V.COMMICHAU
PROJECT: GAPD BIAS SUPPLY V02		
COMPANY: IPP ETHZ ADDRESS: SCHAFMATTSTR.20 CITY CH-8093 ZUERICH COUNTRY: SWITZERLAND#	FILE:CONN_1.SCH	
INITIAL 30.06.2009	PAGE: 3	OF: 4

HV CRATE CONTROLLER

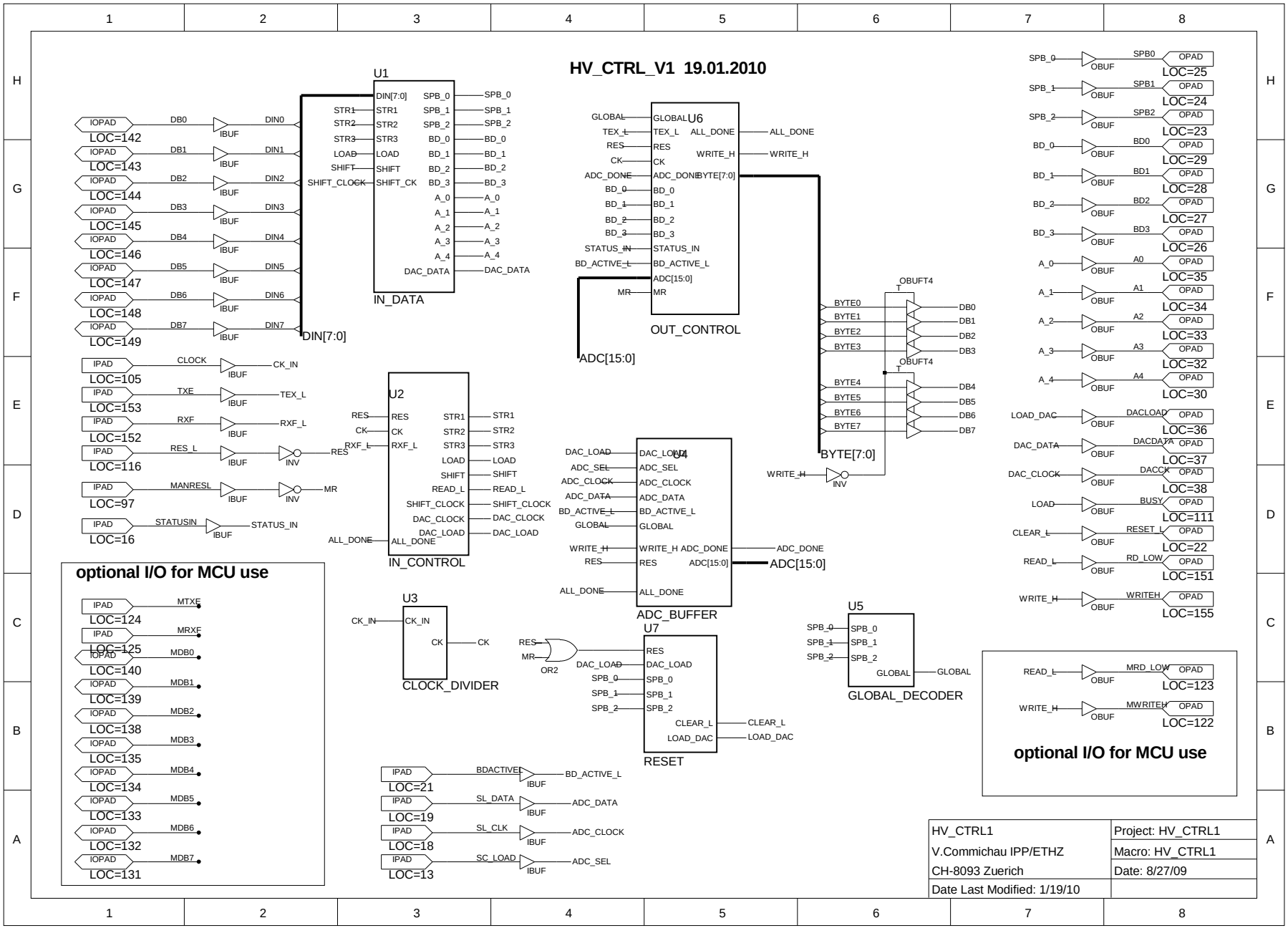


POWER SWITCH

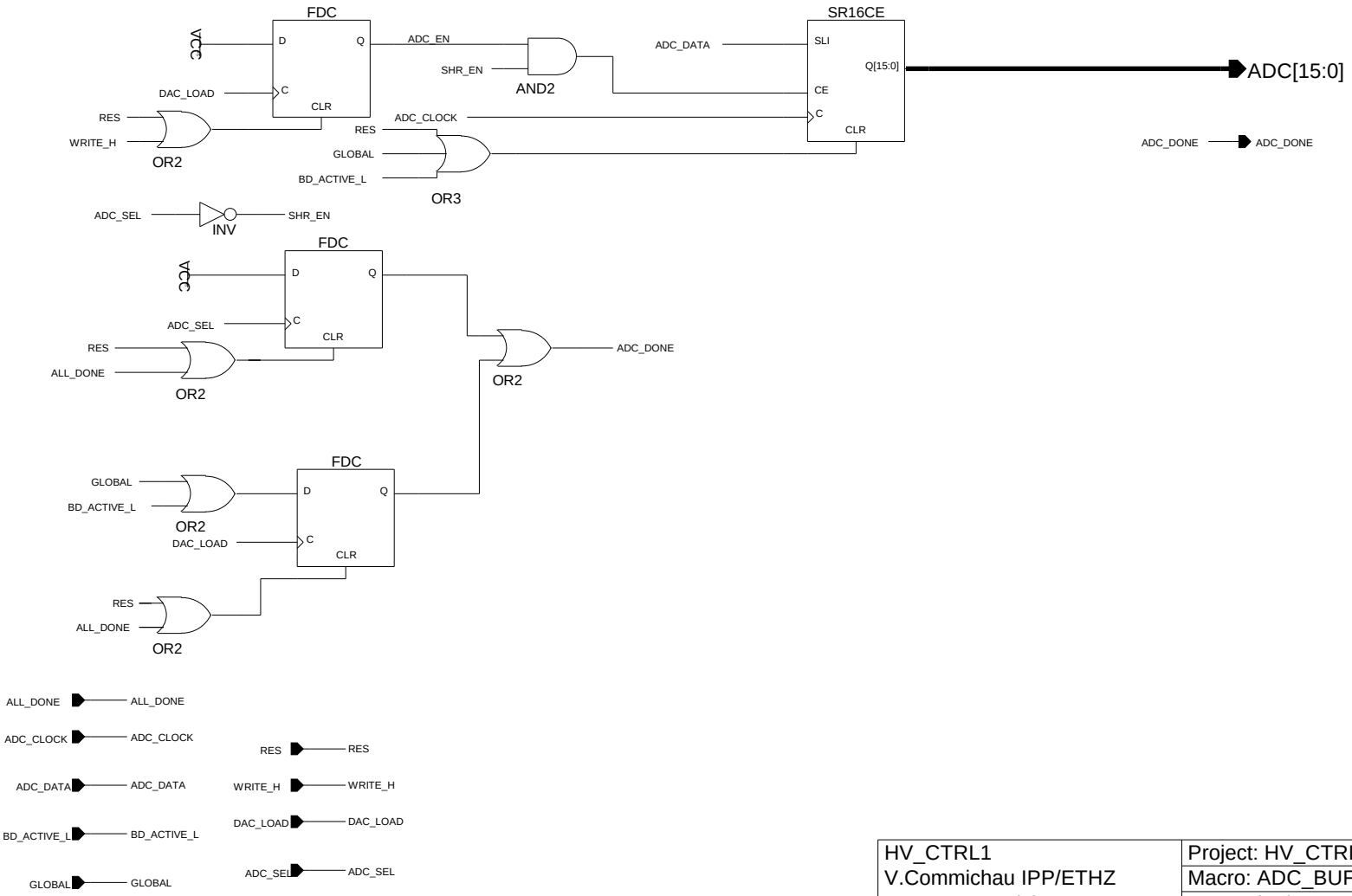




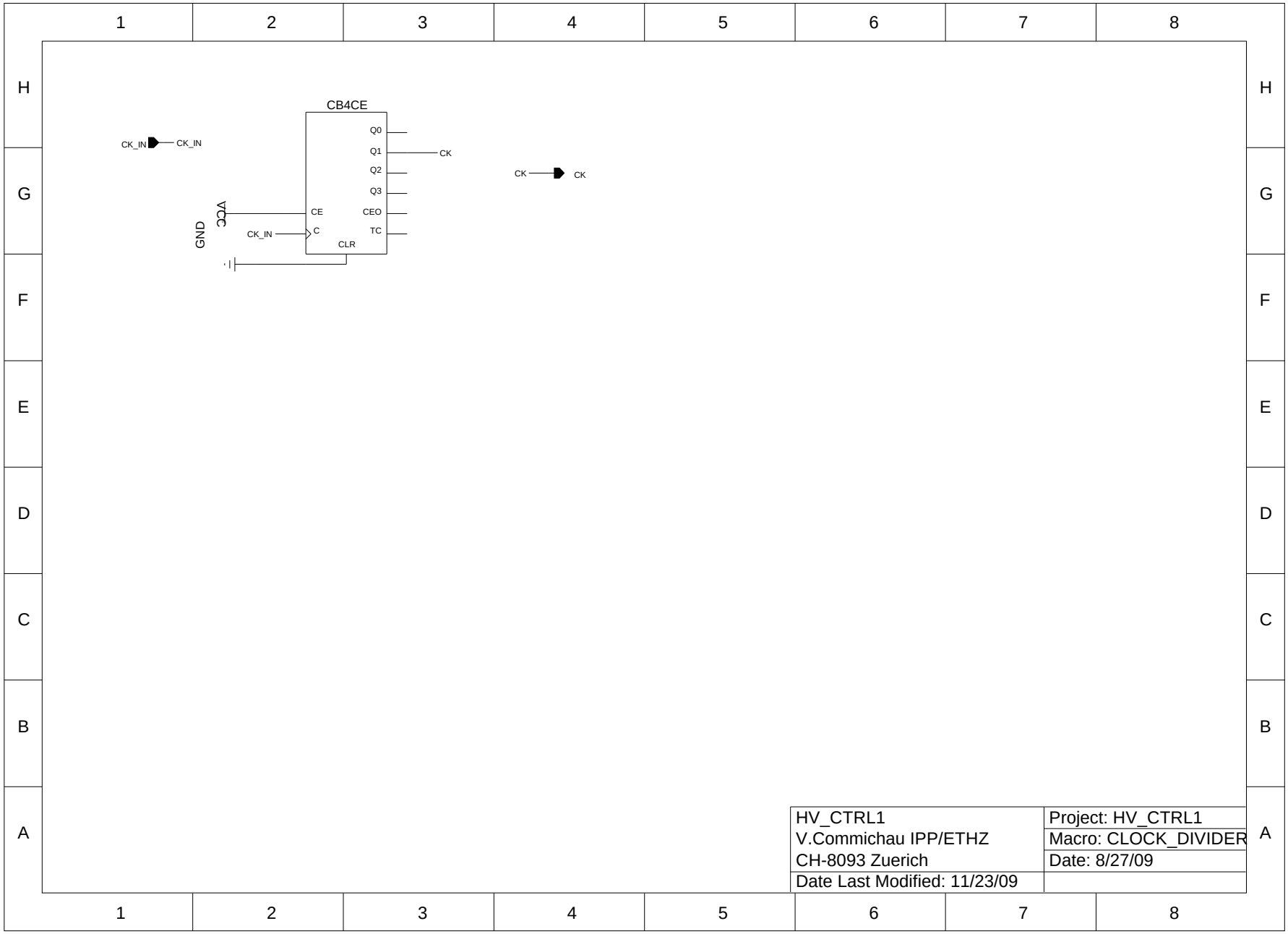
REV: A	DATE: 13.07.2009	ENG: V.COMMICHAU
PROJECT:	GAPD BIAS SUPPLY V02 SYSTEM CONTROLLER	
COMPANY: IPP ETHZ ADDRESS: SCHAFMATTSTR.20 CITY CH-8093 ZUERICH COUNTRY: SWITZERLAND#	FILE:POWSWI.SCH	
INITIAL 30.06.2009	PAGE: 4	OF: 4

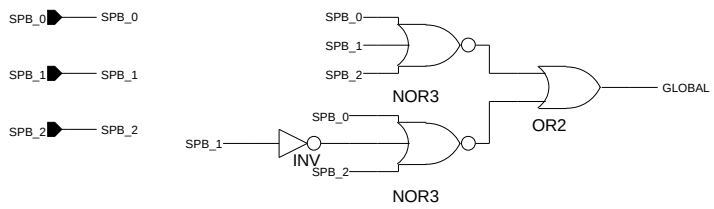

HV_CTRL_V1 19.01.2010
U1
IN_DATA
DIN[7:0]
U6
OUT_CONTROL
ADC[15:0]
U2
IN_CONTROL
U4
ADC_BUFFER
ADC[15:0]
U3
CLOCK_DIVIDER
U7
RESET
U5
GLOBAL_DECODER
BYTE[7:0]
optional I/O for MCU use
optional I/O for MCU use
HV_CTRL1
V.Commichau IPP/ETHZ
CH-8093 Zuerich
Date Last Modified: 1/19/10
Project: HV_CTRL1
Macro: HV_CTRL1
Date: 8/27/09

ADC DATA BUFFER



HV_CTRL1	Project: HV_CTRL1
V.Commichau IPP/ETHZ	Macro: ADC_BUFFER
CH-8093 Zuerich	Date: 8/27/09
Date Last Modified: 11/24/09	

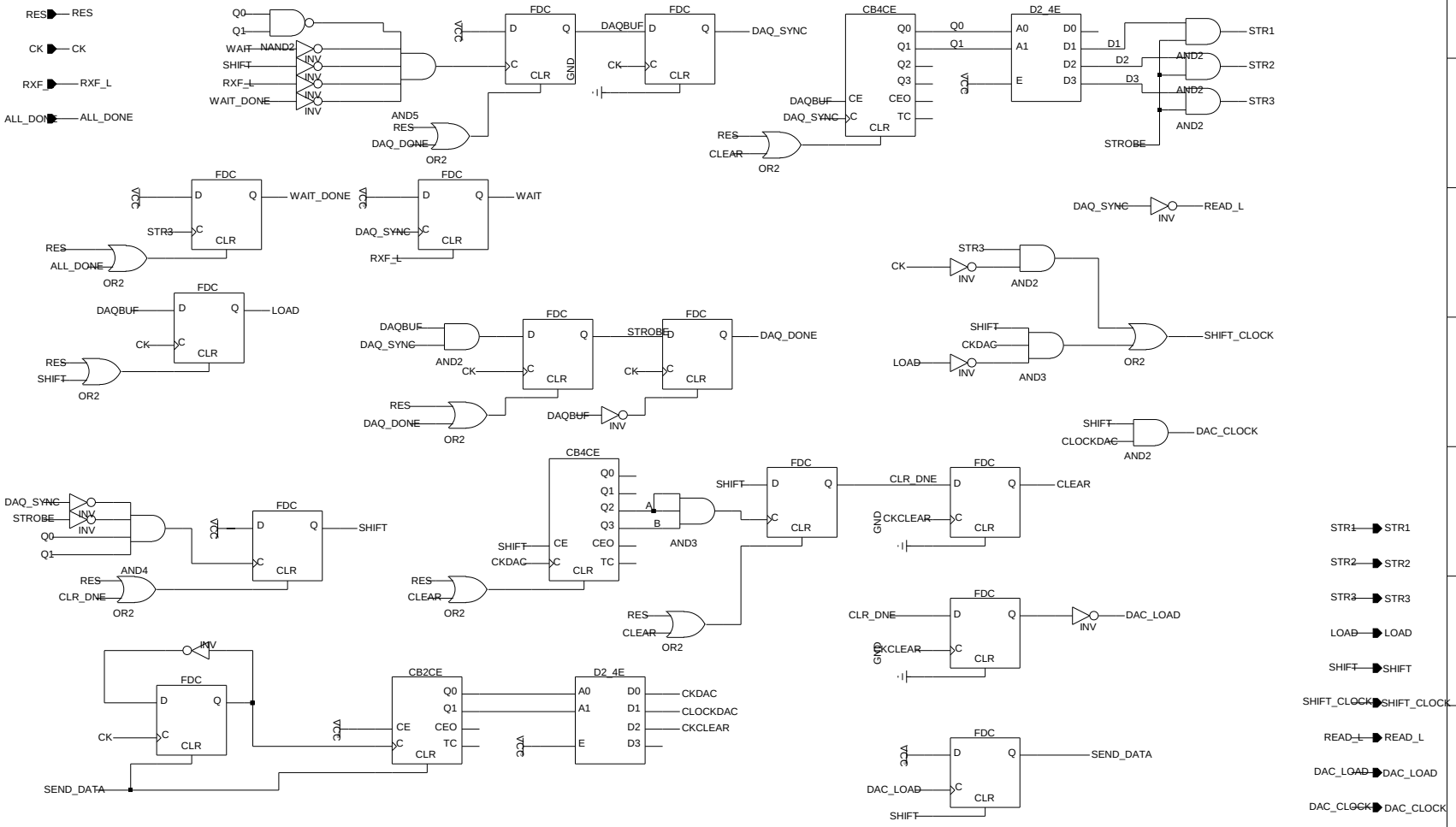

1
2
3
4
5
6
7
8
H
G
F
E
D
C
B
A
CB4CE
Q0
Q1
Q2
Q3
CE
CEO
C
TC
CLR
CK_IN
CK_IN
CK
CK
CK
CK_IN
VCC
GND
HV_CTRL1
V.Commichau IPP/ETHZ
CH-8093 Zuerich
Date Last Modified: 11/23/09
Project: HV_CTRL1
Macro: CLOCK_DIVIDER
Date: 8/27/09



Global for Reset & Set

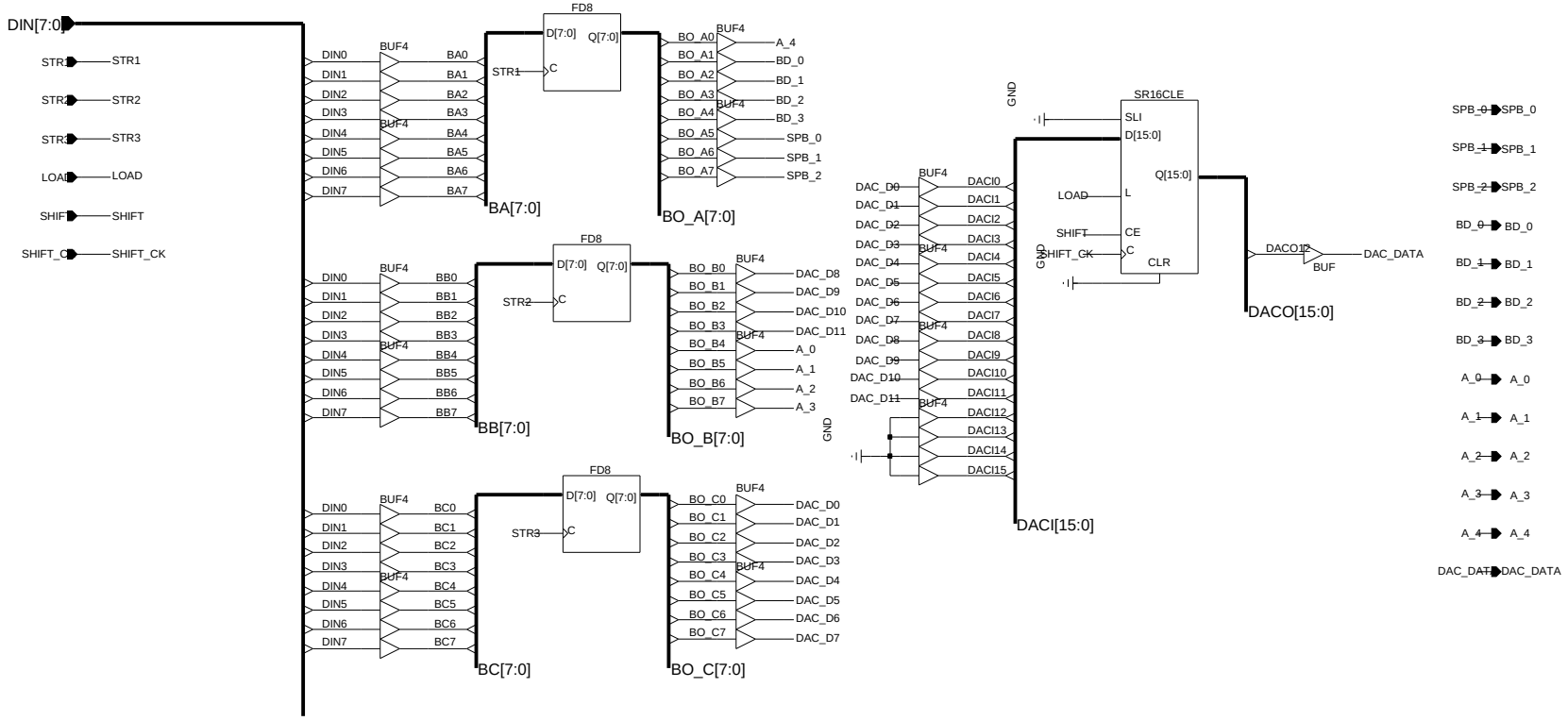
HV_CTRL1	Project: HV_CTRL1
V.Commichau IPP/ETHZ	Macro: GLOBAL_DECODER
CH-8093 Zuerich	Date: 8/27/09
Date Last Modified: 9/11/09	

INPUT CONTROL

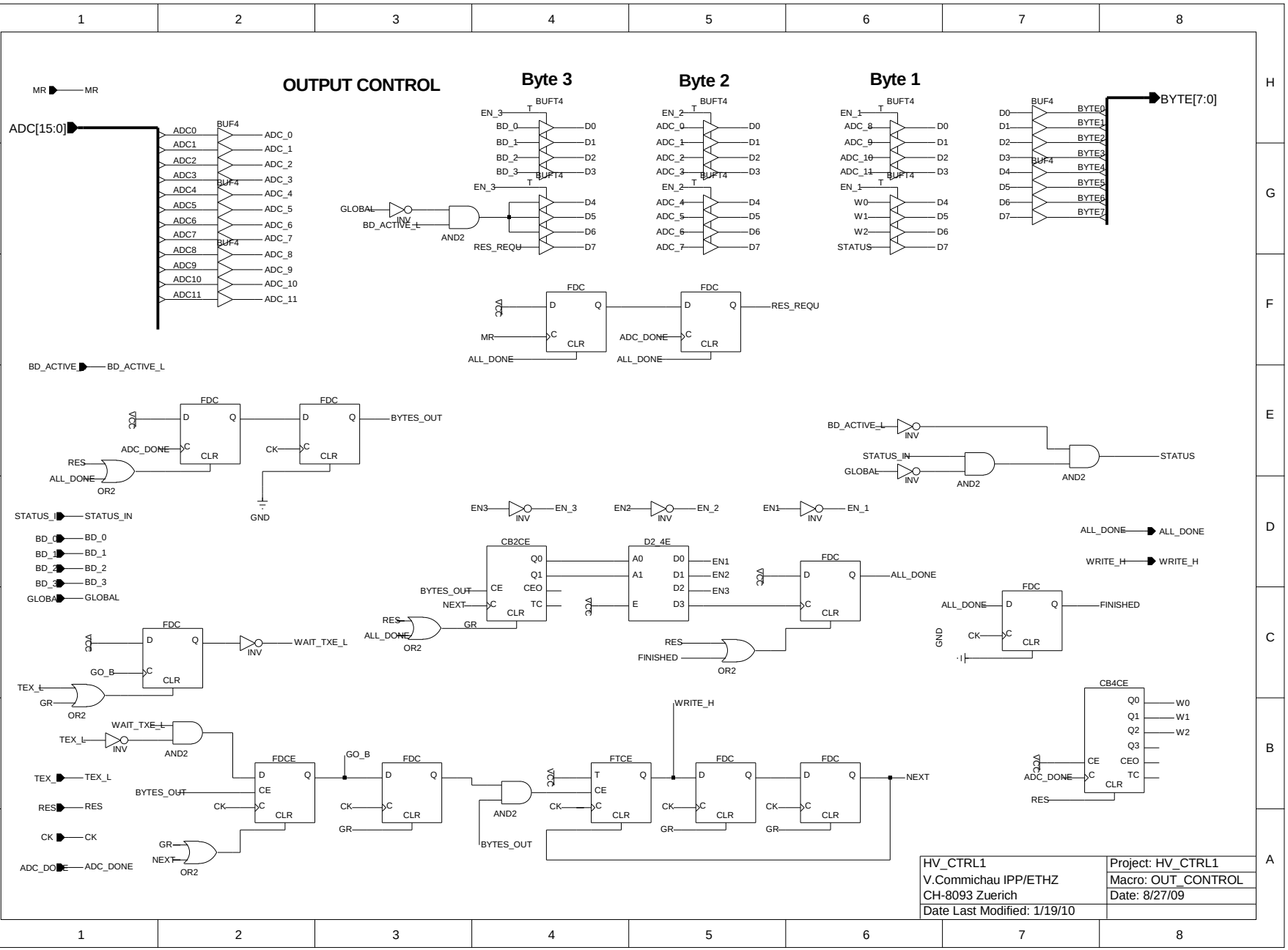


HV_CTRL1	Project: HV_CTRL1
V.Commichau IPP/ETHZ	Macro: IN_CONTROL
CH-8093 Zuerich	Date: 8/27/09
Date Last Modified: 1/19/10	

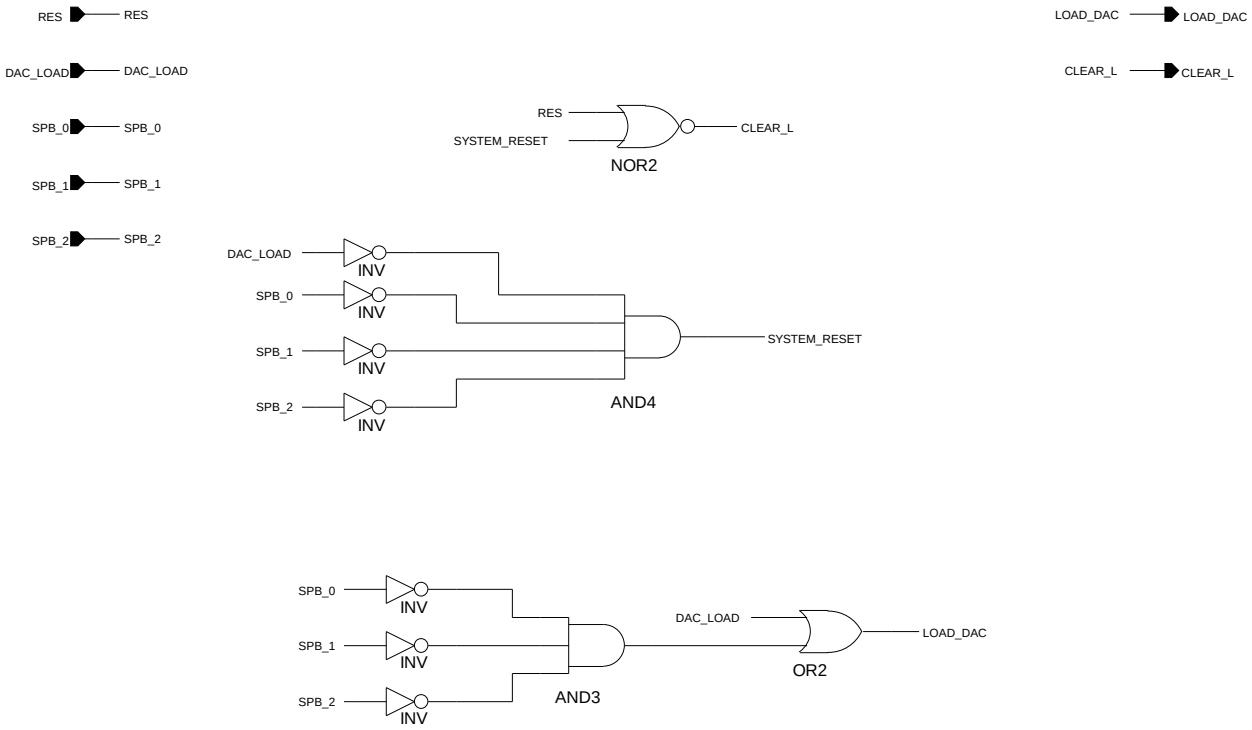
INPUT DATA BUFFER



HV_CTRL1	Project: HV_CTRL1
V.Commichau IPP/ETHZ	Macro: IN_DATA
CH-8093 Zuerich	Date: 8/27/09
Date Last Modified: 11/17/09	


OUTPUT CONTROL
Byte 3
Byte 2
Byte 1
MR
ADC[15:0]
BUF4
BUFT4
INV
AND2
OR2
FDC
FDCE
CB2CE
CB4CE
D2_4E
FTCE
GND
VCC
BYTE[7:0]
BD_ACTIVE
BD_ACTIVE_L
STATUS_IN
STATUS
BYTES_OUT
WAIT_TXE_L
RES_REQU
ALL_DONE
WRITE_H
FINISHED
NEXT
HV_CTRL1
V.Commichau IPP/ETHZ
CH-8093 Zuerich
Project: HV_CTRL1
Macro: OUT_CONTROL
Date: 8/27/09
Date Last Modified: 1/19/10

Reset from Hard&Soft



HV_CTRL1	Project: HV_CTRL1
V.Commichau IPP/ETHZ	Macro: RESET
CH-8093 Zuerich	Date: 8/27/09
Date Last Modified: 9/15/09	

HV CONTROL DAQ & ADC SEQUENCE

A.) Three BYTES INPUT SEQUENCE

1. Wait RXF goes to low
2. if: no WAIT, no SHIFT, no WAIT_DONE => set DAQBUF =1
3. DAQBUF & next SYSCK set LOAD = 1
4. DAQ_SYNC on next system clock (sysck)
5. WAIT = 1, by DAQ_SYNC
6. STROBE high on next sysck
7. Byte counter =1
8. STROBE & D1 => STR1
9. next sysck DAQ_DONE =1
10. DAQBUF = 0, => STROBE = 0, DAQ_DONE = 0
11. RXF goes to high, clears WAIT
12. Sequence #1 to #11 for STR2
13. Squence #1 to #8 for STR3
14. STR3 sets WAIT_DONE, stays high until ALL_DONE =1
15. STR3 clocks data into DAC shift register

B.) DAC SHIFT SEQUENCE

1. Byte counter = 3, STROBE = 0, DAQ_SYNC = 0 set SHIFT = 1
2. LOAD cleared by SHIFT = 1
3. SHIFT clock counter toggles to 12, sets CLR_DNE
4. Next sysck CLEAR = 1, clears SHIFT
5. DAC_LOAD generated by CLR_DNE&CLEAR on next sysck

C.) ADC SEQUENCE

1. On DAC_LOAD 0/1 ADC_EN = 1

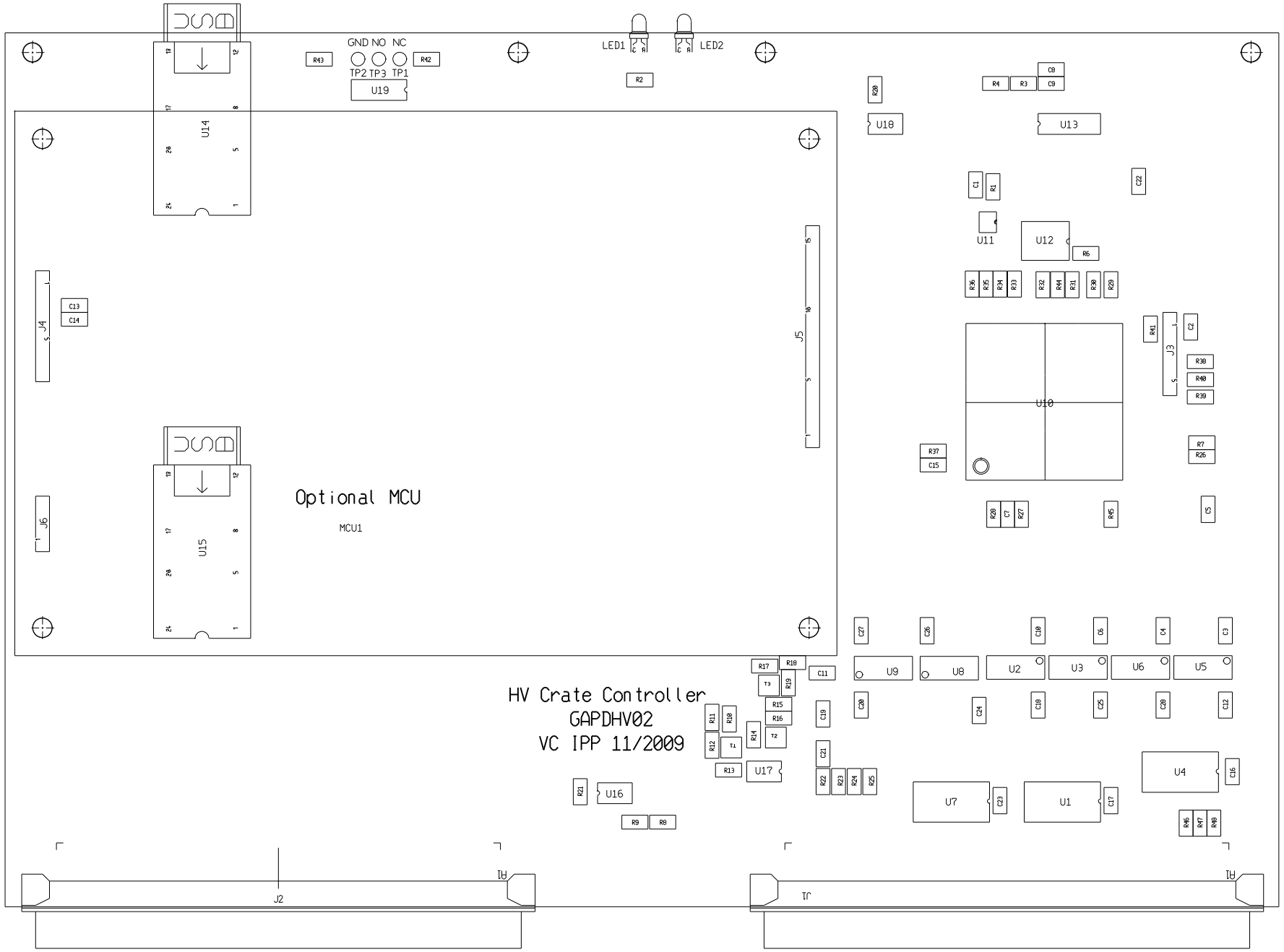
2. Slave ADC_SEL & ADC_EN enable serial input to shift register
3. ADC_CLOCK 0/1 clock data to shift register
4. GLOBAL or BD_ACTIVE_L = 1 clears shift register (all zeros)
5. Normal case: On ADC_SEL 0=>1 ADC_DONE = 1
6. Special case: Global or BD_ACTIVE_L = 1 generate ADC_DONE = 1

D.) THREE BYTES OUTPUT

1. ADC_DONE …next sysck sets BYTES_OUT = 1
2. Byte counter = 0, EN1 = 1 => EN_1 = 0, byte one low Z
3. On TEX_L = 0 & WAIT_TXE_L = 1, next sysck generates GO_B = 1
4. WAIT_TEX_L = 0
5. Write strobe generator enabled => WRITE_H = 1, byte one transferred
6. Next sysck NEXT = 1, WRITE_H = 0
7. Byte counter incremented to 1, => byte two low Z
8. TXE_L goes to one, WAIT_TXE_L = 1
9. Sequence continued until byte counter points to byte 4
10. ALL_DONE = 1, BYTES_OUT = 0, write sequencer stopped
11. ALL_DONE = 1 clears WAIT_DONE => enables next input byte(s)
12. On next sysck FINISHED = 1, ALL_DONE = 0
13. Next sysck FINISHED = 0

E.) RESET & SPECIAL SIGNALS

1. On SPB 0-2 = ZERO & DAC_LOAD = 0 => SYSTEM_RESET = ONE
2. Local RESET or SYSTEM_RESET = 1, => CLEAR = 1


GND NO NC
TP2 TP3 TP1
LED1
LED2
U19
U14
U15
U16
U17
U10
U13
U11
U12
U9
U8
U2
U3
U6
U5
U4
U7
U1
J4
J5
J6
J3
J2
J1
Optional MCU
MCU1
HV Crate Controller
GAPDHV02
VC IPP 11/2009

	GAPDHV02	**Crate Power Supplies**				
						TRACO
	32 Channel Board			**13 Units**		
	+5V	0,40		5.2A	26W	TML40105C
	+12V	0,01		0.2A	12W	TML20112C
	-12V	0,25		4A	48W	TMT50112C
	Controller			**1 Unit**		
	+5V			0.5A	2.5W	TIW 06-105
	90-100VDC	0,005		2A	180W (Crate)	HP extern

		APDHVNEW Parts List	
	Quantity	Value	Shape
	1	10UF	R/C1206
	1	BAV99	SOT23
	1	RED	R/C1206
	1	HDR_14	RM 2.54
	2	22K	R/C1206
	1	100K	R/C1206
	1	100	R/C1206
	1	10K	3266X POTI
	1	39K	R/C1206
	1	1K	R/C1206
	1	BC817-40	SOT23
	3	TESTPIN	
	1	74LVCG74	VSSOP8
	1	MAX4480	5SOT23
	1	HV7800	5SOT23
	1	OPA454	SO8P
	1	DAC8043U	SO8

Components	GAPDHV Board				
Quantity	Value	Shape	Distrelec	Farnell	
32	1NF	R/C1206			
16	100NF	R/C1206			
5	10UF	R/C1206			PRECI-DIP,CH
32	HDR_14	HDR1X14SP			714-87-114-31-018101
4	HDR_9	DB9FL	12 45 56		
1	HDR_6	HDR1X6	12 28 30		
2	DIN_64AC	DIN41612AC	12 10 74		
1	LED 3mm green	LED3R2_5H	63 21 25		
64	100K	R/C1206			
32	15K	R/C1206			
34	10K	R/C1206			
9	4K7	R/C1206			
2	680K	R/C1206			
1	10K	TRIM-3296Y	74 24 32		
1	39K	R/C1206			
1	680	R/C1206			
1	DIPSWITCH	DIP2X4	20 08 06		
1	BC807-40	SOT23	60 23 67		
33	AD8628	SOT23_5		13 194 76	
1	MAX6701LKA	SOT23-8			MAXIM
1	VX3_10MHZ	VX3E-1000	64 48 31		
1	XC95108-10-PC84C	$PLCC84			XILINX
1	74HCT221D	SO16	64 97 21		
1	ADR01AR	SO8		13 193 15	
1	LM321MF	SOT23_5	66 22 09		
3	SN74LS645-DW	SOL20		15 17 582	
1	LM79L05ACM	SO8	64 49 38		
1	REF195FSZ	SO8		13 195 22	
2	ADG706BRU	RU-28		90 04 332	
1	AD7476ARTZ	MO-178-AB		16 512 42	
4	74HCT151D	SO16	64 96 97		
2	74HCT154D	SOL24	64 97 01		
8	74HCT08D	SO14	64 96 53		

GAPDHV Controller Parts List						
Qantity	Value	Shape		Farnell	Distrelec	Other
1	DIP connector	DIP24		11 038 36		
5	100NF	R/C1206				
3	10UF	R/C1206				
1	DIN_64AC	DIN41612AC			12 63 33	
1	DIN_96ABC	DIN41612ABC			12 63 34	
1	HDR_6	HDR1X6			12 28 30	
1	HDR_8	HDR1X8				
1	HDR_16	HDR1X16				
1	HDR_4	HDR1X4				
2	LED	LED3R2_5H				
24	4K7	R/C1206				
1	680	R/C1206				
2	680K	R/C1206				
2	68K	R/C1206				
4	22K	R/C1206				
1	12K	R/C1206				
3	100K	R/C1206				
1	47K	R/C1206				
1	2K2	R/C1206				
1	0	R/C1206				
4	1K	R/C1206				
3	BC817-40	SOT23				
6	SN74LS645-1DW	SOL20		12 362 56		
6	HCPL-090J	NBSOIC16		16 113 23		
1	XC95216-10PQ160I	$PQ160				XILINX
1	MAX6701LKA	SOT23-8				MAXIM
1	VX3E-1000	10 MHz			64 48 31	
2	74HCT221	SO16		10 853 13		
1	UM245R	UM245R				Reselec AG
2	IRF6216	SO8		12 984 88		
2	IRF7451	SO8		10 134 60		
2	74HCT74	SO14		10 853 04		

HV Input Connector

Pin	Signal
1	**+95VDV**
2	**AGND**
3	
4	**Protective Ground**

78 DSUB HV Output Connector

Board N	Pin	HV Connector	HV Connector	Board N +1	Pin
HV0	C32	1	40	A13	AGND
HV1	C31	2	41	A14	AGND
HV2	C30	3	42	A15	AGND
HV3	C29	4	43	A16	AGND
HV4	C28	5	44	A17	AGND
HV5	C27	6	45	A18	AGND
HV6	C26	7	46	A19	AGND
HV7	C25	8	47	C32	HV0
HV8	C24	9	48	C31	HV1
HV9	C23	10	49	C30	HV2
HV10	C22	11	50	C29	HV3
HV11	C21	12	51	C28	HV4
HV12	C20	13	52	C27	HV5
HV13	C19	14	53	C26	HV6
HV14	C18	15	54	C25	HV7
HV15	C17	16	55	C24	HV8
HV16	C16	17	56	C23	HV9
HV17	C15	18	57	C22	HV10
HV18	C14	19	58	C21	HV11
HV19	C13	20	59	C20	HV12
HV20	C12	21	60	C19	HV13
HV21	C11	22	61	C18	HV14
HV22	C10	23	62	C17	HV15
HV23	C9	24	63	C16	HV16
HV24	C8	25	64	C15	HV17
HV25	C7	26	65	C14	HV18
HV26	C6	27	66	C13	HV19
HV27	C5	28	67	C12	HV20
HV28	C4	29	68	C11	HV21
HV29	C3	30	69	C10	HV22
HV30	C2	31	70	C9	HV23
HV31	C1	32	71	C8	HV24
AGND	A13	33	72	C7	HV25
AGND	A14	34	73	C6	HV26
AGND	A15	35	74	C5	HV27
AGND	A16	36	75	C4	HV28
AGND	A17	37	76	C3	HV29
AGND	A18	38	77	C2	HV30
AGND	A19	39	78	C1	HV31