David Nguyen

Lab 1

Section A

10/12/2018

Lab 1 Writeup

Purpose:

The purpose of this lab is to get an introduction to the Oscilloscope, Basys3 board, and Vivado. I also familiarized myself with the equipment and safety procedures in BE104. I learned how to connect and adjust the oscilloscope to get a stable image using a trigger. I then learned how to design a Verilog file, convert the file into a bit file, and run the bit file on the Basys3 board

Methods:

Part 1:

1. The first part is plugging in the oscilloscope probes into the oscilloscope. The probes pick up signal voltage and transfer this to be displayed on the oscilloscope. The next part of the oscilloscope is to learn how to adjust the scope. This starts by turning on the scope and setting it to a default state. There are knobs to adjust the vertical and horizontal scale of the respective channels. Here I am making sure the scope in the right scale to read the data from the waves.
2. I then need to adjust the trigger to get a table image. To get a stable image I change the mode to single mode and can force scope to take a sample of both signals. If the sampling is not synchronized, I would change the trigger type to edge and rising. I would then use knob labeled 5 to adjust the trigger level within the signal provided. The scope should now display the signal when the event occurs.
3. I then displayed the two waveforms first by connecting the wires and pins to the probes on the Bassys3 board as shown by the pictures in the lab. I then configured the FPGA with the ce100.bit files following the steps to configure the board. From here, it was reporting what we observed into our lab books.

Part 2:

1. The first part of part 2 is entering a schematic into Verilog file by creating a project and adding a design source. In this design course, I would add inputs and outputs based on the schematic given in the lab with variable names related to the switch and buttons used. I then added assign statements based on the logic of the gates in the schematic given. I also had to edit the Basys3_master.xdc file so the input and output names match on the constraint file.
2. When completing these steps, I used Elaborated Design to view the schematic and inspected it to see if it was correct. I would then generate the Bitstream which runs the implementation which in turns synthesizes, maps, places, and routes the house.

Results

For channel 1:

- Horizontal graduation = 15µs
- Vertical graduation = 3.225v
- Sweep rate = 50.00 µs
- Vertical gain = 2.00v
- Frequency = 6.667khz

For channel 2:

- Horizontal graduation = 1.75 µs
- Vertical graduation = 70 mv
- Sweep rate = 2.0 µs
- Vertical gain = 50.0 mv
- Frequency = 571.4281khz
- (notes, second signal was not like clear signal with clear ups and downs in the corner, picture will be included and also estimated drawn on the lab notebook. TA said to just write down the result of the machine and didn't know what was wrong).

Conclusion

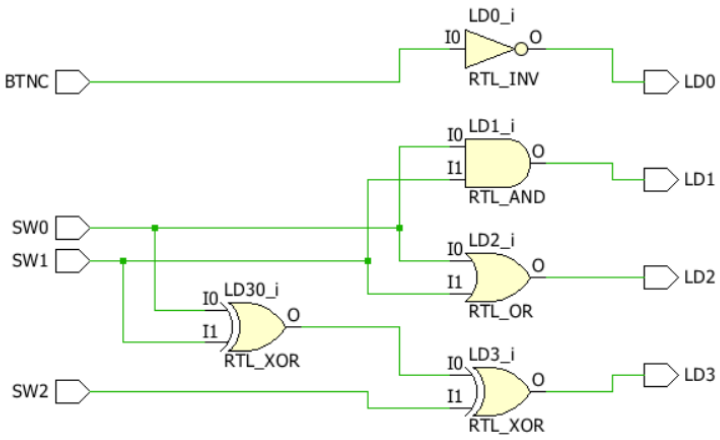
In conclusion, this lab acted as a preface for other labs coming up this quarter. In part 1, we worked with the bypass board and oscilloscope while figuring out how to display the bit file with the FPGA and oscilloscope. In part 2, I figured out how design and implement a schematic that lights up LEDs based on the given switches. This can be useful not to light up just LEDs, but can be used to implement a truth table or lighting up a 7 segment display.

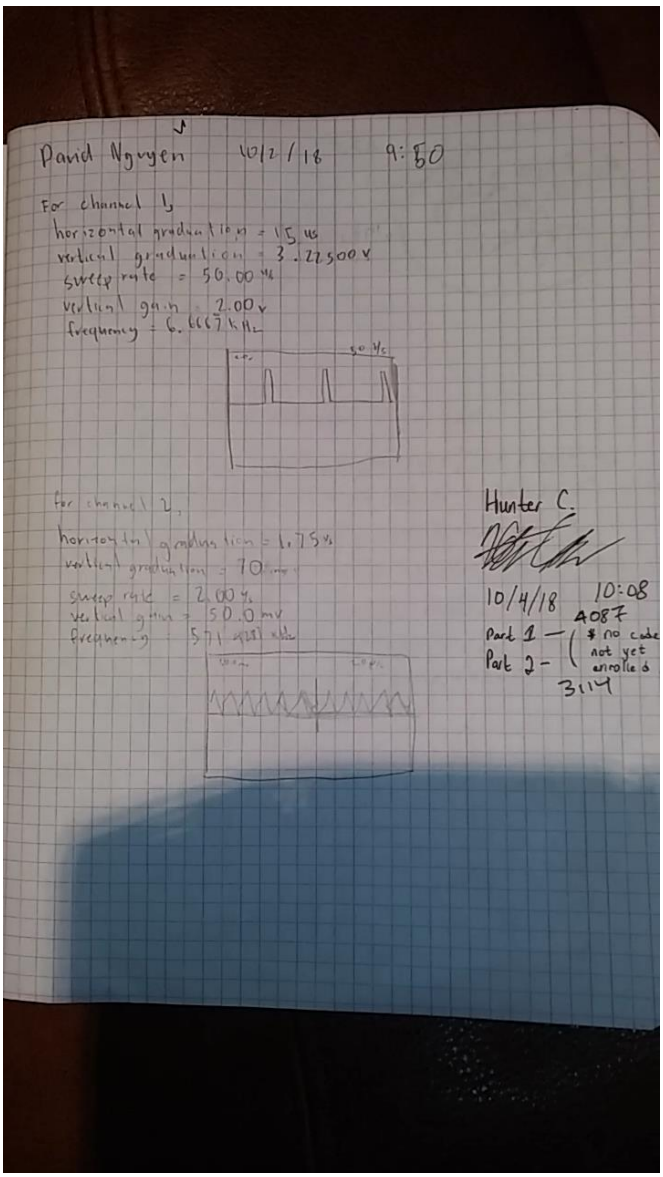
Supplementary material

```
module AND(
    input SW0,
    input SW1,
    input SW2,
    input BTNC,
    output LD0,
    output LD1,
    output LD2,
    output LD3
    );

    assign LD0 = ~BTNC;
    assign LD1 = SW0 & SW1;
    assign LD2 = SW0 | SW1;
    assign LD3 = SW0 ^ SW1 ^ SW2;

endmodule
```





David Nguyen 10/2/18 9:50

For channel 1:
horizontal graduation = 15 us
vertical graduation = 3.22500 V
sweep rate = 50.00 us
vertical gain = 2.00 V
frequency = 6.6667 kHz

for channel 2:
horizontal graduation = 6.75 us
vertical graduation = 70 mV
sweep rate = 2.00 us
vertical gain = 50.0 mV
frequency = 571 kHz

Hunter C.

10/4/18 10:08
Part 1 — 4087
Part 2 — ($ no cube not yet enrolled
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