

# **Systems with Analog integrated Circuits**

## **Analog Interface Design and Simulation**

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Year/Series/Group : 3<sup>rd</sup>-EA-2031/3

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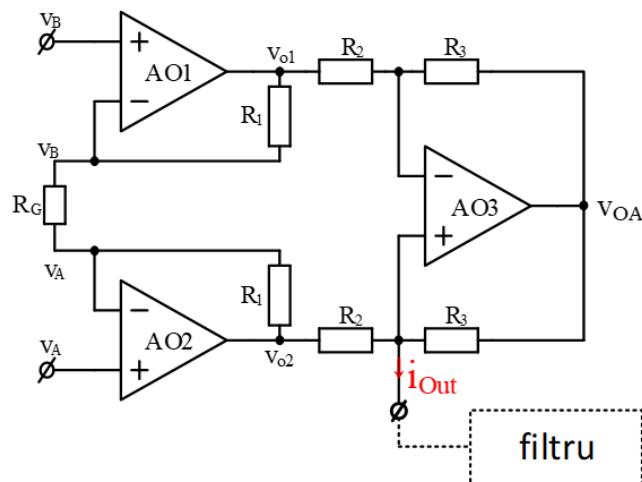
## Contents

1.	Project Thematic .....	3
1.1	Specifications.....	3
First stage.....	3	
Second stage.....	4	
Third stage.....	5	
Fourth stage.....	6	
2.	Components sizing.....	7
First stage.....	7	
Second stage.....	8	
Third stage.....	9	
Fourth stage.....	10	
3.	Analysis and Characterization .....	11
First stage.....	11	
Second stage.....	15	
Third stage.....	17	
Fourth stage.....	23	
4.	The Final Schematic and Functionality .....	24
5.	Conclusion .....	25

# 1. Project Thematic

## 1.1 Specifications

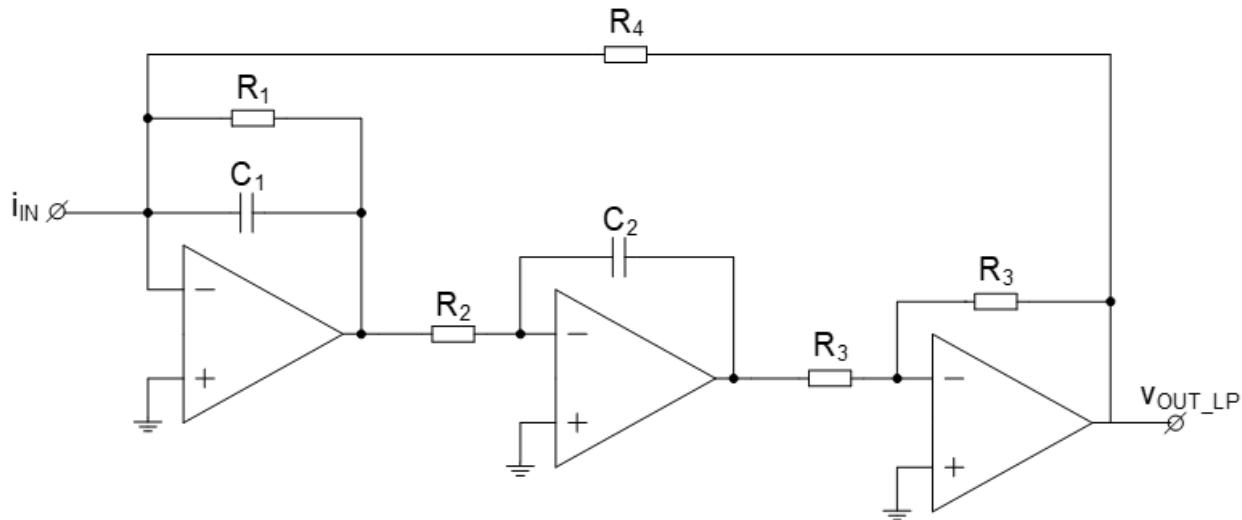
### First stage



Characteristics:

Sursa semnal	amplitudine minima (pt castig maxim PGA)	amplitudine maxima (pt castig minim PGA)	unitate masura	Tip Etaj 1	Castig  etaj 1 (liniar)
2	7.05E-02	1.41E-01	V (differential)	8	0.002

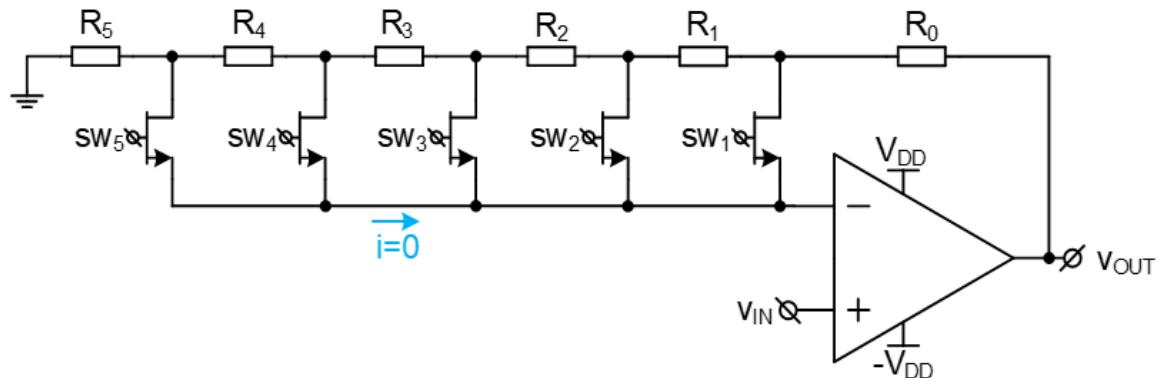
## Second stage



Characteristics

tip Etaj 2	$ H_0 $ castig liniar in banda de trecere	Rintrare minim	Banda	Q
6	5000	-	3.00E+03	1.41

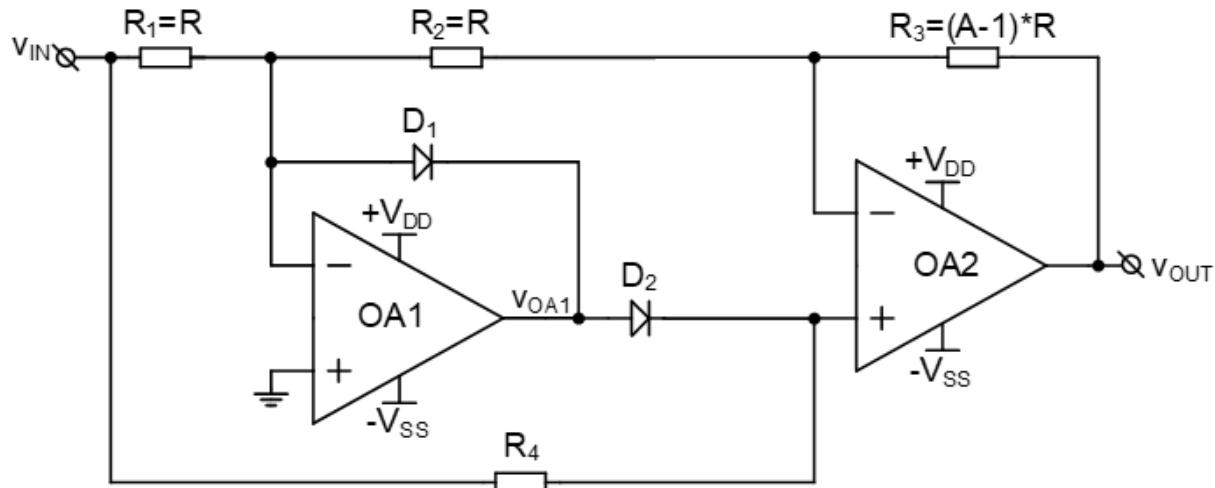
### Third stage



### Characteristics

tip Etaj 3	castig minim [dB]	rezolutie (pas minim) [dB]	nr pasi	castig maxim [dB]	Rintrare minim
.	6	5	2	4	11

## Fourth stage

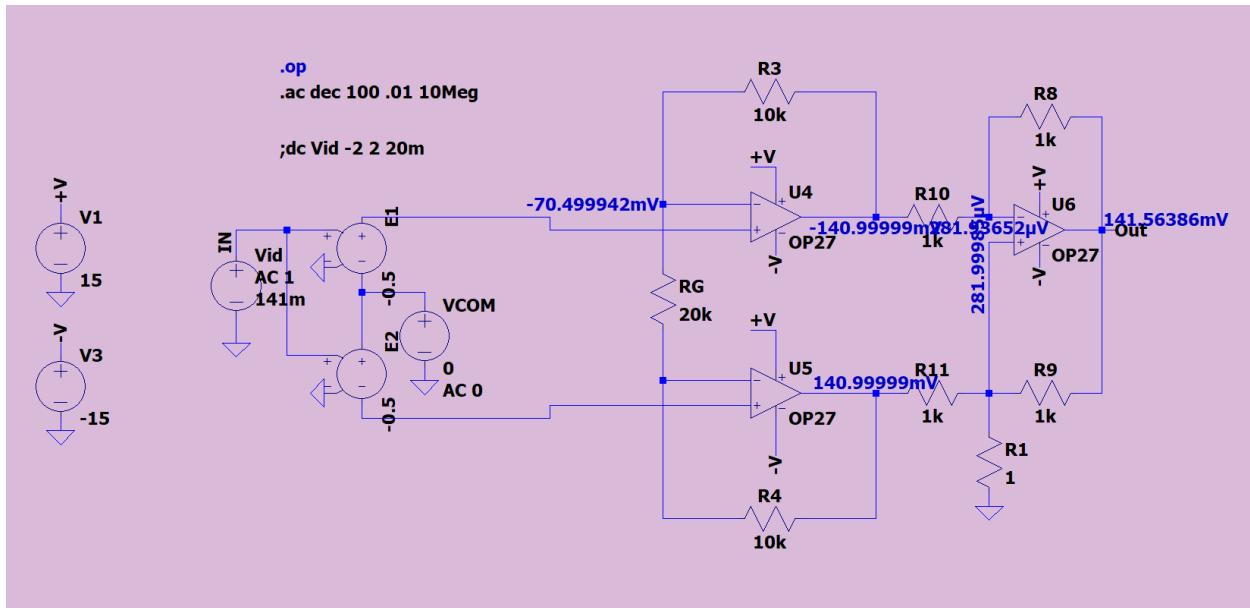


Characteristics

tip Etaj 4	Castig  etaj 4 (liniar)	Tip AO
3	2	9

## 2. Components sizing

### First stage



The circuit is designed to take a small differential input voltage (Vid) and amplify it while rejecting common-mode noise

$$\text{The total gain is } A_{total} = \left(1 + \frac{R_3 + R_4}{R_G}\right)$$

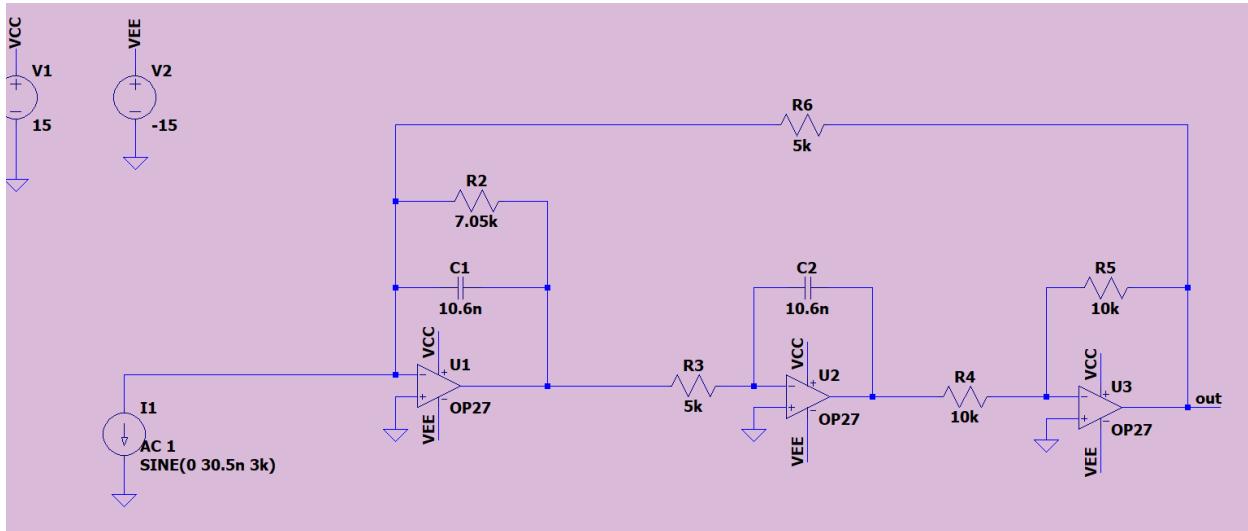
$$\Rightarrow R_3 = R_4 = 19\text{k}\Omega$$

$$R_{10} = R_{11} = 1\text{k}\Omega$$

$$R_8 = R_9 = 1\text{k}\Omega$$

$$R_1 = 1\Omega$$

## Second stage



w0 [rad/sec]	Q	f0 [Hz]	H0 [linear]	
1.88E+04	1.41E+00	3.00E+03	5.00E+03	
C1=C2 [F]	R1 [Ohm]	R2 [Ohm]	R3 [Ohm]	R4 [Ohm] = H0
1.06E-08	7.05E+03	5.00E+03	1.00E+04	5.00E+03

LPF transfer function parameters

$$H_0 = R_4; \omega_0 = \frac{1}{\sqrt{R_2 R_4 C_1 C_2}} \quad Q = R_1 \sqrt{\frac{C_1}{C_2} \cdot \frac{1}{R_2 R_4}}$$

Sizing strategy:

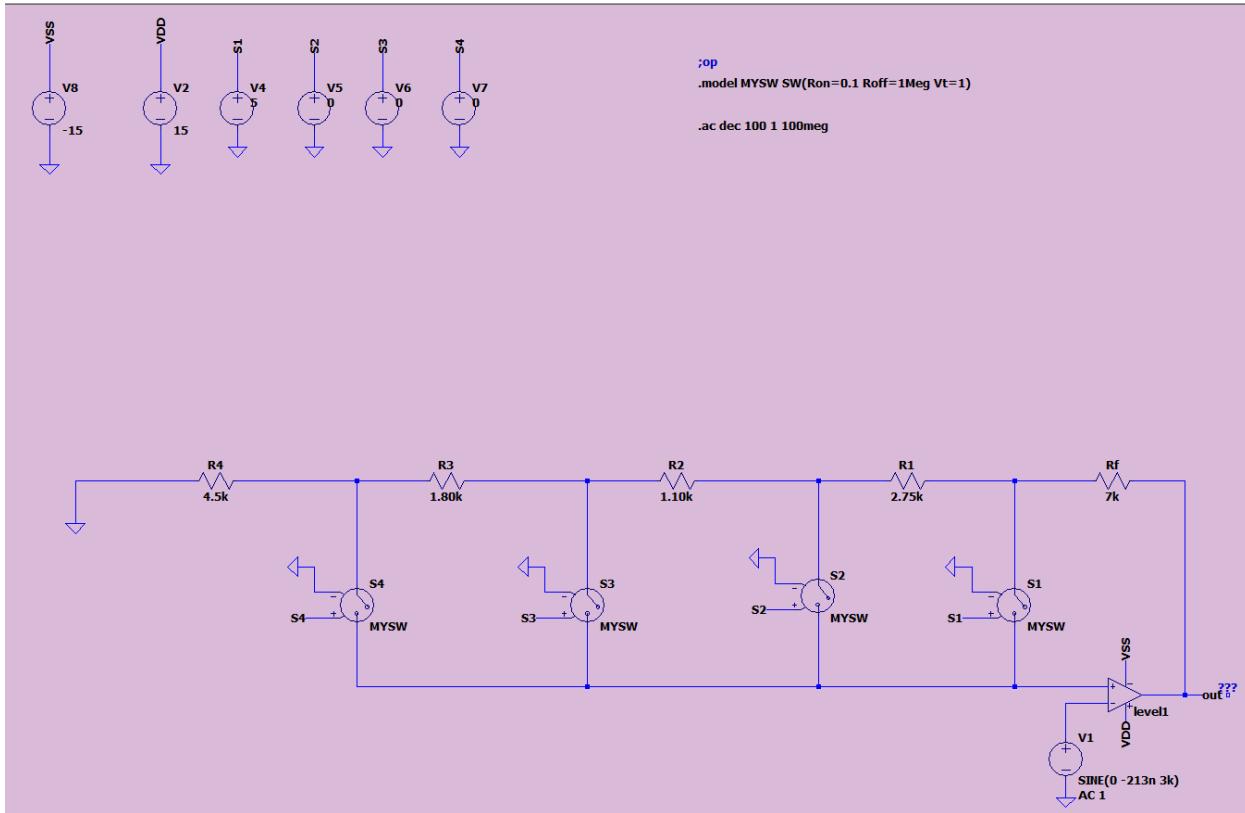
$$H_0 = R_4;$$

set  $R_2 = R_4$ ; choose the value of  $R_3$

$$C_1 = C_2 = \frac{1}{\omega_0 \cdot R_2}$$

$$R_1 = Q \cdot R_2.$$

## Third stage

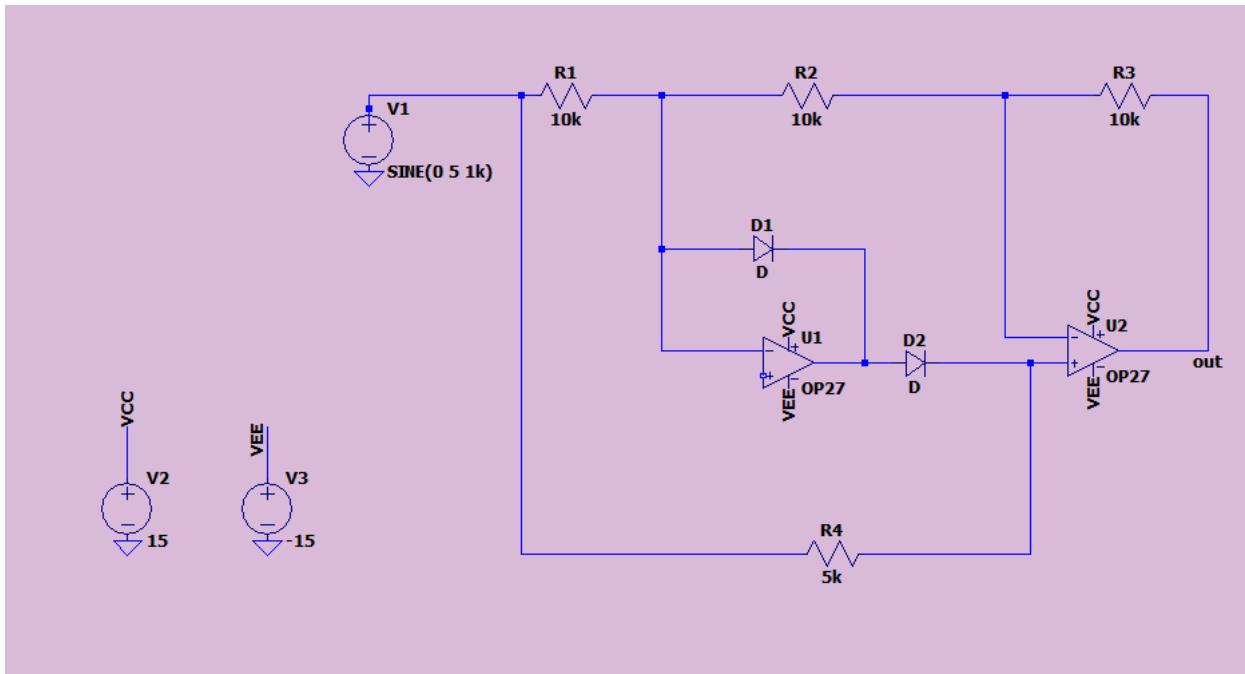


$$A_v = 1 + \frac{Rf}{Rg} \quad R_g = -\frac{Rf}{Av - 1}$$

Choose  $R_f = 7k\Omega$

- 11dB (Av=3.55k):**  $S_4$  is ON.  $R_4=4.5\text{ k}\Omega$ .
  - 9dB (Av=2.82l):**  $S_3$  is ON.  $R_3=1.80\text{ k}\Omega$
  - 7dB (2.24k):**  $S_2$  is ON.  $R_2=1.10\text{ k}\Omega$ .
  - 5dB (1.78k):**  $S_1$  is ON.  $R_1=2.75\text{ k}\Omega$

## Fourth stage



$$V_{out} = -V_{in} \left( \frac{R_3}{R_4} \right)$$

$R_3/R_4=2 \Rightarrow R_3=10k, R_4=5k$

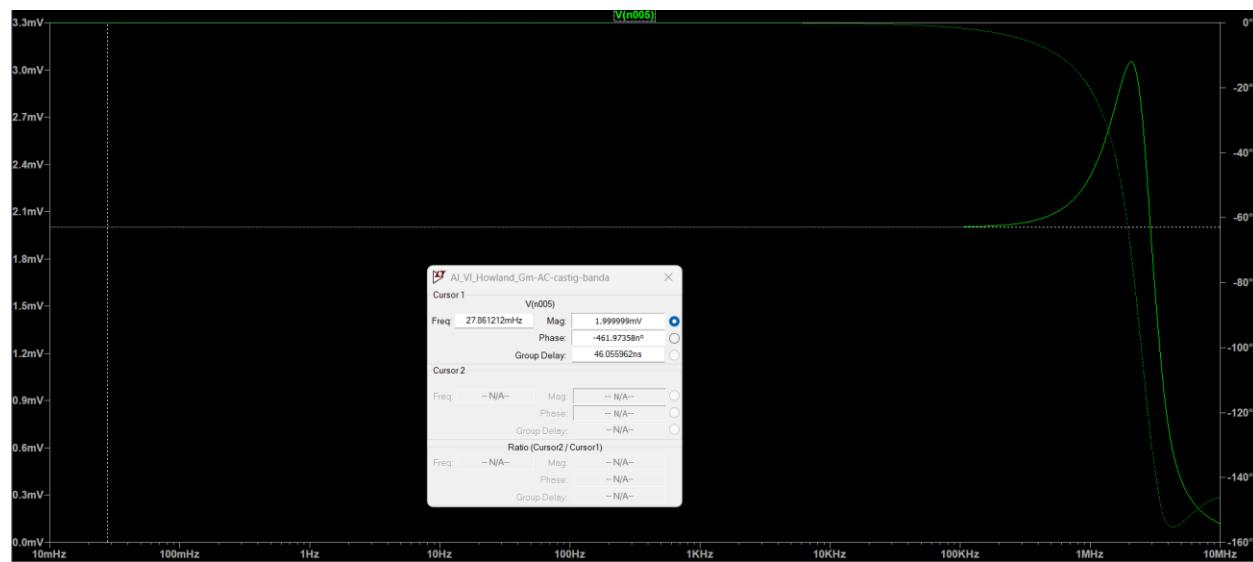
### 3. Analysis and Characterization

#### First stage

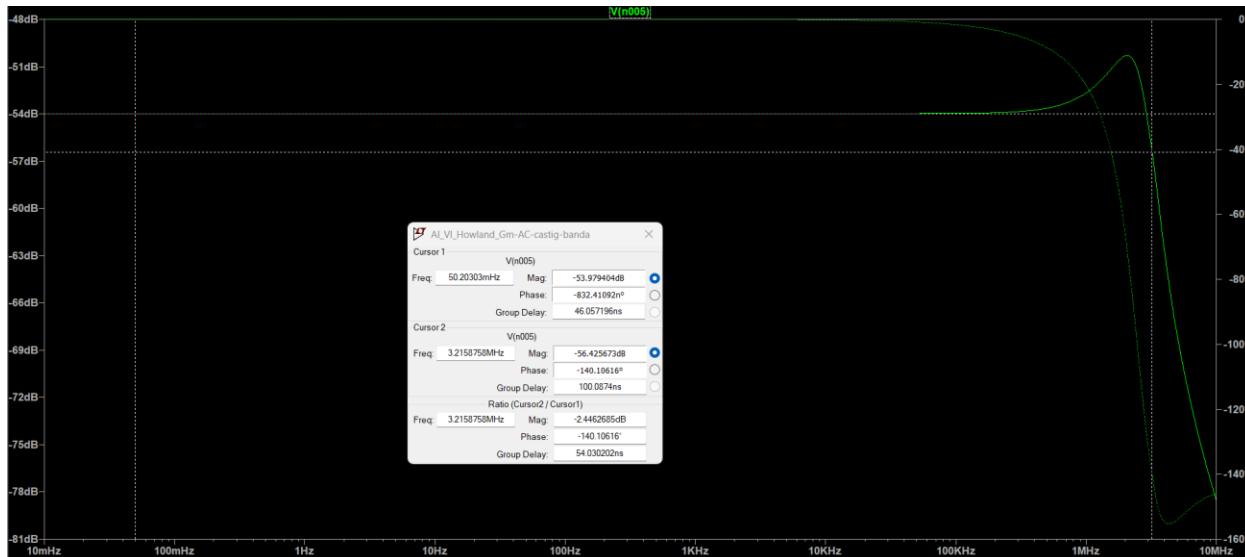
##### OP Analysis

--- Operating Point ---		
V(-v) :	-15	voltage
V(out) :	0.0707819	voltage
V(n003) :	0.000140968	voltage
V(n002) :	-0.0705	voltage
V(n007) :	0.03525	voltage
V(n004) :	-0.03525	voltage
V(n009) :	0.03525	voltage
V(+v) :	15	voltage
V(in) :	0.0705	voltage
V(n005) :	0.000141	voltage
V(n008) :	0.0705	voltage
V(n001) :	-0.03525	voltage
V(n006) :	0	voltage
I(V1) :	-0.00897508	device_current
I(Vid) :	0	device_current
I(R9) :	7.06409e-05	device_current
I(R10) :	7.0641e-05	device_current
I(RG) :	-3.525e-06	device_current
I(VCOM) :	4.91277e-19	device_current
I(E2) :	5.88014e-12	device_current
I(R1) :	0.000141	device_current
I(R8) :	7.0641e-05	device_current
I(R11) :	-7.0359e-05	device_current
I(R3) :	-3.525e-06	device_current
I(R4) :	3.525e-06	device_current
I(E1) :	5.88014e-12	device_current
I(V3) :	0.00883408	device_current
---		
V(-v) :	-15	voltage
V(out) :	0.141564	voltage
V(n003) :	0.000281937	voltage
V(n002) :	-0.141	voltage
V(n007) :	0.0704999	voltage
V(n004) :	-0.0705	voltage
V(n009) :	0.0705	voltage
V(+v) :	15	voltage
V(in) :	0.141	voltage
V(n005) :	0.000282	voltage
V(n008) :	0.141	voltage
V(n001) :	-0.0704999	voltage
V(n006) :	0	voltage
I(V1) :	-0.00905156	device_current
I(Vid) :	0	device_current
I(R9) :	0.000141282	device_current
I(R10) :	0.000141282	device_current
I(RG) :	-7.04999e-06	device_current
I(VCOM) :	9.8227e-19	device_current
I(E2) :	1.17603e-11	device_current
I(R1) :	0.000282	device_current
I(R8) :	0.000141282	device_current
I(R11) :	-0.000140718	device_current
I(R3) :	-7.05001e-06	device_current
I(R4) :	7.05001e-06	device_current
I(E1) :	1.17603e-11	device_current
I(V3) :	0.00876956	device_current
---		

##### Low frequency gain

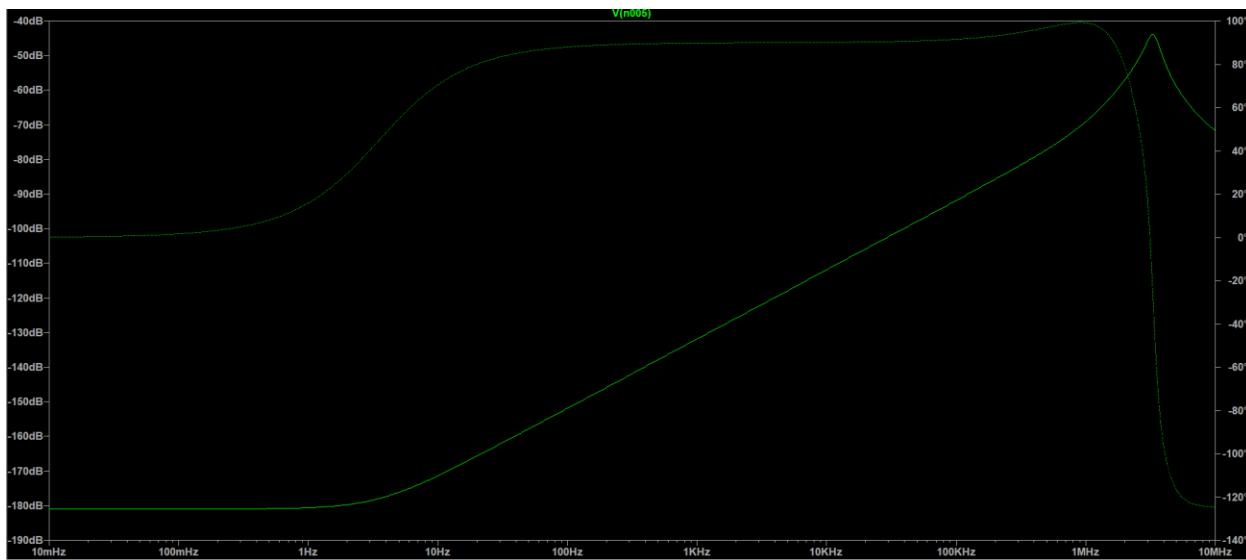


### Bandwidth>Bw filter



The frequency response of the amplifier stage was analyzed to ensure the bandwidth exceeds the requirements of the subsequent filtering stages. Simulation results confirm a stable mid-band gain of **0.002 (-53.42 dB)** from DC. Using the -3 dB criterion, the amplifier bandwidth was measured at **3.215MHz**. The filter bandwidth is 3kHz ( $3.215\text{MHz} > 3\text{kHz}$ )

### CMRR

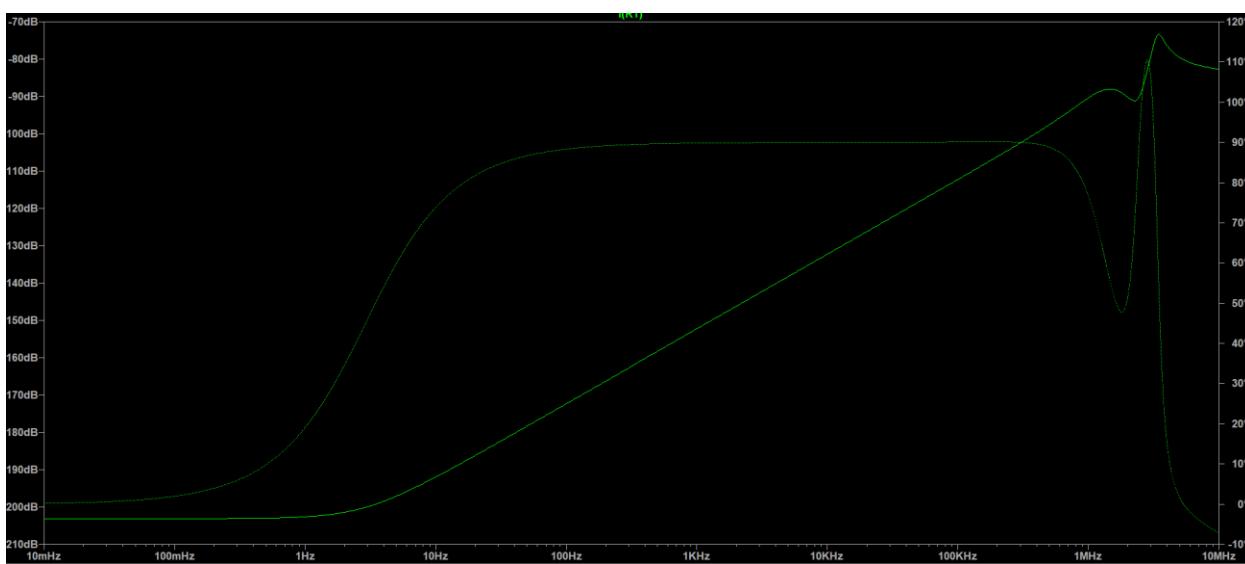


The common-mode rejection ratio (CMRR) is defined as the ratio between the differential gain (AD) and the common-mode gain (ACM).

$$CMRRdB = Av[dB] - ACM[dB]$$

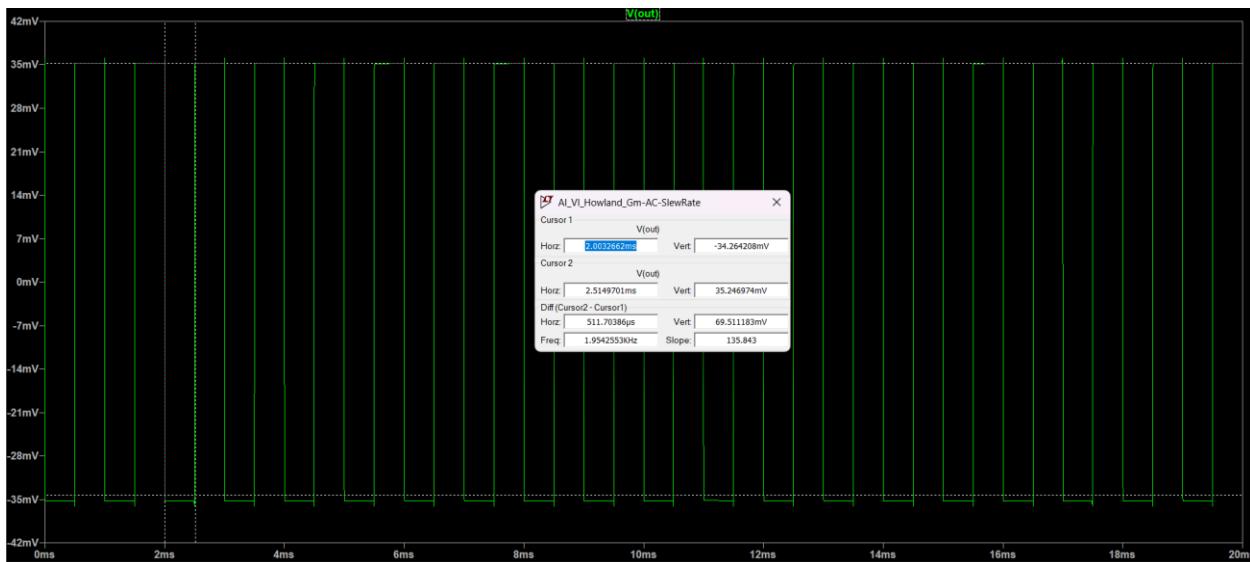
From the simulation the CMRR at low frequencies is around -180 dB(Acm) and the differential gain is -53.42 dB (Av). This gives a final value of approx. 126 dB which confirms excellent CMRR for the instrument amplifier.

## PSRR

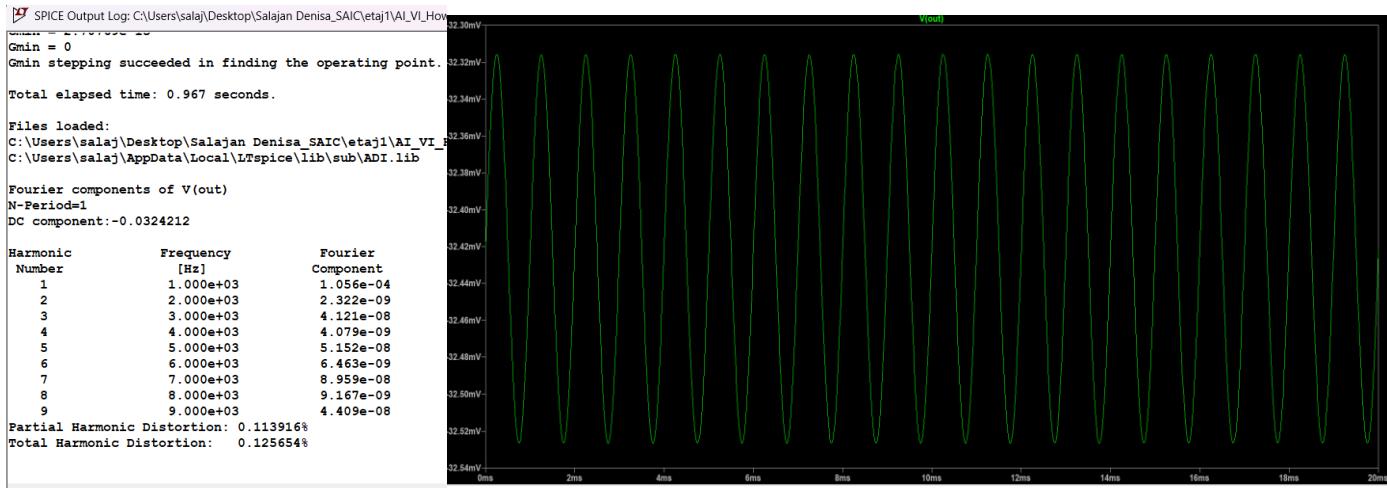


The **PSRR (Power Supply Rejection Ratio)** simulation confirms high circuit stability against power supply fluctuations. At critical ripple frequencies (**50–100 Hz**), the rejection is approximately **-105dB**, ensuring an extremely stable output current that remains immune to noise originating from the voltage regulators.

Slew Rate =  $\Delta V / \Delta T = \text{slope}$



THD<1%

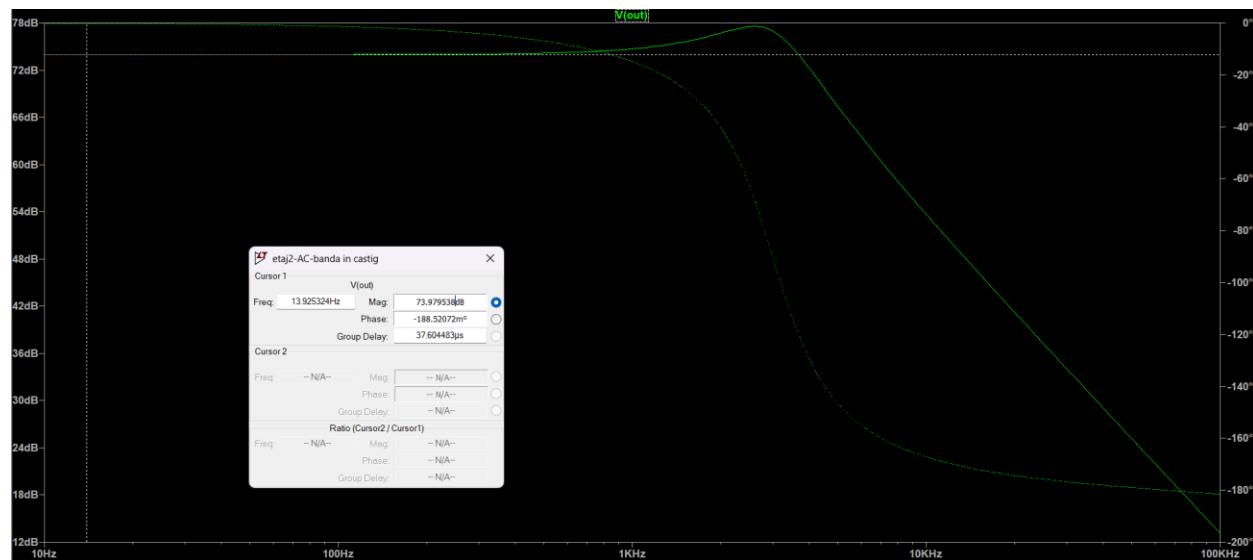


## Second stage

DCOP

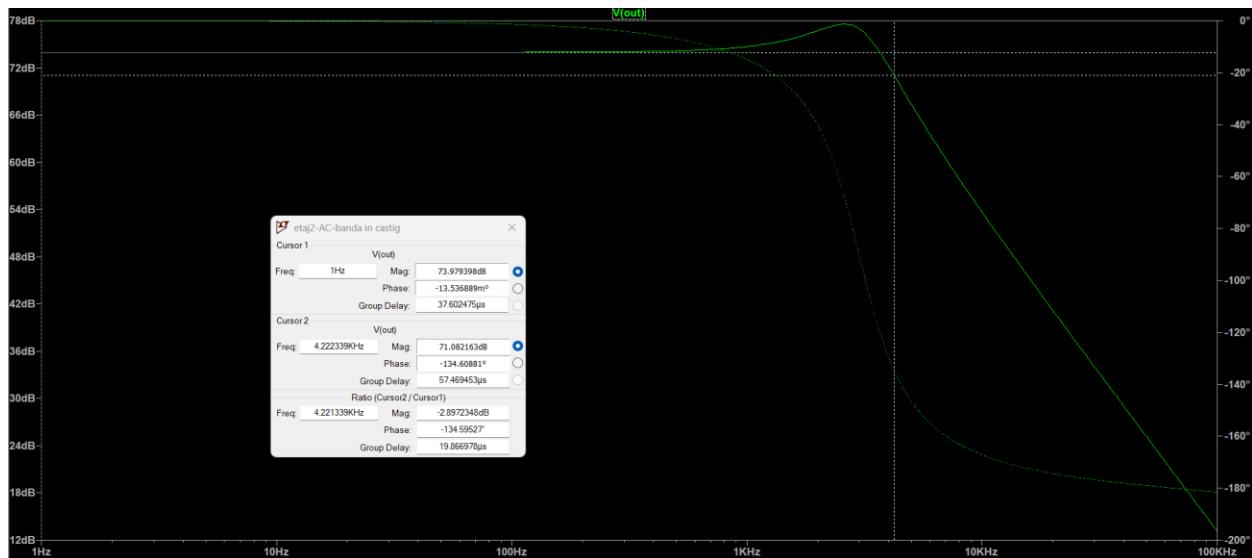
```
C:\Users\salaj\Desktop\Salajan Denisa_SAIC\etaj2\etaj2-AC-band
--- Operating Point ---
V(vee) : -15 voltage
V(n001) : 0 voltage
V(n003) : 0 voltage
V(n004) : 0 voltage
V(vcc) : 15 voltage
V(n002) : 0 voltage
V(n005) : 0 voltage
V(out) : 0 voltage
I(V1) : -0.00890259 device_current
I(R2) : 0 device_current
I(R4) : 0 device_current
I(R5) : 0 device_current
I(C2) : 0 device_current
I(R3) : 0 device_current
I(R6) : 0 device_current
I(I1) : 0 device_current
I(V2) : 0.00890259 device_current
I(C1) : 0 device_current
Ix(u2:1) : 0 subckt_current
Ix(u2:2) : 0 subckt_current
Ix(u2:3) : 0.00296753 subckt_current
Ix(u2:4) : -0.00296753 subckt_current
Ix(u2:5) : 0 subckt_current
Ix(u1:1) : 0 subckt_current
Ix(u1:2) : 0 subckt_current
Ix(u1:3) : 0.00296753 subckt_current
Ix(u1:4) : -0.00296753 subckt_current
... /-1.5 ... -----
```

AC Analysis(castig in banda de trecere)



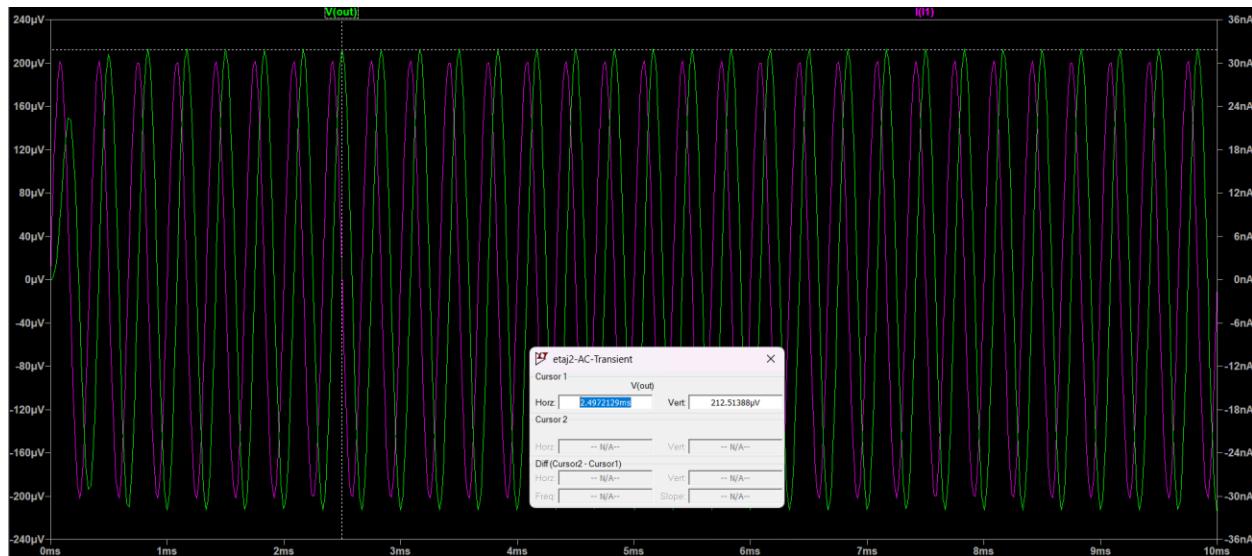
$$74\text{db} = H_0 = 5000$$

## Bandwidth



The simulation result is at 4.22kHz which represents a deviation from the specification of 3kHz, confirming the accuracy of the integration constants (R and C)

THD<1%



```

SPICE Output Log: C:\Users\salaj\Desktop\Salajan Denisa_SAIC\etaj2\etaj2-AC-Transient.log

Gmin = 0
Gmin stepping succeeded in finding the operating point.

Total elapsed time: 0.659 seconds.

Files loaded:
C:\Users\salaj\Desktop\Salajan Denisa_SAIC\etaj2\etaj2-AC-Transient.net
C:\Users\salaj\AppData\Local\LTspice\lib\sub\ADI.lib

Fourier components of V(out)
N-Period=1
DC component:-9.27909e-08

Harmonic      Frequency          Fourier          Normalized          Phase
Number       [Hz]             Component        Component        [deg]
  1           3.000e+03     2.115e-04    1.000e+00     -179
  2           6.000e+03     1.353e-07    6.397e-04     -179
  3           9.000e+03     4.753e-07    2.247e-03      -64
  4           1.200e+04     1.500e-07    7.092e-04      167
  5           1.500e+04     1.803e-07    8.526e-04      46
  6           1.800e+04     7.014e-08    3.316e-04     166
  7           2.100e+04     1.458e-07    6.893e-04      62
  8           2.400e+04     8.554e-08    4.044e-04     132
  9           2.700e+04     2.394e-07    1.132e-03      94

Partial Harmonic Distortion: 0.295274%
Total Harmonic Distortion: 0.582156%

```

## Third stage

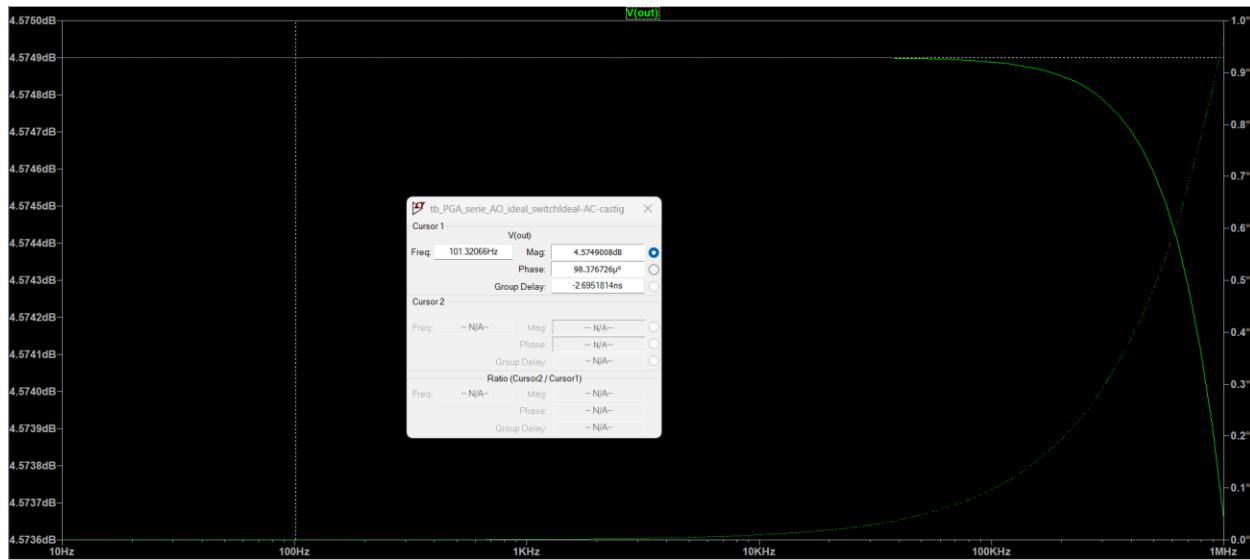
DCOP (min and max)

--- Operating Point ---			--- Operating Point ---		
V(n006) :	1	voltage	V(n006) :	1	voltage
V(n004) :	1	voltage	V(n004) :	2.24597	voltage
V(s1) :	5	voltage	V(s1) :	0	voltage
V(s3) :	0	voltage	V(s3) :	0	voltage
V(n001) :	0.445711	voltage	V(n001) :	1	voltage
V(n005) :	1	voltage	V(n005) :	1	voltage
V(vss) :	-15	voltage	V(vss) :	-15	voltage
V(vdd) :	15	voltage	V(vdd) :	15	voltage
V(n003) :	0.730924	voltage	V(n003) :	1.63828	voltage
V(s2) :	0	voltage	V(s2) :	0	voltage
V(s4) :	0	voltage	V(s4) :	5	voltage
V(out) :	1.69334	voltage	V(out) :	3.80155	voltage
V(n002) :	0.622997	voltage	V(n002) :	1.3959	voltage
I(V5) :	0	device_current	I(V5) :	0	device_current
I(Rf) :	9.90488e-05	device_current	I(Rf) :	0.000222225	device_current
I(R4) :	-9.90468e-05	device_current	I(R4) :	-0.000222223	device_current
I(S3) :	3.77005e-07	device_current	I(S3) :	-3.95901e-07	device_current
I(V2) :	-2.8e-08	device_current	I(V2) :	-2.8e-08	device_current
I(R1) :	-9.78464e-05	device_current	I(R1) :	-0.000220979	device_current
I(V6) :	0	device_current	I(V6) :	0	device_current
I(S2) :	2.69078e-07	device_current	I(S2) :	-6.38276e-07	device_current
I(V8) :	3.2e-08	device_current	I(V8) :	3.2e-08	device_current
I(V1) :	-2e-09	device_current	I(V1) :	-2e-09	device_current
I(V7) :	0	device_current	I(V7) :	0	device_current
I(R3) :	-9.84925e-05	device_current	I(R3) :	-0.000219945	device_current
I(R2) :	-9.81155e-05	device_current	I(R2) :	-0.000220341	device_current
I(S1) :	-1.20237e-06	device_current	I(S1) :	-1.24597e-06	device_current
I(C1) :	5.54000e-07	device_current	I(C1) :	2.07815e-06	device_current

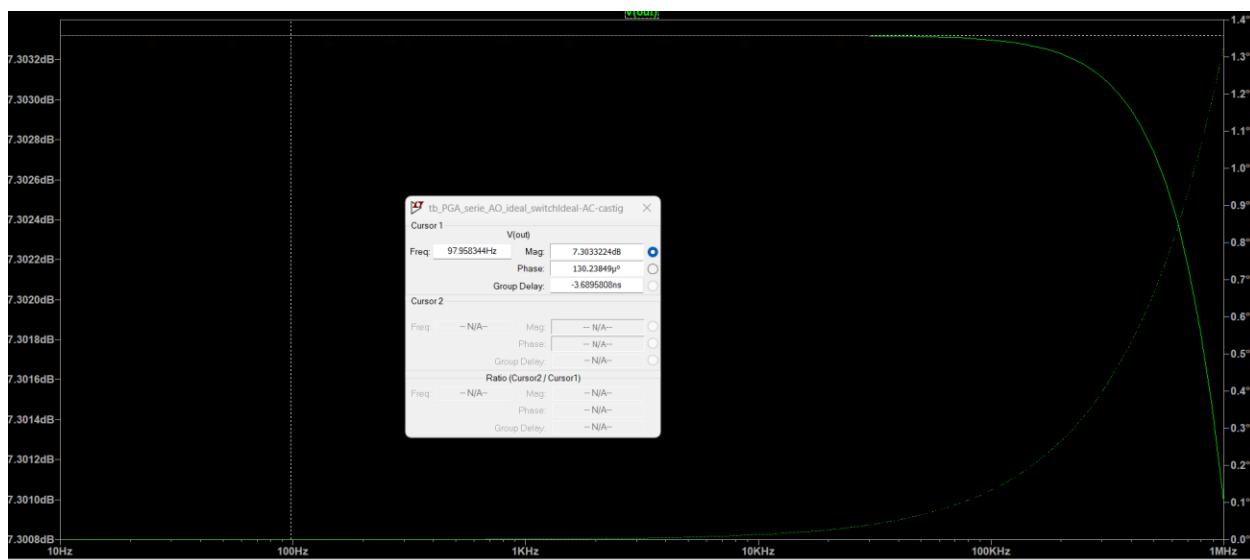
$$20 \log_{10}(1.69) = 4.57 \text{ dB}$$

$$20 \log_{10}(3.80) = 11.6 \text{ dB}$$

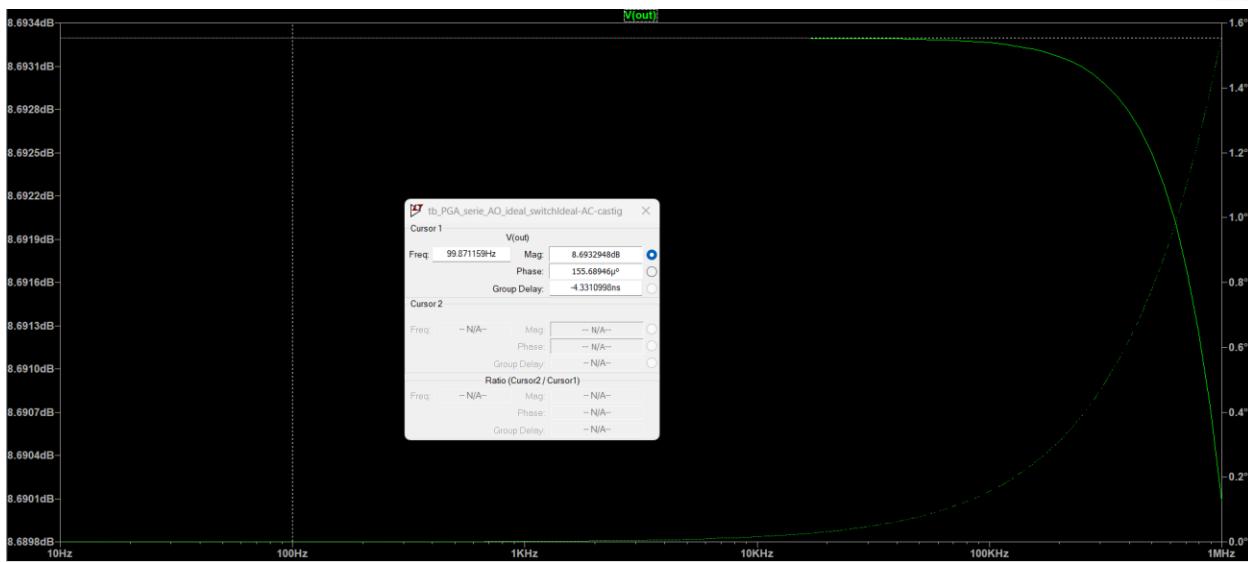
### AC Analysis(toate treptele de castig)



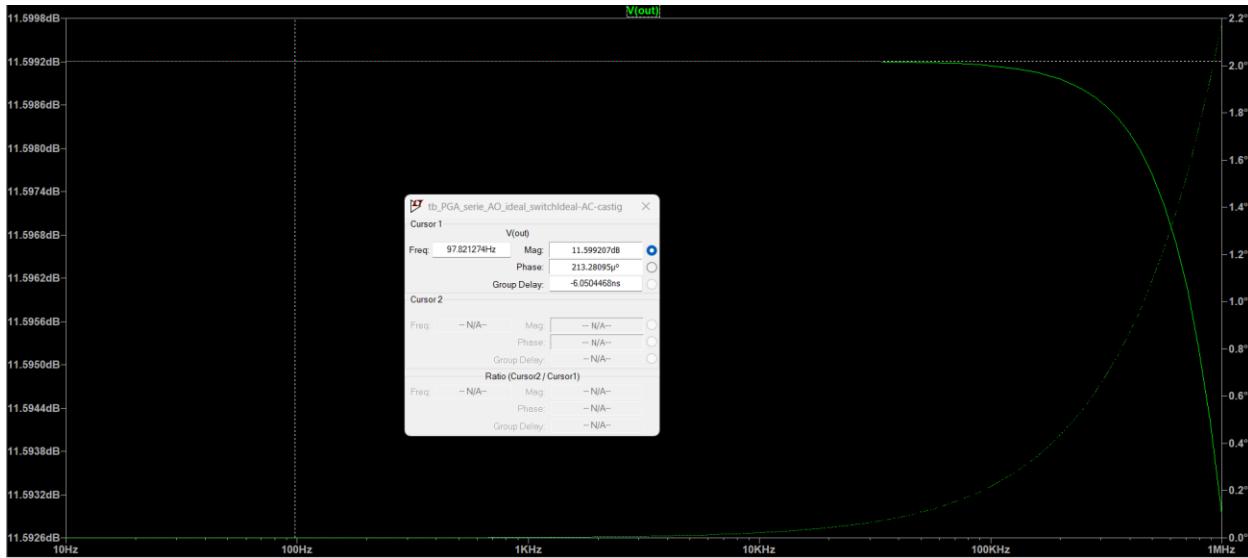
Gain=4.57db through S1



Gain=7.30db through S2



Gain=8.69dB through S3



Gain=11.59dB through S4

## Banda PGA>Banda filtru



freq 26.34MHz>3kHz



freq 36.92MHz>3kHz

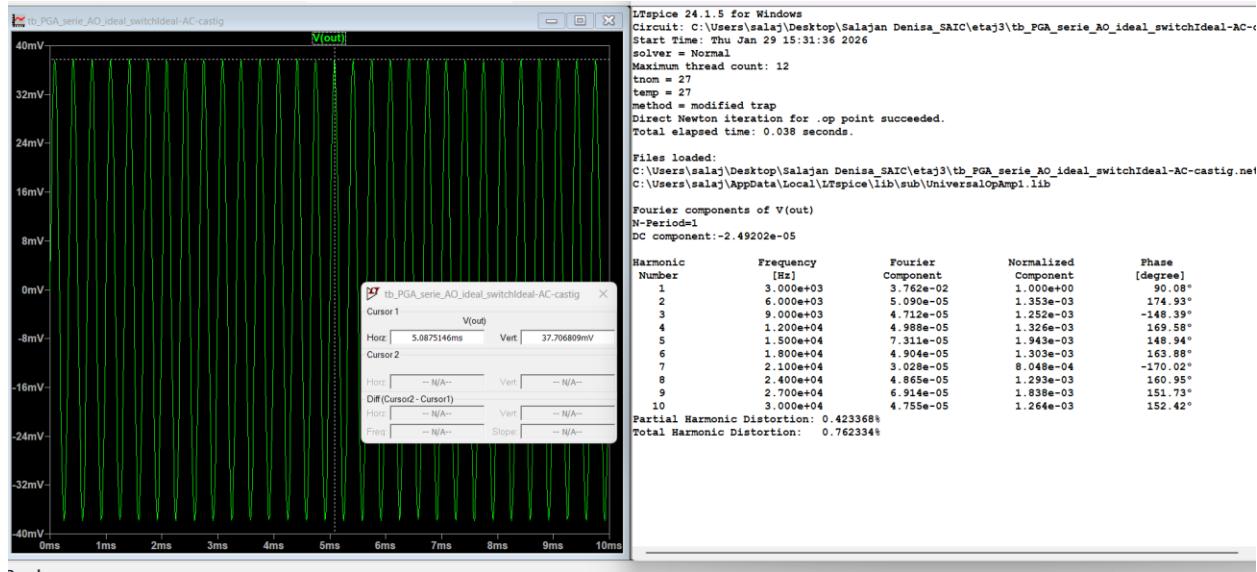


freq 43.44MHz>3kHz

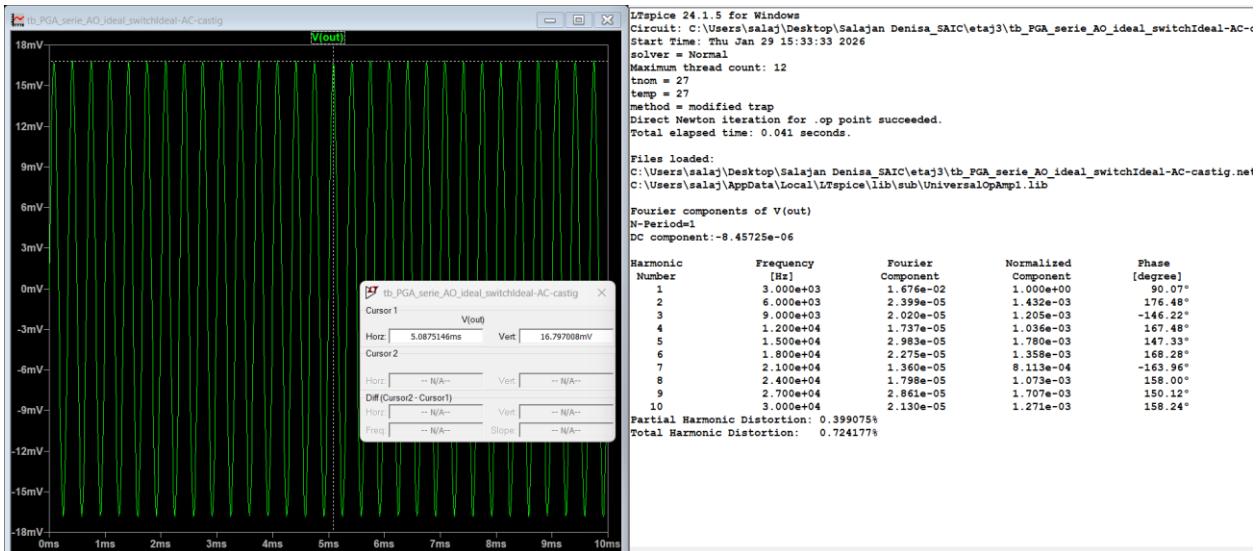


freq 58.91MHz>3kHz

### THD pt castig min cu amplitudine max



### THD pt castig max cu amplitudine min



## Fourth stage

DCOP

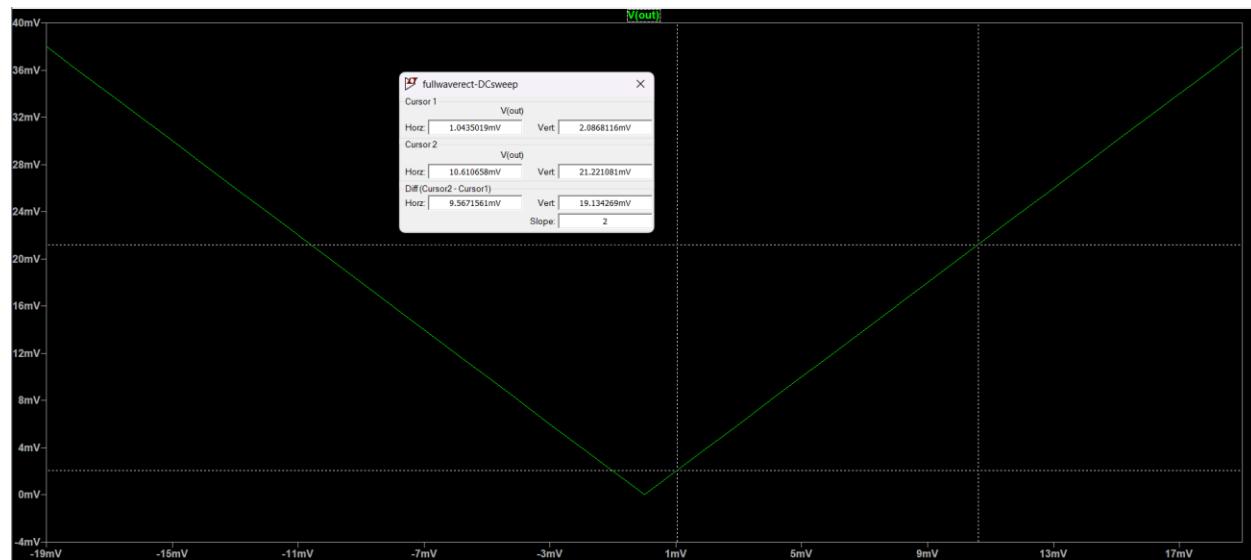
 C:\Users\salaj\Desktop\Salajan Denisa\_SAI\etaj4\fullwaverect-D

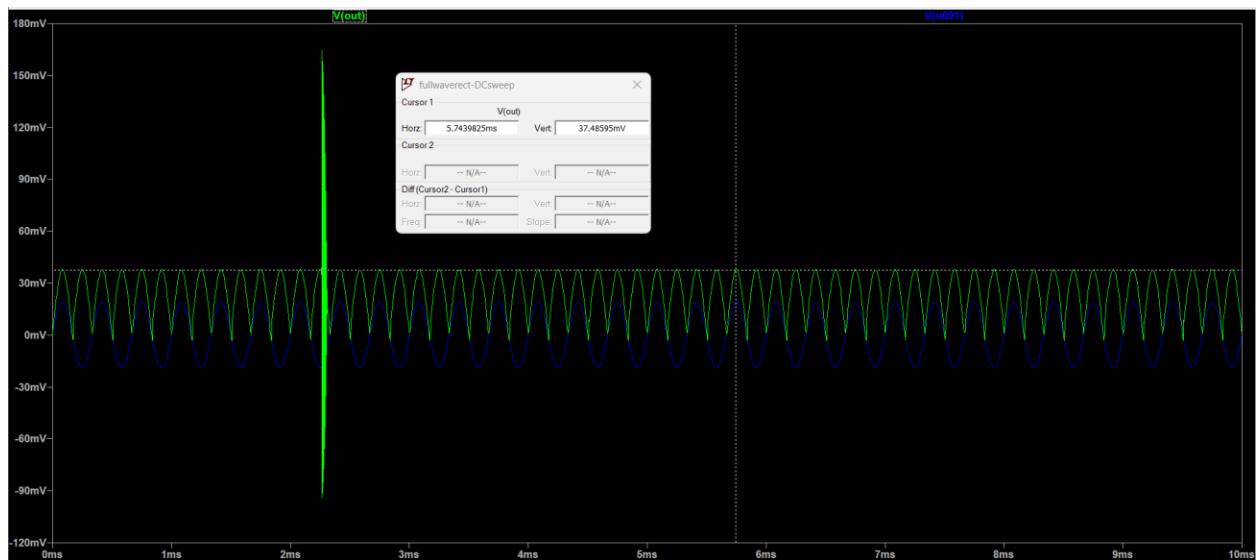
--- Operating Point ---

```

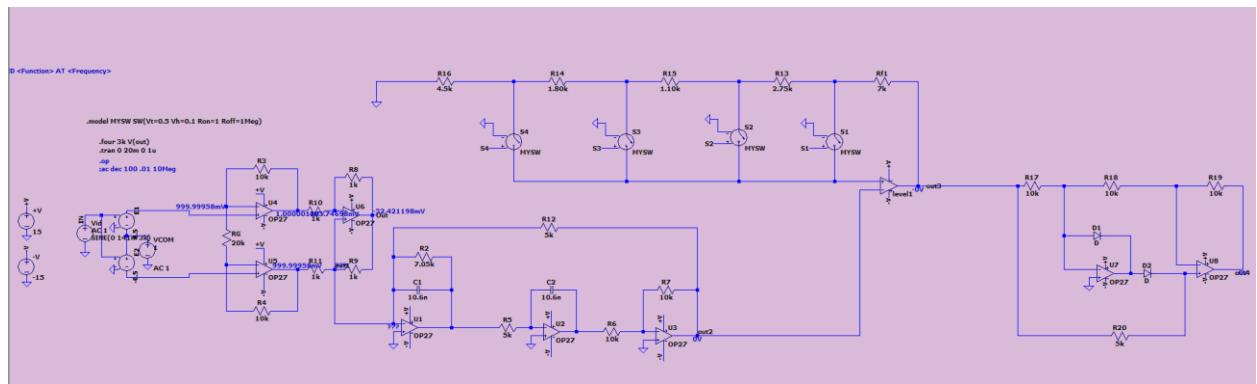
V(n004) :      -0.61349      voltage
V(vcc) :       15           voltage
V(vee) :      -15           voltage
V(out) :        2           voltage
V(n002) :   2.63842e-07   voltage
V(n005) :     0.999999    voltage
V(n003) :     0.999998    voltage
V(n001) :       1           voltage
I(R4) :    -1.68432e-10   device_current
I(D1) :      0.0002       device_current
I(R1) :     -0.0001       device_current
I(V2) :   -0.00589403   device_current
I(V3) :     0.00599403   device_current
I(R2) :    9.99998e-05   device_current
I(R3) :      0.0001       device_current
I(V1) :     -0.0001       device_current
I(D2) :   -1.62349e-12   device_current
Ix(u2:1) :   1.66809e-10  subckt_current
Ix(u2:2) :   1.66524e-10  subckt_current
Ix(u2:3) :   0.00302263  subckt_current
Ix(u2:4) :  -0.00292263  subckt_current
Ix(u2:5) :   -0.0001       subckt_current
Ix(u1:1) :  -4.39736e-14  subckt_current
Ix(u1:2) :  4.40176e-14   subckt_current
Ix(u1:3) :   0.0028714   subckt_current
Ix(u1:4) :  -0.0030714   subckt_current
Ix(u1:5) :   0.0002       subckt_current
  
```

DC Sweep +Transient





## 4. The Final Schematic and Functionality



## 5. Conclusion

Parameters:	Expected Value	Simulated Value
<b><i>First stage</i></b>		
Gain	0.002V/V	1.99mV
Bandwidth Freq.	>3kHz	3.215MHz
THD	<1%	0.12
<b><i>Second stage</i></b>		
Bandwidth	3k	4.22kHz
Castig in banda(H0)	5000	74dB=5000
THD	<1%	0.58%
<b><i>Third stage</i></b>		
Castig maxim	11dB	11.6dB
Castig minim	5dB	4.57dB
Banda castig minim	>3kHz	58.91MHz
Banda castig maxim	>3kHz	26.34MHz
THD castig min	<1%	0.72%
THD castig max	<1%	0.76%
<b><i>Fourth stage</i></b>		
Castig	2	2.06mV