紫紅底

數位邏輯設計實驗結報

- 實驗班別：□資工(星期三)
- 實驗名稱：(07) 4 位元 ripple 加法器
- 實驗日期：2022 年 05 月 04 日
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一、實驗目的

以 Verilog HDL 硬體描述語言，在 DE2-115 實驗平台上實作 4 位元加法器。

二、完整程式碼

```
1  module half_adder(output S, C, input x, y);
2      // instantiate primitive gates
3      xor (S, x, y);
4      and (C, x, y);
5  endmodule
6
7  module full_adder(output S, C, input x, y, z);
8      wire       S1, C1, C2; //Outputs of first XOR and two AND gates
9      half_adder HA1(S1, C1, x, y);
10     half_adder HA2(S, C2, S1, z);
11     or         g1(C,C2,C1);
12 endmodule
13
14 module test(output C4, input[3:0] A, B, input C0, output [6:0] seg);
15     wire       C1, C2, C3;
16     wire       [3:0]Sum;
17     full_adder FA0(Sum[0], C1, A[0], B[0], C0);
18     full_adder FA1(Sum[1], C2, A[1], B[1], C1);
19     full_adder FA2(Sum[2], C3, A[2], B[2], C2);
20     full_adder FA3(Sum[3], C4, A[3], B[3], C3);
21     segment7(Sum, seg);
22
23 endmodule
24
```

```
25  module segment7(input wire [3:0]bcd, output reg [6:0] seg);
26      always @(bcd)
27      begin
28          case (bcd) //case statement
29              4'b0000 : seg = 7'b1000000;
30              4'b0001 : seg = 7'b1111001;
31              4'b0010 : seg = 7'b0100100;
32              4'b0011 : seg = 7'b0110000;
33              4'b0100 : seg = 7'b0011001;
34              4'b0101 : seg = 7'b0010010;
35              4'b0110 : seg = 7'b0000010;
36              4'b0111 : seg = 7'b1111000;
37              4'b1000 : seg = 7'b0000000;
38              4'b1001 : seg = 7'b0010000;
39              4'b1010 : seg = 7'b0001000;
40              4'b1011 : seg = 7'b0000011;
41              4'b1100 : seg = 7'b1000110;
42              4'b1101 : seg = 7'b0100001;
43              4'b1110 : seg = 7'b0000110;
44              4'b1111 : seg = 7'b0001110;
45              //switch off 7 segment character when the bcd digit is not a decimal number.
46              default : seg = 7'b1110001;
47          endcase
48      end
49
50  endmodule
```

三、實驗結果