## 數位邏輯設計實驗結報

● 實驗班別:□資工(星期三)

● 實驗名稱:( 07 ) 4 位元 ripple 加法器

● 實驗日期: <u>2022</u> 年 <u>05</u> 月 <u>04</u> 日

● 組別編號: 20

● 成員名單:(學號) 410921202 (姓名) 林芷萱

410921203 林芯卉

## 一、實驗目的

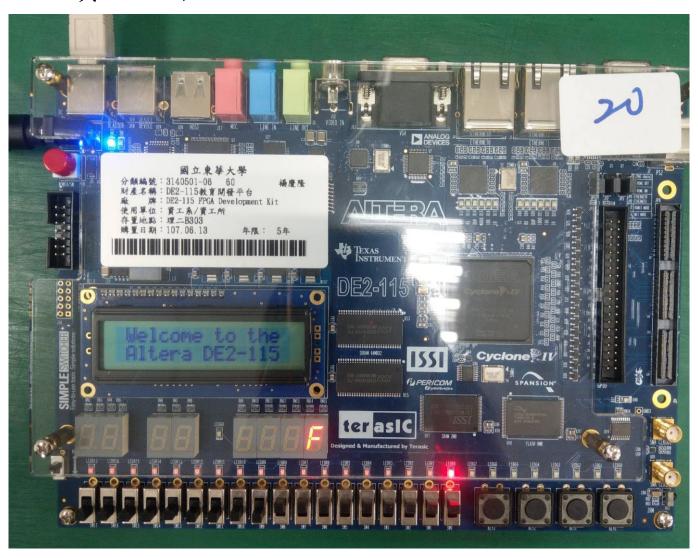
以Verilog HDL 硬體描述語言,在DE2-115實驗平台上實作4位元加法器。

## 二、完整程式碼

```
module half_adder(output S, C, input x, y);
         // instantiate primitive gates
 3
         xor(S, x, y);
         and (C, x, y);
 5
    endmodule
 6
    module full_adder(output S, C, input x, y, z);
 7
         wire S1, C1, C2; //Outputs of first XOR and two AND gates half_adder HA1(S1, C1, x, y);
 8
9
         half_adder HA2(S, C2, S1, z);
10
                    g1(C,C2,C1);
11
        or
    endmodule
12
13
    module test(output C4, input[3:0] A, B, input C0, output [6:0] seg);
14
15
         wire
                    C1, C2, C3;
                     [3:0]Sum;
16
         full_adder FA0(Sum[0], C1, A[0], B[0], C0);
17
         full_adder FA1(Sum[1], C2, A[1], B[1], C1);
18
         full_adder FA2(Sum[2], C3, A[2], B[2], C2);
19
20
         full_adder FA3(Sum[3], C4, A[3], B[3], C3);
21
         segment7(Sum, seg);
22
23
    endmodule
24
```

```
25
    module segment7(input wire [3:0]bcd, output reg [6:0] seg);
26
         always @(bcd)
27
         begin
28
             case (bcd) //case statement
29
                 4'b0000 : seg = 7'b1000000;
                 4'b0001 : seg = 7'b1111001;
30
                 4'b0010 : seg = 7'b0100100;
31
                 4'b0011 : seg = 7'b0110000;
32
                 4'b0100 : seg = 7'b0011001;
33
                 4'b0101 : seg = 7'b0010010;
34
                 4'b0110 : seg = 7'b0000010;
35
                 4'b0111 : seg = 7'b1111000;
36
37
                 4'b1000 : seg = 7'b00000000;
                 4'b1001 : seg = 7'b0010000;
38
                 4'b1010 : seg = 7'b0001000;
39
                 4'b1011 : seg = 7'b0000011;
40
                 4'b1100 : seg = 7'b1000110;
41
                 4'b1101 : seg = 7'b0100001;
42
                 4'b1110 : seg = 7'b0000110;
43
                 4'b1111 : seg = 7'b0001110;
44
45
                 //switch off 7 segment character when the bcd digit is not a decimal number.
46
                 default : seg = 7'b1110001;
47
             endcase
48
         end
49
50 endmodule
```

## 三、實驗結果



頁