SPUR CORRELATION IN AN ARRAY
OF DIRECT DIGITAL SYNTHESIZERS

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Abstract

Many applications, including communications, test and measurement, and radar, require the generation of signals with a high degree of spectral purity. One method for producing tunable, low-noise signals is to combine the outputs of multiple direct digital synthesizers (DDSs) arranged in a parallel configuration. In such an approach, if all noise is uncorrelated across channels, the noise power will decrease relative to the combined signal power, increasing the signal-to-noise ratio. However, if the noise or spurious components are correlated, the gains achieved by parallelization will be limited. This work examines the potential correlation of spurious components in an array of DDSs, with a focus on phase truncation spurs, quantization noise, and spurs from quantizer nonlinearities. We measured the levels of correlation among DDS channels on a custom 14-channel DDS testbed.

Our study shows that the phase truncation spurs are uncorrelated, at least in our system. We believe this decorrelation is due to the existence of a mechanism in our DDS array that is unaccounted for in our current DDS model. This mechanism, likely due to some timing element in the FPGA, randomizes the relative phases of the truncation spurs from channel to channel each time the DDS array is powered on. This randomness decorrelates the phase truncation spurs, providing the potential for spur-free dynamic range improvement from a DDS array.

Our measurements also show that the quantization noise of each DDS channel is uncorrelated for 3-bit or higher digital-to-analog converters (DAC). This suggests that for an N-channel array of DDSs, a near N gain in signal-to-quantization noise is possible. This gain will be most apparent for low-bit DACs in which quantization noise is notably higher than the thermal noise contribution.

Lastly, our measurements of quantizer nonlinearity spurs demonstrate that the second and third harmonics are highly correlated across channels for all frequencies tested, suggesting that there is no benefit to using an array of DDSs for implementations in which in-band quantizer nonlinearities dominate. As a result, alternate methods of harmonic spur management must be employed to mitigate these errors.

INTRODUCTION

The direct digital synthesizer (DDS) is a commonly used device in modern radio frequency (RF) applications. A DDS offers the fastest frequency jumping and the finest frequency tuning resolution of any technology available today in a digitally controlled environment. As a result, DDSs have found wide application in fields including communications and test and measurement equipment; however, the DDS topology generates errors that limit its performance. These errors include random noise and periodic deterministic errors that manifest themselves as spurs in the frequency domain. As has been the tendency in digital design, we seek to improve the performance of a single DDS by placing multiple DDSs in parallel in order to take advantage of the decorrelation of noise across units and achieve improved signal purity in the combined output.

Previously we showed that, excluding common noise due to the clock, DDS phase noise can be improved by combining outputs from parallel DDSs **[1]**. In this work, we examine the impact of DDS parallelization on the output signal's spurious content, focusing on phase truncation spurs, quantization noise, and quantizer nonlinearity harmonics. We utilized a custom 14-channel DDS testbed to experimentally determine the level of spur correlation among DDS channels for each of these spur types. Results suggest that, for our system, parallelization leads to gains in spur-free dynamic range (SFDR) and signal-to-quantization noise ratio (SQNR) when the dominant spurs arise from phase truncation or quantization noise, but does not improve SFDR limited by digital-to-analog converter (DAC) quantizer nonlinearities. These measurements can serve as a guide to both the advantages and limitations of using parallel DDSs in a real system application.

A conventional DDS consists of five primary elements: a driving clock; a phase accumulator (PA); a phase-to-amplitude converter, often implemented through a look-up table (LUT); a DAC; and a reconstruction filter **[2-4]**. At each clock cycle, the PA, which is effectively a counter, is incremented by the frequency control word (FCW), k, updating the signal phase. The phase stored by the PA is converted to the corresponding sine-wave amplitude by the LUT and then passed to the DAC, which converts it to an analog output. This output is then smoothed by passing it through a reconstruction filter. As the phase is increased by k each subsequent clock cycle, the amplitude output steps through the sine LUT, generating the desired analog sinusoidal signal. The amplitude of this generated signal is set by digitally scaling the input to the DAC or by placing a physical attenuator at the output. The signal frequency is tuned by varying k: a larger k results in the PA moving through the period of the LUT more quickly, producing a higher-frequency sinusoid at the output. The maximum DDS output frequency is determined by its source clock, limited by Nyquist constraints to one half of the clock frequency. It can be further limited by the cutoff frequency of the lowpass reconstruction filter at the output.

Figure 1 shows the functional block diagram of the specific DDSs used in these experiments **[5]**. This design implements the PA and the LUT within a Xilinx Virtex 4 FPGA, with a single FPGA controlling two DDS channels. In our implementation, both the FCW and the PA are $M = 32$ bits long. Each LUT has 2^{15} entries, but utilizes the symmetry of the sine function to create effectively 2^{17} entries; each entry is a 14-bit word containing a sinusoid amplitude. Because of the experimental nature of our work, our implementation includes a bit mask at the input of the LUT to allow the user to vary the number of bits extracted from the PA (W), from $W=1$ to $W=17$, effectively varying the LUT size**[6]**.
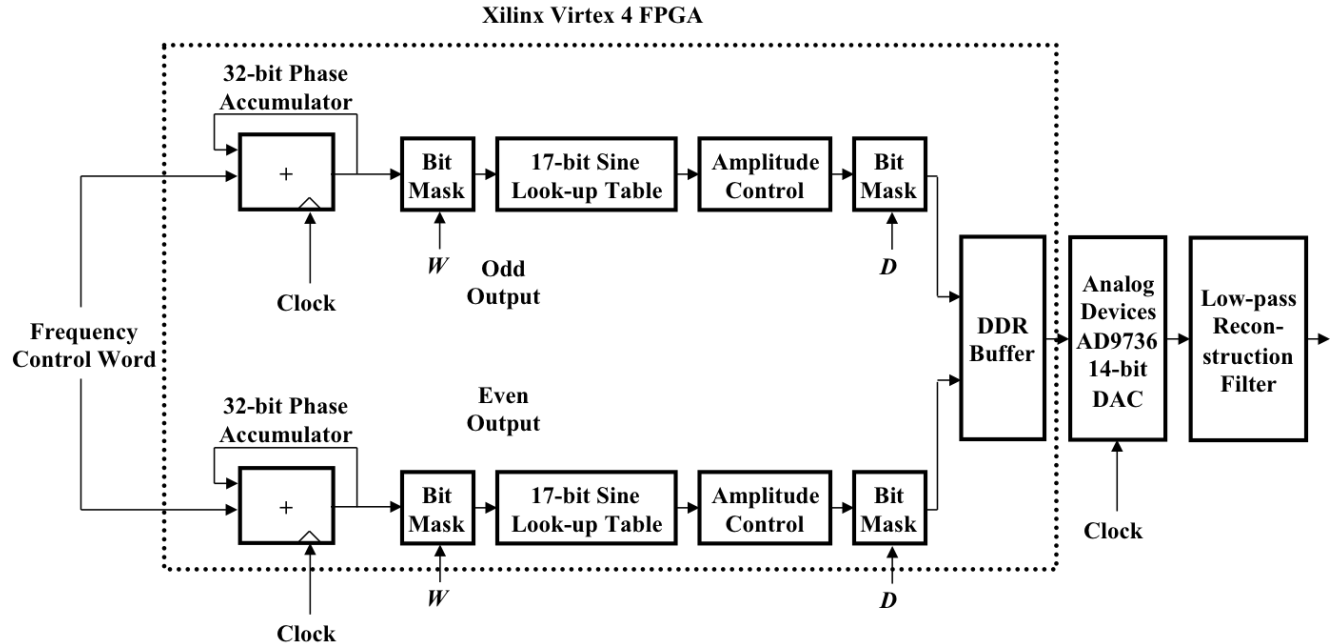
Figure 1. Functional block diagram of the DDSs used in this work. Note the dual PA/LUT structure and the bit masks prior to the LUT and the DDR Buffer.

In the standard DDS topology, the output of the LUT is directly connected to a DAC. In our DDS implementation, because the FPGA runs at half the rate of the source clock, there are two sets of PAs and LUTs whose outputs, even and odd, are alternated by a double-data-rate (DDR) buffer before being sent to the DAC. Digital-to-analog conversion is performed by a 14-bit Analog Devices 9736 DAC with a bit mask at the input that allows the user to adjust D, the number of bits fed to the DAC, from 1 to 14 by truncating the LSBs of the LUT output. This allows us to emulate the effect of varying the number of bits in the DAC.

The source clock used in our DDS system was based on a 100 MHz ultra-low-phase-noise, oven-controlled crystal oscillator that was frequency-multiplied to 800 MHz. The 800 MHz clock drives the DAC directly, while the FPGA is clocked at 400 MHz, half of the DAC rate. Our DDS systems also have 7th-order Chebyshev reconstruction filters, which limit the maximum output frequency of each DDS to 360 MHz.

Because of characteristics inherent to its architecture, a DDS does not generate perfect sinusoids and its output frequency spectrum commonly includes spurious signals arising from phase truncation, quantization noise, and quantizer nonlinearities.

The mechanisms generating all three of these error types are deterministic; assuming that each DDS in an array is architecturally identical and has the same phase sequence, the errors occur in an identical manner and should produce identical spurs in each channel. Therefore, spurs across channels should sum coherently at the output resulting in no net reduction in spur magnitude due to DDS parallelization. The following sections examine each of these error types individually and their level of correlation in our DDS array. A more detailed introduction to each error type is provided, as well as the results from our testbed measurements.

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PHASE TRUNCATION SPURS

THEORETICAL ANALYSIS OF PHASE TRUNCATION SPURS

In practical DDS designs, the LUT is implemented using a finite-sized, read-only memory (ROM) with limited output precision. Often several of the LSBs of the PA are truncated to create waveforms with fractional frequency while preventing the size of the LUT from becoming unwieldy. For example, our DDS architecture has a 32-bit PA. Connecting this to an equally-sized LUT would require a ROM with 2^{32} entries, with each entry 14 bits in length so as to use the entire dynamic range of the DAC. The resulting ROM would be 7 gigabytes in size, which is prohibitively expensive for most systems. Truncating the 15 LSBs of the PA reduces the required memory by a factor of 2^{15} to 224 kilobytes, a much more reasonable and affordable size. Although this phase truncation is necessary for practical reasons, for some FCW values it creates a periodic error, as shown in Figure 2, that manifests itself as spurs in the frequency domain [7].
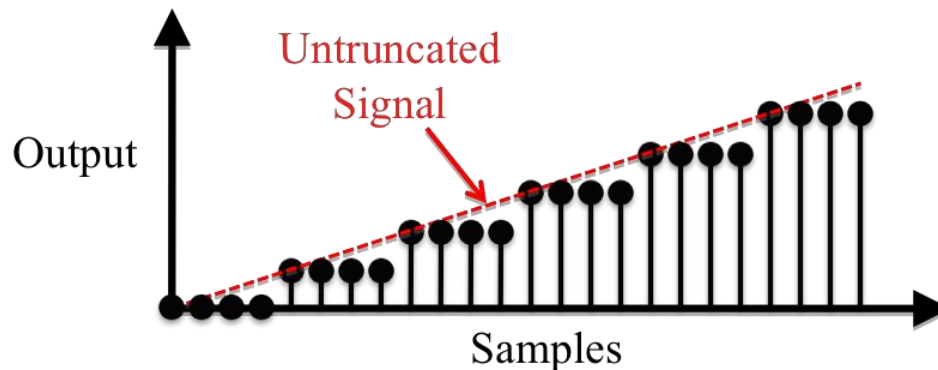

Figure 2. Example of the output of the LUT for a phase-truncated signal.

Consider a DDS with a *W*-bit LUT and an *M*-bit FCW having value *k* as shown in Figure 3. We define the number of active bits, *R*, to be the number of FCW bits, M, minus the number of trailing zeros in the FCW. Note that an *M*-bit FCW whose *M - R* LSBs are zeros is effectively the same as an *R*-bit FCW [8]. *k* and the number of truncated bits, *R - W*, determine the characteristics of the phase truncation spurs.

From the analyses given in [8,9], we can establish several baseline facts regarding phase truncation spurs. Firstly, the worst-case (i.e., largest) spur magnitude occurs when $R-W=1$, which means that the *R*-th MSB in *k* is one (i.e., *k* = XXXX.1) and there is only a single phase truncation spur in the signal spectrum. The magnitude of this spur is given by

$$20\log_{10}\left(\frac{\pi}{2^{(W+1)}}\right) \qquad (1)$$

measured in decibels relative to the carrier (dBc) [10]. Secondly, the magnitude of the worst-case phase truncation spur decreases by 6 dB for each bit of increase in the size of *W*. Lastly, the frequency, magnitude, and phase of these spurs are entirely deterministic; therefore, we expect phase truncation spurs to be correlated across channels, summing coherently and leading to no net gain in SFDR due to parallelization.
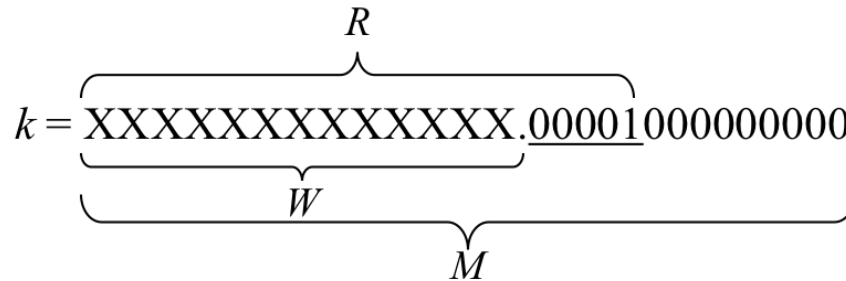
$$k = \underbrace{\underbrace{XXXXXXXXXXXXXX}_{W}.\underline{00001}000000000}_{M}$$

with R bracing above and M bracing below.

Figure 3. Example FCW in which M is the number of bits in the PA; R is the number of active bits, equal to M minus the number of trailing zeroes; W is the number of bits in the LUT; and $R-W$ is the number of truncated bits. The bits after the period are truncated and the underlined bits are the active truncated bits.

EXPERIMENTAL MEASUREMENT OF PHASE TRUNCATION SPURS

To assess the level of phase truncation spur correlation in DDS arrays, we commanded our DDSs to output the same signal and measured the magnitude and phase of the resultant phase truncation spurs. The LUT size, W, was effectively varied via the bit mask prior to the LUT, and the FCWs were chosen to yield the worst-case phase truncation spur for each LUT size. To quantify the correlation, we measured the phase difference between the fundamental signal and the largest phase truncation spur, which occurs at the same frequency on each channel. When a DDS array is used in the field, the phases of the output signals are aligned in some consistent manner, so the statistics of the phase difference give us direct insight into the level of spur correlation, as well as the potential for SFDR gain. Perfectly correlated spurs will have the same phase difference and offer no SFDR gain in the combined output, while fully decorrelated spurs will have truly random phases and yield a SFDR gain of $10\log_{10}(N)$ dB, where N is the number of DDSs in the array.

In order to measure the output of the signal generators, each DDS was connected to a 16-bit Linear Technology LTC2208 analog-to-digital converter (ADC) with nominally identical cables, as shown in Figure 4. The ADCs sampled at 120 MHz and the output signal powers of the DDSs were kept below the ADCs' full-scale input range to minimize any nonlinear ADC distortion [6].

We measured the phase difference between fundamental and spur by capturing the outputs of 14 DDSs ten times for several different values of k. For each capture, we reinitialized the value of the PAs of all DDSs to zero using a common trigger. Table 1 show the W and k values used. For each value of W, we chose the value of k that produced the worst-case spur by setting $R-W=1$. Also plotted in Table 1 are the fundamental frequencies, phase truncation spur frequencies, and SFDR for the single and combined channels. The combined SFDR was calculated from the sum of all of the single channels after they were aligned digitally. As shown, there is an increase in the combined channel SFDR over the single channel. This suggests that the phase truncation spurs are not fully correlated among the channels.
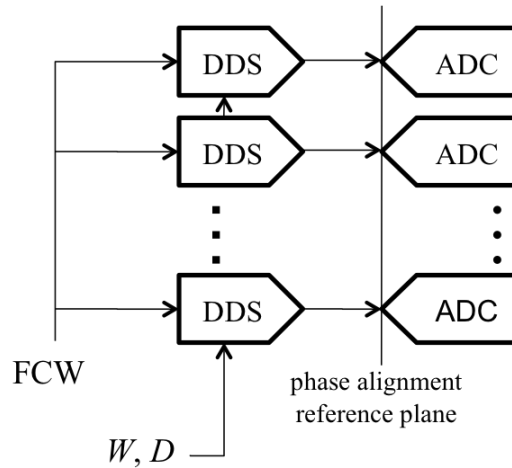
Figure 4. Each DDS was connected to an ADC. *W* was varied for the phase truncation spurs experiments and *D* was varied for the quantization noise power experiments. In the quantization noise power experiments, the DDSs were phase aligned at the inputs to the ADCs to within 170 μrad.

Table 1. *W* and *k* values measured along with their corresponding fundamental and phase truncation spur frequencies in MHz. Truncated bits of *k* are shown to the right of the decimal point. Also included are the SFDRs for a single channel and all of channels combined.

W	*k*	Fundamental Frequency (MHz)	Spur Frequency (MHz)	Single Channel SFDR (dBc)	Combined Channel SFDR (dBc)
4	0011.1	87.5	112.5	22.02	24.71
6	001100.1	78.125	118.125	33.84	49.16
8	00110000.1	75.78125	115.78125	46.09	53.99
10	0011000000.1	75.1953125	115.1953125	58.33	68.45

Figure 5 shows a histogram plotting the measured phase difference of the worst case spur for all ten runs for each of the 14 channels in 10°-wide bins. As shown, the phase differences for subsequent runs cluster heavily together for each channel, indicating that after retriggering the phase remains consistent. This is most apparent in the *W*=6 and *W*=8 cases, where all ten runs for each channel have a different spur phase relative to the fundamental. In the *W*=4 case, the truncation spur phase is offset by 180 degrees for 3 runs, which we believe to be an artifact arising from the dual PA architecture. For the *W*=10 case, the phase truncation spur power drops to a level comparable to the thermal noise power, degrading the phase measurement and causing some spreading in the phase difference. Most importantly, however, though the phase difference is constant across runs for a given channel in each case, the relative phases of the 14 channels vary widely, suggesting truncation spur power can be reduced through parallelization, as reported in Table 1.
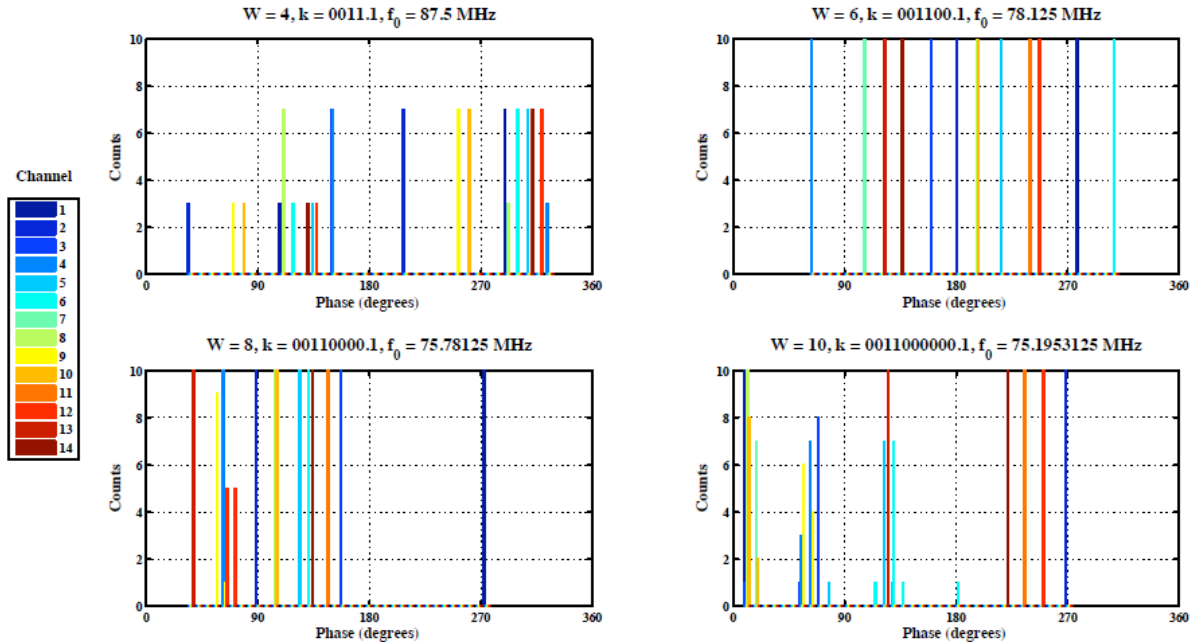
Figure 5. Plot of the truncation spur phase difference for 10 captures on each of 14 DDS channels for four different fundamental output frequencies, as determined by the FCW, k (see Table 1).

In these measurements, subsequent data runs were captured without power cycling the DDSs. We took an additional set of measurements in which the DDSs were powered-down between each run. Figure 6 shows a histogram of these results, plotting the measured phase differences of the phase truncation spur for 32 captures on each of the 14 DDS channels, with $W=4$ and $k=0011$. The W and k values were selected to yield maximum spur-to-noise ratio to facilitate phase measurement. As is shown, after power reset, the phase difference of the truncation spur is random, even within a given channel, with a near equal distribution for all possible phases.

These results suggest that the primary determinant of phase truncation spur phase difference is some parameter that is established upon FPGA initialization, causing the phase difference of the truncation spurs to vary from channel-to-channel. Our current model does not account for this parameter, but the measurements presented in Figure 6 suggest that it is likely a uniformly distributed random variable. It is possible that other DDS arrays which implement their PAs, LUTs, and buffers in a different way, for instance, with an application-specific integrated circuit (ASIC), might not have the same randomness; however, at least in DDS architectures similar to ours, our measurements indicate that the phase truncation spurs are naturally decorrelated and that an increase in SFDR for truncation spurs can be achieved. Future work might be able to identify the mechanism that determines the truncation spur phase and potentially use it to purposely decorrelate these spurs to maximize SFDR gain.
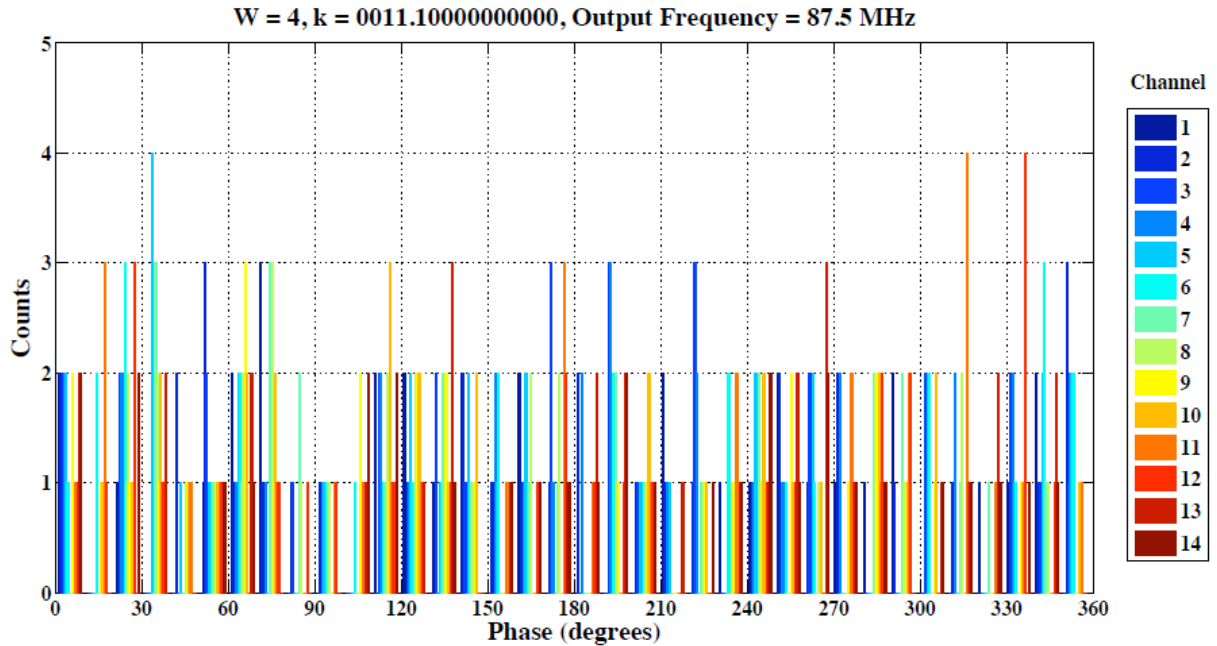
Figure 6. Plot of the truncation spur phase difference for 32 captures on 14 DDS channels for a fundamental output frequency of 87.5 MHz.

QUANTIZATION NOISE SPURS

THEORETICAL ANALYSIS OF QUANTIZATION NOISE SPURS

The analog output of a DAC is quantized and, as a result, its spectrum is composed of a fundamental tone at the desired output frequency, as well as harmonics arising from the signal distortion [11]. These harmonics alias with respect to the DDS's source clock and appear as a very large number of spurs, the collection of which is referred to as quantization noise. The ratio of the signal power to the quantization noise power (SQNR) is given in dB by [12]:

$$ \text{SQNR} = 1.76 + 6.02D + 20 \log (\text{FFS}) \tag{2} $$

where D is the number of DAC bits and FFS is the fraction of full scale power at which the DAC operates. When the DAC is operating at full-scale, the last term becomes zero and does not contribute. As shown in (2) and Figure 7, SQNR decreases by approximately 6 dB with each increasing bit of DAC resolution. Theoretically, the quantization noise for each DAC should be perfectly correlated, since the outputs of the aligned channels should have the same amplitude and suffer the same quantization error; however, any calibration error or spectral differences across channels, such as phase truncation errors, may partially decorrelate the quantization noise. This partial decorrelation would allow for some SQNR gain from combining multiple DDS channels in an array.

We assess the level of quantization noise correlation by comparing the actual quantization noise power of the summed output to the theoretical quantization noise powers for fully correlated and fully uncorrelated cases, as summarized schematically in Figure 7. The theoretical correlated quantization noise power, shown by the blue line, is the total summed power, assuming each channel's individual power adds coherently:

$$P_{N,correlated} = \left(\sqrt{P_1} + \cdots + \sqrt{P_N}\right)^2 \tag{3}$$

where P_1, P_2, ..., P_N are the quantization noise powers of each individual channel in both cases. The theoretical uncorrelated power, shown by the green line, is the total summed power, assuming each channel's individual power adds incoherently:

$$P_{N,uncorrelated} = (P_1 + \cdots + P_N). \tag{4}$$

The actual measured power, shown by the red line, is found by squaring the sum of the noise voltages of the individual channels and is bounded by the fully correlated and fully decorrelated limits. The more decorrelated the quantization noise is across channels, the closer the actual power will be to the fully decorrelated value.
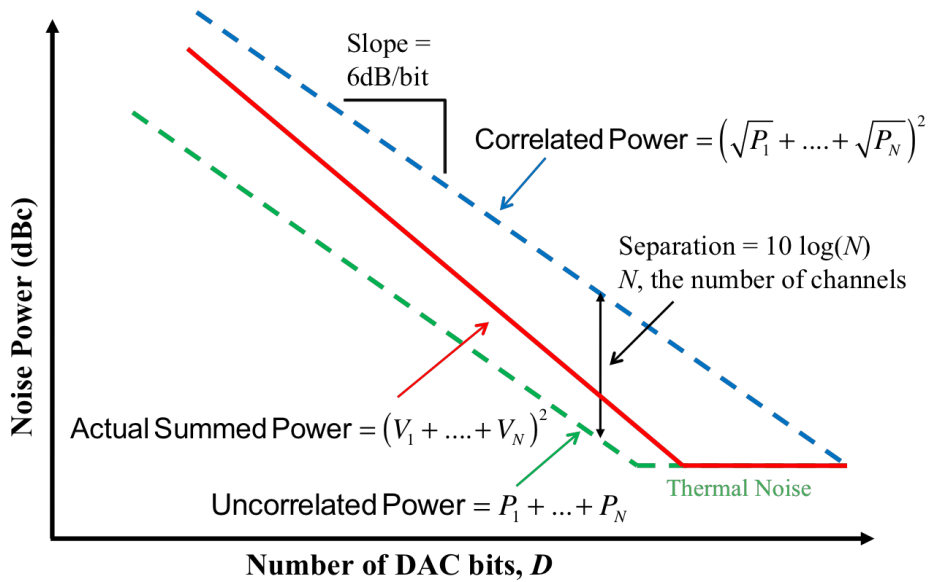

Figure 7. Schematic example noise power correlation plot. The blue line shows the theoretical correlated power, the green line shows the theoretical uncorrelated power, and the red line shows the actual measured power.

EXPERIMENTAL ANALYSIS OF QUANTIZATION NOISE SPURS

In order to assess the correlation of quantization noise spurs across DDS channels, we first needed to phase-align the channels to achieve maximum signal gain from the array. We would have preferred to phase-align the system by reinitializing the DDSs using only the trigger, but our trigger had a rise time of 3 ns, which was significantly longer than our 1.25 ns clock period, resulting in unreliable timing. Instead, we captured a single-tone calibration signal using the ADCs and determined the phase difference of each channel relative to the first channel. We then incremented the PA of each DDS to align channel phases. This calibration approach achieves excellent phase alignment, with signals generally matched to within 170 μrad at the ADC inputs [6].

Measurements of single-channel quantization noise power for all 14 channels were taken for varying DAC resolutions, with *D* ranging from 2 to 13 bits, by adjusting the bit mask prior to the DDR buffer. The DDSs were operated at full-scale with no amplitude attenuation so as to utilize the entire dynamic range of the DAC. Each DDS's full-scale power was measured and verified to be within 1 dB of each other. The output frequencies of the DDSs were chosen to be in the second Nyquist zone of the ADCs (60 MHz to 120 MHz). The exact experimental frequency (and the corresponding FCW) was chosen to fall in the center of an output fast Fourier transform (FFT) bin for computational ease. Each data capture was 2^{17} points long, covering at least 70000 periods of the DDS-generated sine-wave. Each output stream's variance was digitally normalized to further equalize the fundamental signal powers. After capturing the data for each individual channel, we calculated the quantization noise power of each set by squaring the FFT of the digital output. We weighted the signal with a flat-top window and compensated for the window loss in order to improve our amplitude accuracy. The flat-top window was an appropriate choice because the noise spectrum was composed of a large number of tones, not white noise **[13]**. We next zeroed out the bin with the largest signal and the 15 surrounding bins on each side to remove the fundamental signal power. We summed the linear (not decibel) values of the remaining bins to find the total noise power in each channel. We then calculated the correlated and uncorrelated powers from (3) and (4). To find the actual measured power, we summed the digital voltage outputs from all of the ADCs and calculated the quantization noise power as we did for the individual channels. Our approach requires that quantization noise be the dominant noise source. We minimized the phase truncation spurs by using an LUT with *W*=17, the maximum size allowed. Also, when the value of *D* is set below 10, theory predicts quantization noise spurs to be much higher than quantizer nonlinearity spurs.

Figure 8 shows the results of these quantization noise power measurements at four different output frequencies. The 6 dB decrease per additional DAC resolution bit seen for lower values of *D* – which matches theory – supports our assumption that quantization noise dominates other sources of noise. For DAC resolutions above 10 bits, our results were inconclusive because this assumption was no longer valid. However, our analysis shows that the measured quantization noise power is fairly decorrelated among DDS channels for all of the lower DAC resolutions. These trends were independent of DDS output frequency. The measured and calculated uncorrelated powers never quite overlap after reaching the thermal noise limit, which we attribute to a small level of correlation in the ADC noise power between channels and not to any correlation across the DDSs **[14]**.

It is unclear why the quantization noise power is uncorrelated, but we note that the relative phases of the quantization noise spurs determine the extent of noise power correlation. It is possible that small variations among the channels could serve to modify the phase of the quantization noise spurs, as was observed for the phase truncation spurs. Nevertheless, the results suggest that a large array of low-bit DACs that are amplitude and phase-aligned could yield high SQNR without a huge penalty from correlated quantization noise.
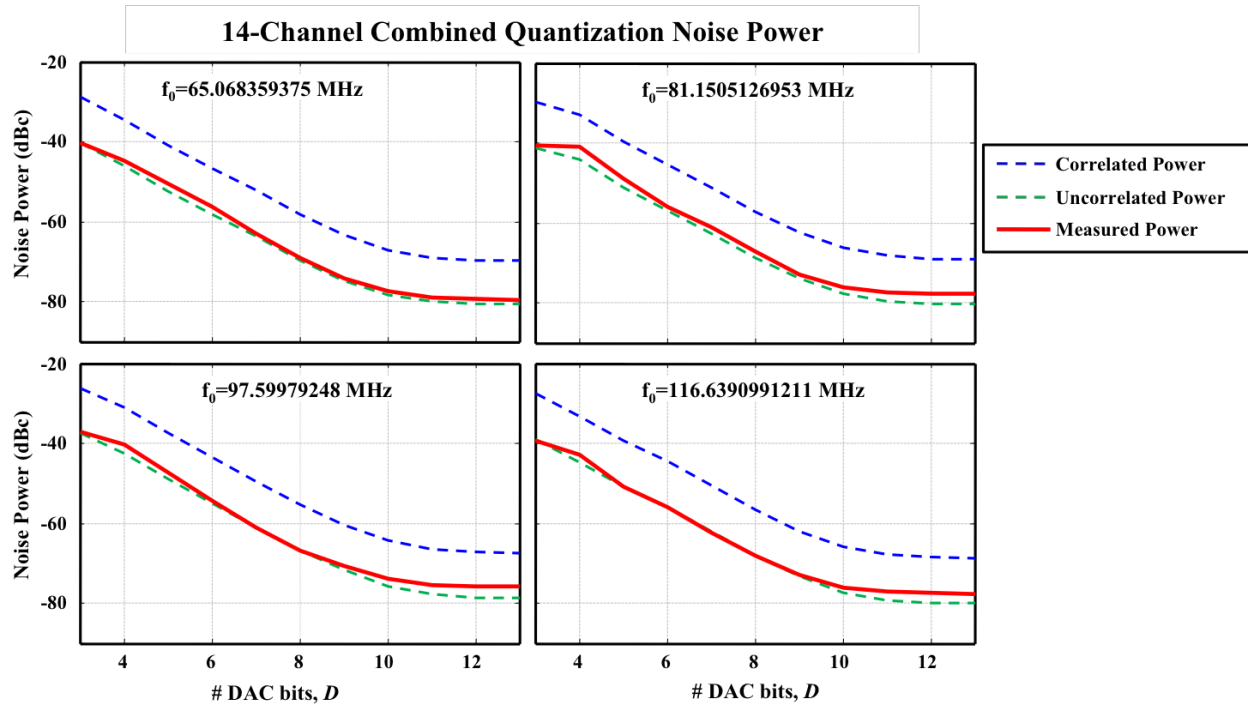
14-Channel Combined Quantization Noise Power

Figure 8. Quantization noise power results for four different fundamental frequencies.

QUANTIZER NONLINEARITY SPURS

THEORETICAL ANALYSIS OF QUANTIZATION NONLINEARITY SPURS

Every DAC possesses a transfer function that converts an input digital code to an output analog signal. In an ideal DAC, this transfer function maps the digital codes to evenly spaced (i.e., linear) slices of the device's full-scale range. However, in real DACs, design and fabrication imperfections result in an actual voltage output that differs from the ideal output level. These errors, termed quantizer nonlinearities, result in spectral content at multiples of the fundamental output signal frequency. Harmonics whose frequencies are higher than half of the DDS clock frequency will alias back into the first Nyquist zone [12]. While the frequency of quantizer nonlinearity spurs is deterministic, their amplitudes are not readily predictable and may depend on the particular imperfections of each DAC or the specific DAC architecture being used. Since these spurs are harmonics of the fundamental, the phases of the second and third harmonics should be twice and thrice the phase of the fundamental, respectively, and so on for higher order harmonics. Therefore, when the fundamental phases are aligned within a small phase error, we expect the lower harmonics to be aligned within a small phase error and, thus, to be correlated, resulting in no improvement in SFDR of low-order quantizer nonlinearity spurs in a parallel DDS array. As the harmonic number increases, the phase error becomes less negligible, potentially resulting in a decorrelation of the higher order spurs among the channels.

EXPERIMENTAL ANALYSIS OF QUANTIZATION NONLINEARITY SPURS

In order to assess the level and correlation of quantization nonlinearity spurs in our system, we set the bitmasks such that D=14 and W=17. Doing so reduces the phase truncation spurs and the quantization noise spurs, as suggested by (1) and (2), and ensures that both types of spurs are negligible compared to

the quantizer nonlinearity spurs. As the harmonics from ADC nonlinearities can overlap with the DAC harmonics in the frequency ranges of interest, we instead used an Agilent E4440A spectrum analyzer to measure the DDS outputs as shown in Figure 9. The spectrum analyzer also generates spurs at the harmonics of the input signal, but the attenuation of the spectrum analyzer can be adjusted to ensure that the magnitude of these internally generated spurs are reduced to the level of the noise floor.
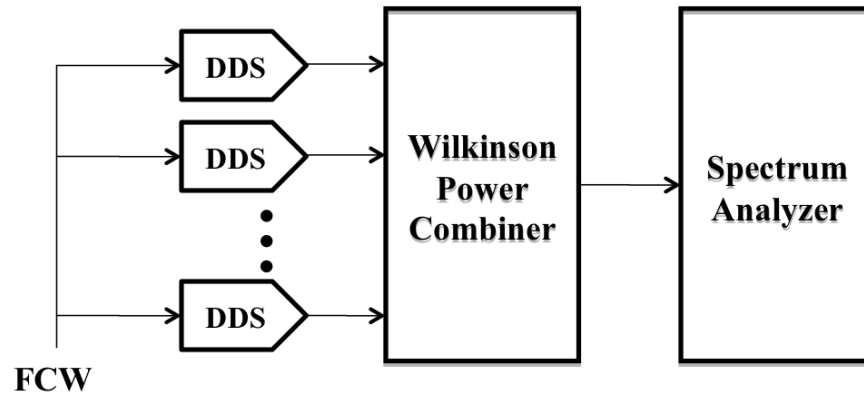

Figure 9. The quantizer nonlinearity spur powers of each DDS were measured individually and then eight DDSs were combined and aligned so the quantizer nonlinearity spurs of the array output could be measured.

The output of each channel was measured individually in order to calculate the theoretical correlated and uncorrelated powers of the spurious components. For each measurement, the powers of the fundamental signal and its harmonics were measured using the flat-top window setting. In order to assess the power of the combined output, the individual DDS outputs were summed using an eight-way Wilkinson power combiner, the largest we had available. To align the channels, we implemented an analog DDS phase calibration technique in which one channel was selected as a reference. Each subsequent channel was then compared against the reference and its phase accumulator incremented to achieve maximum destructive interference between the two channels. After maximum destructive interference was reached, 180 degrees were added to the second channel's phase accumulator to place the two channels in-phase; we then verified the expected gain in power over the single channel's power, $20\log_{10}(2)=6$ dB. After following the procedure for all eight channels, we combined all eight DDSs and verified the expected $20\log_{10}(8)=18$ dB gain in power over the single channel's power. With this alignment complete, we measured the power of the fundamental and harmonics of the combined signal as described above, adjusting for the insertion loss of the power combiner. Measured results for a fundamental output frequency of 20.5 MHz are plotted in Figure 10. The plot shows the theoretical correlated and uncorrelated powers, along with the actual measured power from the combiner, for each harmonic. As is shown, there is strong correlation for the second, third, and fourth harmonics, while we observe more erratic behavior for harmonics greater than the sixth. This erratic behavior is likely because the magnitudes of the higher harmonics are smaller and, thus, more sensitive to noise. These results were consistent for measurements taken at varying fundamental frequencies.
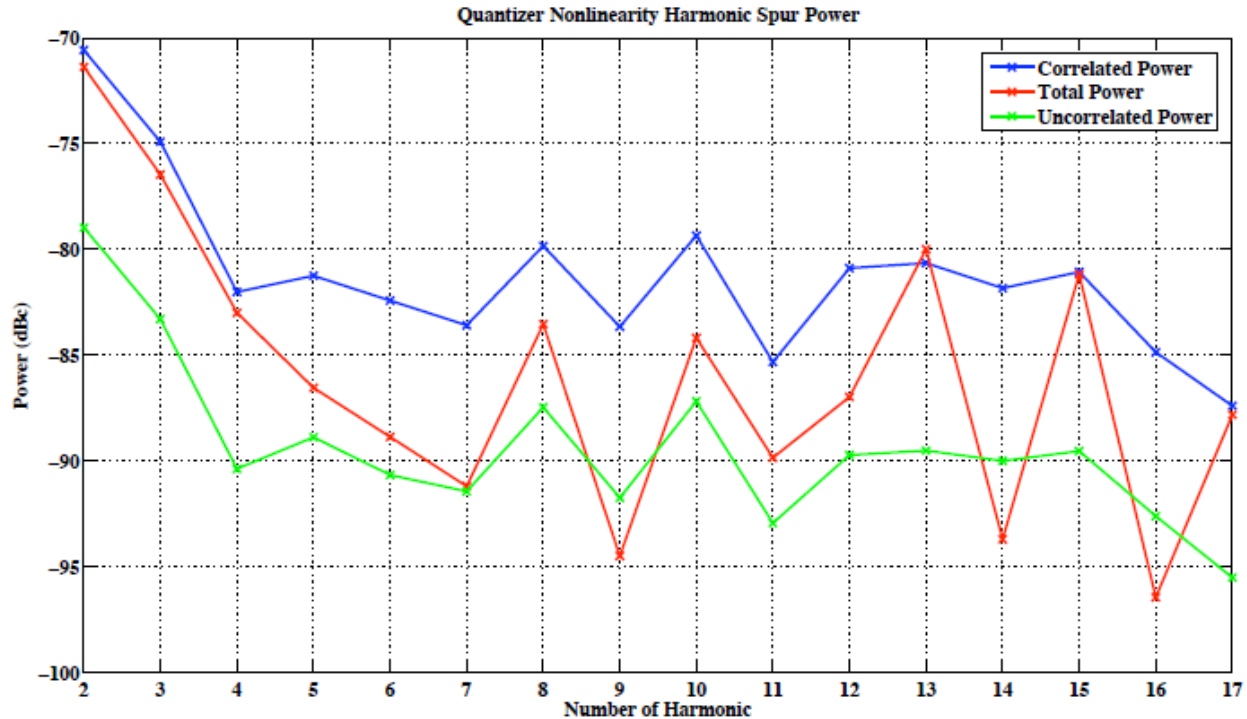
Figure 10. Plots of the total power of multiple harmonics for a DDS output frequency of 20.5 MHz.

The high correlation observed suggests that, for the lowest order harmonics, there is little benefit to using an array of DDSs to decrease the effect of in-band quantizer nonlinearities. Instead, system designers must address the problem of these spurs using alternate methods, such as careful frequency planning, to ensure that high-power harmonics (particularly the second and third) are adequately filtered and do not alias into the frequency band of interest [12]. Channels could also be phased such that specific low-order harmonics destructively interfere [15].

CONCLUSIONS

In summary, we have used a custom-built 14-channel DDS testbed to experimentally investigate the correlation of spurs in parallel DDS arrays. We focused on three primary error-types common to the DDS architecture: phase truncation spurs, quantization noise, and quantizer nonlinearity spurs. Our measurements indicate that, at least in our system, phase truncation spurs are uncorrelated across multiple channels, contrary to the theoretical prediction. We believe this decorrelation arises from an unidentified mechanism in the FPGA that randomizes the relative phases of the truncation spurs upon power-up. This mechanism decorrelates the phase truncation spurs, opening the potential for SFDR gain in the combined output of a DDS array. Our analysis of the quantization noise spurs reveals that the total quantization noise power of each DDS channel is uncorrelated for DAC resolutions ranging from 3 to 10 bits. This suggests that a near ideal gain of $10\log_{10}(N)$ dB in SQNR is possible for an N-channel array of DDSs. This gain will be most apparent for DDSs incorporating low-resolution DACs, in which the quantization noise is considerably higher than the thermal noise contribution. Lastly, our measurements of quantizer nonlinearity spurs demonstrate that, at least for the range of frequencies tested, the largest,

low-order harmonics are highly-correlated across channels. As a result, alternate methods of harmonic spur management must be employed to reduce these spectral components. Taken together, our measurements indicate that, dependent upon the type of spur dominant in a given system implementation and application, parallel DDS architectures have the potential to yield significant gains in a system's SFDR.

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