

# DISCIPLINED RANGE TIME CODE TRANSLATORS WITH SUB-MICROSECOND ACCURACY

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Serial Time Code signals have long been used to transfer time over various communication channels and media over both short and long distances. Generally, the accuracy of this method of time transfer has been thought of in terms resolution of the code modulation — for instance, 1 second for IRIG-B, 0.1 seconds for IRIG-A, etc. However, in most Time Codes, the carrier frequency is coherent with the modulation and thus provides the means for much greater resolution and accuracy. In the case of the IRIG-B code, with its 1 kHz carrier, time resolution of better than one thousandth of a carrier cycle is now possible, leading the way to sub-microsecond time transfer accuracy. Newly developed precision Time Code Translators with this capability are now being used to improve the accuracy of time transfer throughout several large Missile Test Range timing networks.

A typical Range timing distribution network is shown in Fig. 1A. Precision time is kept at a central timing site on the Range; converted at that site to all the various time signals required by the Range users; then all of these signals are transferred to the various remote sites on the Range by use of a communication network. Because of the wide variety of bandwidths of the many different timing signals used on a large Range, the distribution and communication elements are complex, inaccurate, and difficult to maintain. As shown in Figure 1B, a Range timing network can be greatly simplified by using only IRIG-B (modulated 1 kHz) to transfer time from Timing Central to all remote sites. This signal was selected because of its ease of transmission over relatively narrow band communication networks. To obtain good time transfer accuracy the chief constraint on a communication channel is that it must have propagation delay that is very stable with regard to time and temperature. The noise properties of the communication channel are not very important since the noise that is picked up in transmission can be overcome by the use of long term filtering at the receiving end. The key to this timing system approach was the development of a precision, low cost time code translator to be put at each remote site to receive the IRIG-B signal and to regenerate the various timing signals needed by individual users. At the more important sites, an IRIG-B signal from the translator output can be returned to Timing Central to monitor the performance of the overall system.

Trak Systems in Tampa, FL has developed two time code instruments for these applications: The Model 8700 and the Model 8400B, as shown in figure 2. The units are essentially identical except for the greater number of different types of time signals available from the larger Model 8700. Both units use an internal ovenized quartz oscillator that is disciplined to the incoming IRIG-B code by use of a micro-processor based second order phase locked loop. During periods of poor signal reception the units free run with the quartz oscillator locked to its latest corrected frequency. Thus, when the IRIG-B signal is present, the quartz oscillator in the translator is kept continuously calibrated to the accuracy of the Timing Central IRIG-B, which is usually based on Cesium Standards. The disciplined quartz oscillators are of  $10^{-9}$  per day stability, which allow a loop time constant in the

order of 1 hour for this application. This time constant provides excellent filtering of the noise picked up by the IRIG-B signal during transmission over the communication system.

The performance of these Translators is summarized in Figure 3. The primary problem in the development of these translators has been in achieving a phase locked loop algorithm that acquires rapidly; that is stable; and that provides good noise filtering. Our objective was to provide output timing signals with long and short term accuracy of better than 1 microsecond with an acquisition time of less than 2 hours from a cold oscillator start. In actual Range installations, the 8700's have typically yielded output timing noise levels of 500 nsec pp. The 8400B's have an improved phase detector design are typically yielding output timing noise levels of 300 nsec pp. Much of the evaluation has been done over a 12 mile telephone pair land line. When used on quiet short haul lines these translators exhibit output noise levels as low as 100 nsec pp. Much more testing is needed to fully determine the long term accuracy of the translators and the long term stability of the communication system propagation delays, however it appears that the overall system goal of 1  $\mu$ sec is now being realized.

Figure 4A is an example of the time base noise on an IRIG-B signal at the input of the Translator after transmission over 12 miles of telephone cable and terminating amplifiers. This noise was observed to be typically 10 microseconds peak-to-peak with worse cases to 30 microseconds pp. The spectral properties of this noise has not been adequately measured. The larger noise spikes appear to be a few seconds in duration. Noise components of 1  $\mu$ sec amplitude were observed to exist for up to 30 second durations. The resulting output from the Translator is shown in Figure 4B.

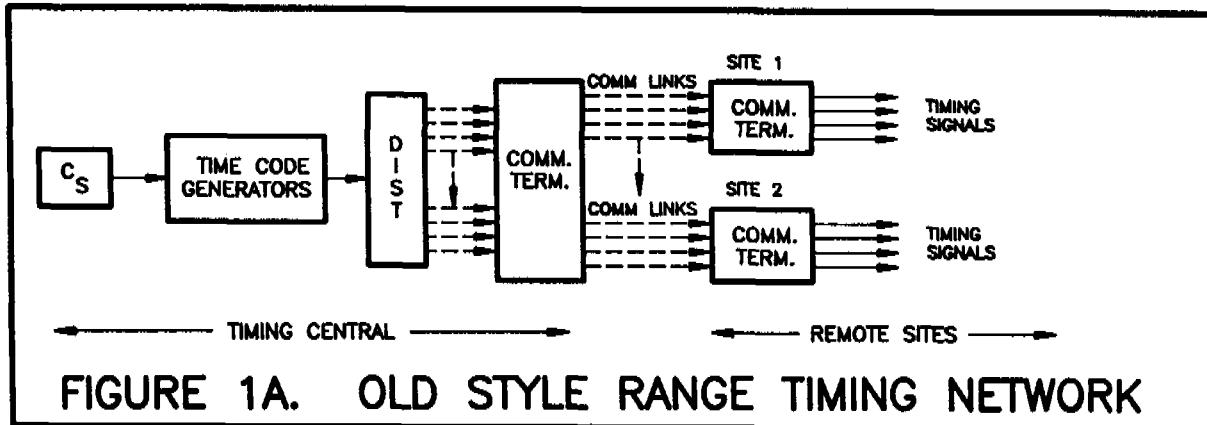
Figure 5 shows the major circuit elements used in these translators. The incoming IRIG-B code is detected and processed by somewhat conventional time code reader circuitry. When several frames of error free and sequential code have been detected, the incoming code is used to initially jam synchronize the translator. Very accurate detection of the carrier zero crossing near the middle of the once per second frame marker pulse is then used to measure both the frequency of the phase of the internal local oscillator as compared to the incoming signal. A micro-processor is used to process the error signals and to slowly correct the oscillator frequency and phase by analog frequency control of the oscillator thru a DAC. At initial turn-on, the DAC is first used to control the frequency of the oscillator. After about 15 to 20 minutes, when the oscillator drift has reached acceptable levels, the translator is again jam synchronized to the incoming code to a phase accuracy of about 10  $\mu$ sec. The final phase control process then begins. The reduction of the initial phase error from the 10  $\mu$ sec level down to less than 1  $\mu$ sec typically takes about an hour. The micro-processor is also used to control the action of most of the other circuit elements. Once a code error or a code dropout is detected, the unit immediately inhibits external time updates; freezes the DAC at its average control point; and proceeds to free run on the internal oscillator. To avoid the use of bad code, strict code re-acquisition rules must then be met before returning to the use of the incoming code. The translator has internal dip switches for setting fixed propagation delay corrections to a resolution of 1  $\mu$ sec. Conventional code generators are used to provide a multiplicity of output codes and rates.

Figure 6 shows the main elements of the final control algorithm. The phase error between the internal oscillator and the incoming code is measure once per second to an resolution of 100 nsec. The error signal is then filtered with an 8 second moving average. To obtain the lead time constant necessary to stabilize the second order loop, the error is in essence processed over two parallel paths: a proportional path and an integrating path. These paths are combined and applied to the DAC to control the frequency of the oscillator. The oscillator itself provides the second integration (from frequency to phase). The DAC provides a total frequency control range of about  $\pm 10^{-6}$  with a resolution of  $10^{-9}$ . The effective time constant of the closed loop is about 1 hour. In the current implementation, the proportional path is in fact very non-linear and is limited to just three values 0, +X, and -X. The value of X was chosen to give reasonably fast acquisition, but also to limit the frequency changes in the oscillator at any one time. This type of control, with a small value of X has

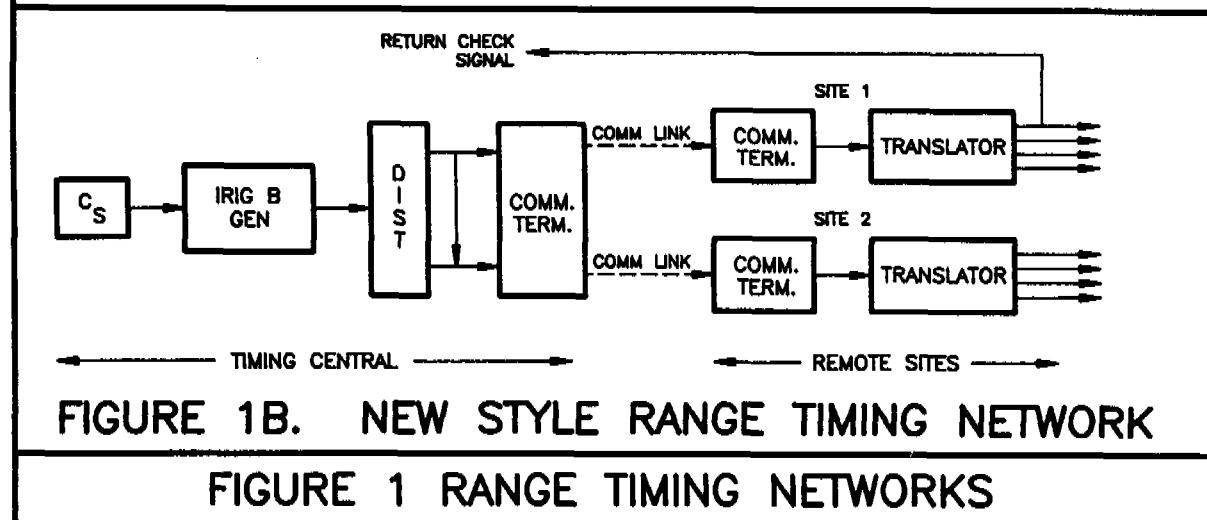
the advantage making the unit almost insensitive to input noise amplitude. The integrating path is accomplished digitally by the micro-processor, forming a perfect drift-free integrator.

Computer simulation studies were used to optimize the control algorithms. Initial studies were done on a PC, using Lotus 123 (c) and were very effective in solving early stability problems. Later and more comprehensive simulations at Trak used an AT computer and "C". The simulations were found to be very useful in speeding up the development, as the time required for testing of the actual hardware is quite long. One interesting finding in the simulations was that the control actually improves with some input noise. The noise acts like "dither" in a mechanical servo and allows control beyond the resolution of the phase measuring circuit and the DAC. It was also noted that the initial moving average processing is of no particular value and can in fact contribute to loop instability if the average is too long. A short moving average was thought to be necessary for protection against large noise spikes, but it is really not needed because of the hard limits put on the oscillator control. Figure 7 shows typical result of some of the early stability studies that were done with Lotus 123. The limit cycle oscillation around the 100 nsec resolution limit of the phase detector was seen in actual test data, but its amplitude is reduced by input noise.

In achieving 1 microsecond time transfer accuracy with IRIG-B, we are near the limit of accuracy of the phase detector. With the 1 khz carrier, this implies that the phase detector errors are less than 1/1000 of a carrier cycle. Thus, if higher levels of accuracy are needed, the use of higher frequency codes is recommended: IRIG-A for 100 nsec systems; and ultimately IRIG-G for 10 nsec systems. For the higher levels of accuracy, development is needed on a more precise time code Generator for use at the central site. In fact some of the data accumulated with the 1 microsecond systems indicate that the Generator may be a substantial source of error in these systems. By far the largest body of work yet to be done is in better understanding propagation delay changes in the communication links. For the first time, with these precision Translators, we have the tools to see and to measure the components of system error that were previously masked by the inaccuracy and noise in the Translator.

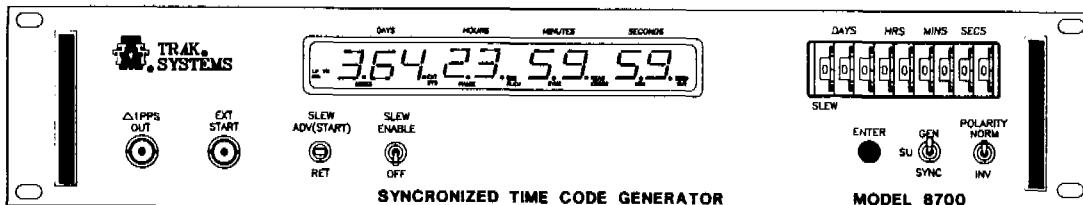


**FIGURE 1A. OLD STYLE RANGE TIMING NETWORK**



**FIGURE 1B. NEW STYLE RANGE TIMING NETWORK**

**FIGURE 1 RANGE TIMING NETWORKS**



- IRIG B INPUT
- MULTI-CODE OUTPUTS
- INTERNAL OVENIZED QUARTZ OSCILLATOR
- 2nd ORDER PHASE - LOCKED LOOP
- MICROPROCESSOR BASED

**FIGURE 2 TRAK MODELS 8700 AND 8400B**

	<u>TRAK MODEL</u>	
<u>GOALS</u>	<u>8700</u>	<u>8400B</u>
PEAK-TO-PEAK NOISE (OVER COMM. LINES)	1 $\mu$ SEC	500 nSEC    300 nSEC
OVERALL ACCURACY (OVER COMM. LINES)	1 $\mu$ SEC	* 1 $\mu$ SEC    *1 $\mu$ SEC
PEAK-TO-PEAK NOISE (OVER QUIET LINES)	—	200 nSEC    100 nSEC
ACQUISITION TIME	2 HRS	2 HRS    2 HRS

(\*) NOT FULLY EVALUATED.

### FIGURE 3 PERFORMANCE GOALS & RESULTS

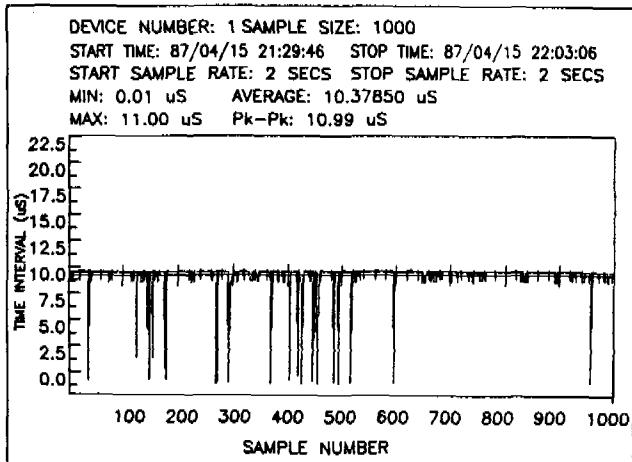


FIGURE 4A TYPICAL INPUT NOISE

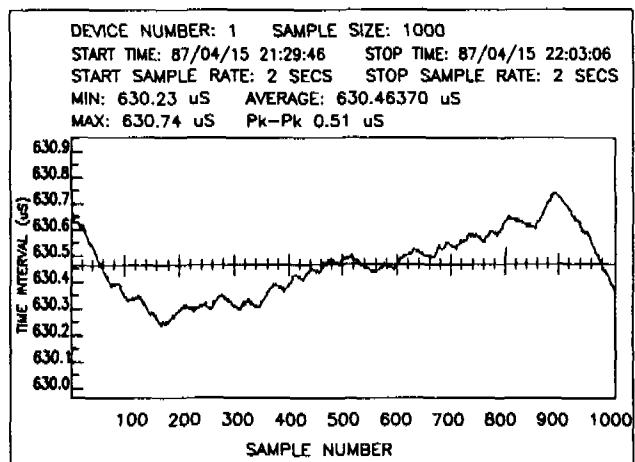
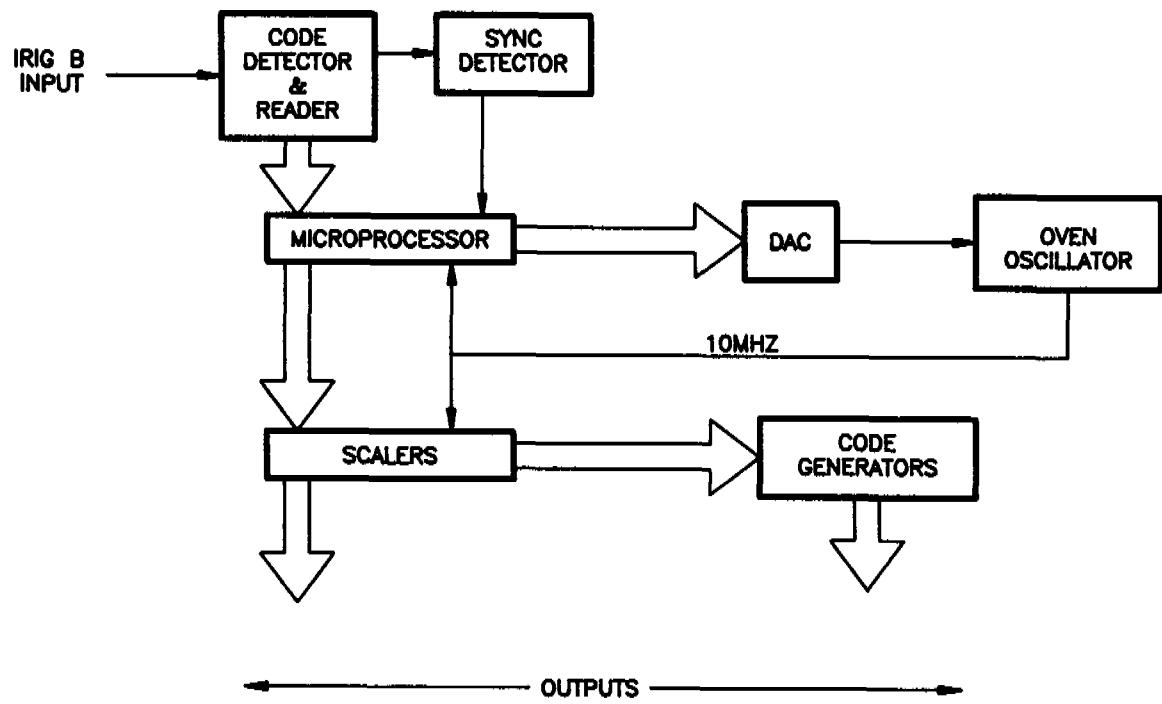
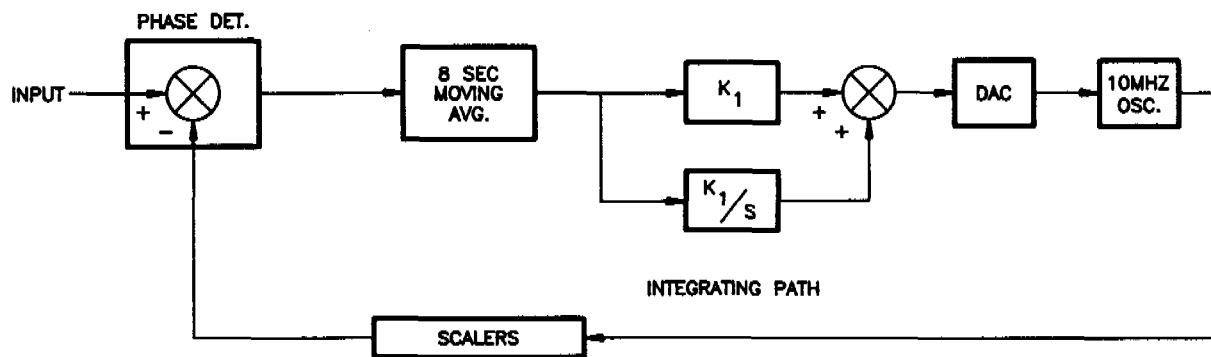


FIGURE 4B TYPICAL OUTPUT DEVIATION  
(WITH 10μS INPUT NOISE)



**FIGURE 5 TRAK SYSTEMS MODEL 8400B  
SIMPLIFIED BLOCK DIAGRAM**

### PROPORTIONAL PATH



**FIGURE 6 TRAK SYSTEMS MODEL 8700/8400B  
FINAL CONTROL ALGORITHM**

# MODEL 8700 PHASE CONTROL #1

10 SEC AVERAGING; OSC T/C=0

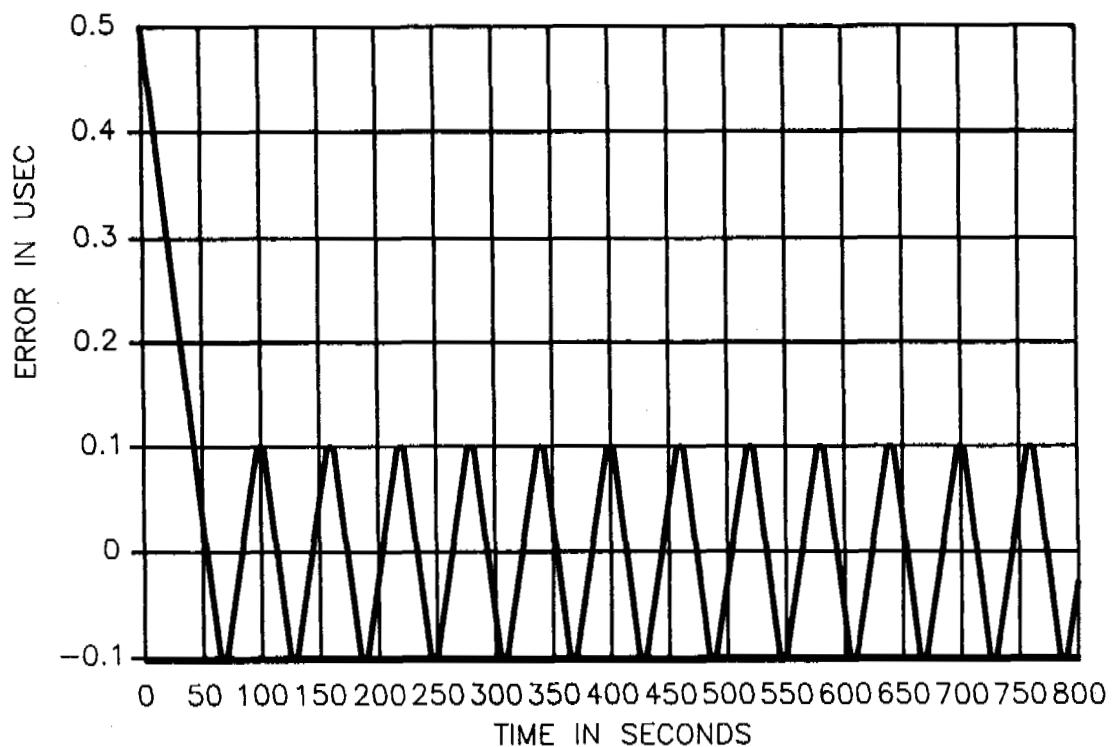


FIGURE 7 SIMULATION STUDIES TYPICAL PLOTS