

METAS NEW TIME SCALE GENERATION SYSTEM – A PROGRESS REPORT

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Abstract

Up to now, UTC (CH) has been defined as a paper time scale which is computed for a single epoch every day: UTC 00:00. In 2006, we have started to phase in the hardware for a new system, still under development, which should allow us to define UTC (CH) as a real time scale generated by a master clock, i.e. a time scale defined for all epochs. The new system should preserve the advantages of the original system while improving reliability, availability, and compatibility with other UTC (k)'s.

INTRODUCTION

UTC (CH) is different from the other national time scales in the sense that it is actually a *computed* time scale defined only for epoch UTC 00:00 of each day. The paper time scale, noted UTC (CH.P), is a weighted average of five free-running atomic clocks and it is steered monthly to track UTC. As shown in Figure 1, two GPS links and a TWSTFT station are used for remote T&F comparisons. The GPS TAI link is driven by one of the atomic clocks defined as the REF clock.

During 2006, we have started to phase in a new system intended to supersede the original one sometime next year. Herewith, UTC (CH) becomes the signal output from a master clock; hence, it is defined for all epochs. Moreover, both the multi-channel phase comparison system and the master clock are now redundant, which greatly improves the reliability of the system.

ADVANTAGES AND DISADVANTAGES OF A PAPER CLOCK

The advantages of a paper definition of UTC (CH) are, first, that a time scale based on a clock ensemble is more stable than the best of the participating clocks and, second, that the time scale continues to run should there be a failure of one of the clocks.

The disadvantages are, first, that the virtual synchronization between the hardware clocks and the software clocks is part of the TAI link calibration. Consequently, if the virtual synchronization is lost, so is the TAI link calibration. Second, because the paper time scale UTC (CH.P) is computed every day for

a single epoch, measurements performed at other epochs can be referred to UTC (CH) only via an interpolation. This is a source of inaccuracy.

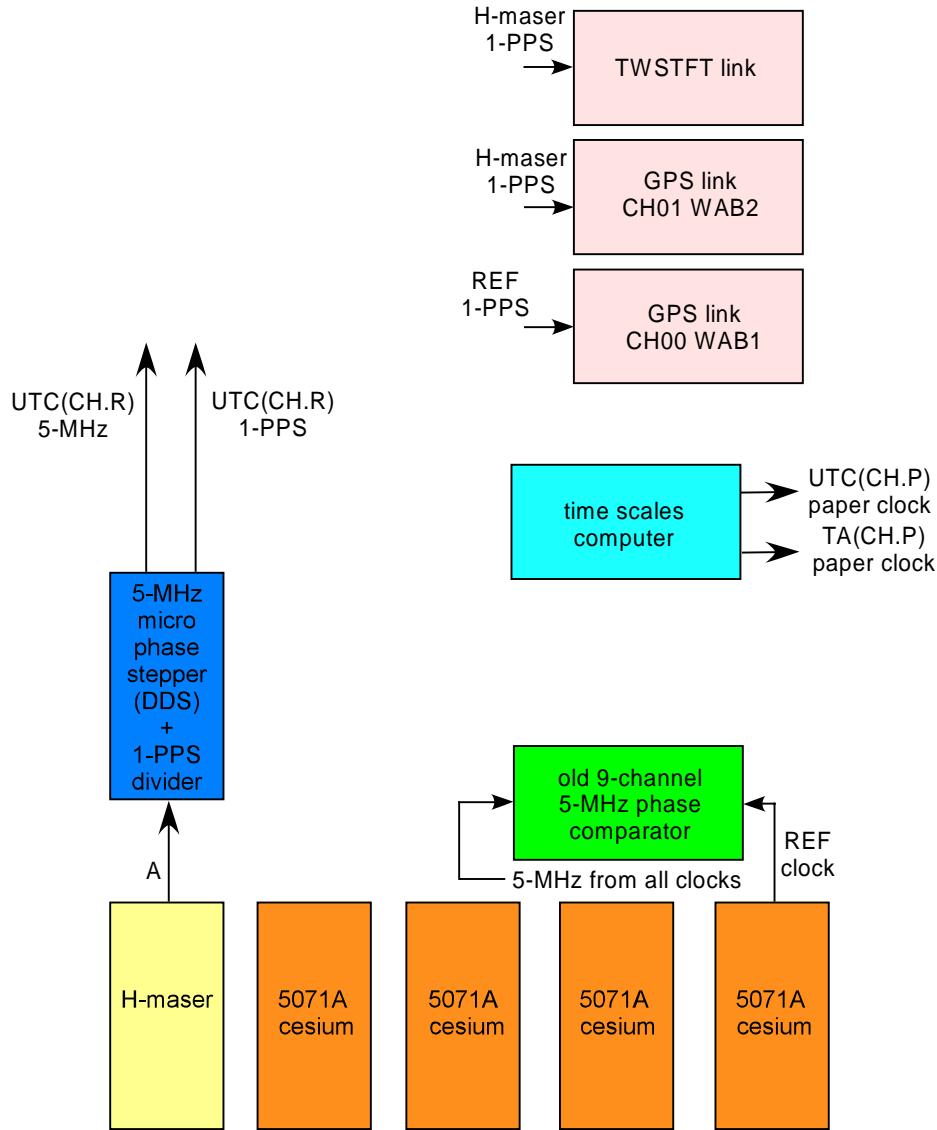


Figure 1. Original system: UTC (CH) defined as a paper clock.

DRAWBACKS OF THE ORIGINAL PHASE COMPARISON SYSTEM

The original 5 MHz nine-channel phase comparison system that we use to compare the atomic clocks requires one of them to be singled out to be used as the reference and connected to a hardware reference channel. The disadvantage of such a design is that the REF clock is a single-point-failure node in the system. As a matter of fact, if the REF clock fails, the whole phase difference measurement process is

disrupted as well as the time scale generation process, whereas if any other clock fails, the processes continue with $n - 1$ clocks instead of n clocks.

DESCRIPTION OF THE NEW ARCHITECTURE

Figure 2 shows the new time scale generation system whereby UTC (CH) is defined as a hardware master clock, noted UTC (CH.RT). The definition of UTC (CH) via hardware eliminates the drawbacks of the paper clock definition. Measurements can be referred to UTC (CH) for all epochs without interpolation and the TAI link calibration does not depend on the virtual synchronization between the paper and hardware clocks. Moreover, the advantages of a paper clock definition are preserved, since the steered master clock inherits the high stability of the paper time scale.

A new 5 MHz 12-channel phase comparison system was procured in addition to the original 9-channel phase comparison system. Hence, we can now rely on a hardware redundancy that makes the phase comparison process failsafe. Moreover, the new phase comparison system has a lower noise level and has a reduced temperature sensitivity as compared to the original phase comparison system.

The new 5 MHz phase comparison system has also its own internal reference clock. This eliminates the necessity for a hardware reference clock channel; the reference clock can be selected by software, and there is no single-point-failure node in the system.

The UTC (CH.RT) hardware definition of UTC (CH) is chosen from one of two independent master clocks: UTC (CH.A) and UTC (CH.B). Each is the output from a DDS synthesizer, used as a Micro-Phase Stepper (MPS). Each is driven by one of the free-running atomic clocks, and steered to track the paper time scale UTC (CH.P).

Auto-sense Fault Switches (AFS) are used to choose UTC (CH.RT) between the A/B master clocks. The hardware redundancy between UTC (CH.A) and UTC (CH.B) has two advantages. One is reliability: if one master clock fails, switching to the backup master clock is instantaneous. The second is continuity of service: if some maintenance of one master clock becomes necessary, for example for the purpose of calibration, it is possible to switch to the other master clock at one's convenience without interruption of service.

Calibration of each master clock can be performed independently. As before, the paper time scale

UTC (CH.P) can be used as a stable flywheel to interpolate UTC between the monthly publications of *Circular T*. However, the calibration of the TAI link no longer depends on the synchronization between hardware and paper clocks. Should the virtual synchronization be lost, the only consequence would be a transient of UTC (CH.P), which can be corrected by a subsequent steering.

The GPS and TWSTFT links can be driven either by the 1-PPS signal from the UTC (CH.RT) master clock or by any free-running clock, depending on the stability requirements.

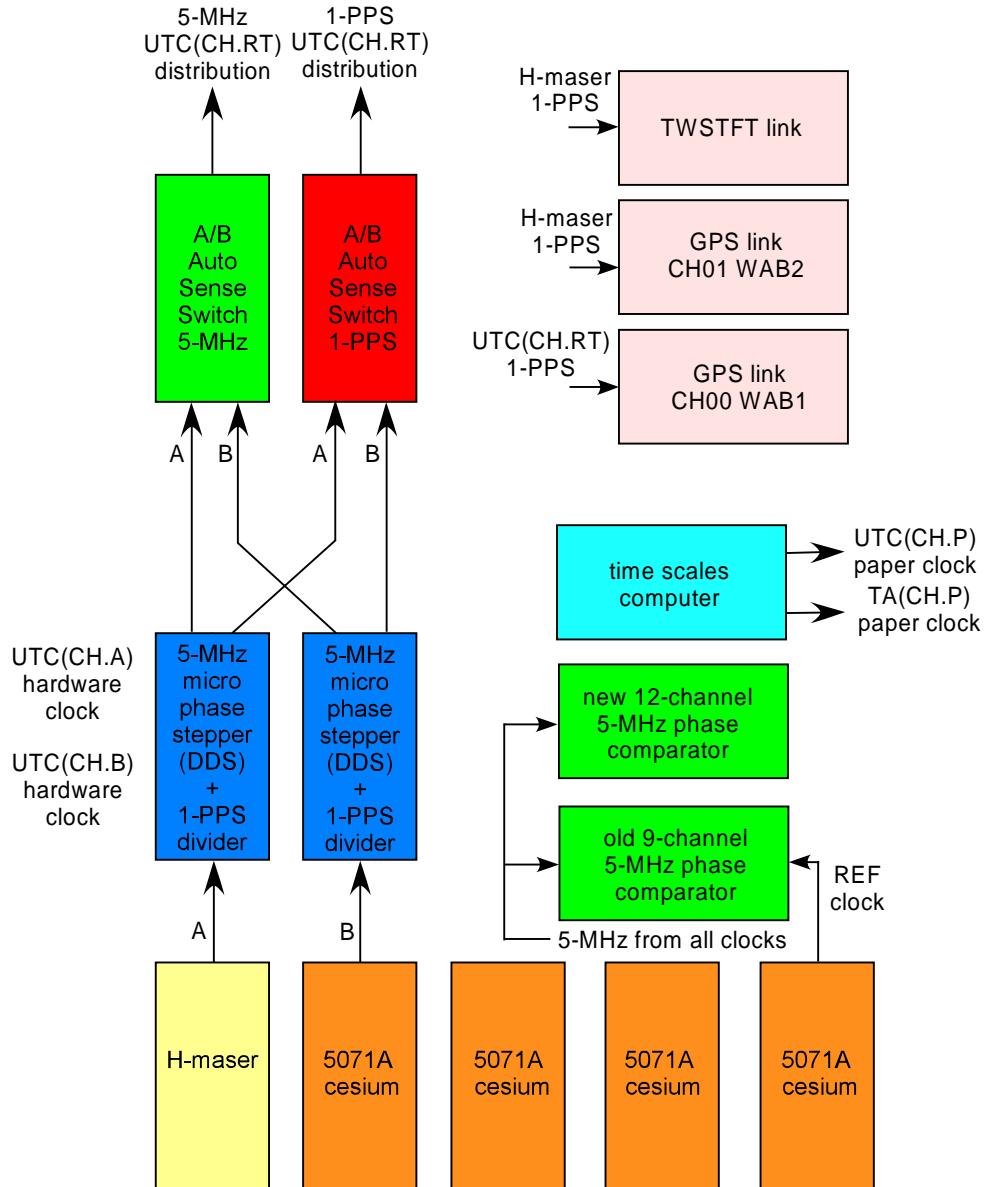


Figure 2. New system: UTC (CH) defined as a master clock steered to the paper clock.

CALIBRATION OF THE TAI LINK WHEN UTC (CH) IS A PAPER CLOCK

Figure 3 illustrates the calibration procedure of the TAI link in the original system, in which UTC (CH) is a paper clock. Note that in both Figure 3 and Figure 4, the phase/time state of each clock is represented by a rotating phasor. A full circle represents one period of the 5 MHz signal. Hardware clocks are represented by bold phasors, while paper clocks are represented by dotted line phasors. When we perform with BIPM a differential calibration of the GPS TAI link, we declare the delay REFPLY (TAI), which is actually that between the 1-PPS reference plane of the REF hardware clock and the 1-PPS input

of the GPS receiver. The REFDLY constant is declared in the header of the CGGTTS common-view files. Then the BIPM compares the CGGTTS data from the TAI receiver with the CGGTTS data from a co-located travelling reference receiver.

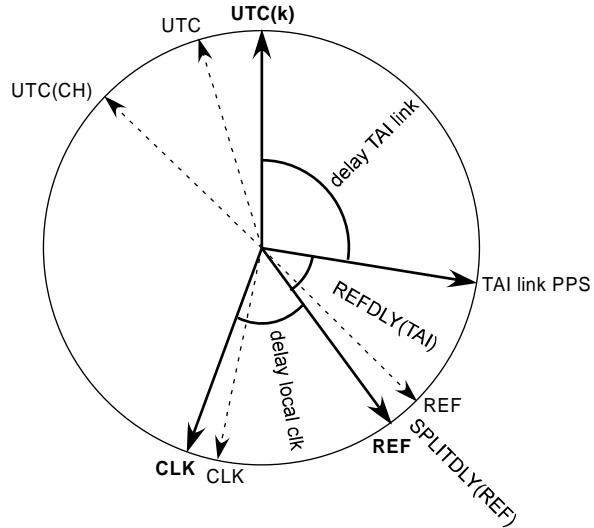


Figure 3. Calibration of the TAI link when UTC (CH) is a paper clock. Hardware clocks are represented by bold phasors, whereas paper clocks are represented by dotted line phasors. The REF clock *split delay* is the unwanted offset between the hardware REF clock and the paper REF clock that occurs when virtual synchronization is lost.

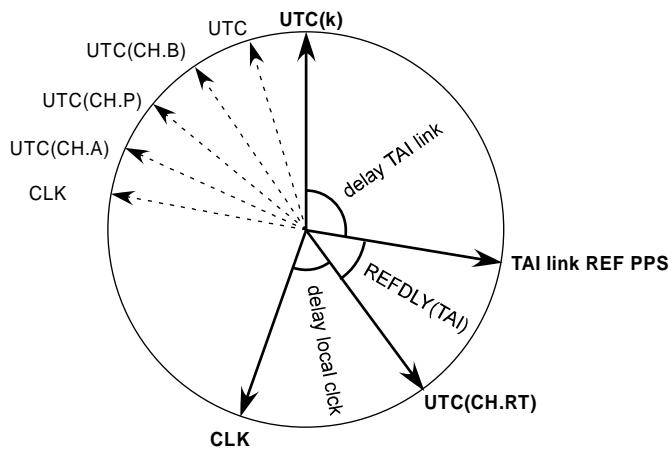


Figure 4. Calibration of the TAI link when UTC (CH) is a master clock. Hardware clocks are represented by bold phasors, whereas paper clocks are represented by dotted line phasors. If UTC (CH) is a hardware clock, all the delays involved in the TAI link calibration are measurable hardware delays.

On the one hand, the BIPM uses the CGGTTS data from the travelling reference receiver to determine the reference TAI link delay, i.e. the delay between the 1-PPS input of the traveling reference receiver and the UTC (k) 1-PPS signal of a pivot NMI. On the other hand, the BIPM determines the DUT TAI link delay, as measured by the DUT receiver, and adjusts the DUT internal delay constants so that the DUT TAI link delay matches the reference TAI link delay. Once the differential calibrations have been made in every NMI using the same traveling reference receiver, the international UTC (k) comparisons become consistent, even though the absolute internal delays in the receivers are not calibrated.

By definition, the 1-PPS reference plane of the REF hardware clock is the plane for which 1-PPS REF - UTC (k) hardware measurements made via the TAI link are consistent with the REF - UTC (CH) paper clock differences computed by the time scales computer and with the UTC (CH) – UTC (k) paper clock differences published by BIPM in *Circular T*.

$$[UTC(CH) - UTC(k)]_{CircularT} = [REF - UTC(k)]_{1-PPS} - [REF - UTC(CH)]_{paper\ clocks} \quad (1)$$

Consequently, after a differential calibration with BIPM, we have a virtual synchronization between the REF paper clock and the REF 1-PPS hardware clock, i.e. a reset of the REF clock *split delay*, as defined in Figure 3.

$$SPLITDLY(REF) = REF_{1-PPS} - REF_{paper} = 0 \quad (2)$$

which describes the time/phase discrepancy between the REF 1-PPS and the REF paper clock.

The virtual synchronization of the hardware REF clock with the paper REF clock may be understood as follows. On the one hand, the hardware state of each clock is defined by its 1-PPS output signal. On the other hand, the paper clock states are software state variables that express the computed differences between each clock and UTC (CH).

Every day, when the time scale is computed, the state variable of each clock is updated on the basis of the NBS time scale algorithm [3]. The experimental input data used by the time scale algorithm to determine the new clock states are actually the measured daily increments of the 5 MHz phase differences of each clock *versus* the REF clock, measured between UTC 00:00 of the previous day and UTC 00:00 of the current day. In that context, the virtual synchronization of the paper clocks *versus* the hardware clocks is simply the correct programming of the software state variables, so that the software states of the clocks are consistent with the hardware state of their 1-PPS signals.

The consistency of the clock to clock paper state differences can be set and verified easily via local measurements of the phase/time differences between the 1-PPS signals. On the other hand, however, because UTC (CH) is a paper clock, the paper state difference between the REF clock and UTC (CH) cannot be verified via a local 1-PPS measurement. It can be verified only via equation (1), which involves both a remote comparison with a hardware UTC (k) time scale generated in another NMI and the paper difference UTC (CH) – UTC (k) as published in *Circular T*.

Such a consistency check yields the actual value of SPLITDLY (REF). Once the *split delay* is determined, the virtual synchronization can be restored by introducing a step of the UTC (CH.P) paper time scale with respect to UTC. In practice, a step of UTC (CH) versus UTC is implemented by applying a step to the state variable of all the paper clocks *versus* UTC (CH). However, since the 1-PPS of the

REF clock does not make a step and evolves smoothly versus UTC, the BIPM correctly interprets the step as a step of UTC (CH) versus UTC.

In conclusion, every time the TAI link is calibrated by BIPM, the REF clock *split delay* is reset to zero. However, if for some reason the virtual synchronization is lost, for example when the phase difference measurement is disrupted by a software or hardware failure, so is the TAI link calibration, and a new calibration must be performed.

CALIBRATION OF THE TAI LINK WHEN UTC (CH) IS A HARDWARE CLOCK

Figure 4 illustrates the calibration procedure of the TAI link in the new system in which UTC (CH) is a master clock. In such a system, the calibration of the TAI link involves only measurable hardware delays. Hence, there is no virtual hardware *versus* paper clock synchronization to lose. In case of an accident with the phase measurements or with the time scale generation, the paper time scale might suffer a transient but the calibration would not be affected.

NOISE CHARACTERISTICS OF THE MMS

The new 5 MHz 12-channel phase measurement system is a Timing Solutions Corp. TSC-12032 Multi-Channel Measurement System (MMS). The MMS has its own internal common reference oscillator. Hence, there is no need for a dedicated REF clock; all atomic clock phase measurements generated by the MMS are in fact time/phase differences measured with respect to the common oscillator. The frequency offset and frequency instabilities of the latter are cancelled out as a common mode noise source, since the time scale generation process is based on atomic clock phase/time differences, i.e. on differential measurements taken between pairs of MMS channels.

Figure 5 shows the residual, i.e. the measurement offset by an arbitrary constant to remove the average value, of the difference between two channels of the MMS driven by a common atomic clock. It can be observed that there is a small transient, probably thermal, when the input signals are connected to the MMS. Figure 6 shows the time deviation of the residual. The time deviation in units of time is derived from the modified Allan deviation as follows:

$$\sigma_x(\tau) = \frac{1}{\sqrt{3}} \times \tau \times \text{mod} \sigma_y(\tau) \quad (3)$$

A time deviation of $\sigma_x(1s) = 0.15 \text{ ps}$ is observed. In terms of the Allan deviation, this is equivalent to a white phase noise floor at a level of $\sigma_y(\tau) = 2 \times 10^{-13} \times \tau^{-1}$. Actually a white phase noise is observed up to 100 s, while for higher integration intervals a flicker of phase is observed. The level of the phase flicker floor is about $\sigma_x(1000s) = 0.02 \text{ ps}$. Some random walk of phase seems to be present, but the recording interval was too short for a precise estimation. These results show that the excellent temperature stability maintained in the laboratory ($< 0.1^\circ\text{C}$) combined with the very low temperature sensitivity of the MMS produce very low levels of long-term environmental phase noise.

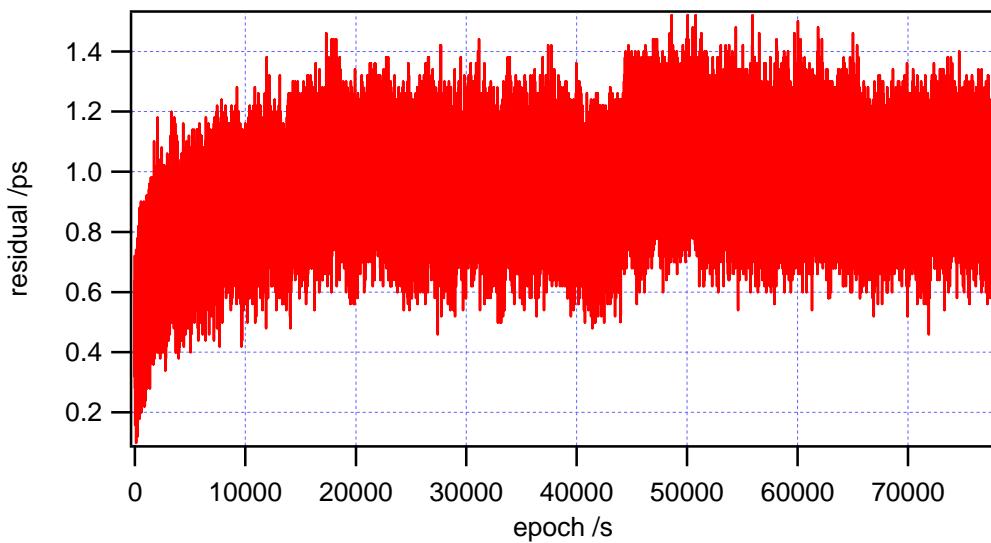


Figure 5. Difference between two MMS channels driven by a common clock.

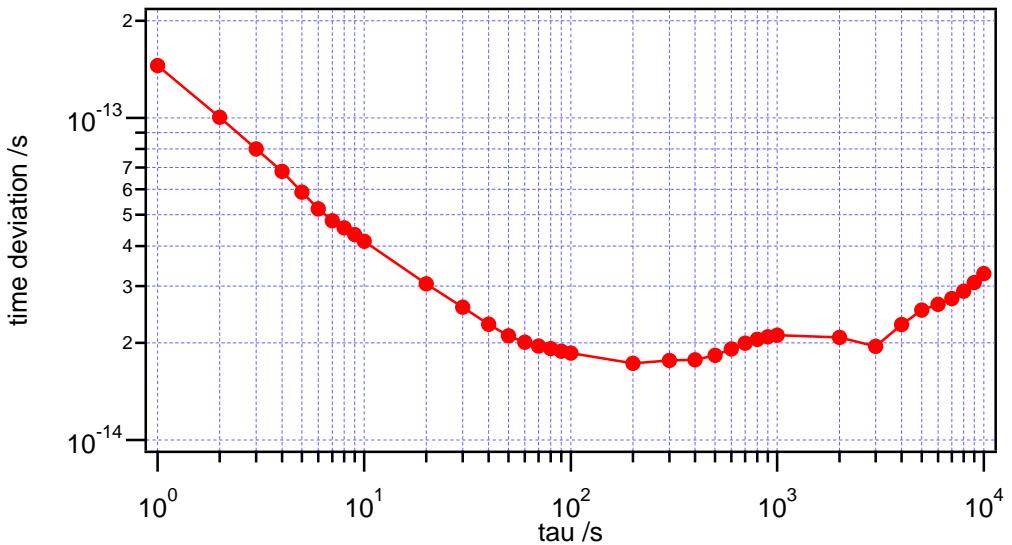


Figure 6. Time deviation of the difference between two MMS channels driven by a common clock.

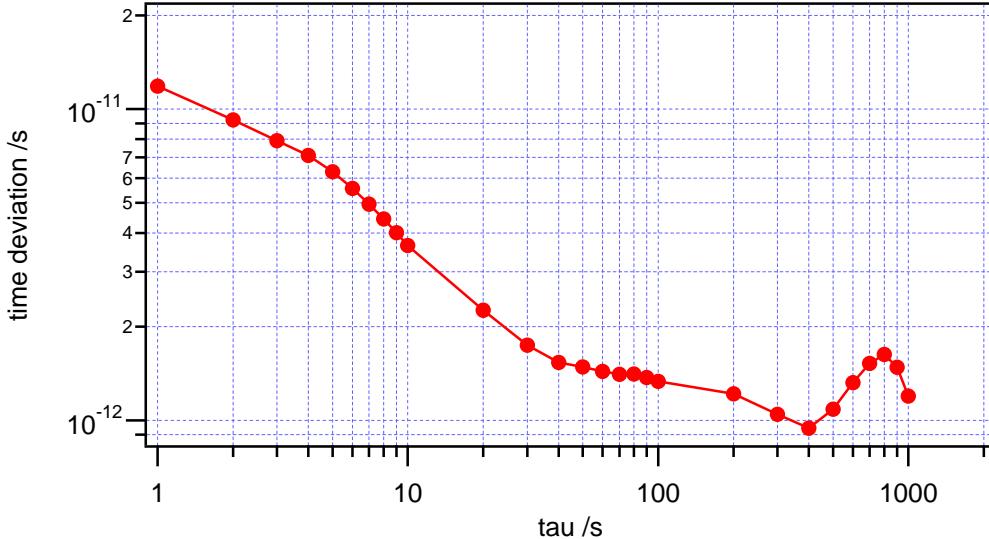


Figure 7. Time deviation of the difference between two MPS driven by a common clock.

NOISE CHARACTERISTICS OF THE MICRO-PHASE STEPPERS

The Micro-Phase Steppers (MPS) used to generate the master clocks UTC (CH.A) and UTC (CH.B) are actually TSC-2043B DDS synthesizer modules and TSC-2061 1-PPS divider modules. Figure 7 shows the time deviation measurement of the noise floor of the micro-phase steppers. A common source drives the pair of micro-phase steppers and each is measured by the MMS. The measurement shown is the difference between the MMS channels connected to each micro-phase stepper. The observed white phase noise level is $\sigma_x(1\text{s}) = 10\text{ps}$ for a pair of micro-phase steppers, i.e. two orders of magnitude higher than the noise floor of the MMS alone. The observed flicker phase noise level is $\sigma_x(100\text{s}) = 1.5\text{ps}$, i.e. also two orders of magnitude higher than the noise floor of the MMS alone.

STEERING OF THE MASTER CLOCKS

The micro-phase steppers are used to generate UTC (CH.A) and UTC (CH.B). The steering of the master clocks is performed once a day since the time scales are computed at this rate. A predictive steering algorithm is used [1,2]. UTC (CH.A) is generated by the steering of the hydrogen maser, whereas

UTC (CH.B) is generated by the steering of a standard performance 5071A cesium clock. Hence,

UTC (CH.A) is expected to track UTC (CH.P) with a smaller rms deviation than UTC (CH.B) due to the better short-term stability of the hydrogen maser. Figure 8 and Figure 9 show the experimental measured difference between the steered master clocks A and B with respect to the paper time scale. The master clock A shows an rms deviation of 1 ns, whereas the master clock B shows an rms deviation of 3 ns. This threefold ratio between the A/B rms deviations confirms the expectation that the master clock A should show a better tracking of the paper time scale because it is driven by a hydrogen maser.

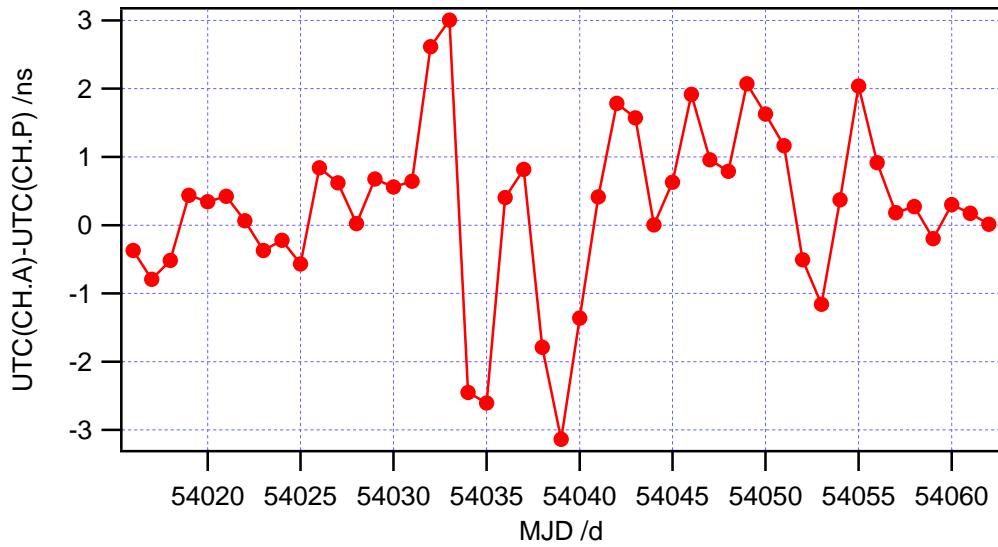


Figure 8. Recording of UTC (CH.A) – UTC (CH.P). Master clock driven by hydrogen maser.

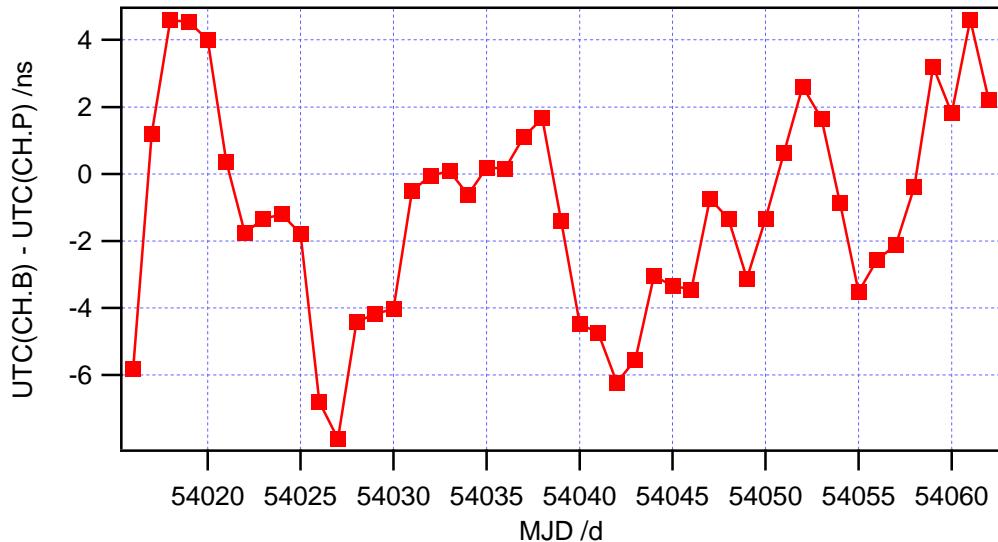


Figure 9. Recording of UTC (CH.B) – UTC (CH.P). Master clock driven by a commercial cesium.

CONCLUSION

This paper reports the current development status of our new time scale generation system. In the new system, the original paper clock definition of UTC (CH) is replaced by a master clock definition. The scheme of a pair of redundant master clocks steered to a common paper time scale that we have adopted for the new system eliminates the drawbacks of a paper clock definition, while preserving the advantages.

The new hardware is now fully operational and we already benefit from the increased reliability given by the parallel operation of the original and new multi-channel phase comparators. However, the control software is still under development, but should be fully operational by mid 2007. METAS intends to switch to the new official definition of UTC (CH) before the end of 2007 after a few months of validation testing.

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