AC	
Item No.	

UNIVERSITY OF MUMBAI



Bachelor of Engineering

in

Electronics and Telecommunication Engineering

Second Year with Effect from AY 2020-21

Third Year with Effect from AY 2021-22

Final Year with Effect from AY 2022-23

(REV- 2019 'C' Scheme) from Academic Year 2019 – 20

Under

FACULTY OF SCIENCE & TECHNOLOGY

(As per AICTE guidelines with effect from the academic year 2019–2020)

AC	_
Item No	_

UNIVERSITY OF MUMBAI



Syllabus for Approval

Sr. No.	Heading	Particulars
1	Title of the Course	Third Year in Bachelor of Electronics and Telecommunication Engineering
2	Eligibility for Admission	After Passing Second Year Engineering as per the Ordinance 0.6243
3	Passing Marks	40%
4	Ordinances / Regulations (if any)	Ordinance 0.6243
5	No. of Years / Semesters	8 semesters
6	Level	P.G. / U.G. /- Diploma / Certificate (Strike out which is not applicable)
7	Pattern	Yearly / Semester (Strike out which is not applicable)
8	Status	New / Revised (Strike out which is not applicable)
9	To be implemented from Academic Year	With effect from Academic Year: 2021-2022

Date 15-05-2021

Dr. S. K. Ukarande Associate Dean Faculty of Science and Technology University of Mumbai Dr Anuradha Muzumdar Dean Faculty of Science and Technology University of Mumbai

Preamble

To meet the challenge of ensuring excellence in engineering education, the issue of quality needs to be addressed, debated and taken forward in a systematic manner. Accreditation is the principal means of quality assurance in higher education. The major emphasis of accreditation process is to measure the outcomes of the program that is being accredited. In line with this Faculty of Science and Technology (in particular Engineering)of University of Mumbai has taken a lead in incorporating philosophy of outcome based education in the process of curriculum development.

Faculty resolved that course objectives and course outcomes are to be clearly defined for each course, so that all faculty members in affiliated institutes understand the depth and approach of course to be taught, which will enhance learner's learning process. Choice based Credit and grading system enables a much-required shift in focus from teacher-centric to learner-centric education since the workload estimated is based on the investment of time in learning and not in teaching. It also focuses on continuous evaluation which will enhance the quality of education. Credit assignment for courses is based on 15 weeks teaching learning process, however content of courses is to be taught in 13 weeks and remaining 2 weeks to be utilized for revision, guest lectures, coverage of content beyond syllabus etc.

There was a concern that the earlier revised curriculum more focused on providing information and knowledge across various domains of the said program, which led to heavily loading of students in terms of direct contact hours. In this regard, faculty of science and technology resolved that to minimize the burden of contact hours, total credits of entire program will be of 171, wherein focus is not only on providing knowledge but also on building skills, attitude and self learning. Therefore in the present curriculum skill based laboratories and mini projects are made mandatory across all disciplines of engineering in second and third year of programs, which will definitely facilitate self learning of students. The overall credits and approach of curriculum proposed in the present revision is in line with AICTE model curriculum.

The present curriculum will be implemented for Second Year of Engineering from the academic year 2020-21. Subsequently this will be carried forward for Third Year and Final Year Engineering in the academic years 2021-22, 2022-23, respectively.

Dr. S. K. Ukarande Associate Dean Faculty of Science and Technology University of Mumbai Dr Anuradha Muzumdar Dean Faculty of Science and Technology University of Mumbai

Incorporation and Implementation of Online Contents from NPTEL/ Swayam Platform

The curriculum revision is mainly focused on knowledge component, skill based activities and project based activities. Self learning opportunities are provided to learners. In the revision process this time in particular Revised syllabus of 'C' scheme wherever possible additional resource links of platforms such as NPTEL, Swayam are appropriately provided. In an earlier revision of curriculum in the year 2012 and 2016 in Revised scheme 'A' and 'B' respectively, efforts were made to use online contents more appropriately as additional learning materials to enhance learning of students.

In the current revision based on the recommendation of AICTE model curriculum overall credits are reduced to 171, to provide opportunity of self learning to learner. Learners are now getting sufficient time for self learning either through online courses or additional projects for enhancing their knowledge and skill sets.

The Principals/ HoD's/ Faculties of all the institute are required to motivate and encourage learners to use additional online resources available on platforms such as NPTEL/ Swayam. Learners can be advised to take up online courses, on successful completion they are required to submit certification for the same. This will definitely help learners to facilitate their enhanced learning based on their interest.

Dr. S. K. Ukarande
Associate Dean
Faculty of Science and Technology
University of Mumbai

Dr Anuradha Muzumdar Dean Faculty of Science and Technology University of Mumbai

Preface By BoS

Technological developments in the field of electronics and telecommunication engineering have revolutionized the way people see the world today. Hence, there is a need for continuously enriching the quality of education by a regular revision in the curriculum, which will help our students achieve better employability, start-ups, and other avenues of higher studies. The current revision in the Bachelor of Engineering program (REV- 2019 'C' Scheme) aims at providing a strong foundation with required analytical concepts in the field of electronics and telecommunication engineering.

Some of the salient features of this revised curriculum are as below and they fall in line with the features in AICTE Model Curriculum.

- 1. The curriculum is designed in such a way that it encourages innovation and research as the total number of credits has been reduced from around 200 credits in an earlier curriculum to 171 credits in the current revision.
- 2. In the second and third-year curriculum, skill-based laboratories and mini-projects are introduced.
- 3. It will result in the students developing a problem-solving approach and will be able to meet the challenges of the future.
- 4. The University of Mumbai and BoS Electronics and Telecommunication Engineering will ensure the revision of the curriculum on regular basis in the future as well and this update will certainly help students to achieve better employability; start-ups and other avenues for higher studies.

The BoS would like to thank all the subject experts, industry representatives, alumni, and various other stakeholders for their sincere efforts and valuable time in the preparation of course contents, reviewing the contents, giving valuable suggestions, and critically analyzing the contents.

Board of Studies in Electronics and Telecommunication Engineering

Dr. Faruk Kazi: Chairman

Dr. V. N. Pawar: Member

Dr. Ravindra Duche: Member

Dr. Milind Shah: Member

Dr. R. K. Kulkarni: Member

Dr. Baban U. Rindhe: Member

Dr. Mrs. Nair: Member

Dr. Nalbarwar: Member

Dr. Sudhakar Mande: Member

Dr. S. D. Deshmukh: Member

Program Structure for Third Year Engineering Semester V & VI

UNIVERSITY OF MUMBAI

(With Effect from 2021-2022)

Semester V

Course Code	Course Name		ching Sche ntact Hou		Credits Assigned			
Code		Theory	Pract.	Tut.	Theory	Pract.	Tut.	Total
ECC501	Digital Communication	3			3			3
ECC502	Discrete Time Signal Processing	3			3			3
ECC503	Digital VLSI	3			3			3
ECC504	Random Signal Analysis	3		1	3		1	4
ECCDLO 501X	Department Optional Course-1	3			3			3.
ECL501	Digital Communication Lab	1	2	1		1		1
ECL502	Discrete Time Signal Processing Lab	-	2	-		1		1
ECL503	Digital VLSI Lab		2			1		1
ECL504	Professional Communication & Ethics - II		2*+2~)	2
ECM501 Mini Project 2A- Embedded System Project			4\$	~		2		2
	Total		14	1	15	07	1	23

st Theory should be conducted for the full class.

Batch-wise practical's to be conducted
 Indicates work load of a learner (Not Faculty) for Mini Project 2A. Faculty Load: 1 hour per week per four groups.

		* (>	Examin	nation Schen	ne			
Course	G V			Theory						
Code	Course Name	Intern	al Assessi	nent	End	Exam.	Term Work	Pract. & oral	Total	
		Test 1	Test 2	Avg.	Sem. Exam	Duration (in Hrs)	WUIK	& orai		
ECC501	Digital Communication	20	20	20	80	3			100	
ECC502	Discrete Time Signal Processing	20	20	20	80	3			100	
ECC503	Digital VLSI	20	20	20	80	3			100	
ECC504	Random Signal Analysis	20	20	20	80	3	25		125	
ECCDLO 501X	Department Level Optional Course-1	20	20	20	80	3			100	
ECL501	Digital Communication Lab	1	1	1			25	25	50	
ECL502	Discrete Time Signal Processing Lab	-	-	-			25	25	50	
ECL503	Digital VLSI Lab						25	25	50	
ECL504	Business Communication and Ethics Lab						25	25	50	
ECM501	Mini Project 2A- Embedded System Project						25	25	50	
	Total			100	400		150	125	775	

Department Level Optional Course-1

Course Code	Department Level Optional Course-1
ECCDLO5011	Digital and IPTV Engineering
ECCDLO5012	Data Compression and Cryptography
ECCDLO5013	IT Infra and Security
ECCDLO5014	Data Structures and Algorithm
ECCDLO5015	Sensor Technology

Course Code	Course Name		eaching Schen Contact Hour			Credits As	signed	
		Theory	Practical	Tutorial	Theory	Practical	Tutorial	Total
ECC501	Digital communication	03			03			03

Course	Course				Examina	tion Scheme			
Code	Name		The	eory Mar	ks	Exam	Term	Practical	Total
		Internal Assessment			End Sem.	Duration	Work	and Oral	
		Test1	Test2	Avg.	Exam.	(Hrs.)			
ECC501	Digital								
	communi- cation	20	20	20	80	03		11	100

Course Pre-requisite:

ECC401 - Engineering Mathematics-IV

ECC404 - Signals and Systems

ECC405 - Principles of Communication Engineering

Course Objectives:

- 1. To describe the basics of information theory and source coding.
- 2. To illustrate various error control codes.
- 3. To describe baseband system.
- 4. To learn different digital modulation and demodulation techniques

Course Outcomes:

After successful completion of the course student will be able to:

- 1. Apply the concepts of information theory in source coding.
- 2. Compare different error control systems and apply various error detection codes.
- 3. Analyze different error correction codes.
- 4. Compare various baseband transmission methods for digital signals.
- 5. Evaluate the performance of optimum baseband detection in the presence of white noise.
- 6. Compare the performances of different digital modulation techniques

Module No.	Unit No.	Topics	Hrs.					
1.0	Information Theory and Source Codes							
	1.1	Block diagram of digital communication system, Information content of a source symbol, Source entropy, Average information rate, AWGN channel, and Shannon-Hartley channel capacity theorem.	03					
	1.2	Introduction of source code, Huffman code, Shannon-Fano code.	02					
2.0		Error Control System and Error Detection Codes	03					
	2.1	Introduction of error control system, Automatic Retransmission Query (ARQ) system, Types of ARQ systems and comparison, Forward error correction (FEC) system. Comparison between FEC and ARQ.	01					
	2.2	Error detection codes: Vertical Redundancy Check (VRC) code, Longitudinal Redundancy Check (VRC) code, Cyclic Redundancy Check (CRC) code and Checksum code.	02					
3.0		Error Correction Codes	10					
	3.1	Linear block code: Code generation, calculation of minimum Hamming distance, error detection capability, error correction capability, implementation of encoder, error detection, syndrome table, error correction and implementation of decoder.	03					
	3.2	Cyclic code: Code generation, calculation of minimum Hamming distance, error detection capability, error correction capability, implementation of encoder, error detection, syndrome table, error correction and implementation of decoder.	03					
	3.3	Convolutional code: Generation, path responses, encoder, state transition table, state diagram, tree diagram, trellis diagram, decoding using Viterbi's algorithm.	04					
4.0		Baseband Transmission	05					
	4.1	Block diagram of baseband transmitter-receiver system, Line codes (RZ and NRZ UniPolar formats, RZ and NRZ Polar formats, NRZ Bipolar format (AMI format), NRZ Manchester format, and Quaternary Polar format). Comparison of line codes with respect to bandwidth, power requirement, synchronization capability, DC level, polarity inversion error and complexity. Power spectral density and spectrum of NRZ Unipolar and Polar formats.	03					
	4.2	Inter Symbol Interference (ISI), Inter Channel Interference (ICI). Nyquist criterion for distortionless baseband binary transmission, Nyquist bandwidth and practical bandwidth.	02					
5.0		Optimum Detection of Baseband Signal	04					
7	5.1	Matched filter, Output SNR, Transfer function, Impulse response and Error probability. Integrate and dump receiver, Correlator receiver.	04					
6.0		Digital Modulations	12					
	6.1	Generation, Detection, Error probability (using signal space representation and Euclidean distance), Bandwidth (using PSD and spectrum except for MSK) and applications of the following modulations: Binary ASK, Binary PSK, Quadrature PSK, Off-Set QPSK, M-ary PSK, Binary FSK, M-ary FSK, 16-ary QASK and MSK.	12					
		Total	39					

- 1.H. Taub, D. Schlling, and G. Saha-Principles of Communication Systems, Tata Mc-Graw Hill, New Delhi, Third Edition, 2012.
- 2. Lathi B P, and Ding Z-Modern Digital and Analog Communication Systems, Oxford University Press, Fourth Edition, 2017.
- 3. Haykin Simon-Digital Communications, John Wiley and Sons, New Delhi, Fourth Edition, 2014.
- 4. John G. Proakis-Digital Communications, McGraw-Hill, Fourth Edition

Reference Books:

- 1. Sklar B, and Ray P. K.-Digital Communication: Fundamentals and applications, Pearson, Dorling Kindersley (India), Delhi, Second Edition, 2009.
- 2. T L Singal-Analog and Digital Communication, Tata Mc-Graw Hill, New Delhi, First Edition, 2012.
- 3. P Ramakrishna Rao-Digital Communication, Tata Mc-Graw Hill, New Delhi, First Edition, 2011.
- 4. K. Sam Shanmugam-Digital and analog communication Systems, John Wiley and sons.
- 5. Upamanyu Madhow- Fundamentals of Digital Communication- Cambridge University Press
- 6. W.C. Huffman, Vera Pless-Fundamentals of Error Correcting Codes, Cambridge University Press
- 7. Graham Wade-Coding Techniques, Palgrave, New York

NPTEL/Swavam Course:

- 1. https://nptel.ac.in/courses/108/101/108101113/
- 2. https://nptel.ac.in/courses/108/102/108102096
- 3. https://nptel.ac.in/courses/108/102/108102120

Internal Assessment (20-Marks):

Internal Assessment (IA) consists of two class tests of 20 marks each. IA-1 is to be conducted on approximately 40% of the syllabus completed and IA-2 will be based on remaining contents (approximately 40% syllabus but excluding contents covered in IA-I). Duration of each test shall be one hour, Average of the two tests will be considered as IA marks.

End Semester Examination (80-Marks):

- 1. Question paper will comprise of total 06 questions, each carrying 20 marks.
- 2. Question No: 01 will be compulsory and based on entire syllabus wherein 4 to 5 subquestions will be asked.
- 3. Remaining questions will be mixed in nature and randomly selected from all the modules.
- 4. Weightage of each module will be proportional to number of respective lecture hours as mentioned in the syllabus.
- 5. Total 04 questions need to be solved.

Course Code	Course Name		eaching Scher Contact Hour			Credits As	signed	
		Theory	Practical	Tutorial	Theory	Practical	Tutorial	Total
ECC502	Discrete-Time Signal Processing	03			03			03

Course	Course		Examination Scheme								
Code	Name		Theo	ry Mar	ks	Exam	Term	Practical	Total		
		Internal Assessment			End Sem.	Duration	Work	and Oral			
		Test1	Test2	Avg.	Exam.	(Hrs.)					
ECC502	Discrete- Time Signal Processing	20	20	20	80	03		1	100		

Course Pre-requisite:

ECC404 Signals & Systems

Course Objectives:

- 1. To develop a thorough understanding of discrete Fourier transform and its use in spectral analysis and frequency domain filter designing.
- 2. To design and realize IIR filters and FIR filters, gain an appreciation for the tradeoffs necessary in the filter design and to evaluate the effects of finite word lengths on the filters.
- 3. To introduce applications of digital signal processing in the field of biomedical and audio signal processing.

Course Outcomes:

After successful completion of the course student will be able to:

- 1. Recall the system representations and understand the relation between different transforms.
- 2. Understand the concepts of discrete-time Fourier transform, fast Fourier transform and apply in system analysis.
- 3. Design digital IIR and FIR filters to satisfy the given specifications and evaluate the frequency response and pole-zero representations to choose a particular filter for the given application.
- 4. Interpret the different realization structures of Digital IIR and FIR filters.
- 5. Analyze the impact of hardware limitations on the performance of digital filters.
- 6. Apply signal processing concepts, algorithms in applications related to the field of biomedical and audio signal processing.

Module No.	Unit No.	Topics	Hrs.
1.0		Discrete Fourier Transform & Fast Fourier Transform	08
	1.1	Discrete Fourier transform (DFT), DFT as a linear transformation, Properties of the DFT, Relationship of the DFT to other transforms, Filtering of long data sequences: Overlap-Save and Overlap-Add Method	05
	1.2	Fast Fourier Transform: Radix-2 Fast Fourier Transforms (FFT), Radix-2 decimation in time and decimation in frequency FFT algorithms, Inverse FFT	03
2.0		IIR Digital filters	08
	2.1	LTI systems as frequency-selective filters like low pass, high pass, band pass, notch, comb, all-pass filters, and digital resonators, Analog filter approximations: Butterworth, Chebyshev I, Elliptic	03
	2.2	Mapping from s-plane to the z-plane - impulse invariant and bilinear transformation, Design of IIR digital filters (Butterworth and Chebyshev-I) from analog filters using impulse invariant and bilinear transformation techniques, Analog and digital frequency transformations	05
3.0		FIR Digital Filters	09
	3.1	Characteristics of linear phase FIR digital filters, Symmetric and antisymmetric FIR filter, Location of the zeros of linear phase FIR filters, Minimum, maximum and mixed phase systems	04
	3.2	Design of FIR filters using Window techniques (Rectangular, Hamming, Hanning, Blackman, Bartlett), Design of FIR filters using Frequency Sampling Technique – Type I low pass filter design, Comparison of IIR and FIR filters	05
4.0		Digital Filter Structures	05
	4.1	Realization structures for FIR systems: Cascade form, Frequency sampling structure, Lattice structure, Computational complexities for N length filter	02
	4.2	Realization structures for IIR systems: Cascade form and parallel form structures, Lattice Ladder structure, Computational complexities for N order filter	03
5.0		Finite Word Length Effects in Digital Filters	05
4	4.1	Rounding and truncation errors, Quantization error, Output noise power from a digital system	02
	4.2	Product quantization, Noise model for direct form and cascaded IIR structure (first order), Coefficient quantization error and zero input limit cycle	03
6.0		Applications of Digital Signal Processing	04
	6.1	Application of DSP for ECG and EEG signals analysis.	02
*	6.2	Application of DSP for echo cancellation and sub-band coding of speech signal	02
		Total	39

- 1. Proakis J., Manolakis D., "Digital Signal Processing", 4th Edition, Pearson Education.
- 2. Emmanuel C. Ifeachor, Barrie W. Jervis," Digital Signal Processing", A Practical Approach", Pearson Education
- 3. A Nagoor Kani "Digital Signal Processing", 2nd Edition. Tata Mc Graw Hill Education Private Limited

Reference books

- 1. Sanjit K. Mitra, "Digital Signal Processing A Computer Based Approach ", 4th Edition McGraw Hill Education (India) Private Limited, 2013
- 2. Oppenheim A., Schafer R., Buck J., "Discrete Time Signal Processing", 2nd Edition, Pearson Education, 3rd Edition, 2010
- 3. L. R. Rabiner and B. Gold, "Theory and Applications of Digital Signal Processing", Prentice-Hall of India, 2006.
- 4. S Salivahan, C Gnanapriya, "Digital Signal Processing", Mc Graw Hill Education (India) limited, 4th Edition, 2015
- 5. Monson H Hayes, "Digital Signal Processing", Schaum's Outline Series, 2nd Edition, 2011
- 6. Rangaraj M. Rangayyan, "Biomedical Signal Analysis- A Case Study Approach", Wiley 2002.

NPTEL/Swayam Course:

- 1. Course: Digital Signal Processing By Prof. S.C Dutta Roy, IIT Delhi http://www.nptelvideos.in/2012/12/digital-signal-processing.html
- 2. Course: Digital Signal Processing By Prof. V. M. Gadre, IIT Bombay https://nptel.ac.in/courses/108/101/108101174/
- 3. Course: Digital Signal Processing By Prof. T. K. Basu, IIT Kharagpur https://nptel.ac.in/courses/108/105/108105055/

Internal Assessment (20-Marks):

Internal Assessment (IA) consists of two class tests of 20 marks each. IA-1 is to be conducted on approximately 40% of the syllabus and IA-2 will be based on remaining contents (approximately 40% syllabus but excluding contents covered in IA-I). Duration of each test shall be one hour. Average of the two tests will be considered as IA marks.

End Semester Examination (80-Marks):

- 1. Question paper will comprise of total 06 questions, each carrying 20 marks.
- 2. Question No: 01 will be compulsory and based on entire syllabus wherein 4 to 5 sub-questions will be asked.
- 3. Remaining questions will be mixed in nature and randomly selected from all the modules.
- 4. Total 04 questions need to be attempted.

Course	Course Name	Te	aching Schen	ne	Credits Assigned				
Code		(0	Contact Hours	s)					
		Theory	Theory Practical Tutorial			Practical	Tutorial	Total	
ECC503	Digital VLSI	03			03			03	

Course	Course		Examination Scheme									
Code	Name		The	eory Mar	ks	Exam	Term	Practical	Total			
		Internal Assessment			End Sem.	Duration	Work	and Oral				
		Test1	Test2	Avg.	Exam.	(Hrs.)						
ECC503	Digital											
	VLSI	20	20	20	80	03		(1)	100			

Course Pre-requisite:

ECC302 - Electronic Devices and Circuits

ECC303 – Digital System Design

ECC403 – Linear Integrated Circuits

Course Objectives:

- 1. To introduce process flow of VLSI Design.
- 2. To understand MOSFET operation from VLSI design perspective.
- 3. To learn VLSI design performance metric and various tradeoffs.
- 4. To design, implement and verify combinational and sequential logic circuits using various MOS design styles.
- 5. To provides an exposure to RTL design and programming

Course Outcomes:

After successful completion of the course student will be able to:

- Know various tools and processes used in VLSI Design.
 Explain working of various CMOS combinational and sequential circuits used in VLSI Design.
- 3. Derive expressions for performance parameters of basic building blocks like CMOS inverter.
- 4. Relate performance parameters with design parameters of VLSI circuits.
- 5. Select suitable circuit and design style for given application.
- 6. Design and realize various combinational and sequential circuits for given specifications.

Module No.	Unit No.	Topics	Hrs.
1.0		Review of MOSFET operation and Fabrication	08
	1.1	Overview of VLSI Design Flow, Review of MOSFET operation, MOSFET Capacitances, MOSFET scaling, Short channel effects	03
	1.2	Fabrication process flow of NMOS and CMOS, Lambda based design rules	03
	1.3	Novel MOSFET Architectures FinFET, GAA-FET, CNTFET	02
2.0		Combinational CMOS Logic Circuits	06
	2.1	CMOS inverter operation, Voltage Transfer characteristics (VTC), Noise Margins, Propagation Delay, Power Dissipation, Design of CMOS Inverter, Layout of CMOS Inverter	03
	2.2	Realization of CMOS NAND gate, NOR gate, Complex CMOS Logic Circuits, Layout of CMOS NAND, NOR and complex CMOS circuits	03
3.0		MOS Design Logic Styles	09
	3.1	Static CMOS, Pass Transistor Logic, Transmission Gate, Pseudo NMOS, Dynamic Logic, Domino Logic, NORA, Zipper, C ² MOS	04
	3.2	Setup time, Hold time, clocked CMOS SR Latch, CMOS JK Latch, MS –JK Flip Flop, Edge triggered D-Flip Flop and realization using design styles	03
	3.3	Realization of Shift Register, MUX, Decoder using above design styles ,1-bit full adder	02
4.0		Semiconductor Memories	06
	4.1	ROM array, 6T-SRAM (operation, design strategy, leakage currents, sense amplifier), layout of SRAM	03
	4.2	Operation of 1T and 3T DRAM Cell, NAND and NOR flash memory	03
5.0		Data path and system design issues	06
	5.1	Ripple carry adder, CLA adder, carry save adder, carry select adder, carry skip adder, Array Multiplier	04
	5.2	On chip clock generation and distribution, Interconnect delay model, interconnect scaling and crosstalk	02
6.0		RTL Design	04
1	6.1	High Level state machines, RTL design process	02
	6.2	RTL design of Soda dispenser machine, FIR Filter	02
		Total	39

- 1. Sung-Mo Kang and Yusuf Leblebici, "CMOS Digital Integrated Circuits Analysis and Design", Tata McGraw Hill, 3rd Edition, 2012.
- 2. Jan M. Rabaey, Anantha Chandrakasan and Borivoje Nikolic, "*Digital Integrated Circuits: A Design Perspective*", Pearson Education, 2nd Edition.
- 3. Frank Vahid, "Digital Design with RTL design, VHDL and VERILOG", John Wiley and Sons Publisher 2011.

Reference Books:

- 1. Neil H. E. Weste, David Harris and Ayan Banerjee, —*CMOS VLSI Design: A Circuits and Systems Perspective*, Pearson Education, 3rd Edition.
- 2. John P. Uyemura, "Introduction to VLSI Circuits and Systems", Wiley, Student Edition, 2013.
- 3. R. Jacob Baker, "CMOS Circuit Design, Layout and Simulation", Wiley, 2nd Edition, 2013

NPTEL/Swayam Course:

- **1.** https://nptel.ac.in/courses/117/101/117101058/
- 2. https://nptel.ac.in/courses/108/107/108107129/

Internal Assessment (20-Marks):

Internal Assessment (IA) consists of two class tests of 20 marks each. IA-1 is to be conducted on completion of approximately 40% of the syllabus and IA-2 will be based on remaining contents (approximately 40% syllabus but excluding contents covered in IA-I). Duration of each test shall be one hour. Average of the two tests will be considered as IA marks.

End Semester Examination (80-Marks):

- 1. Question paper will comprise of total 06 questions, each carrying 20 marks.
- 2. **Question No: 01** will be **compulsory** and based on entire syllabus wherein 4 to 5 subquestions will be asked.
- 3. Remaining questions will be mixed in nature and randomly selected from all the modules.
- 4. Weightage of each module will be proportional to number of respective lecture hours as mentioned in the syllabus.
- 5. Total 04 questions need to be solved.

Course Code	Course Name		eaching Scher Contact Hour		Credits Assigned				
		Theory	Practical	Tutorial	Theory	Practical	Tutorial	Total	
ECC504	Random Signal Analysis	03		01	03		01	04	

Course	Course				Examina	tion Scheme			
Code	Name	Theory Marl			ks	Exam	Term	Practical	Total
		Internal Assessment		End Sem.	Duration	Work	and Oral		
		Test1	Test2	Avg.	Exam.	(Hrs.)			
ECC504	Random								
	Signal	20	20	20	80	03	25		125
	Analysis								

Course Pre-requisite:

ECC401- Engineering Mathematics IV

ECC404 - Signals and Systems

Course Objectives:

- 1. To strengthen the foundations of probability
- 2. To teach continuous and discrete random variables.
- 3. To explain statistical behavior of one dimensional and two dimensional random variables.
- 4. To describe the concept of random process which is essential for random signals and systems encountered in Communications and statistical learning.
- 5. To develop problem solving skills and explain how to make the transition from a real world problem to a probabilistic model.

Course Outcomes:

After successful completion of the course student will be able to:

- 1. Apply theory of probability in identifying and solving relevant problems.
- 2. Differentiate continuous and discrete random variables and their distributions.
- 3. Analyze mean, variance, and distribution function of random variables and functions of random variables.
- 4. Define a random process, determine the type of the process and find the response of LTI system for WSS process.
- 5. Explain linear regression algorithms and apply for predictive applications.

Module No.	Unit No.	Topics	Hrs.
1.0		Basic Concepts in Probability	04
	1.1	Definitions of probability, joint, conditional, and total probability, Bayes' theorem, independence of events, binary symmetric communication channel analysis using Bayes' theorem.	
2.0		Introduction to Random Variables	08
	2.1	Continuous, discrete, and mixed random variables, probability density function, probability distribution function, and probability mass function, properties of PDF and CDF	
	2.2	Special distributions- Binomial, Poisson, Uniform, Gaussian and Rayleigh Distributions Mean, variance and moments of random variables	
3.0		Operations on One Random Variable	08
	3.1	Function of a random variable and their distribution and density functions.	
	3.2	Expectation, variance, moments, and characteristic function of random variable.	
	3.3	Transformation of a random variable, Markov and Chebyshev inequality, characteristic functions, moment theorem.	
4.0		Multiple Random Variables and Convergence	08
	4.1	Pairs of random variables, joint CDF and joint PDF.	
	4.2	One function of two random variables; joint moments, covariance and correlation-independent, uncorrelated and orthogonal random variables.	
	4.3	Central limit theorem and its significance	
5.0		Random Processes	06
	5.1	Definitions, statistics of stochastic processes, n^{th} order distribution, second-order properties: mean and autocorrelation, Poisson process, normal processes, SSS, WSS.	
	5.2	Mean and correlation ergodic processes, transmission of WSS through LTI system, introduction to Markov process.	
6.0		Introduction to Statistical Learning and Applications	05
4	6.1	Regression and model building, simple linear regression, multiple linear regression, least square estimation of the coefficients, residual calculations.	
	6.2	Applications of simple linear regression in prediction of new observations.	
2		Total	39

- 1. T. Veerarajan, "Probability, Statistics and Random Process", Tata McGraw Hill Education, Third Edition (2018).
- 2. Athanasios Papoulis and S. Unnikrishna Pillai, "Probability, Random Variables, and Stochastic Processes", Tata McGraw Hill Education
- 3. Henry Stark & John Woods, "Probability, Statistics, and Random Processes for Engineers, 4th Edition, Pearson Education, 2012

4. Douglas C. Montgomery, Elizabeth A. Peck and G. Geoffrey Vining, "Introduction to linear regression Analysis", student edition, Wiley publications.

Reference Books

- 1. Scott Miller and Donald Childers, "Probability and Random Processes with Applications to Signal Processing and Communications", Elsevier Publication.
- 2. Hwei Hsu, "Theory and Problems of Probability, Random Variables, and Random Processes", Schaum's Outline Series, McGraw Hill, 1997.
- 3. P. Ramesh Babu, "Probability Theory and Random Process", Tata McGraw Hill Education.
- 4. Alberto Leon Garcia, "Probability and Random Processes for Electrical Engineering", second edition, Pearson education.
- 5. Daniela Witten, Trevor Hastie, Robert Tibshirani, "An Introduction to Statistical Learning by Gareth James", 7th Edition, Springer 2017.
- 6. Ronald Walpole, et. al., "Probability and Statistics for Engineers and Scientists", 8th edition, Pearson Education.
- 7. P. Kousalya, "Probability, Statistics, and Random Processes", Pearson Education.

NPTEL/Swayam Course:

- 1. Introduction to probability and Statistics, Prof. G. Srinivasan (IIT Madras); https://onlinecourses.nptel.ac.in/noc21 ma01/preview
- 2. Probability and Probability Distributions By Dr. P.Nagesh: https://onlinecourses.swayam2.ac.in/cec21 ma02/preview

Internal Assessment (20-Marks):

Internal Assessment (IA) consists of two class tests of 20 marks each. IA-1 is to be conducted on approximately 40% of the syllabus completed and IA-2 will be based on remaining contents (approximately 40% syllabus but excluding contents covered in IA-I). Duration of each test shall be one hour. Average of the two tests will be considered as IA marks.

End Semester Examination (80-Marks):

Weightage to each of the modules in end-semester examination will be proportional to number of respective lecture hours mentioned in the curriculum.

- 1. Question paper will comprise of total 06 questions, each carrying 20 marks.
- 2. Question No: 01 will be compulsory and based on entire syllabus wherein 4 to 5 subquestions will be asked.
- 3. Remaining questions will be mixed in nature and randomly selected from all the modules.
- 4. Weightage of each module will be proportional to number of respective lecture hours as mentioned in the syllabus.
- 5. **Total 04 questions** need to be solved.

Term Work (25-Marks):

At least 08 Tutorials covering entire syllabus must be given during the "Class Wise Tutorial". Term work assessment must be based on the overall performance of the student with every tutorial graded from time to time. The grades will be converted to marks as per "Credit and Grading System" manual and should be added and averaged. Based on above scheme grading and term work assessment should be done.

Course Code	Course Name		eaching Scher Contact Hour		Credits Assigned				
		Theory	Practical	Tutorial	Theory	Practical	Tutorial	Total	
ECCDLO	Digital and IP								
5011	TV	03			03			03	
	Engineering								

	Subject Name		Examination Scheme									
Subject Code		Theory Marks Internal assessment			End	Exam Duration	Term Practical		Total			
		Test1	Test 2	Avg.	Sem. Exam	(Hrs.)	work	and Oral	Total			
ECCDLO 5011	Digital and IP TV Engineering	20	20	20	80	03		-	100			

Prerequisite:

- 1. Basics of various Television standards and operation
- 2. TCP/IP Protocol
- 3. Basics of conventional video camera and standards

Course Objectives:

- 1. To provide in depth knowledge about Digital Television system
- 2. To familiarize students' various types of advanced types of Video cameras and Displays
- 3. To introduce the students to different television standards and applications
- 4. Acquaintance with HDTV and 3D TV system
- 5. To familiarize the students to IPTV, Its architecture, Protocols and hardware
- 6. To Introduce students to IP delivery networks, threats and mitigation

Course Outcomes:

After successful completion of the course student will be able to:

- 1) Understand the working principles of advanced digital television systems.
- 2) Enable to choose or develop an appropriate camcorder and displays based on applications.
- 3) Familiar with current digital TV standards.
- 4) Evaluate the Stereoscopic images and binocular depth perception.
- 5) Acquire knowledge of IPTV and develop hardware and protocols.
- 6) Ability to provide customized IPTV services to end user.

Module No	Unit No	Topics	Hrs
1		Fundamentals of Digital Television	7
	1.1	Fundamentals of colour television, Compatibility, and reverse	
		compatibility, colour perception, Three colour theory, luminance, hue	
		and saturation. Interlaced scanning, Composite video signal	
	1.1	Introduction to Digital TV, Digital TV signals and parameters	
	1.2	Digital TV transmitter and Receiver its merits and demerits	
	1.3	MAC Signals and advanced MAC Signal Transmission	
	1.4	Digitization, Chroma sub sampling, Digital audio compression	
		techniques and video compression techniques	
		MPEG1,MPEG2,H.264,MPEG- 4,AVC,H.265, SMPTE 421M,	
	1.5	Set Top Box with recording	
2		Digital Video Cameras, Displays and Streaming media device	5
	2.1	Colour TV Digital cameras, Camcorders, Handycams, and Digicams	
	2.2	LED, LCD, OLED, PLASMA,	
		Quantum Dot LED Displays	
	2.3	Chromecast	
	2.4	Consumer applications: DVD, Blue ray DVD	
3		Digital TV standards and advanced TV	8
	3.1	DVB-T, and its successors	
	3.2	ISDB -T	
	3.3	ATSC	
	3.4	ISD TV	
	3.5	DTMB	
	3.6	Ultra HDTV	
	3.7	CCTV	
	3.8	Direct to Home TV(DTH)	
	3.9	Smart TV and its functions	
	3.10	3D TV	
4		IPTV	6
-	4.1	Introduction to IPTV	
	4.2	IP TV hardware	
	4.3	Features of IPTV	
	4.4	Architecture of IPTV	
	4.5	Bandwidth requirement	
▼	4.6	IPTV Set top Box, Smart TV comparison	
5		IP TV Protocols and Applications	9
	5.1	Internet Group Management Protocol (IGMP)	
	5.2	Real-Time Streaming Protocol (RTSP)	
	5.3	Real-Time Messaging Protocol (RTMP)	
	5.4	Hypertext Transfer Protocol (HTTP).	
	5.5	Applications of IPTV	

	5.6	IPTV Delivery: Broad cast. Unicast, Multicast
	5.7	IPTV Streaming: Time Shifted Stream-On -the- fly streaming
	5.8	experimental framework used for evaluating the classification
		algorithm
	5.9	Experimental framework for evaluating the classification algorithm
		(Self learning)
		Configuring IPTV to android phone, Tablet, Television and
		Computer(Self Learning)
6		IPTV Network Security: Threats and Countermeasures 4
	6.1	Threats on IPTV Delivery Networks, Theft or Abuse of Network
		Assets, Theft of Service, Theft of IPTV-Related Data, Disruption of
		Service, Privacy Breach, Compromise of Platform Integrity
	6.2	Security Issues of IPTV Delivery Networks: Protocols
		Vulnerabilities, Countering the threats
	6.3	Advantages and disadvantages of IPTV
	6.4	Future of IPTV
		Total 39

Textbooks:

- 1. Television and video Engineering, A. M. Dhake, Tata McGraw Hill Publication.
- 2. Video Demystified, Kelth jack, Hand book for digital engineers, Newness, Elsevier
- 3. Digital Television Systems. Marcelo S. Alencar, Cambridge University Press
- 4. Understanding IPTV, Gilbert Held, CRC Press

Reference Books:

- 1. The digital evolution of Television, D. Gerbarg, Springer
- 2. Applications and Usability of interactive TV, Maris Jos Abisolo, Springer
- 3. IPTV Delivery network, Suliman Mohamed Fati, Saiful Azad, Al-Sakib Khan Pathan, Wiley Publications
- 4. Television Engineering & Video Systems, R. G. Gupta, McGraw Hill Publication
- 5. Quantum dot based light emitting diodes, Morteza Sasani Ghamsari, Google book

Internal Assessment (20-Marks):

Internal Assessment (IA) consists of two class tests of 20 marks each. IA-1 is to be conducted on approximately 40% of the syllabus completed and IA-2 will be based on remaining contents (approximately 40% syllabus but excluding contents covered in IA-I). Duration of each test shall be one hour. Average of the two tests will be considered as IA marks.

End Semester Examination (80-Marks):

- 1. Question paper will comprise of total 06 questions, each carrying 20 marks.
- 2. **Question No: 01** will be **compulsory** and based on entire syllabus wherein 4 to 5 subquestions will be asked.
- 3. Remaining questions will be mixed in nature and randomly selected from all the modules.
- 4. Weightage of each module will be proportional to number of respective lecture hours as mentioned in the syllabus.
- 5. **Total 04 questions** need to be solved.



Course Code	Course Name	Teaching Scheme (Hrs.)			Credits Assigned				
		Theory	Practical	Tutorial	Theory	Practical	Tutorial	Total	
ECCDL O5012	Data Compression and Cryptography	03			03			03	

Course	Course Name		Examination Scheme							
Code			The	eory Marks		Exam.	Term	Practical	Total	
		In	Internal assessment End				Work	and Oral		
		Test 1	Test	Avg. Of	Sem.	(in Hrs)				
			2	Test 1 and	Exam					
				Test 2						
ECCDL	Data	20	20	20	80	03			100	
O5012	Compression and									
	Cryptography									

Course Objectives:

- 1. Gain a fundamental understanding of data compression methods for text, images, video and audio.
- 2. Understand the concepts of cryptography and different algorithms to provide system security.

Course Outcomes:

After successful completion of the course student will be able to

- 1. Apply various compression techniques for text and understand image compression and its standards.
- 2. Select suitable compression techniques for specified lossless and lossy audio and video applications.
- 3. Compare between symmetric and asymmetric cryptography and also describe different symmetric cryptographic techniques and standards.
- 4. Apply number theory concepts to solve the cryptographic problems.
- 5. Analyze different public key cryptography algorithms and also describe methods that provide the goals for integrity, confidentiality and authentication.
- 6. Describe system security facilities designed to protect a computer system from security threats and also appreciate ethical issues related to system security.

1.1	Introduction to Data Compression Data compression, modelling and coding, Lossless and Lossy Compression, Arithmetic	06
1.1	•	
		00
	Coding – Decoding, Dictionary Based Compression, Sliding Window Compression:	
	LZ-77, LZ-78, LZW.	
1.2	Image Compression	
	DCT, JPEG, JPEG – LS, Differential Lossless Compression, DPCM, JPEG – 2000	
		0.0
2.1		06
2.1		
2 2		
4.4		
		10
3.1		10
J.J		04
<u> </u>		04
4.1		
4.2	Chinese Remainder Theorem	
	Asymmetric Key Cryptography	09
5.1	Principles of Public Key Crypto System, RSA, Key Management, Deffie-Hellman Key	
	C S S S S S S S S S S S S S S S S S S S	
5.2		
		0.4
6 1	· · · · · · · · · · · · · · · · · · ·	04
U. 2		39
	3.2 3.3 4.1 4.2	Standards. Video and Audio Compression Video compression: Motion compensation, temporal and spatial prediction, MPEG-4, H.264 encoder and decoder. Sound, Digital Audio, µ-Law and A-Law Companding, MPEG –4 Audio Layer, Advanced Audio Coding (AAC) standard. Data Security Security Goals, Cryptographic Attacks and Techniques Symmetric Key: Substitution Cipher, Transposition Cipher, Stream and Block Cipher DES, double DES and triple DES, AES Number Theory 1.1 Prime Numbers, Fermat's and Euler's Theorem. Asymmetric Key Cryptography 5.1 Principles of Public Key Crypto System, RSA, Key Management, Deffie-Hellman Key Exchange. Message Integrity, Message Authentication and Hash Functions, SHA, HMAC, Digital Signature Standards. System Security 6.1 Intrusion Detection System, Secure Electronic Transactions.

Textbooks:

- 1. Khalid Sayood, 3rd Edition, Introduction to Data Compression, Morgan Kauffman
- 2. Mark Nelson, Jean-Loup Gailly, The Data Compression Book, 2nd edition, BPB Publications
- 3. William Stallings ,|Cryptography and Network Security Principles and Practices 5th Edition|, Pearson Education.
- 4. Behrouz A. Forouzan, |Cryptography and Network Security|, Tata McGraw-Hill.

Reference Books:

- 1. 1. David Salomon, Data Compression: The Complete Referencell, Springer.
- 2. Matt Bishop, |Computer Security Art and Science||, Addison-Wesley.
- 3. Bernard Menesez, Network Security and Cryptography Delmar Cengage Learning, 7th Edition.

Internal Assessment (20-Marks):

Internal Assessment (IA) consists of two class tests of 20 marks each. IA-1 is to be conducted on approximately 40% of the syllabus completed and IA-2 will be based on remaining contents (approximately 40% syllabus but excluding contents covered in IA-I). Duration of each test shall be one hour. Average of the two tests will be considered as IA marks.

End Semester Examination (80-Marks):

- 1. Question paper will comprise of total 06 questions, each carrying 20 marks.
- 2. **Question No: 01** will be **compulsory** and based on entire syllabus wherein 4 to 5 subquestions will be asked.
- 3. Remaining questions will be mixed in nature and randomly selected from all the modules.
- 4. Weightage of each module will be proportional to number of respective lecture hours as mentioned in the syllabus.
- 5. Total 04 questions need to be solved.

Subject Code	Subject Name	Т	Ceaching Sche (Hrs.)	me	Credits Assigned			
		Theory	Practical	Tutorial	Theory	Practical	Tutorial	Total
ECCDLO 5013	IT Infra & Security	03			03			03

Course	Course		Examination Scheme							
Code	Name		Theo	ry Marl	ks	Exam	Term	Practical	Total	
		Internal Assessment			End Sem.	Duration	Work	and Oral		
		Test1	Test2	Avg.	Exam.	(Hrs.)				
ECCDLO 5013	IT Infra & Security	20	20	20	80	03		7-	100	

Course prerequisite:

• Principles of Communication

Course Objectives:

- 1. To introduce basic fundamentals of IT Infrastructure and its Management.
- 2. To develop underlying principles of infrastructure security.
- 3. To explore software vulnerabilities and attacks.
- 4. To introduce the protection mechanisms for operating systems and database security.
- 5. To explore the security aspects of wireless network infrastructure and protocols.
- 6. To investigate the different attacks on Web Applications and Web services.

Course Outcomes: Students will be able to:

- 1. Understand IT Infrastructure and its Management.
- 2. Understand the concept of Information securities.
- 3. Summarize the concepts of vulnerabilities, attacks and protection mechanisms.
- 4. Analyze software vulnerabilities and attacks on databases and operating systems.
- 5. Explain the need for security protocols in the context of wireless communication.
- 6. Analyze the different attacks on Open Web Applications and Web services.

Module No.	Unit No.	Topics	Hrs
1.0		Overview of Networks and IT Infrastructure	09
	1.1	Overview of OSI and TCP/ IP Networks, introduction to IP Addressing scheme, introduction to Networking Components	
	1.2	Information Technology, Design Issues of IT Organizations and IT Infrastructure, Information System Design Process, IT Infrastructure Management, Challenges in IT Infrastructure Management, Determining Customers, Requirements, Security controls and safeguards, IT security Plans.	
2.0		Introduction to Information Security	06
		Cyber-attacks, Vulnerabilities, Defense Strategies and Techniques, Authentication Methods- Password, Token and Biometric, Access Control Policies and Models (DAC, MAC, RBAC, BIBA, Bell La Padula), Authentication and Access Control Services- RADIUS, TACACS, and TACACS+	
3.0		Software Vulnerabilities	04
		Buffer overflow, Format String, Cross-Site Scripting, SQL Injection, Malware: Viruses, Worms, Trojans, Logic Bomb, Bots, Rootkits	
4.0		Operating System and Database Security	08
	4.1	Introduction operating system security, system security planning, Application security, Linux/ Unix security, Windows, security, Security Maintenance,	
	4.2	Database Security Requirements, Reliability and Integrity, Sensitive Data, Inference Attacks, Multilevel Database Security	
5.0		Wireless Security	05
~	5	The need for Wireless Network Security, Attacks on Wireless Networks, Security services, WEP & WPA protocols, Mobile IP, Virtual Private Network (VPN): PPTP, L2TP, IPSec	
6.0		Web Security	07
		Introduction: Transport Protocol and Data Formats, Web Browser, Threat Model Authenticated Sessions: Cookie Poisoning, Cookies and Privacy, Making Ends Meet Code Origin Policies, Cross-Site Scripting: Cookie Stealing, Defending against XSS, Cross-Site Request Forgery, JavaScript Hijacking	
		Total	39

- 1. Gupta, "IT Infrastructure & Its Management", First Edition, Tata McGraw-Hill Education.
- 2. Computer Security Principles and Practice, William Stallings, Sixth Edition, Pearson Education
- 3. Computer Security, Dieter Gollmann, Third Edition, Wiley Publications.
- 4 Data Communications and Networking, Forouzan, Fourth Edition, Mc Graw Hill Publication
- 5 Wireless Networks, P. Nicopolitidis, M.S. Obaidat, G.I Papadimitriou, A.S Pomportsis, Wiley Publications

Reference Books:

- 1. Security in Computing, Charles P. Pfleeger, Fifth Edition, Pearson Education
- 2. CCNA Security Study Guide, Tim Boyle, Wiley Publications
- 3. Introduction to Computer Security, Matt Bishop, Pearson.

Internal Assessment (20-Marks):

Internal Assessment (IA) consists of two class tests of 20 marks each. IA-1 is to be conducted on approximately 40% of the syllabus and IA-2 will be based on remaining contents (approximately 40% syllabus but excluding contents covered in IA-I). Duration of each test shall be one hour. Average of the two tests will be considered as IA marks.

End Semester Examination (80-Marks):

- 1. Question paper will comprise of total 06 questions, each carrying 20 marks.
- 2. Question No: 01 will be compulsory and based on entire syllabus wherein 4 to 5 sub-questions will be asked.
- 3. Remaining questions will be mixed in nature and randomly selected from all the modules.
- 4. Total 04 questions need to be attempted.

Subject Code	Subject Name	Т	eaching Sche (Hrs.)	me	Credits Assigned			
		Theory	Practical	Tutorial	Theory	Practical	Tutorial	Total
ECCDLO	Data Structure	03			03			03
5014	& Algorithm							

Course	Course		Examination Scheme							
Code	Name	Theory Marl			ks	Exam	Term	Practical	Total	
		Intern	Internal Assessment		End Sem.	Duration	Work	and Oral		
		Test1	Test2	Avg.	Exam.	(Hrs.)				
ECCDLO	Data									
5014	Structure &	20	20	20	80	03			100	
3014	Algorithm									

Course pre-requisite:

ECL404 Skill Lab: Python Programming

Course Objectives:

The course aims:

- 1. To Introduce the fundamental knowledge & need of Data Structures.
- 2. To Abstract the concept of Algorithm and these concepts are useful in problem solving.
- 3. To Implement fundamental knowledge and applications of Stack, Queue, Linked List, Trees, Graphs etc.
- 4. To Understand the working of different Sorting, Searching & Hashing techniques.
- 5. To understanding about writing algorithms and step by step approach in solving problems with the help of fundamental data structures.

Course Outcome:

After successful completion of the course the student will:

- 1. Compare functions using asymptotic analysis and describe the relative merits of worst-, average-, and best-case analysis.
- 2. Apply various operations on Stack and Queue.
- 3. Ability to demonstrate the operation of Linked list.
- 4. Ability to demonstrate and apply Trees & Graph data structures.
- 5. Become familiar with various Sorting and Searching Algorithms and their performance characteristics.
- 6. Describe the hash function and concepts of collision and its resolution methods

Module No.	Unit No.	Topics	Hrs.
		Prerequisite: Control Structures, Arrays, Recursion, Pointers, Structures, Memory Allocation Techniques, Self-referential structures.	
1.0		Introduction to Data Structure & Algorithm	5
	1.1	Introduction to Data Structures, Concept of ADT, Types of Data Structures- Linear and Nonlinear, Operations on Data Structures.	
	1.2	Algorithm: Performance characteristics of algorithm, Importance of Algorithm Analysis, Complexity of an Algorithm, Introduction to Asymptotic Analysis and Notations.	
2.0		Stack & Queue	8
	2.1	Introduction to Stack, ADT of Stack, Operations on Stack, Array Implementation of Stack	
	2.2	Applications of Stack- Infix to Postfix Expression Conversion, Infix Expression to Prefix Expression Conversion, Postfix Expression Evaluation	
	2.3	Introduction to Queue, ADT of Queue, Operations on Queue, Array Implementation of Queue, Types of Queue-Circular Queue, Priority Queue, Introduction to Double Ended Queue	
	2.4	Applications of various types of Queue	
		Self-Learning Topic: Well form-ness of Parenthesis using Stack	
3.0		Linked List	7
	3.1	Introduction, Linked List v/s Array, Representation of Linked List, Types of Linked List - Singly Linked List, Doubly Linked List	
	3.2	Operations on Singly Linked List and Doubly Linked List	
	3.3	Singly Linked List Application-Polynomial Representation and Addition, Doubly Linked List Application	
		Self-Learning Topic: Stack and Queue using Singly Linked List	
4.0		Trees & Graph	9
	4.1	Introduction, Tree Terminologies, Binary Tree, Binary Tree Representation, Types of Binary Tree, Binary Tree Traversals, Binary Search Tree, Operations on Binary Search Tree,	
<	4.2	Applications of Binary Tree- Expression Tree, Huffman Encoding.	
	4.3	Graph: Introduction, Graph Terminology, Memory Representation of Graph, Operations Performed on Graph.	
	4.4	Graph Traversal, Breadth First Search, Depth First Search, Applications of the Graph, Shortest Path, Minimum Spanning Tree.	
5.0		Searching & Sorting	6
	5.1	Searching: Sequential Search, Index Sequential Search, Binary Search	
	5.2	Sorting: Bubble Sort, Quick Sort, Merge Sort	
		Self-Learning Topic: Selection Sort, Insertion Sort	
6.0		Hashing	4
	6.1	Hashing-Concept, Hash Functions, Common hashing functions	
	6.2	Collision resolution Techniques	
		Total	39

- 1. Jean Paul Tremblay, P. G. Sorenson, "Introduction to Data Structure and its Applications", McGraw-Hill Higher Education
- 2. "Fundamentals of Computer Algorithms" Ellis Horowitz, Sartaj Sahani and Sanguthevar Rajasekaran, Second Edition, Universities Press (India) Pvt. Ltd.
- 3. "Learning with Python" Allen Downey, Jeffrey Elkner, Chris Meyers, Dreamtech Press

Reference Books:

- 1. Jean Paul Tremblay, Paul G. Sorenson; An introduction to data structures with applications; Tata McGrawHill; 1984
- 2. Sanjoy Dasgupta, Christos Papadimitriou, Umesh Vazirani, "Algorithms", Tata McGrawHill Edition.

Internal Assessment (20-Marks):

Internal Assessment (IA) consists of two class tests of 20 marks each IA-1 is to be conducted on approximately 40% of the syllabus completed and IA-2 will be based on remaining contents (approximately 40% syllabus but excluding contents covered in IA-1). Duration of each test shall be one hour. Average of the two tests will be considered as IA marks.

End Semester Examination (80-Marks):

- 1. Question paper will comprise of total 06 questions, each carrying 20 marks.
- 2. **Question No: 01** will be **compulsory** and based on entire syllabus wherein 4 to 5 subquestions will be asked.
- 3. Remaining questions will be mixed in nature and randomly selected from all the modules.
- 4. Weightage of each module will be proportional to number of respective lecture hours as mentioned in the syllabus.
- 5. Total 04 questions need to be solved.

Subject	Subject Name	Tea	aching Schem	ie	Credits Assigned				
Code			(Hrs.)						
		Theory	Practical	Tutorial	Theory	Practical	Tutorial	Total	
ECCDLO	Sensor	03			03			03	
5015	Technology								

Subject	Subject Name		Examination Scheme							
Code			Th	eory Marks		Exam	Term	Practical	Total	
		Internal assessment			End	Duration	Work	and Oral		
		Test 1	Test	Avg. of Test	Sem.	(in Hrs.)				
			2	1 and Test 2	Exam					
ECCDLO	Sensor	20	20	20	80	03			100	
5015	Technology									

Course Pre-requisite:

- 1. FEC202 Engineering Physics-II
- 2. ECC302 -- Electronic Devices & Circuits
- 3. ECC403 Linear Integrated Circuits

Course Objectives:

- 1. To understand various physical parameters and its sensing techniques
- 2. To familiarize about MEMS sensors and Actuators
- 3. To introduce wireless sensing technologies
- 4. To develop understanding about signal conditioning using ADC and DAC
- 5. To provide insight into various sensor applications

Course Outcome:

After successful completion of the course student will be able to

- 1. Understand the transduction principal of various sensors.
- 2. Select sensors suitable for required application
- 3. Analyze wireless sensing techniques
- 4. Design the data acquisition system
- 5. Identify signal conditioning method for particular application
- 6. Create an application using various sensor technologies

Module No.	Unit No.	Topics	Hrs.
1.0		Introduction	03
	1.1	Classification of Sensors : The sensors are classified with criteria like primary physical quantity to be sensed, transduction principle, material and technology used and application	
	1.2	Criteria to choose a Sensor: Accuracy, Environmental condition, Range, Calibration, Resolution, Cost and Repeatability	
	1.3	Digital sensors : Principle and its advantage over analog sensors	
	1.4	Smart Sensors: Low-power, Self –diagnostic and Self- calibration	
2.0		Types of Sensors	09
	2.1	Temperature Sensors: RTD, Thermocouple and Thermistors sensor	
	2.2	Proximity Sensors : Inductive (LVDT), Capacitive, Photoelectric and Ultrasonic sensors	
	2.3	Chemical Sensors: Gas, Smoke, Conductivity and pH sensor	
	2.4	Other Sensors: Optical, Infrared (IR), Sound, Motion, Pressure, Level, Moisture, Humidity, Laser, Image and GPS sensor	
3.0		MEMS Sensors and Actuators	06
	3.1	MEMS SENSORS: General design methodology, techniques for sensing, Pressure sensor, Mass Flow sensor, Acceleration sensor, Angular Rate sensor and Gyroscopes, Micro machined microphones, Chemical sensors, Taguchi Gas sensor, Combustible Gas sensors	
	3.2	MEMS ACTUATORS: Techniques for actuation, Digital Micro mirror Device, Micro Machined Valves	
4.0		Wireless Sensing Technologies	05
	4.1	Bluetooth: Concepts of Pico net, Scatter net, Link types, Network connection establishments	
	4.2	ZigBee: components, architecture, network topologies	
	4.3	Ultra Wide Band (UWB), Near Field Communication (NFC) and RFID: technical requirements, components and characteristics	
	4.4	WLAN (WiFi): WLAN Equipment, WLAN topologies, IEEE 802.11 Architecture	
5.0		Data Acquisition and Signal Conditioning	08
	5.1	Fundamentals of Data Acquisition: Analog and Digital data acquisition system with different configurations. Data loggers, Noise and interference	
	5.2	Signal Conditioning: Wheatstone Bridge, Flash ADC, R2R DAC	
	5.3	Utilization of Signal conditioning circuits for Temperature, Pressure, Optical, Strain gauges, Displacement and piezoelectric Transducers	
6.0	4	Sensor Applications	08
	6.1	Onboard Automobile sensing system, Home appliances sensors, Aerospace Sensors, Sensors for Environmental Monitoring, Biomedical Sensing Applications	
	6.2	Radio sensors for industrial applications, Radio Astronomy, Remote Sensing, Ground Penetrating Radars, Underwater sensing, LIDAR	
		Total	39

Textbooks:

- 1. D.V.S. Murthy, "Transducers and Instrumentation", PHI Learning, 2nd Edition, 2013.
- 2. D. Patranabis Sensor and Transducers (2e) Prentice Hall, New Delhi, 2003
- 3. Antti V. Raisanen, Arto Lehto, "Radio Engineering for Wireless Communication and Sensor Applications", Artech House mobile communications series, USA, 2003.

- 4. Sensors and Signal Conditioning, Ramon Pallas Areny, John G. Webster, 2nd edition, John Wiley and Sons, 2000.
- 5. Vijay K. Garg, "Wireless Communication and Networking", Morgan -Kaufmann Series in Networking, Elsevier, 2010.

Reference Books:

- **1.** An Introduction to Microelectromechanical Systems Engineering, Nadim Maluf, <u>Kirt</u> Williams, Artech House, 2004.
- 2. Micro Electro Mechanical System Design, James J. Allen, Taylor and Francis, 2005
- **3.** A.K. Sawhney, "A Course in Electrical and ElectronicMeasurements and Instrumentation", Dhanpatrai & Co., 19th Edition, 2011.
- 4. Nathan Ida, "Sensors, Actuators and their Interfaces: A Multidisciplinary Introduction", Second Edition, IET Control, Robotics and Sensors Series 127, 2020
- 5. Instrumentation Devices and System, C.S. Rangan, G.R. Sarma, V.S. Mani, TMH, 1997.
- 6. Jacob Fraden Handbook of Modern Sensors Physics, Designs, and Applications Fourth Edition, Springer, 2010.

NPTEL / Swayam Course:

https://nptel.ac.in/courses/108/108/108108147/ https://www.youtube.com/watch?v=vjhp0zTXEsc

Internal Assessment (20-Marks):

Internal Assessment (IA) consists of two class tests of 20 marks each. IA-1 is to be conducted on approximately 40% of the syllabus completed and IA-2 will be based on remaining contents (approximately 40% syllabus but excluding contents covered in IA-I). Duration of each test shall be one hour. Average of the two tests will be considered as IA marks.

End Semester Examination (80-Marks):

- 1. Question paper will comprise of total 06 questions, each carrying 20 marks.
- 2. **Question No: 01** will be **compulsory** and based on entire syllabus wherein 4 to 5 subquestions will be asked.
- 3. Remaining questions will be mixed in nature and randomly selected from all the modules.
- 4. Weightage of each module will be proportional to number of respective lecture hours as mentioned in the syllabus.
- 5. Total 04 questions need to be solved.

Course Code	Course Name		Ceaching Sche		Credits Assigned			
Code		Theory	Practical	Tutorial	Theory	Practical	Tutorial	Total
ECL501	Digital Communication Lab	1	02			01		01

Course Code	Course Name		Examination Scheme							
			Theor	y Marks	Term	Practical	Total			
		Interi	ıal assessı	ment	Work	and Oral				
		Test 1	Test 2	Avg.	Exam.		1			
ECL501	Digital communication Lab				<	25	25	50		

Course objectives:

- 1. To learn source coding and error control coding techniques
- 2. To compare different line coding methods
- 3. To distinguish various digital modulations
- 4. To use different simulation tools for digital communication applications

Course outcomes:

After the successful completion of the course student will be able to

- 1. Compare various source coding schemes
- 2. Design and implement different error detection codes
- 3. Design and implement different error correction codes
- 4. Compare various line coding techniques
- 5. Illustrate the impulse response of a matched filter for optimum detection
- 6. Demonstrate various digital modulation techniques

Suggested list of experiments: (Course teacher can design their own experiments based on the prescribed syllabus)

- 1. Huffman code generation
- 2. Shannon-Fano code generation
- 3. Vertical redundancy Check (VRC) code generation and error detection
- 4. Horizontal Redundancy Check (HRC) code generation and error detection
- 5. Cyclic redundancy Check (CRC) code generation and error detection
- 6. Checksum code generation and error detection
- 7. Compare the performances of HRC and Checksum
- 8. Linear block code generation and error detection
- 9. Error detection and correction using Hamming code virtual lab http://vlabs.iitb.ac.in/vlabs-dev/labs/mit_bootcamp/comp_networks_sm/labs/exp1/index.php
- 10. Cyclic code generation and error detection
- 11. Convolutional code generation

- 12. Line Codes generation and performance comparison
- 13. Spectrum of line codes (NRZ unipolar and polar)
- 14. Impulse responses of ideal (Nyquist filter) and practical (Raised cosine filter) solution for zero ISI
- 15. Matched filter impulse response for a given input
- 16. Generation (and detection) of Binary ASK
- 17. Generation (and detection) of Binary PSK
- 18. Generation (and detection) of Binary FSK
- 19. Generation (and detection) of QPSK
- 20. Generation (and detection) of M-ary PSK
- 21. Generation (and detection) of M-ary FSK
- 22. Generation (and detection) of 16-ary QASK
- 23. Generation (and detection) of MSK

Term Work, Practical and Oral:

At least 8 experiments covering the entire syllabus must be given "Batch Wise". The experiments can be conducted with the help of simulation tool (preferably open source) and breadboard and components. Teacher should refer the suggested list of experiments and can design additional experiments to acquire practical design skills. The experiments should be student centric and attempt should be made to make experiments more meaningful, interesting and innovative.

Term work assessment must be based on the overall performance of the student with every experiment and assignments graded from time to time. The grades will be converted to marks as per "Credit and Grading System" manual and should be added and averaged. Based on the above scheme grading and term work assessment should be done.

The practical and oral examination will be based on entire syllabus. Students are encouraged to share their experiments codes on online repository. Practical exam slip should cover all the 8 experiments for examination.

Course Code	Course Name		Ceaching Sche Contact Hou		Credits Assigned				
Code		Theory	Practical	Tutorial	Theory	Practical	Tutorial	Total	
ECL502	Discrete-Time Signal Processing Laboratory		02			01		01	

Course Code	Course Name			Exa	eme			
			Theor	y Marks		Term	Practical	Total
		Inter	Internal assessment End Sem.				and Oral	
		Test 1	Test 2	Avg.	Exam.			
	Discrete-Time							
ECL502	Signal					25	25	50
ECL502	Processing					23	23	30
	Laboratory							

Course objectives:

- 1. To carryout basic discrete time signal processing operations.
- 2. To implement and design FIR filters and IIR filters.
- 3. To implement applications related to the field of biomedical signal processing and audio signal processing.

Course outcomes:

Learners will be able to .

- 1. Perform basic discrete time signal processing operations such as Linear Convolution, Circular Convolution, Auto Correlation, Cross Correlation, etc. and interpret the results.
- 2. Demonstrate their ability towards interpreting and performing frequency analysis of different discrete time sequences and systems.
- 3. Design and implement the FIR and IIR Filters for given specifications.
- 4. Implement and analyse applications related to the field of biomedical signal processing and audio signal processing.

Suggested list of experiments:

- 1) To perform linear convolution of two signals, auto correlation of non-periodic signals, periodic signals and random noise and interpret the results obtained.
- 2) To linearly convolve swept frequency sinusoidal wave with LPF and HPF impulse response filters in time domain and interpret the results obtained.

- 3) To obtain cross correlation of a signal with its delayed and attenuated version (Concept of radar signal processing).
- 4) To perform block convolution using overlap add method and overlap-save method.
- 5) To determine impulse, magnitude, phase response and pole-zero plot of given transfer functions.
- 6) To perform circular convolution and linear convolution of two sequences using DFT.
- 7) To perform the DFT of DT sequence and sketch its magnitude and phase spectrum or To Generate a discrete time signal having minimum three frequencies and analyse its frequency spectrum.
- 8) To study the effect of frequency resolution and zero padding.
- 9) DFT based spectral analysis to detect the signal buried in noise.
- 10) To perform denoising of a speech signal using circular convolution.
- 11) Design of IIR digital filters and use the designed filter to filter an input signal which has both low and high frequency components or real-world signal like ECG/EEG, speech signal etc).
- 12) Design a notch filter to supress the power supply hum in audio signals.
- 13) Design a comb filter to suppress 50Hz hum in biomedical signals.
- 14) Design of FIR filter using windowing method and use the designed filter to filter an input signal which has both low and high frequency components or real-world signal like ECG/EEG, speech signal etc.
- 15) Design of FIR filter using frequency sampling technique.
- 16) Design of minimum phase, maximum phase and mixed phase systems.
- 17) To verify the location of zeros in symmetric and antisymmetric FIR filters.
- 18) To reconstruct DT signals contaminated with sinusoidal interference using FIR filters.
- 19) To realise an IIR filter in cascade and parallel form.
- 20) To obtain lattice parameters of a given transfer function (FIR and IIR systems).
- 21) To perform coefficient quantisation using truncation and rounding.
- 22) To study the effect of coefficient quantisation on the frequency response of an IIR filter.
- 23) To study the effect of coefficient quantisation on the frequency response of an FIR filter.
- 24) To investigate the behaviour of limit cycle in an IIR system.
- 25) To generate the ECG signal and detect the characteristic points.
- 26) Classification of ECG signals.
- 27) To read an ECG signal and separate the QRS Complex.
- 28) To filter out the noise in an ECG signal using Spectral subtraction.
- 29) To extract delta, theta, alpha, sigma, and beta waveforms from EEG signal.
- 30) Perform sub-band coding on speech signal.
- 31) To generate Echo, Reverberation, Flanging effects in a sound signal.
- 32) Musical tone generation.
- 33) DTMF tone generation and detection.
- 34) Echo cancellation.

Also check

Virtual Laboratory http://vlabs.iitkgp.ernet.in/dsp/# for demonstration of concepts like DFT and its inverse, FIR filter using windowing method etc

Term Work:

At least 08 experiments covering the entire syllabus must be given "Batch Wise" and implemented using any software namely C, Python, Scilab, Matlab, Octave, etc. The experiments should be set to have well predefined inference and conclusion. Application oriented one course-project can be conducted for maximum batch of four students. Teacher should refer the suggested experiments and can design additional experiment to maintain better understanding and quality.

The experiments should be student centric and attempt should be made to make experiments more meaningful, interesting and innovative.

Term work assessment must be based on overall performance of the student with every experiment graded. The grade must be converted to marks as per credit and grading system manual, and should be added and averaged. Based on above scheme, grading and term work assessment should be done. Practical and oral examination will be based on entire syllabus. Students are encouraged to share their experiments codes on online repository. Practical exam slip should cover all 08 experiments for examination.



Course Code	Course Name	Teaching Scheme (Contact Hours)			Credits Assigned				
Code		Theory	Practical	Tutorial	Theory	Practical	Tutorial	Total	
ECL503	Digital VLSI Lab		02			01		01	

Course Code	Course Name		Examination Scheme							
			Theor	ry Marks		Term	Practical	Total		
		Intern	Internal assessment End Sem.				and Oral			
		Test 1	Test 2	Avg.	Exam.	C	Z			
ECL503	Digital VLSI Lab				25	25	50			

Course objectives:

- 1. To become familiar with open source circuit simulation tools like Ngspice, Magic etc.
- 2. To perform various type of analysis of combinational and sequential CMOS circuits
- 3. To evaluate performance of given combinational and sequential CMOS circuits
- 4. To design, implement and verify combinational and sequential CMOS circuits using open source VLSI design tools.

Course outcomes:

After the successful completion of the course student will be able to

- 1. Write spice code for given combinational and sequential CMOS circuits.
- 2. Perform various analysis like operating point, dc, transient etc of given CMSO circuits.
- 3. Evaluate performance of given CMOS circuits.
- 4. Draw layout of given CMOS circuit and also able extract various parasitic using open source layout tool like Magic.
- 5. Design, simulate, and verify CMOS circuit for given specifications.

Suggested list of experiments: (Course teacher can design their own experiments based on the prescribed syllabus)

- 1. Constant Voltage and Constant field MOSFET scaling
- 2. Layout of MOSFET and extraction of parasitic capacitances
- 3 Voltage transfer characteristics of CMOS inverter and calculation of Noise Margin and static power
- 4. Transient Analysis of CMOS inverter and calculation of tpHL, tpLH, tr, tf, average power
- 5. Design of CMOS inverter for given specifications
- 6. Layout of CMOS inverter and comparison of pre layout and post layout performance.
- 7. Voltage transfer characteristics of 2 input NAND/NOR gate and calculation of noise margins and validation using equivalent inverter approach.
- 8. Transient Analysis of 2 input NAND/NOR CMOS gate and calculation of tpHL, tpLH, tr, tf, average power and validation using equivalent inverter approach.

- 9. Layout of 2 input CMOS NAND/NOR gate and comparison of pre layout and post layout performance.
- 10. Static and transient analysis of Complex CMOS gate.
- 11. Layout of complex CMOS gate using euler path.
- 12. Implementation of various combinational and sequential circuits using different design styles.
- 13. Design and implementation of NAND based and NOR based ROM array.
- 14. Performance analysis of 6T-SRAM Cell
- 15. Design of 6T SRAM cell robust read and write operation.
- 16. Performance analysis of 1T and 3T DRAM Cell
- 17. RTL design of Soda dispenser machine
- 18. RTL design of FIR Filter

Link for virtual lab http://www.vlsi-iitg.vlabs.ac.in

Term Work, Practical and Oral:

At least 8 experiments (at least three experiments on layout) covering the entire syllabus must be given "Batch Wise". The experiments can be conducted with the help of simulation tool (preferably. Teacher should refer the suggested list of experiments and can design additional experiments to acquire practical design skills. The experiments should be student centric and attempt should be made to make experiments more meaningful, interesting and innovative.

Term work assessment must be based on the overall performance of the student with every experiment and assignments graded from time to time. The grades will be converted to marks as per "Credit and Grading System" manual and should be added and averaged. Based on the above scheme grading and term work assessment should be done.

The practical and oral examination will be based on entire syllabus. Students are encouraged to share their experiments codes on online repository. Practical exam slip should cover all the 8 experiments for examination.

Course Code	Course Name	7	Teaching scheme			Credit	assigned	
ECL504	Professional	Theory	Pract.	Tut.	Theory	Pract.	Tut.	Total
	Communication & Ethics-II		2*+ 2 Hours (Batch-wise)			2		02

^{*}Theory class to be conducted for full class.

		Examination Scheme										
Course	Course Name	Theory					Term			Internal		
Code	Course Maine	Intern	al Assessi	ment	End	Duration	uration		work Pract	Oral	Oral Oral	Total
		Test 1	Test 2	Avg.	sem	(hrs)	WUIK		•	Ofai		
ECL504	Professional											
	Communication) '		
	& Ethics-II						25			25	50	
	(abbreviated											
	PCE-II)											

Course Code	Course Name Credits
ECL504	Business Communication & Ethics 02
Course	This curriculum is designed to build up a professional and ethical approach
Rationale	effective oral and written communication with enhanced soft skills. Through
	practical sessions, it augments student's interactive competence and confidence
	to respond appropriately and creatively to the implied challenges of the globa
	Industrial and Corporate requirements. It further inculcates the socia
	responsibility of engineers as technical citizens.
Course	To discern and develop an effective style of writing important
Objectives	technical/business documents.
	To investigate possible resources and plan a successful job campaign.
	To understand the dynamics of professional communication in the form of
	group discussions, meetings, etc. required for career enhancement.
	To develop creative and impactful presentation skills.
	To analyze personal traits, interests, values, aptitudes and skills.
	• To understand the importance of integrity and develop a personal code of ethics.

Course	Learner will be able to
Outcomes	 plan and prepare effective business/ technical documents which will in turn provide solid foundation for their future managerial roles. strategize their personal and professional skills to build a professional image and meet the demands of the industry. emerge successful in group discussions, meetings and result-oriented agreeable solutions in group communication situations. deliver persuasive and professional presentations. develop creative thinking and interpersonal skills required for effective professional communication. apply codes of ethical conduct, personal integrity and norms of organizational behaviour.

	1.6. Technical Paper Writing	
	• Parts of a Technical Paper (Abstract, Introduction,	
	Research Methods, Findings and Analysis, Discussion, Limitations,	
	Future Scope and References)	
	Language and Formatting	
	Referencing in IEEE Format	
	EMPLOYMENT SKILLS	
	2.1. Cover Letter & Resume	
	Parts and Content of a Cover Letter	
	Difference between Bio-data, Resume & CV	
	Essential Parts of a Resume	
	Types of Resume (Chronological, Functional & Combination)	
	2.2 Statement of Purpose	
	Importance of SOP	
	Tips for Writing an Effective SOP	
	2.3 Verbal Aptitude Test	
_	Modelled on CAT, GRE, GMAT exams	
2	2.4. Group Discussions	06
	Purpose of a GD	
	Parameters of Evaluating a GD	
	 Types of GDs (Normal, Case-based & Role Plays) 	
	GD Etiquettes	
	2.5. Personal Interviews	
	Planning and Preparation	
	Types of Questions	
	 Types of Interviews (Structured, Stress, Behavioural, Problem 	
	Solving & Case-based)	
	• Modes of Interviews: Face-to-face (One-to one and Panel)	
	Telephonic, Virtual	
4	BUSINESS MEETINGS	
	1.1. Conducting Business Meetings	
	Types of Meetings Poles and Despensibilities of Chairmanan Secretary and Marchana	
_	Roles and Responsibilities of Chairperson, Secretary and Members	9 -
3	Meeting Etiquette	02
11	3.2. DocumentationNotice	
	Agenda Minutes	
	• Minutes	

	TECHNICAL / DUCINIECC DDECENTE A TIONIC						
	TECHNICAL/ BUSINESS PRESENTATIONS 1.1 Effective Presentation Strategies						
	 Defining Purpose 						
	 Analyzing Audience, Location and Event 						
	Gathering, Selecting & Arranging Material						
	• Structuring a Presentation						
	Making Effective Slides						
4	Types of Presentations Aids	02					
	Closing a Presentation						
	Platform skills						
	1.2 Group Presentations						
	Sharing Responsibility in a Team						
	Building the contents and visuals together						
	• Transition Phases						
	INTERPERSONAL SKILLS						
	1.1. Interpersonal Skills						
	Emotional Intelligence						
	Leadership & Motivation						
	Conflict Management & Negotiation						
5	Time Management	08					
	Assertiveness						
	Decision Making						
	5.2 Start-up Skills						
	Financial Literacy						
	Risk Assessment						
	Data Analysis (e.g. Consumer Behaviour, Market Trends, etc.)						
	CORPORATE ETHICS 6.1Intellectual Property Rights						
	• Copyrights						
	• Trademarks						
	• Patents						
,	Industrial Designs	0.5					
6	Geographical Indications	02					
	Integrated Circuits						
	Trade Secrets (Undisclosed Information)						
	6.2 Case Studies						
	 Cases related to Business/ Corporate Ethics 						
•	Cases related to Business/ Corporate Etines						

List of assignments:

(In the form of Short Notes, Questionnaire/ MCQ Test, Role Play, Case Study, Quiz, etc.)

- 1. Cover Letter and Resume
- 2. Short Proposal

- 3. Meeting Documentation
- 4. Writing a Technical Paper/ Analyzing a Published Technical Paper
- 5. Writing a SOP
- 6. IPR
- 7. Interpersonal Skills
- 8. Aptitude test (Verbal Ability)

Note:

- 1. The Main Body of the project/book report should contain minimum 25 pages (excluding Front and Back matter).
- 2. The group size for the final report presentation should not be less than 5 students or exceed 7 students.
- 3. There will be an end-semester presentation based on the book report.

Assessment:

Term Work:

Term work shall consist of minimum 8 experiments.

The distribution of marks for term work shall be as follows.

Assignment : 10 Marks
Attendance : 5 Marks
Presentation slides : 5 Marks
Book Report (hard copy) : 5 Marks

The final certification and acceptance of term work ensures the satisfactory performance of laboratory work and minimum passing in the term work.

Internal oral:

Oral Examination will be based on a GD & the Project/Book Report presentation.

Group Discussion : 10 marks
Project Presentation : 10 Marks
Group Dynamics : 5 Marks

Books Recommended:

Textbooks and Reference books:

- 1. Arms, V. M. (2005). Humanities for the engineering curriculum: With selected chapters from Olsen/Huckin: Technical writing and professional communication, second edition. Boston, MA: McGraw-Hill.
- 2. Bovée, C. L., & Thill, J. V. (2021). *Business communication today*. Upper Saddle River, NJ: Pearson.
- 3. Butterfield, J. (2017). *Verbal communication: Soft skills for a digital workplace*. Boston, MA: Cengage Learning.
- 4. Masters, L. A., Wallace, H. R., & Harwood, L. (2011). *Personal development for life and work*. Mason: South-Western Cengage Learning.
- 5. Robbins, S. P., Judge, T. A., & Campbell, T. T. (2017). Organizational behaviour. Harlow,

- England: Pearson.
- 6. Meenakshi Raman, Sangeeta Sharma (2004) Technical Communication, Principles and Practice. Oxford University Press
- 7. Archana Ram (2018) Place Mentor, Tests of Aptitude For Placement Readiness. Oxford University Press
- 8. Sanjay Kumar & PushpLata (2018). Communication Skills a workbook, New Delhi: Oxford University Press.



Subject	Subject Name	Teach	Teaching Scheme (Hrs.)			Credits Assigned			
Code		Theory	Practical	Tutorial	Theory	Practical	Tutorial	Total	
ECM501	Mini Project 2A: Embedded System Project		04\$			02		02	

\$ Indicates work load of a learner (Not Faculty) for Mini Project 2A. Faculty Load: 1 hour per week per four groups.

Subject	Subject Name	Examination Scheme							
Code			The	ory Marks					
		Internal Assessment			End	Term	Practical		
					Sem.	Work	and	Total	
					Exam	4	Oral		
		Test 1	Test 2	Avg. of Test 1		1			
				and Test 2					
	Mini Project 2A:								
ECM501	Embedded System					25	25	50	
	Project								

Course Pre-requisite:

- 1. ECC402- Microcontrollers
- 2. ECC403- Linear Integrated Circuits
- 3. ECM401- Mini Project 1B: Arduino & Raspberry Pi based Projects

Course Objectives

- 1. To develop background knowledge Embedded Systems.
- 2. To understand designing of embedded systems.
- 3. To choose proper microcontroller for Embedded systems
- 4. To understand use of wireless sensors/communications with Embedded systems
- 5. To understand communication techniques.
- 6. To write programs for embedded systems and real time operating systems /IoT

Course Outcomes

After successful completion of the course, the student will be able to

- 1. Understand the embedded systems with design metrics.
- 2. Understand microcontrollers and programming in Embedded C.
- 3. Implementation of Embedded systems with different sensors and peripherals as IoT.
- 4. Implementation of Embedded systems with different communication protocols as IoT.
- 5. Analyze concepts of Real time operating systems.
- 6. Design embedded system applications using sensors, peripherals and RTOS

A. Guideline to maintain quality of mini project are as follows:

- To achieve proper selection of Mini Projects. Students should do survey of different microcontroller board from given microcontroller series, tools and identify which is most suitable for their selected topic. They should consult with their Guide/Mentors / Internal committee to finalize it.
- 2. Students shall submit implementation plan in the form of Smart Report/Gantt/PERT/CPM chart, which will cover weekly activity of mini project.
- 3. A log book to be prepared by each group, wherein group can record weekly work progress. Guide/ supervisor will verify it and will put notes/comments.

- 4. Guide/supervisor guidance is very much important during mini project activities; however, focus shall be on self-learning.
- 5. The solution to be verified with standard tools and procedures and report to be compiled in standard format of University of Mumbai.

6. Suggested steps for mini project selection and implementation

- i. Mini project should be completely microcontroller based
- ii. Follow these steps
 - a) Take specification, using these specifications design project.
 - b) Select proper microcontroller board considering features and requirements of project.
 - c) Program it using Embedded C and perform verification of each module (sensors/communication protocol)
 - d) Test Functional Simulation and verify it using simulation tool.
 - e) Make hardware connection on GPP of peripherals with microcontroller board and execute the program.
 - f) Troubleshoot if not get expected result.

B. Project Topic selection and approval:-

- 1. The group may be of **maximum FOUR (04)** students.
- 2. Topic selection and approval by **2 Expert** faculty from department at the start of semester
- 3. **Log Book** to be prepared for each group to record the work progress in terms of milestones per week by students. Weekly comment, remarks to be put by guiding faculty. Both students and faculty will put signature in it per week. The log book can be managed **online** with proper authentication method using google sheets/forms or open source project management software.

C. Project Report Format:

- 1. Report should not exceed **30 pages**. Simply staple it to discourage use of plastic.
- 2. Report must contain block diagram, circuit diagram, screenshot of outputs and datasheets of microcontrollers and peripherals (Include **only required** information pages).
- 3. The recommended report writing format is in LaTeX. (https://youtu.be/YLm3sXIKpHQ)

Term Work:

1. Term Work evaluation and marking scheme:

- a. The review/ progress monitoring committee shall be constituted by Head of Departments of each institute.
- b. The progress of mini project to be evaluated on continuous basis, minimum two reviews in each semester.
- c. At end of semester the above 2 expert faculty who have approved the topic will internally **evaluate the performance**.
- d. Students have to give presentation and demonstration on the Embedded Systems Mini Project- 2-A at end of semester before submission to above experts.
- e. In the evaluation each individual student should be assessed for his/her contribution, understanding and knowledge gained about the task completed. Based upon it the marks will be awarded to student.

f. Distribution of 25 Marks scheme is as follows:

- i. Marks awarded by guide/supervisor based on log book and output: 10
- ii. Marks awarded by review committee: 10
- iii. Quality of Project report: 05

2. Guidelines for Assessment of Mini Project Practical/Oral Examination:

- **a.** Report should be prepared as per the guidelines issued by the University of Mumbai.
- **b.** Mini Project shall be assessed through a presentation and demonstration of working model by the student project group to a panel of Internal and **External Examiners preferably from industry or research organisations** having experience of more than five years approved by head of Institution.

Students shall be motivated to present their mini project work done

- 1. Participate in Project Competition
- 2. Publish paper in Conferences/Journals.

Module	Unit	Detailed Content	Hours
No.	No.		
1		Introduction	8
	1.1	Definition of Embedded System, Embedded Systems Vs General Computing	
		Systems, Classification, Major Application Areas. Characteristics and quality	
		attributes (Design Metric) of embedded system.	
	1.2	Identification of Project Title	
2		Controller boards and Programming – Embedded C	8
	2.1	ARM LPC 21XX (2148), STM32 boards and Texas MSP 430 lunchbox/ Tiva C board and PIC/PSoc*	
	2.2	Comparison of C and embedded C, Data Types, Variable, Storage Classes, Bit	
		operation, Arrays, Strings, Structure and unions, Classifier	
	2.3	Exercise: Identify the suitable board required for the particular application	
		with respect to design metrics.	
		(Hint: check clock frequency (speed), memory (program and data), no. of	
		ports for peripherals, timers/counters and serial communication requirement for	
		project)	
	2.4	Suggested Way to Identify: https://predictabledesigns.com/how-to-select-	
		the-microcontroller-for-your-new-product/	
3		Interfacing Sensors and peripherals using Embedded C	10
	3.1	Sensors and Signal Conditioning Circuits amplifiers /attenuators /filters	
		/comparators/ADC and DAC), Interfacing with GLCD/TFT display, Relays	
		and Drivers for interfacing Motors (DC and stepper)	
	3.2	and Drivers for interfacing Motors (DC and stepper) Interfacing with BLDC motors and drivers, USB/HDMI camera interfacing	
	3.2	and Drivers for interfacing Motors (DC and stepper) Interfacing with BLDC motors and drivers, USB/HDMI camera interfacing Exercise: Understand the Interfacing requirement like drivers, signal	
	3.3	and Drivers for interfacing Motors (DC and stepper) Interfacing with BLDC motors and drivers, USB/HDMI camera interfacing Exercise: Understand the Interfacing requirement like drivers, signal condition circuits for sensors, etc. for the selected application	
		and Drivers for interfacing Motors (DC and stepper) Interfacing with BLDC motors and drivers, USB/HDMI camera interfacing Exercise: Understand the Interfacing requirement like drivers, signal condition circuits for sensors, etc. for the selected application Study Material: For LCD interfacing with MSP430 LaunchPad	
	3.3	and Drivers for interfacing Motors (DC and stepper) Interfacing with BLDC motors and drivers, USB/HDMI camera interfacing Exercise: Understand the Interfacing requirement like drivers, signal condition circuits for sensors, etc. for the selected application Study Material: For LCD interfacing with MSP430 LaunchPad https://microcontrollerslab.com/lcd-interfacing-msp430-	
	3.3	and Drivers for interfacing Motors (DC and stepper) Interfacing with BLDC motors and drivers, USB/HDMI camera interfacing Exercise: Understand the Interfacing requirement like drivers, signal condition circuits for sensors, etc. for the selected application Study Material: For LCD interfacing with MSP430 LaunchPad https://microcontrollerslab.com/lcd-interfacing-msp430-launchpad/#:~:text=LCD%20interfacing%20with%20MSP430%20microcontro	
	3.3	and Drivers for interfacing Motors (DC and stepper) Interfacing with BLDC motors and drivers, USB/HDMI camera interfacing Exercise: Understand the Interfacing requirement like drivers, signal condition circuits for sensors, etc. for the selected application Study Material: For LCD interfacing with MSP430 LaunchPad https://microcontrollerslab.com/lcd-interfacing-msp430-launchpad/#:~:text=LCD%20interfacing%20with%20MSP430%20microcontroller,Now%20I%20will&text=It%20requires%205%20volts%20dc,and%20seco	
	3.3	and Drivers for interfacing Motors (DC and stepper) Interfacing with BLDC motors and drivers, USB/HDMI camera interfacing Exercise: Understand the Interfacing requirement like drivers, signal condition circuits for sensors, etc. for the selected application Study Material: For LCD interfacing with MSP430 LaunchPad https://microcontrollerslab.com/lcd-interfacing-msp430-launchpad/#:~:text=LCD%20interfacing%20with%20MSP430%20microcontroller,Now%20I%20will&text=It%20requires%205%20volts%20dc,and%20second%20pin%20is%20vcc.	
4	3.4	and Drivers for interfacing Motors (DC and stepper) Interfacing with BLDC motors and drivers, USB/HDMI camera interfacing Exercise: Understand the Interfacing requirement like drivers, signal condition circuits for sensors, etc. for the selected application Study Material: For LCD interfacing with MSP430 LaunchPad https://microcontrollerslab.com/lcd-interfacing-msp430-launchpad/#:~:text=LCD%20interfacing%20with%20MSP430%20microcontroller,Now%20I%20will&text=It%20requires%205%20volts%20dc,and%20second%20pin%20is%20vcc. Communication with programming in Embedded C	10
4	3.3	and Drivers for interfacing Motors (DC and stepper) Interfacing with BLDC motors and drivers, USB/HDMI camera interfacing Exercise: Understand the Interfacing requirement like drivers, signal condition circuits for sensors, etc. for the selected application Study Material: For LCD interfacing with MSP430 LaunchPad https://microcontrollerslab.com/lcd-interfacing-msp430-launchpad/#:~:text=LCD%20interfacing%20with%20MSP430%20microcontroller,Now%20I%20will&text=It%20requires%205%20volts%20dc,and%20second%20pin%20is%20vcc.	10
4	3.4	and Drivers for interfacing Motors (DC and stepper) Interfacing with BLDC motors and drivers, USB/HDMI camera interfacing Exercise: Understand the Interfacing requirement like drivers, signal condition circuits for sensors, etc. for the selected application Study Material: For LCD interfacing with MSP430 LaunchPad https://microcontrollerslab.com/lcd-interfacing-msp430-launchpad/#:~:text=LCD%20interfacing%20with%20MSP430%20microcontroller,Now%20I%20will&text=It%20requires%205%20volts%20dc,and%20second%20pin%20is%20vcc. Communication with programming in Embedded C	10
4	3.3	and Drivers for interfacing Motors (DC and stepper) Interfacing with BLDC motors and drivers, USB/HDMI camera interfacing Exercise: Understand the Interfacing requirement like drivers, signal condition circuits for sensors, etc. for the selected application Study Material: For LCD interfacing with MSP430 LaunchPad https://microcontrollerslab.com/lcd-interfacing-msp430-launchpad/#:~:text=LCD%20interfacing%20with%20MSP430%20microcontroller,Now%20I%20will&text=It%20requires%205%20volts%20dc,and%20second%20pin%20is%20vcc. Communication with programming in Embedded C Serial communication, CAN bus, I2C, MOD bus, SPI	10
4	3.3	and Drivers for interfacing Motors (DC and stepper) Interfacing with BLDC motors and drivers, USB/HDMI camera interfacing Exercise: Understand the Interfacing requirement like drivers, signal condition circuits for sensors, etc. for the selected application Study Material: For LCD interfacing with MSP430 LaunchPad https://microcontrollerslab.com/lcd-interfacing-msp430-launchpad/#:~:text=LCD%20interfacing%20with%20MSP430%20microcontroller,Now%20I%20will&text=It%20requires%205%20volts%20dc,and%20second%20pin%20is%20vcc. Communication with programming in Embedded C Serial communication, CAN bus, I2C, MOD bus, SPI Interfacing with Wi-Fi, Bluetooth ,ZigBee, LoRa, RFID and putting data on	10
4	3.3 3.4 4.1 4.2	and Drivers for interfacing Motors (DC and stepper) Interfacing with BLDC motors and drivers, USB/HDMI camera interfacing Exercise: Understand the Interfacing requirement like drivers, signal condition circuits for sensors, etc. for the selected application Study Material: For LCD interfacing with MSP430 LaunchPad https://microcontrollerslab.com/lcd-interfacing-msp430-launchpad/#:~:text=LCD%20interfacing%20with%20MSP430%20microcontroller,Now%20I%20will&text=It%20requires%205%20volts%20dc,and%20second%20pin%20is%20vcc. Communication with programming in Embedded C Serial communication, CAN bus, I2C, MOD bus, SPI Interfacing with Wi-Fi, Bluetooth ,ZigBee, LoRa, RFID and putting data on IoT	10

	4.5	Study Material: Serial Communication Interface:					
		STM32: https://controllerstech.com/serial-transmission-in-					
		stm32/#:~:text=Serial%20Transmission%20in%20Stm32&text=UART%20is					
		%20widely%20used%20for,amongst%20which%20communication%20is%20					
		done.					
		LPC2148: https://www.electronicwings.com/arm7/lpc2148-uart0					
		MSP430: https://www.ti.com/lit/ml/slap117/slap117.pdf					
5		Real Time Operating Systems[RTOS]	08				
	5.1	Operating system basics, Types of OS, Tasks, process, Threads					
	5.2	Multiprocessing and ,Multitasking , Task scheduling					
	5.3	RTLinux/ Free RTOS and Mbed OS, Implementation with RTOS					
6		Cloud/Web server	08				
	6.1	Implementation on web server,					
	6.2	Thingspeak, AWS cloud platform for IoT based programming and modelling					
	6.3	Exercise: perform ESP8266 interface with microcontroller					
	6.4	Study Material:					
		STM32: https://circuitdigest.com/microcontroller-projects/interfacing-					
		esp8266-with-stm32f103c8-stm32-to-create-a-webserver					
		LPC2148: https://circuitdigest.com/microcontroller-projects/iot-based-ARM7-					
		LPC2148-webserver-to-control-an-led					
		MSP430: https://circuitdigest.com/microcontroller-projects/sending-email-					
		using-msp430-and-esp8266					
	·	Total	52				

NOTE:

- * Advanced Microcontroller: Like PSoc and PIC may be used as per the student's intellectual ability and strength.
- ** Module 5 and 6 (RTOS and Cloud/Web Server): Can be included by Guide /supervisor /Mentor depending upon need and scope of the project for selected topic and its application.

Textbooks:

- 1. Shibu K.V," Introduction to Embedded Systems", Mc Graw Hill, 2nd edition.
- 2. Frank Vahid, and Tony Givargis, "Embedded System Design: A unified Hardware/Software Introduction", Wiley Publication.
- 3. Raj Kamal," Embedded Systems Architecture, Programming and design", Tata MCgraw-Hill Publication.
- 4. Dr. K.V.K.K. Prasad, "Embedded Real Time Systems: Concepts, Design & Programming", Dreamtech Publication.
- 5. Iyer, Gupta," Embedded real systems Programming", TMH
- 6. David Simon, "Embedded systems software primer', Pearson
- Andrew Sloss, Dominic Symes and Chris Wright, "ARM_System_Developers_Guide-Designing and Optimizing System Software" Elsevier and Morgan Kaufmann Publishers.
- 8. Michel J Pont "Embedded C" Pearson

Suggested Software tools:

- 1. Tinkercad: https://www.tinkercad.com/
- 2. Proteus software
- 3. KEIL for ARM LPC 2148
- 4. STM32Cube software

- 5. MSP Flasher Command Line Programmer
- 6. msp430 code composer studio

Online Repository:

- 1. https://circuitdigest.com
- 2. www. Github.com
- 3. https://www.electronicshub.org
- 4. https://www.hackster.io/

NPTEL Courses:

- 1. Introduction to Embedded System Design (using MSP430) https://onlinecourses.nptel.ac.in/noc20_ee98/preview
- 2. Embedded System Design with ARM https://onlinecourses.nptel.ac.in/noc20_cs15/preview
- 3. Embedded systems https://nptel.ac.in/courses/108/102/108102045/
- 4. Master Microcontroller and Embedded Driver Development(MCU1) STM32

 https://www.udemy.com/course/mastering-microcontroller-with-peripheral-driverdevelopment/?gclid=CjwKCAjw07qDBhBxEiwA6pPbHslLIEqmAv7E17ysZETbreXe0XMb8Nai4NBqpUAvni5v3fLKsfNBoC8LQQAvD BwE&matchtype=b&utm campaign=LongTail Ia.EN cc.INDIA&ut
 m content=deal4584&utm medium=udemyads&utm source=adwords&utm term= . ag 8287
 6601447 . ad 511749008336 . kw %2Bembedded+%2Bsystems+%2Bcourse . de c . dm
 . pl _ ti kwd-671751469914 . li 1007785 . pd _ .
- 5. Texas Instruments (TI) Trainings
 https://e2e.ti.com/support/archive/universityprogram/educators/w/wiki/2103/training-support
- 6. Texas Instruments (TI) Teaching material/text books
 https://e2e.ti.com/support/archive/universityprogram/educators/w/wiki/2035/textbooks

