

CONFIDENTIAL

Memory Manager for Linux

Release Note: Software

R-Car H3/M3/M3N/E3 Series

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How to Use This Manual

- **[Readers]**

This manual is intended for engineers who develop products which use the R-Car H3/M3/M3N/E3 processor.

- **[Purpose]**

This manual is intended to give users an understanding of the functions of the R-Car H3/M3/M3N/E3 processor device driver and to serve as a reference for developing hardware and software for systems that use this driver.

- **[How to Read This Manual]**

It is assumed that the readers of this manual have general knowledge in the fields of electrical

— engineering, logic circuits, microcontrollers, and Linux.

→ Read this manual in the order of the CONTENTS.

— To understand the functions of a multimedia processor for R-Car H3/M3/M3N/E3

→ See the R-Car H3/M3/M3N/E3 User's Manual.

— To know the electrical specifications of the multimedia processor for R-Car H3/M3/M3N/E3

→ See the R-Car H3/M3/M3N/E3 Data Sheet.

- **[Conventions]**

The following symbols are used in this manual.

Data significance: Higher digits on the left and lower digits on the right

Note: Footnote for item marked with Note in the text

Caution: Information requiring particular attention

Remark: Supplementary information

Numeric representation: Binary ... xxxx, 0bxxxx, or xxxxB

Decimal ... xxxx

Hexadecimal ... 0xxxxx or xxxxH

Data type: Double word ... 64 bits

Word ... 32 bits

Half word ... 16 bits

Byte ... 8 bits

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Table of Contents

| | |
|--|---|
| 1. Introduction..... | 1 |
| 2. List of Memory Manager Software Contents | 2 |
| 2.1 Software (Hosted in github.com) | 2 |
| 2.2 Documentation (Multimedia Reference Software for Linux Doc)..... | 2 |
| 3. Change History | 3 |
| 3.1 Major updates in previous versions..... | 3 |
| 3.2 v2.12.0 | 3 |
| 3.3 v2.16.0 | 3 |
| 3.4 v2.17.0 | 3 |
| 3.5 v2.19.0 | 3 |
| 3.6 v2.21.0 | 3 |
| 3.7 v2.23.0 | 3 |
| 3.8 v2.23.1 | 4 |
| 3.9 v3.4.0 | 4 |
| 3.10 v3.6.0 | 4 |
| 3.11 v3.7.0 | 4 |
| 3.12 v3.9.0 | 4 |
| 3.13 v3.9.0.1 | 4 |
| 3.14 v3.15.0 | 5 |
| 3.15 v3.19.0 | 5 |
| 3.16 v3.21.0 | 5 |
| 3.17 v5.1.0 | 5 |
| 3.18 v5.5.0 | 5 |
| 3.19 v5.9.0 (This Version) | 5 |
| 4. Restriction | 6 |
| 4.1 Known issues | 6 |
| 4.2 Workaround | 6 |
| 4.3 Closed issues | 9 |
| 4.4 Known functional limitations of delivered functions..... | 9 |
| 4.5 Non-validated function | 9 |

1. Introduction

This manual explains the package construction of Memory Manager for Linux and restrictions of the current release.

This software is provided based on the GNU General Public License (GPLv2), MIT License.
Please handle this software according to the conditions of each license.

2. List of Memory Manager Software Contents

The following is included in this software.

2.1 Software (Hosted in github.com)

| No. | Contents | URL | License |
|-----|----------------------------------|---|-------------|
| 1 | Memory Manager (Interface Layer) | https://github.com/renesas-rcar/mmngr_lib (ID: 0322548e54b45a064c9cecea29018ef50cdb8423) | MIT |
| 2 | Memory Manager (Driver layer) | https://github.com/renesas-rcar/mmngr_drv (ID: 2439802426474136312bd10bc4c143fbf1c84850) | MIT / GPLv2 |

2.2 Documentation (Multimedia Reference Software for Linux Doc)

| No. | Contents | File name | Version |
|-----|---------------------------------|--|---------|
| 1 | Release Note (This document) | RENESAS_RCH3M3M3NE3_MMP_MMNGR_Linux_ReleaseNote_E_v5.9.0.pdf | 5.9.0 |
| 2 | User's Manual | RENESAS_RCH3M3M3NE3_MMP_MMNGR_Linux_UME_v3.00.pdf | 3.00 |

3. Change History

3.1 Major updates in previous versions

| No. | Description |
|--------|---|
| #77137 | Initial R-CarH3 support (v2.2.0). |
| #84300 | Add support for Lossy Decompression feature (v2.8.0) |
| #94805 | Add IPMMU (PMB) support for memory allocation (v2.11.0) |

3.2 v2.12.0

| No. | Description |
|--------|--|
| #97336 | Add IPMMU (PMB) registers backup/restore to support System Suspend-to-RAM. |

3.3 v2.16.0

| No. | Description |
|---------|--|
| #103695 | Remove duplicated definitions between user and header file |
| #103676 | Remove staging driver |
| #103933 | Add support for Linux v4.9 stable |
| #108908 | Add IPMMU (PMB) support for 40-bit address space of CMA area for Lossy compression |

3.4 v2.17.0

| No. | Description |
|---------|---|
| #112734 | Add support for R-Car H3 Ver.2.0 |
| #114933 | Add IPMMU (PMB) support for VSPB on R-Car H3 Ver.1.x and M3 Ver.1.0 |

3.5 v2.19.0

| No. | Description |
|---------|---|
| #116810 | Add support for R-Car M3 Ver.1.1, Ver.1.2 |

3.6 v2.21.0

| No. | Description |
|---------|---|
| #117217 | Add IPMMU (MMU) support with 1GB page for memory allocation instead of PMB. |
| #121332 | Fix compiler/sparse warnings |
| #122262 | Disable TLB function in IPMMU-VC0/VC1/VP0/VP1 for R-Car H3 Ver.2.0 |
| #123874 | Add IPMMU (MMU) registers backup/restore to support System Suspend-to-RAM. |
| #124339 | Add IPMMU (MMU) support for 40-bit address space of CMA area for DTV (SSP) |

3.7 v2.23.0

| No. | Description |
|---------|---|
| #128002 | Fix warnings reported by checkpatch and static code analysis tool |

3.8 v2.23.1

| No. | Description |
|---------|-----------------------------------|
| #137570 | Add support for R-Car M3N Ver.1.1 |

3.9 v3.4.0

| No. | Description |
|---------|---|
| #144845 | Add support for Linux v4.14 stable. |
| #145666 | Fix compiler/checkpatch warnings. |
| #145776 | Disable IPMMU TLB cache function in M3N Ver.1.1 due to hardware restriction. |
| #149416 | Update reserved bits handling in IMTTLBR and IPMMU (MMU) initialize sequence. |

3.10 v3.6.0

| No. | Description |
|---------|---|
| #144922 | Fix warnings reported by static code analysis tool. |
| #149423 | Disable IPMMU TLB cache function in E3 Ver.1.0 due to hardware restriction. |
| #149999 | Change the way of parsing reserved memory regions in DT |
| #152933 | Update IPMMU (MMU) deinitialize sequence |
| #153165 | Add support for R-Car E3 Ver.1.0 |

3.11 v3.7.0

| No. | Description |
|---------|--|
| #149466 | Disable IPMMU TLB cache function in selected SoC revision |
| #150847 | Disable TLB function on IPMMU-PV1 cache on H3 Ver.2.0 by BL2 |
| #162283 | Add H3 Ver.3.0 support |
| #162844 | Update CMA memory mapping for R-Car E3 |

3.12 v3.9.0

| No. | Description |
|---------|---|
| #171377 | Add support for Linux v4.14.35 (LTSI candidate) |

3.13 v3.9.0.1

| No. | Description |
|---------|------------------------------|
| #187322 | Fix static analysis warnings |

3.14 v3.15.0

| No. | Description |
|---------|--|
| #142732 | Improve error handling for import phases and close() function |
| #190672 | Add support for Linux v4.14-LTSI |
| #190686 | Remove unnecessary check when parsing reserved memory regions in DT |
| #192478 | Disable IPMMU TLB cache function in E3 Ver.1.x due to hardware restriction |
| #192482 | Add E3 Ver.1.1 support |
| #195715 | Add error handling for mm_probe() function |

3.15 v3.19.0

| No. | Description |
|---------|--|
| #203696 | Add IPMMU(MMU) support for R-Car M3 Ver.3.0 (Not Verified) |

3.16 v3.21.0

| No. | Description |
|---------|---|
| #217803 | Fix dmabuf refcount handling on mm_ioc_import_start() failure |
| #218172 | Remove cache snoop transaction for page table walk request |

3.17 v5.1.0

| No. | Description |
|---------|--|
| #269293 | Make sure IPMMU data for H3 Ver.1.x is set correctly |
| #269293 | Don't register as BUS IOMMU if machine doesn't have IPMMU-VMVA |
| #269293 | Fix build errors in kernel version 5.4 |
| #295363 | Add kernelheap cached buffers support |
| #306997 | Fix a race between close() and dmabuf_map_dma_buf() callbacks |
| #306997 | Fix build errors in kernel version 5.10 |

3.18 v5.5.0

| No. | Description |
|---------|---|
| #320649 | Add default coherent DMA mask |
| #320640 | Update IPMMU(MMU) compatible for R8A77961 M3-W+ |

3.19 v5.9.0

| No. | Description |
|-----|------------------------|
| - | No source code changes |

3.20 v5.10.0 (This version)

| No. | Description |
|-----|------------------------|
| - | No source code changes |

4. Restriction

4.1 Known issues

There are no known issues.

CMA area for MMP, MMP for DTV (SSP) and Lossy compression can be assigned to 40-bit physical address space when IPMMU MMU support config is enabled.

For details, refer to the following table.

| CMAs | 40-bit physical address space | | | | | | |
|--------------------------------|-------------------------------|---------|---------|----------|---------|--------------|--------------|
| | R-Car H3 | | | R-Car M3 | | R-Car M3N | R-Car E3 |
| | Ver.1.x | Ver.2.0 | Ver.3.0 | Ver.1.x | Ver.3.0 | Ver.1.x (*1) | Ver.1.x (*2) |
| Default CMA area | - | - | - | - | - | - | - |
| CMA area for MMP | Support | Support | Support | Support | Support | - | - |
| CMA area for MMP for DTV (SSP) | Support | Support | Support | Support | Support | - | N/A |
| CMA area for Lossy compression | Support | Support | Support | Support | Support | - | - |

*1: On M3N, there's no 40-bit physical address space. Therefore, CMA areas are kept in legacy area.

*2: On E3:

- There's no 40-bit physical address space. Therefore, CMA areas are kept in legacy area.
- It does not support DTV (SSP) feature, so the space reserved as CMA area for MMP for DTV (SSP) is not available.
- Lossy compression feature is only available on Board Ebisu-4D.

4.2 Workaround

- **[H/W Restriction No.71 #9]**

When the addresses from multiple translation requests consecutively hit TLB entries in the IPMMU(cache) (used for a single domain), addresses are either incorrectly translated or stalling condition is being reached.

- R-Car M3 Ver.1.x
The software workaround is unnecessary because TLB function of all IPMMU caches is disabled by hardware.
- R-Car H3 Ver.1.x
The software workaround is to use 1GB page size so that all of page table entries are fully cached in a uTLB. Thus, preventing a page fault makes it possible to use two or more master IPs in IPMMU-VP.
- R-Car H3 Ver.2.0
The software workaround is to disable TLB function of all IPMMU caches.

The followings are shown that Memory manager disables TLB function of IPMMU caches which belong to A3VP and A3VC power domain and IPL does the function of IPMMU caches which belong to always-on power domain.

| IPMMU cache | Power Domain | IPL | Memory Manager |
|-------------|--------------|--------|----------------|
| IPMMU-VI0 | Always-on | ✓ | - |
| IPMMU-VI1 | Always-on | ✓ | - |
| IPMMU-VP0 | A3VP | - | ✓ |
| IPMMU-VP1 | A3VP | - | ✓ |
| IPMMU-VC0 | A3VC | - | ✓ |
| IPMMU-VC1 | A3VC | - | ✓ |
| IPMMU-PV0 | Always-on | ✓ | - |
| IPMMU-PV1 | Always-on | ✓ | - |
| IPMMU-PV2 | Always-on | ✓ | - |
| IPMMU-PV3 | Always-on | ✓ | - |
| IPMMU-IR | A3IR | - (*1) | - (*1) |
| IPMMU-HC | Always-on | ✓ | - |
| IPMMU-RT | Always-on | ✓ | - |
| IPMMU-MP | Always-on | ✓ | - |
| IPMMU-DS0 | Always-on | ✓ | - |
| IPMMU-DS1 | Always-on | ✓ | - |

*1: A user need to disable TLB function of IPMMU caches which belong to A3IR.

● **[H/W Restriction No.100]**

When the timing of entry replacement of the TLB cache in the hierarchical IPMMU and the TLB flush occur at the same time, the address translation information may not be returned correctly in some cases.

- R-Car H3 Ver.1.x
The software workaround is same as [No.71 #9].
- R-Car H3 Ver.2.0
The software workaround is same as [No.71 #9].
- R-Car M3 Ver.1.x
The software workaround is same as [No.71 #9].
- R-Car M3N Ver.1.1
The software workaround is to disable TLB function of all IPMMU caches.

The followings are shown that on R-Car M3N Ver.1.1, Memory manager disables TLB function of IPMMU caches which belong to A3VP and A3VC power domain and IPL disables the function of IPMMU caches which belong to always-on power domain.

| IPMMU cache | Power Domain | IPL | Memory Manager |
|-------------|--------------|-----|----------------|
| IPMMU-VI0 | Always-on | ✓ | - |
| IPMMU-VP0 | A3VP | - | ✓ |
| IPMMU-VC0 | A3VC | - | ✓ |
| IPMMU-PV0 | Always-on | ✓ | - |
| IPMMU-HC | Always-on | ✓ | - |
| IPMMU-RT | Always-on | ✓ | - |
| IPMMU-MP | Always-on | ✓ | - |
| IPMMU-DS0 | Always-on | ✓ | - |
| IPMMU-DS1 | Always-on | ✓ | - |

➤ R-Car E3 Ver.1.x

The software workaround is to disable TLB function of all IPMMU caches.

The followings are shown that on R-Car E3 Ver.1.x, Memory manager disables TLB function of IPMMU caches which belong to A3VC power domain and IPL disables the function of IPMMU caches which belong to always-on power domain.

| IPMMU cache | Power Domain | IPL | Memory Manager |
|-------------|--------------|-----|----------------|
| IPMMU-VI0 | Always-on | ✓ | - |
| IPMMU-VP0 | Always-on | ✓ | - |
| IPMMU-VC0 | A3VC | - | ✓ |
| IPMMU-PV0 | Always-on | ✓ | - |
| IPMMU-HC | Always-on | ✓ | - |
| IPMMU-RT | Always-on | ✓ | - |
| IPMMU-MP | Always-on | ✓ | - |
| IPMMU-DS0 | Always-on | ✓ | - |
| IPMMU-DS1 | Always-on | ✓ | - |

4.3 Closed issues

- **[H/W Restriction No.59]**

The master IPs which are in the same bus domain hierarchy cannot use PMB and MMU function at the same time.

Regarding 40-bit physical address space support, we no longer make use of PMB function.
So, this restriction is not applicable.

- **[H/W Restriction No.71 #4]**

The address translation processing in the identical hierarchy when uTLB which uses a PMB change exists, more than one, when it forms, there is a possibility which causes a mis-conversion and a stall.

Regarding 40-bit physical address space support, we no longer make use of PMB function.
So, this restriction is not applicable.

4.4 Known functional limitations of delivered functions

None.

4.5 Non-validated function

None.

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| REVISION HISTORY | | Memory Manager for Linux Release Note: Software | |
|------------------|-----------|--|---|
| Rev. | Date | Description | |
| | | Page | Summary |
| 2.12.0 | Aug. 2016 | — | New version |
| 2.16.0 | Jan. 2017 | 2 | Update commit ID and document version |
| | | 3 | Add Section 3.3 |
| | | 4 | Because of adding IPMMU (PMB) support for 40 bit address space of CMA area for Lossy compression, - Change the description in section 4.1 - Update the table in section 4.1 - Add the description in section 4.3 |
| 2.17.0 | Mar. 2017 | 2 | Update commit ID and document version |
| | | 3 | Add Section 3.4 |
| | | 4 | Due to [H/W Restriction No.71 #4], - Change the description in section 4.1 - Update the table in section 4.1 - Delete the description in section 4.3 |
| 2.19.0 | Apr. 2017 | 2 | Update document version |
| | | 3 | Add Section 3.5 |
| | | 4 | Update the table in Section 4.1 |
| 2.21.0 | Jun. 2017 | 2 | Update commit ID and document version |
| | | 3 | Add Section 3.6 |
| | | 4 | Update the table in Section 4.1 |
| | | 4 | Add [H/W Restriction No.71 #9] in Section 4.2 |
| | | 4 | Move [H/W Restriction No.59] and [H/W Restriction No.71 #4] in Section 4.3 |
| 2.23.0 | Aug. 2017 | 2 | Update commit ID and document version |
| | | 3 | Add Section 3.7 |
| 2.23.1 | Nov. 2017 | 2 | Update commit ID and document version |
| | | 4 | Add Section 3.8 |
| | | 5 | Update the table in Section 4.1 for M3N |
| 3.4.0 | Jan. 2018 | 2 | Update commit ID and document version |
| | | 4 | Add Section 3.9 |
| | | 5, 6 | Update [H/W Restriction No.71 #9] in Section 4.2 |
| | | 6, 7 | Add [H/W Restriction No.100] in Section 4.2 |
| 3.6.0 | Mar. 2018 | 2 | Update commit ID and document version |
| | | 4 | Add Section 3.10 |
| | | 5 | Update the table in Section 4.1 for E3 |
| | | 6, 7 | Update [H/W Restriction No.100] in Section 4.2 |
| 3.7.0 | Apr. 2018 | 2 | Update commit ID and document version |
| | | 4 | Add Section 3.11 |
| | | 5 | Update the table in Section 4.1 for H3 Ver.3.0 |
| | | 5 | Update Notices about space reserved as CMA area for Lossy compression feature on R-Car E3 |
| 3.9.0 | Jun. 2018 | 2 | Update document version |
| | | 3, 14 | Revise M3 SoC revision information |
| | | 4 | Revise M3N SoC revision information |
| | | 4 | Add Section 3.12 |
| 3.9.0.1 | Oct. 2018 | 2 | Update commit ID and document version |
| | | 4 | Add Section 3.13 |

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| | | | |
|--------|---------------|------|---|
| 3.15.0 | Dec. 2018 | — | Update Address List |
| | | 2 | Update commit ID and document version |
| | | 5 | Add Section 3.14 |
| | | 6 | Update the table in Section 4.1 for E3 Ver.1.1 |
| | | 6 | Update Notices about space reserved as CMA area for Lossy compression feature on R-Car E3 |
| | | 7, 8 | Update IPMMU caches information in H/W restriction No.71 #9 and No.100 |
| 3.19.0 | Apr. 2019 | — | Update Address List |
| | | 2 | Update commit ID and document version |
| | | 5 | Add Section 3.15 |
| | | 6 | Update the table in Section 4.1 |
| 3.21.0 | Jun. 2019 | 2 | Update commit ID and document version |
| | | 5 | Add Section 3.16 |
| | | 6 | Update the table in Section 4.1 |
| 5.1.0 | Apr. 21, 2021 | — | Update Address List |
| | | 2 | Update commit ID and document version |
| | | 5 | Add Section 3.17 |
| 5.5.0 | Aug. 26, 2021 | 2 | Update commit ID |
| | | 5 | Add Section 3.18 |
| 5.9.0 | Dec.10, 2021 | — | Update Notice |
| | | 2 | Update commit ID and document version |
| | | 5 | Add Section 3.19 |
| 5.10.0 | Dec. 25, 2023 | - | Add Kernel 5.10.194 |

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Memory Manager for Linux

Release Note: Software



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