

# 1. Overview

## 1.1 Overview

This manual explains the driver module (this module) that controls the Memory Management Unit for H/W IP (IPMMU) on R-Car H3/M3/M3N/E3/D3/V3U and R-Car V3H Ver.2.0.

## 1.2 Function

This module controls IPMMU that is compatible with the ARMv8 Virtual Memory System Architecture (VMSA) page tables. It is based on Input/Output MMU (IOMMU) framework of standard Linux.

**Table 1.1 Function list (R-Car H3/M3/M3N/D3/E3/V3H)**

| H/W Features  | S/W Functions Support Status                      |
|---|---|
| MMU architecture compatible with Armv8 VMSAv8-64 and VMSAv8-32 including the LPAE | Only support for VMSAv8-32                        |
| Support Privileged space Mapping Buffer (PMB) address translation                 | Not support                                       |
| Page size information in VMSAv8-32  | Only support 4KB page size                        |
| Support Performance monitoring for Armv8 VMSAv8-64 and VMSAv8-32 LPAE             | Not support                                       |
| Stage-2 Address Translation support   | Not support                                       |
| Support multiple Operating System (OS-ID)   | Not support                                       |
| Secure/Non-Secure bank support  | Support Non-Secure bank only                      |
| Number of the MMU context support   | 8   |
| Number of micro-TLB support   | 32  |
| Support Error Handling  | Not support                                       |
| Provide address translation for bus masters outside of the CPU                    | Support   |
| Support ASID  | Not support                                       |
| System Suspend to RAM   | Support (*), except for R-Car D3/V3H Ver.2.0 (**) |

Note:

\* This feature is enabled by default, please refer to R-Car Series, 3rd Generation Power Management Software User's Manual for more details.

\*\* R-Car D3/V3H Ver.2.0 does not support System Suspend to RAM.

**Table 1.2 Function list (R-Car V3U)**

| H/W Features  | S/W Functions Support Status |
|---|------------------------------|
| MMU architecture compatible with Armv8 VMSAv8-64 and VMSAv8-32 including the LPAA | Only support for VMSAv8-32   |
| Support Privileged space Mapping Buffer (PMB) address translation                 | Not support                  |
| Page size information in VMSAv8-32  | Only support 4KB page size   |
| Support Performance monitoring for Armv8 VMSAv8-64 and VMSAv8-32 LPAA             | Not support                  |
| Stage-2 Address Translation support   | Not support                  |
| Support multiple Operating System (OS-ID)   | Not support                  |
| Region-ID   | Not support                  |
| Secure/Non-Secure bank support  | Support Non-Secure bank only |
| Number of micro-TLB support   | 64                           |
| Number of the MMU context support   | 16                           |
| MMU QoS setting   | Not support                  |
| Support Error Handling  | Not support                  |
| Provide address translation for bus masters outside of the CPU                    | Support                      |
| Support ASID  | Not support                  |
| System Suspend to RAM   | Not support (*)              |

Note:

\* Please refer to the latest R-Car Series, 3rd Generation BSP Software Release Note for more detail.

## 1.3 Reference

### 1.3.1 Standard

There is no reference document on standards.

### 1.3.2 Related Document

The following table shows the document related to this module.

**Table 1.3 Related Documents**

| Reference No. | Issue               | Title  | Edition  | Date          |
|---------------|---------------------|--|----------|---------------|
| -             | Renesas Electronics | R-Car Series, 3rd Generation User's Manual: Hardware                               | Rev.2.20 | Jun. 30, 2020 |
| -             | Renesas Electronics | R-Car V3H_2 Additional Document for User's Manual: Hardware                        | Rev.0.50 | Jul. 31, 2020 |
| -             | Renesas Electronics | R-Car V3U Series User's Manual   | Rev.0.5  | Jul. 31, 2020 |
| -             | Renesas Electronics | R-CarH3-SiP System Evaluation Board Salvator-X Hardware Manual RTP0RC7795SIPB0011S | Rev.1.09 | May. 11, 2017 |
| -             | Renesas Electronics | R-CarM3-SiP System Evaluation Board Salvator-X Hardware Manual RTP0RC7796SIPB0011S | Rev.0.04 | Oct. 3, 2016  |
| -             | Renesas Electronics | R-CarH3-SiP/M3-SiP/M3N-SiP System Evaluation Board Salvator-XS Hardware Manual     | Rev.2.04 | Jul. 17, 2018 |
| -             | Renesas Electronics | R-CarE3 System Evaluation Board Ebisu Hardware Manual RTP0RC77990SEB0010S          | Rev.0.03 | Apr. 11, 2018 |
| -             | Renesas Electronics | R-CarE3 System Evaluation Board Ebisu-4D (E3 board 4xDRAM) Hardware Manual         | Rev.1.01 | Jul. 19, 2018 |
| -             | Renesas Electronics | R-CarD3 System Evaluation Board Hardware Manual RTP0RC77995SEB0010S                | Rev.1.20 | Jul. 25, 2017 |
| -             | Renesas Electronics | R-CarV3U System Evaluation Board Falcon Hardware Manual                            | Rev.0.01 | Sep. 11, 2020 |
| -             | Renesas Electronics | R-CarV3H System Evaluation Board Condor-I Hardware Manual                          | Rev.0.02 | Nov. 11, 2019 |

## 1.4 Restrictions

Below table shows the correction status on R-Car series, 3rd Generation.

**Table 1.4 Correction status on R-Car Series, 3rd Generation**

| H/W<br>Restriction<br>list | R-Car Series, 3rd Generation |                        |                        |                        |                         |             |                        |              |                         |
|----------------------------|------------------------------|------------------------|------------------------|------------------------|-------------------------|-------------|------------------------|--------------|-------------------------|
|                            | R-Car<br>H3<br>Ver.2.0       | R-Car<br>H3<br>Ver.3.0 | R-Car<br>M3<br>Ver.1.x | R-Car<br>M3<br>Ver.3.0 | R-Car<br>M3N<br>Ver.1.1 | R-Car<br>D3 | R-Car<br>E3<br>Ver.1.x | R-Car<br>V3U | R-Car<br>V3H<br>Ver.2.0 |
| Restriction<br>No.71#1     | No                           | Yes                    | No                     | Yes                    | Yes                     | Yes         | Yes                    | Yes          | Yes                     |
| Restriction<br>No.71#2     | No                           | Yes                    | No                     | Yes                    | Yes                     | Yes         | Yes                    | Yes          | Yes                     |
| Restriction<br>No.71#3     | No                           | Yes                    | No                     | Yes                    | Yes                     | No          | Yes                    | Yes          | Yes                     |
| Restriction<br>No.71#5     | No                           | Yes                    | No                     | Yes                    | Yes                     | Yes         | Yes                    | Yes          | Yes                     |
| Restriction<br>No.71#6     | No                           | Yes                    | No                     | Yes                    | Yes                     | Yes         | Yes                    | Yes          | Yes                     |
| Restriction<br>No.71#7     | No                           | Yes                    | No                     | Yes                    | Yes                     | Yes         | Yes                    | Yes          | Yes                     |
| Restriction<br>No.71#8     | No                           | Yes                    | No                     | Yes                    | Yes                     | Yes         | Yes                    | Yes          | Yes                     |
| Restriction<br>No.71#9     | No                           | Yes                    | No                     | Yes                    | Yes                     | Yes         | Yes                    | Yes          | Yes                     |
| Restriction<br>No.100      | No                           | Yes                    | No                     | Yes                    | No                      | No          | No                     | Yes          | Yes                     |
| Restriction<br>No.102      | No                           | No                     | No                     | No                     | No                      | No          | No                     | No           | No                      |

**1.4.1 Known issues****[H/W Restriction No.71 #1]**

micro-TLB performs wrong address translation when individual micro-TLB flush or micro-TLB context referenced IPMMU(cache) flush operation is executed during ongoing bus master activity.

Workaround: Flush IPMMU (cache) or micro-TLB operation must only be performed while corresponding bus master is idle (no bus activity). However, it's not implemented on IPMMU driver.

**[H/W Restriction No.71 #2]**

Two notification for IPMMU in conjunction with DMA has to be considered:

Notification 1: Enabling IPMMU address translation for more than one channel per SYS-DMAC/RT-DMAC/AUDIO-DMAC module does not work correctly.

Notification 2: When IPMMU is enabled and DMAC transfer of 16 bytes or more is performed, read data transactions from DRAM might be interleaved with IPMMU address translation maintenance bus transactions. As a result, the on-going DMA data transfer operation might hang-up.

Workaround:

For notification 1:

- If more than one channel per DMAC is being used, disable IPMMU and use descriptor based transfer mode operating on physical address ranges. Consequently, DMACs have to be controlled by host OS in virtualized environment.

For notification 2:

- When using IPMMU, restrict DMA transfer not to exceed 16 bytes.
- Do not use the IPMMU address translation function. Access to 40-bit address space can be enabled by using DMAC extended address function register.
- Hang-up can be avoided by restricting the DMA data transfer to MMU page boundaries i.e. when 1 GB MMU page granularity is used, DMA transfer might be performed within 1 GB page boundaries.

The workaround requires disable IPMMU address translation function. However, it's not implemented on IPMMU driver.

**[H/W Restriction No.71 #6]**

4K page TLB merge functionality (default setting) in IPMMU(main) is not supported.

Workaround: Disable 4 KB page TLB merging functionality before enabling IPMMU functionality. However, it's not implemented on IPMMU driver.

**[H/W Restriction No.71 #7]**

Automatic IPMMU context selection by os\_id passing mechanism does not work correctly in IPMMU-PV (3D GPU) and IPMMU-VC (iVDP1c & VCP4).

Workaround: For multiple MMU context use case:

- In case of 3D GPU virtualization, 3D GPU MMU is to be used instead of IPMMU.
- In case of video codec virtualization, separation and arbitration of guest OS video codec functionality is to be implemented by the host OS driver.

**[H/W Restriction No.71 #9]**

When the addresses from multiple translation requests consecutively hit TLB entries in the IPMMU(cache) (used for a single domain), addresses are either incorrectly translated or stalling condition is being reached.

Workaround: The software workaround is to disable TLB function of all IPMMU caches.

For R-Car M3 Ver.1.x, the TLB function of all IPMMU caches is disabled by hardware.

The following table shows that on R-Car H3 Ver.2.0, IPL disables TLB function of IPMMU caches which belong to always-on power domain. However, disabling A3VP, A3VC, A3IR power domain is not implemented on IPMMU driver.

**Table 1.5 IPL disables TLB cache function of IPMMU caches (always-on power domain) on H3 Ver.2.0**

| IPMMU cache | Power Domain | IPL |
|-------------|--------------|-----|
| IPMMU-VI0   | Always-on    | √   |
| IPMMU-VI1   | Always-on    | √   |
| IPMMU-VP0   | A3VP         | -   |
| IPMMU-VP1   | A3VP         | -   |
| IPMMU-VC0   | A3VC         | -   |
| IPMMU-VC1   | A3VC         | -   |
| IPMMU-PV0   | Always-on    | √   |
| IPMMU-PV1   | Always-on    | √   |
| IPMMU-PV2   | Always-on    | √   |
| IPMMU-PV3   | Always-on    | √   |
| IPMMU-IR    | A3IR         | -   |
| IPMMU-HC    | Always-on    | √   |
| IPMMU-RT    | Always-on    | √   |
| IPMMU-MP    | Always-on    | √   |
| IPMMU-DS0   | Always-on    | √   |
| IPMMU-DS1   | Always-on    | √   |

**[H/W Restriction No.100]**

When the timing of entry replacement of the TLB cache in the hierarchical IPMMU and the TLB flush occur at the same time, the address translation information may not be returned correctly in some cases.

Workaround: The software workaround is to disable TLB function of all IPMMU caches.

For R-Car H3 Ver.2.0, M3 Ver.1.x, the software workaround is same as **[H/W Restriction No.71 #9]**

The following table shows that on R-Car M3N Ver.1.1 and E3 Ver.1.x, IPL disables TLB function of IPMMU caches which belong to always-on power domain. However, disabling A3VP, A3VC, A3IR power domain is not implemented on IPMMU driver.

**Table 1.6 IPL disables TLB cache function of IPMMU caches (always-on power domain) on M3N Ver.1.1**

| IPMMU cache | Power Domain | IPL |
|-------------|--------------|-----|
| IPMMU-VI0   | Always-on    | √   |
| IPMMU-VP0   | A3VP         | -   |
| IPMMU-VC0   | A3VC         | -   |
| IPMMU-PV0   | Always-on    | √   |
| IPMMU-HC    | Always-on    | √   |
| IPMMU-RT    | Always-on    | √   |
| IPMMU-MP    | Always-on    | √   |
| IPMMU-DS0   | Always-on    | √   |
| IPMMU-DS1   | Always-on    | √   |

**Table 1.7 IPL disables TLB cache function of IPMMU caches (always-on power domain) on E3 Ver.1.x**

| IPMMU cache | Power Domain | IPL |
|-------------|--------------|-----|
| IPMMU-VI0   | Always-on    | √   |
| IPMMU-VP0   | Always-on    | √   |
| IPMMU-VC0   | A3VC         | -   |
| IPMMU-PV0   | Always-on    | √   |
| IPMMU-HC    | Always-on    | √   |
| IPMMU-RT    | Always-on    | √   |
| IPMMU-MP    | Always-on    | √   |
| IPMMU-DS0   | Always-on    | √   |
| IPMMU-DS1   | Always-on    | √   |

**1.4.2 Closed issues****[H/W Restriction No.71 #3]**

PMB Address translation is not working correctly in 2 stage address translation mode.

This module doesn't support PMB address translation. Therefore, this issue is not applicable.

**[H/W Restriction No.71 #5]**

Using 2 stage address translation will always generate internal 4K page granularity translation requests for 2nd stage translation.

This module supports 4 KB page size only. Therefore, this issue is not applicable.

**[H/W Restriction No.71 #8]**

Two different behaviors in case of assigned page sizes:

Case 1: When 512MB page size is used, which is supported by ARMv8 VMSAv8-64s, an incorrect address translation might occur.

Case 2: When 64KB page size is set it will be treated as 4KB page size

This module supports VMSAv8-32 only. Therefore, this issue is not applicable.

**[H/W Restriction No.85]**

In case of the usage which allocate the Page Table of IPMMU to SystemRAM, deadlock will be occurred when there are Page Table Walk by IPMMU and DRAM access by IPs.

This module doesn't support SystemRAM. Therefore, this issue is not applicable.

**[H/W Restriction No.102]**

In case applying a virtual address space equal or less than 128MB, an unexpected interrupt is generated by TBL flush operation.

When the virtual address space is set to 128MB or less in the TSZ0/TSZ1 field of IMTTBCRn registers, a not valid conversion/translation fault by the TLB flash operation is detected and an interrupt is generated, if the interrupt is activated by IMCTRN registers.

Workaround: Avoid using the virtual address space to 128 MB or less.

Step1) Set TSZ 0 and TSZ 1 for 256 MB ([VMSAv 8-64] TSZ 0/TSZ 1 = 6'h24 or [VMSAv 8-32] TSZ 0/TSZ 1 = 3'h4)

Step2) Set TLB to restrict unnecessary higher virtual address space 128MB

This module doesn't apply a virtual address space equal or less than 128MB. Therefore, this issue is not applicable.



## 1.5 Notice

- When IPMMU support is enabled, there is a possibility of performance degradation because of the translation fault and management overhead such as a page table walk.
- Some TLB maintenances between an IPMMU and the connected micro-TLBs are performed automatically by hardware. In case that the flush operation is performed via IMCTRN (IMCTRN FLUSH=1), all the micro-TLB which is related to the same MMU tables are applied the TLB flush and clear the all TLB entry in micro-TLB.
- The IPMMU has two register banks, for secure and non-secure modes. Besides H/W restriction No. 85, secure mode operation has not been documented clearly. Therefore, it's currently not implemented in this module.
- The number of contexts varies with generation and instance. For R-Car Series, 3rd Generation, R-Car V3H they supports 8 contexts and for R-Car V3U, it supports 16 contexts.
- R-Car V3H Ver.2.0 **DOESN'T** support IPMMU.
- In current IPMMU driver implementation, each context is mapped to one domain. One domain is associated with each device, one or more micro-TLBs for a single device are kept in the same domain.
- The IPMMU doesn't support module stop control. The IPMMU can be used whenever a master requires address translation through the IPMMU.
- Before a master access, the corresponding micro-TLB must be configured.
- The communication between micro-TLB, IPMMU cache and main IPMMU is described as below:

In case that MMUEN bit of both IMUCTR and IMCTR is set to "1", address translation feature is enabled. After receiving the request from Master IP, micro-TLB search the address translation information which are kept in itself.

When address translation information is kept in the micro-TLB entries, return this information to Master IP immediately. When address translation information are not kept in the micro-TLB, micro-TLB issue the page table walk request to IPMMU cache via common AXI in each hierarchy.

After receiving the page table walk request to IPMMU cache, IPMMU cache search the address translation information in IPMMU cache by similar manner.

When address translation information is kept in the cache entries of IPMMU cache, then return this information to micro-TLB and Master IP as well. On the other hand, address translation information is not kept in the IPMMU cache, page table walk request is issued from IPMMU cache to main IPMMU as well via common AXI interface.

Once main IPMMU receive the page table walk request from IPMMU cache, search TLB-RAM to check whether the target address information exist or not and return address information to IPMMU cache in the same manner.

## 2. Terminology

The following table shows the terminology related to this module.

**Table 2.1 Terminology**

| Terms   | Explanation  |
|---------|--|
| MMU     | <u>M</u> emory <u>M</u> anagement <u>U</u> nit                     |
| IPMMU   | <u>MMU</u> for H/W <u>IP</u>                                       |
| VMSA    | <u>V</u> irtual <u>M</u> emory <u>S</u> ystem <u>A</u> rchitecture |
| IOMMU   | <u>I</u> nput/ <u>O</u> utput <u>MMU</u>                           |
| LPAE    | <u>L</u> arge <u>P</u> hysical <u>A</u> ddress <u>E</u> xtension   |
| PMB     | <u>P</u> rivileged space <u>M</u> apping <u>B</u> uffer            |
| TLB     | <u>T</u> ranslation <u>L</u> ookaside <u>B</u> uffer               |
| uTLB    | <u>Micro TLB</u>   |
| DMA     | <u>D</u> irect <u>M</u> emory <u>A</u> ccess                       |
| DMAC    | <u>DMA C</u> ontroller   |
| DMAE    | <u>DMA E</u> ngine   |
| AXI     | <u>A</u> dvanced e <u>X</u> tensible <u>I</u> nterface             |
| MMNGR   | <u>M</u> emory <u>M</u> anager                                     |
| OS-ID   | Multiple <u>O</u> perating <u>S</u> ystem <u>ID</u>                |
| ASID    | <u>A</u> ddress <u>S</u> pace <u>ID</u>                            |
| RT-DMAC | <u>R</u> ead- <u>T</u> ime <u>DMAC</u>                             |

The following table shows the correspondence between each IPMMU and each bus domain.

**Table 2.2 IPMMU naming**

| IPMMU      | Bus Domain                         |
|------------|------------------------------------|
| IPMMU-VI0  | VIO (Video IO) domain AXI          |
| IPMMU-VI1  | VIO (Video IO) domain AXI          |
| IPMMU-VP0  | VP (Video Processor) domain AXI    |
| IPMMU-VP1  | VP (Video Processor) domain AXI    |
| IPMMU-VC0  | VC (Video Codec) domain AXI        |
| IPMMU-VC1  | VC (Video Codec) domain AXI        |
| IPMMU-PV0  | 3DG (3D-Graphics) domain AXI       |
| IPMMU-PV1  | 3DG (3D-Graphics) domain AXI       |
| IPMMU-PV2  | 3DG (3D-Graphics) domain AXI       |
| IPMMU-PV3  | 3DG (3D-Graphics) domain AXI       |
| IPMMU-IR   | IMP domain AXI                     |
| IPMMU-HC   | HC (High Communication) domain AXI |
| IPMMU-RT0  | RT (Real Time) domain AXI          |
| IPMMU-RT1  | RT (Real Time) domain AXI          |
| IPMMU-MP   | Audio domain AXI                   |
| IPMMU-DS0  | Peripheral domain AXI              |
| IPMMU-DS1  | Peripheral domain AXI              |
| IPMMU-MM   | Main Memory domain AXI             |
| IPMMU-VIP0 | VIP (Vision IP) domain AXI         |
| IPMMU-VIP1 | VIP (Vision IP) domain AXI         |
| IPMMU-3DG  | 3DG (3D-Graphics) domain AXI       |

## 3. Operating Environment

### 3.1 Hardware Environment

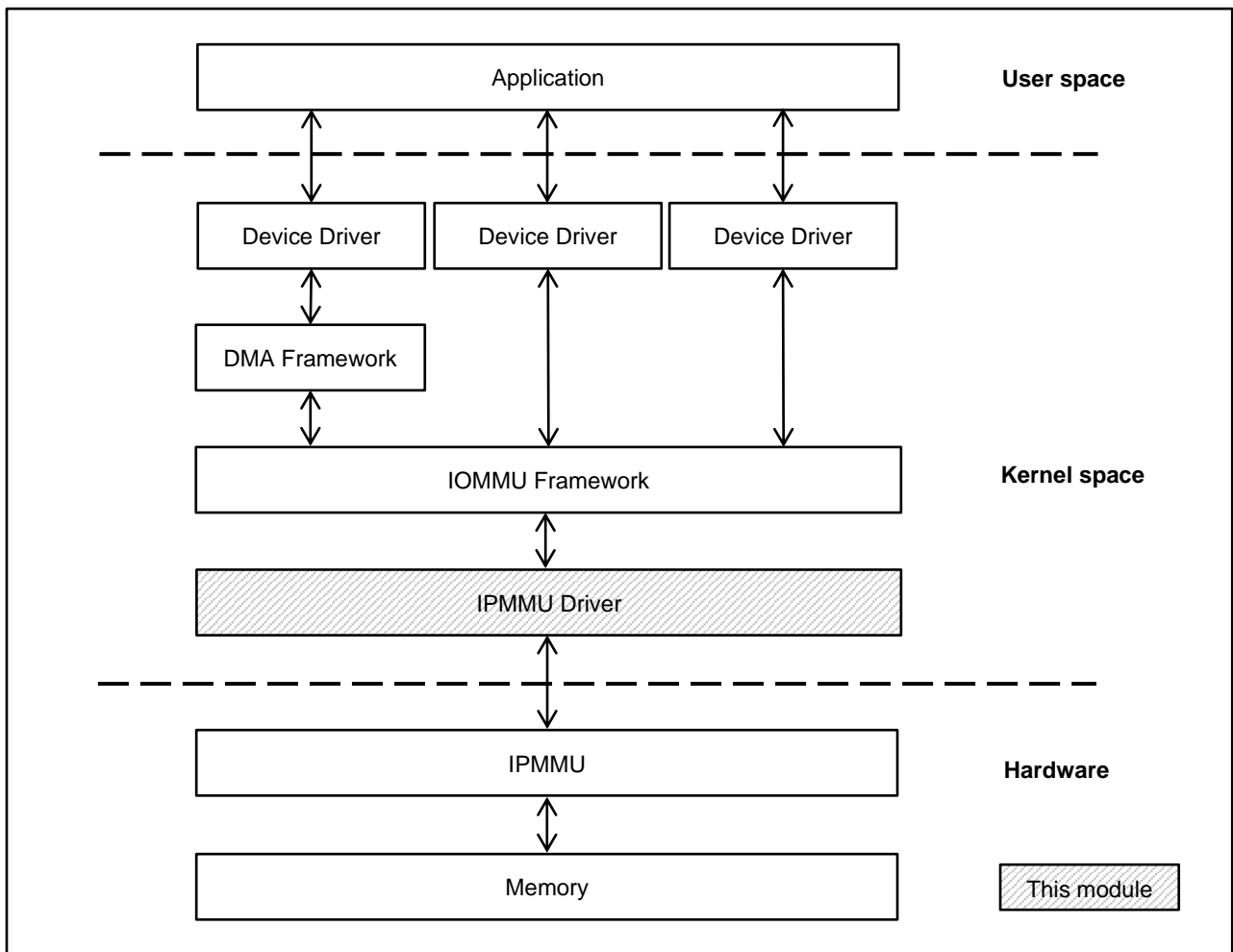
The following table lists the hardware needed to use this module.

**Table 3.1 Hardware environment**

| Name   | Version | Manufacture         |
|--|---------|---------------------|
| R-CarH3-SiP/M3-SiP System Evaluation Board Salvator-X          | -       | Renesas Electronics |
| R-CarH3-SiP/M3-SiP/M3N-SiP System Evaluation Board Salvator-XS | -       | Renesas Electronics |
| R-CarE3 System Evaluation Board Ebisu                          | -       | Renesas Electronics |
| R-CarE3 System Evaluation Board Ebisu-4D                       | -       | Renesas Electronics |
| R-CarD3 System Evaluation Board Draak                          | -       | Renesas Electronics |
| R-CarV3U System Evaluation Board Falcon                        | -       | Renesas Electronics |
| R-CarV3H System Evaluation Board Condor-I                      | -       | Renesas Electronics |

### 3.2 Module Configuration

The following figure shows the configuration of this module.



**Figure 3.1 Module Configuration (R-Car H3/M3/M3N/E3/D3/V3U/V3H)**

### **3.3 State Transition Diagram**

There is no state transition diagram for this module.

## **4. External Interface**

Linux kernel provides a sysfs interface to user about IOMMU groups' information.  
It can be accessed via /sys/kernel/iommu\_groups/

Please see [https://www.kernel.org/doc/Documentation/ABI/testing/sysfs-kernel-iommu\\_groups](https://www.kernel.org/doc/Documentation/ABI/testing/sysfs-kernel-iommu_groups) for more detail.

## 5. Integration

### 5.1 Directory Configuration

The directory configuration is shown below.

```

—— driver/iommu/
    |
    └─ ipmmu-vmsa.c :Renesas R-Car H3/M3/M3N/E3/D3/V3U/V3H IPMMU driver source file
  
```

**Figure 5.1 Directory configuration (R-Car H3/M3/M3N/E3/D3/V3U/V3H)**

### 5.2 Integration Procedure

To enable the function of this module, make the following setting with Kernel Configuration.

```

Device Drivers --->
    [*] IOMMU Hardware Support --->
        [*] Renesas VMSA-compatible IPMMU
            (8)    Input MMU number of MMU's really used
  
```

**Figure 5.2 Kernel configuration (R-Car H3/M3/M3N/E3/D3/V3U/V3H)**

For R-Car H3/M3/M3N/E3/D3/V3H:

In case of making the 8<sup>th</sup> MMU context reservation for MMNGR, change “Input MMU number of MMU's really used” from 8 to 7, the resource assignment is below:

- MMUn (n = 0 to 6) contexts are for IPMMU driver.
- MMUn (n = 7) context is for MMNGR driver.

## 5.3 IPMMU setting

### 5.3.1 Device tree description

For example, R8A77951 IPMMU-DS0 and DMAC0 bus master are described in (arch/arm64/boot/dts/renesas/r8a77951.dtsi) as below:

```

ipmmu_ds0: mmu@e6740000 {
    compatible = "renesas,ipmmu-r8a7795";
    reg = <0 0xe6740000 0 0x1000>;
    renesas,ipmmu-main = <&ipmmu_mm 0>;
    #iommu-cells = <1>;
    status = "disabled";
};

dmac0: dma-controller@e6700000 {
    ...
    iommus = <&ipmmu_ds0 0>, <&ipmmu_ds0 1>,
             <&ipmmu_ds0 2>, <&ipmmu_ds0 3>,
             <&ipmmu_ds0 4>, <&ipmmu_ds0 5>,
             <&ipmmu_ds0 6>, <&ipmmu_ds0 7>,
             <&ipmmu_ds0 8>, <&ipmmu_ds0 9>,
             <&ipmmu_ds0 10>, <&ipmmu_ds0 11>,
             <&ipmmu_ds0 12>, <&ipmmu_ds0 13>,
             <&ipmmu_ds0 14>, <&ipmmu_ds0 15>;
};

```

**Figure 5.3 Example for IPMMU-DS0 and DMAC0 bus master in R-Car H3 device tree**

Above example demonstrates Multi-master IOMMU model for IOMMU description that is currently used in this module.

Please see below Linux kernel documentation for more detail:

- <https://www.kernel.org/doc/Documentation/devicetree/bindings/iommu/iommu.txt>.
- <https://www.kernel.org/doc/Documentation/devicetree/bindings/iommu/renesas%2Cipmmu-vmesa.txt>

Note 1: To confirm the base address for each IPMMU cache (in the example, IPMMU-DS0 base address is e6740000), please refer to “Table 16.2 IPMMU Base Address and Power domain” in Hardware User’s Manual for more detail.

Note 2: Each master is connected to one micro-TLB. To know more about micro-TLB assignment, please refer to chapter “16.4 micro-TLB Assignment” in Hardware User’s Manual for more detail.

### 5.3.2 How to enable IPMMU support

Below table shows the current status of BSP drivers that support IPMMU.

**Table 5.1 Current IPMMU support status on BSP drivers**

| BSP drivers | IPMMU support status and describe how to enable IPMMU |               |               |               |               |               |                   |
|-------------|---|---------------|---------------|---------------|---------------|---------------|-------------------|
|             | R-Car H3  | R-Car M3      | R-Car M3N     | R-Car E3      | R-Car D3      | R-Car V3U     | R-Car V3H Ver.2.0 |
| DU          | √   | √             | √             | √             | √             | √             | √                 |
| MSIOF       | √   | √             | √             | √             | √             | √             | Not support       |
| SATA        | √   | Not available | √             | Not available | Not available | Not available | Not available     |
| SCIF        | √   | √             | √             | √             | √             | √             | √                 |
| SD/MMC (*)  | √   | √             | √             | √             | √             | √             | √                 |
| USB2H       | √   | √             | √             | √             | √             | Not available | Not available     |
| USB3H       | √   | √             | √             | √             | Not available | Not available | Not available     |
| VIN         | √   | √             | √             | √             | √             | √             | √                 |
| SYS-DMAC    | √   | √             | √             | √             | √             | √             | √                 |
| RT-DMAC     | Not support   | Not support   | Not support   | Not support   | Not support   | √             | √                 |
| Audio       | √   | √             | √             | √             | √             | Not available | Not available     |
| Ethernet    | √   | √             | √             | √             | √             | √             | Not support       |
| GEther      | Not available   | Not available | Not available | Not available | Not available | Not available | √                 |
| PCIe        | √   | √             | √             | √             | Not available | √             | √                 |
| USB2F       | √   | √             | √             | √             | √             | Not available | Not available     |
| USB3F       | √   | √             | √             | √             | Not available | Not available | Not available     |
| I2C         | √   | √             | √             | √             | √             | √             | √                 |
| IMP         | Not support   | Not support   | Not available | Not available | Not available | Not support   | Not support       |
| IMR         | Not support   | Not support   | Not support   | Not support   | Not support   | Not support   | Not support       |
| HDMI        | Not support   | Not support   | Not support   | Not available | Not available | Not available | Not available     |

Note:

\* eMMC is enabled IPMMU by default:

- SDHI2 for R-Car H3/M3/M3N SoC on Renesas Salvator-X board.
- SDHI3 for R-Car E3 SoC on Renesas Ebisu board.
- SDHI2 for R-Car D3 SoC on Renesas Draak board.
- MMC0 for R-Car V3U SoC on Renesas Falcon board.
- MMC0 for R-Car V3H Ver.2.0 SoC on Renesas Condor-I board.



From Linux kernel v4.14 onwards, R-Car H3 Ver.1.x device tree (under arch/arm64/boot/dts/renesas/r8a77995-es1.dtsi) is inherited from R-Car H3 Ver.3.0 device tree (i.e. r8a7795.dtsi under same directory).

Therefore, when enabling IPMMU setting for R-Car H3 Ver.3.0 to support IPMMU in specific BSP drivers, modify R-Car H3 Ver.1.x device tree is also required to override obsolete or conflict iommu nodes and vice versa. Please refer to **chapter 5.3.2.1** for more detail.

The following description explains how to enable IPMMU for all support BSP drivers. Please delete unnecessary parts in corresponding files at arch/arm64/boot/dts/renesas/:

- r8a77950.dtsi (R-Car H3 Ver.1.x)
- r8a77951.dtsi (R-Car H3 Ver.2.0/Ver.3.0)
- r8a77960.dtsi (R-Car M3 Ver.1.x)
- r8a77961.dtsi (R-Car M3 Ver.3.0)
- r8a77965.dtsi (R-Car M3N)
- r8a77990-es10.dtsi (R-Car E3 Ver.1.0)
- r8a77990.dtsi (R-Car E3 Ver.1.1)
- r8a77995.dtsi (R-Car D3)
- r8a779a0.dtsi (R-Car V3U)
- r8a77980.dtsi (R-Car V3H Ver.2.0)

("-": Delete a description (default setting), "+": Setting after the modification)

Some R-Car Series, 3rd Generation SoCs have hardware restrictions for IPMMU (Please check **chapter 1.4** for more information), to ensure that the SoC can use IPMMU correctly please refer to the support SoCs listed as below:

- R-Car H3 Ver.3.0 or later
- R-Car M3 Ver.3.0 or later
- R-Car M3N
- R-Car E3
- R-Car D3
- R-Car V3U
- R-Car V3H Ver.2.0

The supported devices are describe in **Table 5.1**

- For unsupported R-Car Series, 3<sup>rd</sup> Generation SoCs, IPMMU will not operate for master devices.
- For unsupported IPMMU master devices, IPMMU will not do address translation.
- For unsupported or incorrect uTLB assignment, IPMMU operation are not guaranteed. Please make sure to confirm the uTLB assignment (as described in **chapter 5.3.2.1 – 5.3.2.5**) in advance.

### 5.3.2.1 For R-Car H3 Ver.2.0/Ver.3.0 (R8A77951)

Edit both r8a7795.dtsi (left column) and r8a7795-es1.dtsi (right one) as below:

a) Enable common IPMMU DT node

| Drivers | r8a77951.dtsi   | r8a77950.dtsi   |
|---------|---|---|
| All     | <pre>ipmmu_mm: iommu@e67b0000 {     ...     -     status = "disabled"; };</pre> | <pre>+ &amp;ipmmu_mm { +     status = "disabled"; + }; + + &amp;ipmmu_vi0 {</pre> |

b) Enable corresponding IPMMU cache

| Drivers  | r8a77951.dtsi   | r8a77950.dtsi  |
|--|---|--|
| Display,<br>Video capture  | <pre>ipmmu_vi0: iommu@febd0000 {     ...     -     status = "disabled"; };  ipmmu_vil: iommu@febe0000 {     ...     -     status = "disabled"; };</pre> | <pre>&amp;ipmmu_vi0 { +     status = "disabled"; };  &amp;ipmmu_vp0 {</pre>        |
| PCIe, SATA,<br>USB 2.0 Host,<br>USB 3.0 Host,<br>USB 2.0<br>Function,<br>USB 3.0<br>Function | <pre>ipmmu_hc: iommu@e6570000 {     ...     -     status = "disabled"; };</pre>   | <pre>+ &amp;ipmmu_hc { +     status = "disabled"; + }; + + &amp;ipmmu_vi0 {</pre>  |
| Audio  | <pre>ipmmu_mp0: iommu@ec6700000 {     ...     -     status = "disabled"; };</pre>   | <pre>+ &amp;ipmmu_mp0 { +     status = "disabled"; + }; + + &amp;ipmmu_vi0 {</pre> |
| DMAC (DMAC0),<br>I2C,<br>SCIF, MSIOF,<br>Ethernet  | <pre>ipmmu_ds0: iommu@e6740000 {     ...     -     status = "disabled"; };</pre>  | <pre>+ &amp;ipmmu_ds0 { +     status = "disabled"; + }; + + &amp;ipmmu_vi0 {</pre> |
| DMAC (DMAC1,<br>DMAC2), I2C,<br>SCIF, MSIOF,<br>SDHI/MMC                                     | <pre>ipmmu_ds1: iommu@e7740000 {     ...     -     status = "disabled"; };</pre>  | <pre>+ &amp;ipmmu_ds1 { +     status = "disabled"; + }; + + &amp;ipmmu_vi0 {</pre> |

c) Enable IPMMU translation for target master device

| Drivers | r8a77951.dtsi  | r8a77950.dtsi   |
|---------|--|---|
| Display | <pre>fcpvd0: fcp@fea27000 {     ... +     iommus = &lt;&amp;ipmmu_vi0 8&gt;; };  fcpvd1: fcp@fea2f000 {     ... +     iommus = &lt;&amp;ipmmu_vi0 9&gt;; };  fcpvd2: fcp@fea37000 {     ... +     iommus = &lt;&amp;ipmmu_vil 10&gt;; };</pre> | <pre>&amp;du { };  + &amp;fcpvd0 { +     /delete-property/ iommus; + }; + + &amp;fcpvd1 { +     /delete-property/ iommus; + }; + + &amp;fcpvd2 { +     /delete-property/ iommus; + };</pre> |

| Drivers          | r8a77951.dtsi   | r8a77950.dtsi   |
|------------------|---|---|
| Video capture    | <pre> vin0: video@e6ef0000 {     ... +    iommu = &lt;&amp;ipmmu_vi0 0&gt;; };  vin1: video@e6ef1000 {     ... +    iommu = &lt;&amp;ipmmu_vi0 0&gt;; };  vin2: video@e6ef2000 {     ... +    iommu = &lt;&amp;ipmmu_vi0 0&gt;; };  vin3: video@e6ef3000 {     ... +    iommu = &lt;&amp;ipmmu_vi0 0&gt;; };  vin4: video@e6ef4000 {     ... +    iommu = &lt;&amp;ipmmu_vil 1&gt;; };  vin5: video@e6ef5000 {     ... +    iommu = &lt;&amp;ipmmu_vil 1&gt;; };  vin6: video@e6ef6000 {     ... +    iommu = &lt;&amp;ipmmu_vil 1&gt;; };  vin7: video@e6ef7000 {     ... +    iommu = &lt;&amp;ipmmu_vil 1&gt;; }; </pre> | <pre> &amp;vin0 { +    /delete-property/ iommu; };  &amp;vin1 { +    /delete-property/ iommu; };  &amp;vin2 { +    /delete-property/ iommu; };  &amp;vin3 { +    /delete-property/ iommu; };  &amp;vin4 { +    /delete-property/ iommu; };  &amp;vin5 { +    /delete-property/ iommu; };  &amp;vin6 { +    /delete-property/ iommu; };  &amp;vin7 { +    /delete-property/ iommu; }; </pre> |
| SATA             | <pre> sata: sata@ee300000 {     ... +    iommu = &lt;&amp;ipmmu_hc 2&gt;; }; </pre>   | <pre> &amp;du { }; + + &amp;sata { +    /delete-property/ iommu; + }; </pre>  |
| USB 3.0 Host     | <pre> xhci0: usb@ee000000 {     ... +    iommu = &lt;&amp;ipmmu_hc 12&gt;; }; </pre>  | <pre> &amp;du { }; + + &amp;xhci0 { +    /delete-property/ iommu; + }; </pre>   |
| USB 3.0 Function | <pre> usb3_peri0: usb@ee020000 {     ... +    iommu = &lt;&amp;ipmmu_hc 13&gt;; }; </pre>   | <pre> &amp;du { }; + + &amp;usb3_peri0 { +    /delete-property/ iommu; + }; </pre>  |

| Drivers            | r8a77951.dtsi   | r8a77950.dtsi  |
|--------------------|---|--|
| USB 2.0 Host       | <pre>ehci0: usb@ee080100 { +   iommus = &lt;&amp;ipmmu_hc 4&gt;; };  ehci1: usb@ee0a0100 { +   iommus = &lt;&amp;ipmmu_hc 5&gt;; };  ehci2: usb@ee0c0100 { +   iommus = &lt;&amp;ipmmu_hc 6&gt;; };  ehci3: usb@ee0e0100 { +   iommus = &lt;&amp;ipmmu_hc 7&gt;; };  ohci0: usb@ee080000 { +   iommus = &lt;&amp;ipmmu_hc 4&gt;; };  ohci1: usb@ee0a0000 { +   iommus = &lt;&amp;ipmmu_hc 5&gt;; };  ohci2: usb@ee0c0000 { +   iommus = &lt;&amp;ipmmu_hc 6&gt;; };  ohci3: usb@ee0e0000 { +   iommus = &lt;&amp;ipmmu_hc 7&gt;; };</pre> | <pre>&amp;du { };  + + &amp;ehci0 { +   /delete-property/ iommus; + }; + + &amp;ehci1 { +   /delete-property/ iommus; + }; + + &amp;ehci2 { +   /delete-property/ iommus; + }; + + &amp;ohci0 { +   /delete-property/ iommus; + }; + + &amp;ohci1 { +   /delete-property/ iommus; + }; + + &amp;ohci2 { +   /delete-property/ iommus; + };</pre> |
| USB 2.0 Function   | <pre>usb_dmac0: dma-controller@e65a0000 { +   iommus = &lt;&amp;ipmmu_hc 9&gt;; };  usb_dmac1: dma-controller@e65b0000 { +   iommus = &lt;&amp;ipmmu_hc 10&gt;; };  usb_dmac2: dma-controller@e6460000 { +   iommus = &lt;&amp;ipmmu_hc 14&gt;; };  usb_dmac3: dma-controller@e6470000 { +   iommus = &lt;&amp;ipmmu_hc 15&gt;; };</pre>  | <pre>&amp;du { };  + + &amp;usb_dmac0 { +   /delete-property/ iommus; + }; + + &amp;usb_dmac1 { +   /delete-property/ iommus; + };</pre>   |
| Ethernet           | <pre>avb: ethernet@e6800000 { +   iommus = &lt;&amp;ipmmu_ds0 16&gt;; };</pre>  | <pre>&amp;du { };  + + &amp;avb { +   /delete-property/ iommus; + };</pre>   |
| SDHI/MMC (SDHI0/3) | <pre>sdhi0: mmc@ee100000 { +   iommus = &lt;&amp;ipmmu_ds1 32&gt;; };  sdhi3: mmc@ee160000 { +   iommus = &lt;&amp;ipmmu_ds1 35&gt;; };</pre>   | <pre>+ &amp;sdhi0 { +   /delete-property/ iommus; + }; + + &amp;sdhi3 { +   /delete-property/ iommus; + }; + &amp;du { };</pre>  |
| SDHI/MMC (SDHI2)   | <p><b>salvator-common.dtsi</b></p> <pre>&amp;sdhi2 { ... +   iommus = &lt;&amp;ipmmu_ds1 34&gt;;    status = "okay"; };</pre>   | <p><b>r8a77950-salvator-x.dts</b></p> <pre>+ &amp;sdhi2 { +   /delete-property/ iommus; + }; + &amp;du { };</pre>  |

| Drivers  | r8a77951.dtsi   | r8a77950.dtsi   |
|--|---|---|
| Audio  | <pre> audma0: dma-controller@ec700000 {     ...     iommu = &lt;&amp;ipmmu_mp0 0&gt;, &lt;&amp;ipmmu_mp0 1&gt;,     &lt;&amp;ipmmu_mp0 2&gt;, &lt;&amp;ipmmu_mp0 3&gt;,     &lt;&amp;ipmmu_mp0 4&gt;, &lt;&amp;ipmmu_mp0 5&gt;,     &lt;&amp;ipmmu_mp0 6&gt;, &lt;&amp;ipmmu_mp0 7&gt;,     &lt;&amp;ipmmu_mp0 8&gt;, &lt;&amp;ipmmu_mp0 9&gt;,     &lt;&amp;ipmmu_mp0 10&gt;, &lt;&amp;ipmmu_mp0 11&gt;,     &lt;&amp;ipmmu_mp0 12&gt;, &lt;&amp;ipmmu_mp0 13&gt;,     &lt;&amp;ipmmu_mp0 14&gt;, &lt;&amp;ipmmu_mp0 15&gt;; };  audma1: dma-controller@ec720000 {     ...     iommu = &lt;&amp;ipmmu_mp0 16&gt;, &lt;&amp;ipmmu_mp0 17&gt;,     &lt;&amp;ipmmu_mp0 18&gt;, &lt;&amp;ipmmu_mp0 19&gt;,     &lt;&amp;ipmmu_mp0 20&gt;, &lt;&amp;ipmmu_mp0 21&gt;,     &lt;&amp;ipmmu_mp0 22&gt;, &lt;&amp;ipmmu_mp0 23&gt;,     &lt;&amp;ipmmu_mp0 24&gt;, &lt;&amp;ipmmu_mp0 25&gt;,     &lt;&amp;ipmmu_mp0 26&gt;, &lt;&amp;ipmmu_mp0 27&gt;,     &lt;&amp;ipmmu_mp0 28&gt;, &lt;&amp;ipmmu_mp0 29&gt;,     &lt;&amp;ipmmu_mp0 30&gt;, &lt;&amp;ipmmu_mp0 31&gt;; }; </pre> | <pre> &amp;du { };  + &amp;audma0 { +     /delete-property/ iommu; + };  + &amp;audma1 { +     /delete-property/ iommu; + }; </pre>   |
| DMAC<br>(DMAC0),<br>I2C,<br>SCIF,<br>MSIOF           | <pre> dmac0: dma-controller@e6700000 {     iommu = &lt;&amp;ipmmu_ds0 0&gt;, &lt;&amp;ipmmu_ds0 1&gt;,     &lt;&amp;ipmmu_ds0 2&gt;, &lt;&amp;ipmmu_ds0 3&gt;,     &lt;&amp;ipmmu_ds0 4&gt;, &lt;&amp;ipmmu_ds0 5&gt;,     &lt;&amp;ipmmu_ds0 6&gt;, &lt;&amp;ipmmu_ds0 7&gt;,     &lt;&amp;ipmmu_ds0 8&gt;, &lt;&amp;ipmmu_ds0 9&gt;,     &lt;&amp;ipmmu_ds0 10&gt;, &lt;&amp;ipmmu_ds0 11&gt;,     &lt;&amp;ipmmu_ds0 12&gt;, &lt;&amp;ipmmu_ds0 13&gt;,     &lt;&amp;ipmmu_ds0 14&gt;, &lt;&amp;ipmmu_ds0 15&gt;; }; </pre>  | <pre> &amp;du { };  + &amp;dmac0 { +     /delete-property/ iommu; + };  + &amp;dmac1 { +     /delete-property/ iommu; + };  + &amp;dmac2 { +     /delete-property/ iommu; + }; </pre> |
| DMAC<br>(DMAC1,<br>DMAC2),<br>I2C,<br>SCIF,<br>MSIOF | <pre> dmac1: dma-controller@e7300000 {     ...     iommu = &lt;&amp;ipmmu_ds1 0&gt;, &lt;&amp;ipmmu_ds1 1&gt;,     &lt;&amp;ipmmu_ds1 2&gt;, &lt;&amp;ipmmu_ds1 3&gt;,     &lt;&amp;ipmmu_ds1 4&gt;, &lt;&amp;ipmmu_ds1 5&gt;,     &lt;&amp;ipmmu_ds1 6&gt;, &lt;&amp;ipmmu_ds1 7&gt;,     &lt;&amp;ipmmu_ds1 8&gt;, &lt;&amp;ipmmu_ds1 9&gt;,     &lt;&amp;ipmmu_ds1 10&gt;, &lt;&amp;ipmmu_ds1 11&gt;,     &lt;&amp;ipmmu_ds1 12&gt;, &lt;&amp;ipmmu_ds1 13&gt;,     &lt;&amp;ipmmu_ds1 14&gt;, &lt;&amp;ipmmu_ds1 15&gt;; };  dmac2: dma-controller@e7310000 {     ...     iommu = &lt;&amp;ipmmu_ds1 16&gt;, &lt;&amp;ipmmu_ds1 17&gt;,     &lt;&amp;ipmmu_ds1 18&gt;, &lt;&amp;ipmmu_ds1 19&gt;,     &lt;&amp;ipmmu_ds1 20&gt;, &lt;&amp;ipmmu_ds1 21&gt;,     &lt;&amp;ipmmu_ds1 22&gt;, &lt;&amp;ipmmu_ds1 23&gt;,     &lt;&amp;ipmmu_ds1 24&gt;, &lt;&amp;ipmmu_ds1 25&gt;,     &lt;&amp;ipmmu_ds1 26&gt;, &lt;&amp;ipmmu_ds1 27&gt;,     &lt;&amp;ipmmu_ds1 28&gt;, &lt;&amp;ipmmu_ds1 29&gt;,     &lt;&amp;ipmmu_ds1 30&gt;, &lt;&amp;ipmmu_ds1 31&gt;; }; </pre>   | <pre> &amp;du { };  + &amp;dmac1 { +     /delete-property/ iommu; + };  + &amp;dmac2 { +     /delete-property/ iommu; + }; </pre>   |

| Drivers  | r8a77951.dtsi  | r8a77950.dtsi   |
|--|--|---|
| PCIe<br>(common)   | <pre> pciec0: pcie@fe000000 {     ...     status = "disabled"; +   iommu = &lt;&amp;iopmmu_hc 0&gt;; +   iommu-map = &lt;0x0 &amp;iopmmu_hc 0x0 0x10000&gt;; +   iommu-map-mask = &lt;0x0&gt;; };  pciec1: pcie@ee800000 {     ...     status = "disabled"; +   iommu = &lt;&amp;iopmmu_hc 1&gt;; +   iommu-map = &lt;0x0 &amp;iopmmu_hc 0x1 0x10000&gt;; +   iommu-map-mask = &lt;0x0&gt;; }; </pre>  | <pre> &amp;du { };  + &amp;pciec0 { +     /delete-property/ iommu; +     /delete-property/ iommu-map; +     /delete-property/ iommu-map-mask; + };  + &amp;pciec1 { +     /delete-property/ iommu; +     /delete-property/ iommu-map; +     /delete-property/ iommu-map-mask; + }; </pre>                         |
| PCIe<br><br>H3 Ver.2.0<br>and<br>H3 Ver.3.0<br>(4x1 GB<br>DDR) | <pre> pciec0: pcie@fe000000 {     ...     /* Map all possible DDR as inbound ranges */ -   dma-ranges = &lt;0x42000000 0 0x40000000 0 0x40000000 0 0x40000000&gt;; +   dma-ranges = &lt;0x42000000 0 0x00000000 0 0x00000000 1 0x00000000&gt;; };  pciec1: pcie@ee800000 {     ...     /* Map all possible DDR as inbound ranges */ -   dma-ranges = &lt;0x42000000 0 0x40000000 0 0x40000000 0 0x40000000&gt;; +   dma-ranges = &lt;0x42000000 0 0x00000000 0 0x00000000 1 0x00000000&gt;; }; </pre>                    | <pre> &amp;du { };  &amp;pciec0 {     ...     /delete-property/ iommu-map-mask; +   dma-ranges = &lt;0x42000000 0 0x40000000 0 0x40000000 0 0x40000000&gt;; };  &amp;pciec1 {     ...     /delete-property/ iommu-map-mask; +   dma-ranges = &lt;0x42000000 0 0x40000000 0 0x40000000 0 0x40000000&gt;; }; </pre> |
| PCIe<br><br>H3 Ver.3.0<br>(4x2 GB<br>DDR)                      | <p><b>r8a77951-salvator-xs.dts</b></p> <pre> &amp;pciec0 {     ...     /* Map all possible DDR as inbound ranges */ -   dma-ranges = &lt;0x42000000 0 0x40000000 0 0x40000000 0 0x40000000&gt;; +   dma-ranges = &lt;0x42000000 0 0x00000000 0 0x00000000 1 0x00000000&gt;; };  &amp;pciec1 {     ...     /* Map all possible DDR as inbound ranges */ -   dma-ranges = &lt;0x42000000 0 0x40000000 0 0x40000000 0 0x40000000&gt;; +   dma-ranges = &lt;0x42000000 0 0x00000000 0 0x00000000 1 0x00000000&gt;; }; </pre> |   |

### 5.3.2.2 For R-Car M3 (R8A77961 for R-Car M3 Ver.3.0 or R8A77960 for R-Car M3 Ver.1.x)

Edit r8a77961.dtsi for R-Car M3 Ver.3.0 or r8a77960.dtsi for R-Car M3 Ver.1.x as below:

a) Enable common IPMMU DT node

| Drivers | r8a77961.dtsi or r8a77960.dtsi  |
|---------|---|
| All     | <pre> ipmmu_mm: iommu@e67b0000 {     ...     - status = "disabled"; }; </pre> |

b) Enable corresponding IPMMU cache

| Drivers  | r8a77961.dtsi or r8a77960.dtsi   |
|--|--|
| Display,<br>Video capture  | <pre> ipmmu_vi0: iommu@febd0000 {     ...     - status = "disabled"; }; </pre> |
| PCIe, SATA,<br>USB 2.0 Host,<br>USB 3.0 Host,<br>USB 2.0 Function,<br>USB 3.0 Function | <pre> ipmmu_hc: iommu@e6570000 {     ...     - status = "disabled"; }; </pre>  |
| Audio  | <pre> ipmmu_mp: iommu@ec6700000 {     ...     - status = "disabled"; }; </pre> |
| DMAC (DMAC0),<br>I2C, SCIF, MSIOF,<br>Ethernet   | <pre> ipmmu_ds0: iommu@e6740000 {     ...     - status = "disabled"; }; </pre> |
| DMAC (DMAC1/2),<br>I2C, SCIF, MSIOF,<br>SDHI   | <pre> ipmmu_ds1: iommu@e7740000 {     ...     - status = "disabled"; }; </pre> |

c) Enable IPMMU translation for target master device

| Drivers  | r8a77961.dtsi or r8a77960.dtsi   |
|--|--|
| DMAC (DMAC0/1/2),<br>I2C, SCIF, MSIOF,<br>Ethernet, SDHI,<br>USB 3.0 Host,<br>USB 3.0 Function | <pre> // The modify contents are same as R-Car H3 Ver.2.0/Ver.3.0. // Please refer to chapter 5.3.2.1 (left column only) for more detail. </pre>   |
| Display  | <pre> fcpvd0: fcp@fea27000 {     ... +   iommus = &lt;&amp;ipmmu_vi0 8&gt;; };  fcpvd1: fcp@fea2f000 {     ... +   iommus = &lt;&amp;ipmmu_vi0 9&gt;; };  fcpvd2: fcp@fea37000 {     ... +   iommus = &lt;&amp;ipmmu_vi0 10&gt;; }; </pre> |

| Drivers          | r8a77961.dtsi or r8a77960.dtsi  |
|------------------|---|
| Video capture    | <pre> vin0: video@e6ef0000 {     ... +    iommus = &lt;&amp;ipmmu_vio 0&gt;; };  vin1: video@e6ef1000 {     ... +    iommus = &lt;&amp;ipmmu_vio 0&gt;; };  vin2: video@e6ef2000 {     ... +    iommus = &lt;&amp;ipmmu_vio 0&gt;; };  vin3: video@e6ef3000 {     ... +    iommus = &lt;&amp;ipmmu_vio 0&gt;; };  vin4: video@e6ef4000 {     ... +    iommus = &lt;&amp;ipmmu_vio 1&gt;; };  vin5: video@e6ef5000 {     ... +    iommus = &lt;&amp;ipmmu_vio 1&gt;; };  vin6: video@e6ef6000 {     ... +    iommus = &lt;&amp;ipmmu_vio 1&gt;; };  vin7: video@e6ef7000 {     ... +    iommus = &lt;&amp;ipmmu_vio 1&gt;; }; </pre> |
| USB 2.0 Host     | <pre> ehci0: usb@ee080100 { +    iommus = &lt;&amp;ipmmu_hc 4&gt;; };  ehci1: usb@ee0a0100 { +    iommus = &lt;&amp;ipmmu_hc 5&gt;; };  ohci0: usb@ee080000 { +    iommus = &lt;&amp;ipmmu_hc 4&gt;; };  ohci1: usb@ee0a0000 { +    iommus = &lt;&amp;ipmmu_hc 5&gt;; }; </pre>   |
| USB 2.0 Function | <pre> usb_dmac0: dma-controller@e65a0000 { +    iommus = &lt;&amp;ipmmu_hc 9&gt;; };  usb_dmac1: dma-controller@e65b0000 { +    iommus = &lt;&amp;ipmmu_hc 10&gt;; }; </pre>  |



| Drivers                         | <b>r8a77961.dtsi or r8a77960.dtsi</b>   |
|---------------------------------|---|
| Audio                           | <pre> audma0: dma-controller@ec700000 {     ...     iommus = &lt;&amp;ipmmu_mp 0&gt;, &lt;&amp;ipmmu_mp 1&gt;,     &lt;&amp;ipmmu_mp 2&gt;, &lt;&amp;ipmmu_mp 3&gt;,     &lt;&amp;ipmmu_mp 4&gt;, &lt;&amp;ipmmu_mp 5&gt;,     &lt;&amp;ipmmu_mp 6&gt;, &lt;&amp;ipmmu_mp 7&gt;,     &lt;&amp;ipmmu_mp 8&gt;, &lt;&amp;ipmmu_mp 9&gt;,     &lt;&amp;ipmmu_mp 10&gt;, &lt;&amp;ipmmu_mp 11&gt;,     &lt;&amp;ipmmu_mp 12&gt;, &lt;&amp;ipmmu_mp 13&gt;,     &lt;&amp;ipmmu_mp 14&gt;, &lt;&amp;ipmmu_mp 15&gt;; };  audma1: dma-controller@ec720000 {     ...     iommus = &lt;&amp;ipmmu_mp 16&gt;, &lt;&amp;ipmmu_mp 17&gt;,     &lt;&amp;ipmmu_mp 18&gt;, &lt;&amp;ipmmu_mp 19&gt;,     &lt;&amp;ipmmu_mp 20&gt;, &lt;&amp;ipmmu_mp 21&gt;,     &lt;&amp;ipmmu_mp 22&gt;, &lt;&amp;ipmmu_mp 23&gt;,     &lt;&amp;ipmmu_mp 24&gt;, &lt;&amp;ipmmu_mp 25&gt;,     &lt;&amp;ipmmu_mp 26&gt;, &lt;&amp;ipmmu_mp 27&gt;,     &lt;&amp;ipmmu_mp 28&gt;, &lt;&amp;ipmmu_mp 29&gt;,     &lt;&amp;ipmmu_mp 30&gt;, &lt;&amp;ipmmu_mp 31&gt;; }; </pre> |
| PCIe<br>(common)                | <pre> pciec0: pcie@fe000000 {     ...     status = "disabled";     iommus = &lt;&amp;ipmmu_hc 0&gt;;     iommu-map = &lt;0x0 &amp;ipmmu_hc 0x0 0x10000&gt;;     iommu-map-mask = &lt;0x0&gt;; };  pciec1: pcie@ee800000 {     ...     status = "disabled";     iommus = &lt;&amp;ipmmu_hc 1&gt;;     iommu-map = &lt;0x0 &amp;ipmmu_hc 0x1 0x10000&gt;;     iommu-map-mask = &lt;0x0&gt;; }; </pre>   |
| PCIe M3 Ver.1.x                 | <p><b>r8a77960.dtsi</b></p> <pre> pciec0: pcie@fe000000 {     ...     /* Map all possible DDR as inbound ranges */     - dma-ranges = &lt;0x42000000 0 0x40000000 0 0x40000000 0 0x80000000&gt;;     + dma-ranges = &lt;0x42000000 0 0x00000000 0 0x00000000 1 0x00000000&gt;; };  pciec1: pcie@ee800000 {     ...     /* Map all possible DDR as inbound ranges */     - dma-ranges = &lt;0x42000000 0 0x40000000 0 0x40000000 0 0x80000000&gt;;     + dma-ranges = &lt;0x42000000 0 0x00000000 0 0x00000000 1 0x00000000&gt;; }; </pre>   |
| PCIe M3 Ver.3.0<br>(2x4 GB DDR) | <p><b>r8a77961.dtsi</b></p> <pre> pciec0: pcie@fe000000 {     ...     /* Map all possible DDR as inbound ranges */     - dma-ranges = &lt;0x42000000 0 0x40000000 0 0x40000000 0 0x80000000&gt;;     + dma-ranges = &lt;0x42000000 0 0x00000000 0 0x00000000 1 0x00000000&gt;; };  pciec1: pcie@ee800000 {     ...     /* Map all possible DDR as inbound ranges */     - dma-ranges = &lt;0x42000000 0 0x40000000 0 0x40000000 0 0x80000000&gt;;     + dma-ranges = &lt;0x42000000 0 0x00000000 0 0x00000000 1 0x00000000&gt;; }; </pre>   |

### 5.3.2.3 For R-Car M3N (R8A77965)

Edit r8a77965.dtsi as below:

a) Enable common IPMMU DT node

| Drivers | r8a77965.dtsi   |
|---------|---|
| All     | <pre> ipmmu_mm: iommu@e67b0000 {     ... -     status = "disabled"; }; </pre> |

b) Enable corresponding IPMMU cache

| Drivers  | r8a77965.dtsi  |
|--|--|
| Display,<br>Video capture  | <pre> ipmmu_vi0: iommu@febd0000 {     ... -     status = "disabled"; }; </pre> |
| PCIe, SATA,<br>USB 2.0 Host,<br>USB 3.0 Host,<br>USB 2.0 Function,<br>USB 3.0 Function | <pre> ipmmu_hc: iommu@e6570000 {     ... -     status = "disabled"; }; </pre>  |
| Audio  | <pre> ipmmu_mp: iommu@ec6700000 {     ... -     status = "disabled"; }; </pre> |
| DMAC (DMAC0),<br>I2C, SCIF, MSIOF,<br>Ethernet   | <pre> ipmmu_ds0: iommu@e6740000 {     ... -     status = "disabled"; }; </pre> |
| DMAC (DMAC1/2),<br>I2C, SCIF, MSIOF,<br>SDHI/MMC                                       | <pre> ipmmu_ds1: iommu@e7740000 {     ... -     status = "disabled"; }; </pre> |

c) Enable IPMMU translation for target master device

| Drivers  | r8a77965.dtsi   |
|--|---|
| DMAC (DMAC0/1/2),<br>I2C, SCIF, MSIOF,<br>Ethernet, SDHI/MMC,<br>USB 3.0 Host,<br>USB 3.0 Function | <pre> // The modify contents are same as R-Car H3 Ver.2.0/Ver.3.0. // Please refer to chapter 5.3.2.1 (left column only) for more detail. </pre>                    |
| USB 2.0 Host,<br>USB 2.0 Function,<br>Video capture,<br>Audio                                      | <pre> // The modify contents are same as R-Car M3. // Please refer to chapter 5.3.2.2 for more detail. </pre>   |
| Display  | <pre> fcvpd0: fcp@fea27000 {     ... +     iommus = &lt;&amp;ipmmu_vi0 8&gt;; };  fcvpd1: fcp@fea2f000 {     ... +     iommus = &lt;&amp;ipmmu_vi0 9&gt;; }; </pre> |

| Drivers             | r8a77965.dtsi   |
|---------------------|---|
| PCIe<br>(common)    | <pre> pciec0: pcie@fe000000 {     ...     status = "disabled"; +   iommu = &lt;&amp;ipmmu_hc 0&gt;; +   iommu-map = &lt;0x0 &amp;ipmmu_hc 0x0 0x10000&gt;; +   iommu-map-mask = &lt;0x0&gt;; };  pciec1: pcie@ee800000 {     ...     status = "disabled"; +   iommu = &lt;&amp;ipmmu_hc 1&gt;; +   iommu-map = &lt;0x0 &amp;ipmmu_hc 0x1 0x10000&gt;; +   iommu-map-mask = &lt;0x0&gt;; }; </pre>   |
| PCIe<br>M3N Ver.1.x | <pre> pciec0: pcie@fe000000 {     ...     /* Map all possible DDR as inbound ranges */ -   dma-ranges = &lt;0x42000000 0 0x40000000 0 0x40000000 0 0x80000000&gt;; +   dma-ranges = &lt;0x42000000 0 0x00000000 0 0x00000000 1 0x00000000&gt;; };  pciec1: pcie@ee800000 {     ...     /* Map all possible DDR as inbound ranges */ -   dma-ranges = &lt;0x42000000 0 0x40000000 0 0x40000000 0 0x80000000&gt;; +   dma-ranges = &lt;0x42000000 0 0x00000000 0 0x00000000 1 0x00000000&gt;; }; </pre> |

### 5.3.2.4 For R-Car E3 (R8A77990)

Edit r8a77990.dtsi as below:

a) Enable common IPMMU DT node

| Drivers | r8a77990.dtsi   |
|---------|---|
| All     | <pre>ipmmu_mm: iommu@e67b0000 {     ...     - status = "disabled"; };</pre> |

b) Enable corresponding IPMMU cache

| Drivers  | r8a77990.dtsi  |
|--|--|
| Display,<br>Video capture  | <pre>ipmmu_vi0: iommu@febd0000 {     ...     - status = "disabled"; };</pre> |
| PCIe, SATA,<br>USB 2.0 Host,<br>USB 3.0 Host,<br>USB 2.0 Function,<br>USB 3.0 Function | <pre>ipmmu_hc: iommu@e6570000 {     ...     - status = "disabled"; };</pre>  |
| Audio  | <pre>ipmmu_mp: iommu@ec6700000 {     ...     - status = "disabled"; };</pre> |
| DMAC (DMAC0),<br>I2C, SCIF, MSIOF,<br>Ethernet   | <pre>ipmmu_ds0: iommu@e6740000 {     ...     - status = "disabled"; };</pre> |
| DMAC (DMAC1/2),<br>I2C, SCIF, MSIOF,<br>SDHI/MMC                                       | <pre>ipmmu_ds1: iommu@e7740000 {     ...     - status = "disabled"; };</pre> |

c) Enable IPMMU translation for target master device

| Drivers  | r8a77990.dtsi   |
|--|---|
| DMAC (DMAC0/1/2),<br>I2C, SCIF, MSIOF,<br>Ethernet,<br>USB 3.0 Host,<br>USB 3.0 Function | <pre>// The modify contents are same as R-Car H3 Ver.2.0/Ver.3.0. // Please refer to chapter 5.3.2.1 (left column only) for more detail.</pre>                |
| USB 2.0 Function,<br>Audio   | <pre>// The modify contents are same as R-Car M3. // Please refer to chapter 5.3.2.2 for more detail.</pre>   |
| Display  | <pre>fcpsvd0: fcp@fea27000 { +   iommus = &lt;&amp;ipmmu_vi0 8&gt;; };  fcpsvd1: fcp@fea2f000 { +   iommus = &lt;&amp;ipmmu_vi0 9&gt;; };</pre>               |
| Video capture  | <pre>vin4: video@e6ef4000 {     ... +   iommus = &lt;&amp;ipmmu_vi0 1&gt;; };  vin5: video@e6ef5000 {     ... +   iommus = &lt;&amp;ipmmu_vi0 1&gt;; };</pre> |

| Drivers   | r8a77990.dtsi   |
|---|---|
| USB 2.0 Host                                    | <pre>ehci0: usb@ee080100 { +   iommus = &lt;&amp;ipmmu_hc 4&gt;; };  ohci0: usb@ee080000 { +   iommus = &lt;&amp;ipmmu_hc 4&gt;; };</pre>   |
| SDHI/MMC<br>(SDHI0/1/3)<br><br>E3 Ver.1.0       | <b>r8a77990-es10-ebisu.dts</b><br><pre>&amp;sdhi0 { +   iommus = &lt;&amp;ipmmu_dsl 32&gt;; };  &amp;sdhi1 { +   iommus = &lt;&amp;ipmmu_dsl 33&gt;; };  &amp;sdhi3 { +   iommus = &lt;&amp;ipmmu_dsl 35&gt;; };</pre>  |
| SDHI/MMC<br>(SDHI0/1/3)<br><br>E3 Ver.1.1       | <b>r8a77990-ebisu.dts</b><br><pre>&amp;sdhi0 { +   iommus = &lt;&amp;ipmmu_dsl 32&gt;; };  &amp;sdhi1 { +   iommus = &lt;&amp;ipmmu_dsl 33&gt;; };  &amp;sdhi3 { +   iommus = &lt;&amp;ipmmu_dsl 35&gt;; };</pre>   |
| PCIe<br>(common)                                | <pre>pciec0: pcie@fe000000 { ... status = "disabled"; +   iommus = &lt;&amp;ipmmu_hc 0&gt;; +   iommu-map = &lt;0x0 &amp;ipmmu_hc 0x0 0x10000&gt;; +   iommu-map-mask = &lt;0x0&gt;; };</pre>   |
| PCIe<br><br>E3 Ver.1.x + Ebisu<br>(1 GB DDR)    | <pre>pciec0: pcie@fe000000 { ... /* Map all possible DDR as inbound ranges */ -   dma-ranges = &lt;0x42000000 0 0x40000000 0 0x40000000 0 0x80000000&gt;; +   dma-ranges = &lt;0x42000000 0 0x00000000 0 0x00000000 1 0x00000000&gt;; };</pre>                            |
| PCIe<br><br>E3 Ver.1.0 + Ebisu-4D<br>(2 GB DDR) | <b>r8a77990-es10-ebisu-4d.dts</b><br><pre>&amp;pciec0 { ... /* Map all possible DDR as inbound ranges */ -   dma-ranges = &lt;0x42000000 0 0x40000000 0 0x40000000 0 0x80000000&gt;; +   dma-ranges = &lt;0x42000000 0 0x00000000 0 0x00000000 1 0x00000000&gt;; };</pre> |
| PCIe<br><br>E3 Ver.1.1 + Ebisu-4D<br>(2 GB DDR) | <b>r8a77990-ebisu-4d.dts</b><br><pre>&amp;pciec0 { ... /* Map all possible DDR as inbound ranges */ -   dma-ranges = &lt;0x42000000 0 0x40000000 0 0x40000000 0 0x80000000&gt;; +   dma-ranges = &lt;0x42000000 0 0x00000000 0 0x00000000 1 0x00000000&gt;; };</pre>      |

### 5.3.2.5 For R-Car D3 (R8A77995)

Edit r8a77995.dtsi as below:

a) Enable common IPMMU DT node

| Drivers | r8a77995.dtsi   |
|---------|---|
| All     | <pre>ipmmu_mm: iommu@e67b0000 {     ... -     status = "disabled"; };</pre> |

b) Enable corresponding IPMMU cache

| Drivers   | r8a77995.dtsi  |
|---|--|
| Video capture,<br>Display                         | <pre>ipmmu_vi0: iommu@febd0000 {     ... -     status = "disabled"; };</pre> |
| USB 2.0 Host,<br>USB 2.0 Function                 | <pre>ipmmu_hc: iommu@e6570000 {     ... -     status = "disabled"; };</pre>  |
| Audio   | <pre>ipmmu_mp: iommu@ec670000 {     ... -     status = "disabled"; };</pre>  |
| DMAC (DMAC0),<br>EthernetAVB                      | <pre>ipmmu_ds0: iommu@e6740000 {     ... -     status = "disabled"; };</pre> |
| DMAC (DMAC1/2),<br>SCIF, I2C,<br>SDHI/MMC (SDHI2) | <pre>ipmmu_ds1: iommu@e7740000 {     ... -     status = "disabled"; };</pre> |

c) Enable IPMMU translation for target master device

| Drivers               | r8a77995.dtsi   |
|-----------------------|---|
| Video capture<br>VIN4 | <pre>vin4: video@e6ef4000 {     ... +     iommus = &lt;&amp;ipmmu_vi0 1&gt;; };</pre>   |
| Display               | <pre>fcvpd0: fcp@fea27000 {     ... +     iommus = &lt;&amp;ipmmu_vi0 8&gt;; };  fcvpd1: fcp@fea2f000 {     ... +     iommus = &lt;&amp;ipmmu_vi0 9&gt;; };</pre> |
| USB2.0 Host           | <pre>ohci0: usb@ee080000 { +     iommus = &lt;&amp;ipmmu_hc 4&gt;; };  ehci0: usb@ee080100 { +     iommus = &lt;&amp;ipmmu_hc 4&gt;; };</pre>                     |

| Drivers                         | r8a77995.dtsi   |
|---------------------------------|---|
| USB2.0 Function                 | <pre> usb_dmac0: dma-controller@e65a0000 {     ...     + iommus = &lt;&amp;ipmmu_hc 9&gt;; };  usb_dmac1: dma-controller@e65b0000 {     ...     + iommus = &lt;&amp;ipmmu_hc 10&gt;; }; </pre>  |
| Audio                           | <pre> audma0: dma-controller@ec700000 {     ...     + iommus = &lt;&amp;ipmmu_mp 0&gt;, &lt;&amp;ipmmu_mp 1&gt;,     + &lt;&amp;ipmmu_mp 2&gt;, &lt;&amp;ipmmu_mp 3&gt;,     + &lt;&amp;ipmmu_mp 4&gt;, &lt;&amp;ipmmu_mp 5&gt;,     + &lt;&amp;ipmmu_mp 6&gt;, &lt;&amp;ipmmu_mp 7&gt;,     + &lt;&amp;ipmmu_mp 8&gt;, &lt;&amp;ipmmu_mp 9&gt;,     + &lt;&amp;ipmmu_mp 10&gt;, &lt;&amp;ipmmu_mp 11&gt;,     + &lt;&amp;ipmmu_mp 12&gt;, &lt;&amp;ipmmu_mp 13&gt;,     + &lt;&amp;ipmmu_mp 14&gt;, &lt;&amp;ipmmu_mp 15&gt;; }; </pre>  |
| DMAC (DMAC0)                    | <pre> dmac0: dma-controller@e6700000 {     ...     + iommus = &lt;&amp;ipmmu_ds0 0&gt;, &lt;&amp;ipmmu_ds0 1&gt;,     + &lt;&amp;ipmmu_ds0 2&gt;, &lt;&amp;ipmmu_ds0 3&gt;,     + &lt;&amp;ipmmu_ds0 4&gt;, &lt;&amp;ipmmu_ds0 5&gt;,     + &lt;&amp;ipmmu_ds0 6&gt;, &lt;&amp;ipmmu_ds0 7&gt;; }; </pre>   |
| EthernetAVB                     | <pre> avb: ethernet@e6800000 {     ...     + iommus = &lt;&amp;ipmmu_ds0 16&gt;; }; </pre>  |
| DMAC (DMAC1/2),<br>SCIF,<br>I2C | <pre> dmac1: dma-controller@e7300000 {     ...     + iommus = &lt;&amp;ipmmu_ds1 0&gt;, &lt;&amp;ipmmu_ds1 1&gt;,     + &lt;&amp;ipmmu_ds1 2&gt;, &lt;&amp;ipmmu_ds1 3&gt;,     + &lt;&amp;ipmmu_ds1 4&gt;, &lt;&amp;ipmmu_ds1 5&gt;,     + &lt;&amp;ipmmu_ds1 6&gt;, &lt;&amp;ipmmu_ds1 7&gt;; };  dmac2: dma-controller@e7310000 {     ...     + iommus = &lt;&amp;ipmmu_ds1 16&gt;, &lt;&amp;ipmmu_ds1 17&gt;,     + &lt;&amp;ipmmu_ds1 18&gt;, &lt;&amp;ipmmu_ds1 19&gt;,     + &lt;&amp;ipmmu_ds1 20&gt;, &lt;&amp;ipmmu_ds1 21&gt;,     + &lt;&amp;ipmmu_ds1 22&gt;, &lt;&amp;ipmmu_ds1 23&gt;; }; </pre> |
| SDHI/MMC (SDHI2)                | <pre> sdhi2: mmc@ee140000 {     ...     + iommus = &lt;&amp;ipmmu_ds1 34&gt;; }; </pre>   |

### 5.3.2.6 For R-Car V3U (R8A779A0)

Edit r8a779a0.dtsi as below:

a) Enable common IPMMU DT node

| Drivers | r8a779a0.dtsi   |
|---------|---|
| All     | <pre> ipmmu_mm: iommu@eefc0000 {     ... -     status = "disabled"; }; </pre> |

b) Enable corresponding IPMMU cache

| Drivers  | r8a779a0.dtsi  |
|--|--|
| Video capture  | <pre> ipmmu_vi0: iommu@eee80000 {     ... -     status = "disabled"; }; </pre> |
| Display  | <pre> ipmmu_vi1: iommu@eeec0000 {     ... -     status = "disabled"; }; </pre> |
| DMAC (DMAC1/2),<br>SDHI/MMC (SDHI0),<br>I2C, SCIF, MSIOF | <pre> ipmmu_ds0: iommu@eed00000 {     ... -     status = "disabled"; }; </pre> |
| PCIe, Ethernet   | <pre> ipmmu_ds1: iommu@eed40000 {     ... -     status = "disabled"; }; </pre> |
| RT-DMAC<br>(RT-DMAC0/1/2/3)                              | <pre> ipmmu_rt1: iommu@ee4c0000 {     ... -     status = "disabled"; }; </pre> |



c) Enable IPMMU translation for target master device

| Drivers                      | r8a779a0.dtsi  |
|------------------------------|--|
| RT-DMAC<br>(RT-DMAC0/1/2/3), | <pre> rt_dmac0: dma-controller@ffd60000 {     ...     iommu = &lt;&amp;ipmmu_rtl 0&gt;, &lt;&amp;ipmmu_rtl 1&gt;,     &lt;&amp;ipmmu_rtl 2&gt;, &lt;&amp;ipmmu_rtl 3&gt;,     &lt;&amp;ipmmu_rtl 4&gt;, &lt;&amp;ipmmu_rtl 5&gt;,     &lt;&amp;ipmmu_rtl 6&gt;, &lt;&amp;ipmmu_rtl 7&gt;,     &lt;&amp;ipmmu_rtl 8&gt;, &lt;&amp;ipmmu_rtl 9&gt;,     &lt;&amp;ipmmu_rtl 10&gt;, &lt;&amp;ipmmu_rtl 11&gt;,     &lt;&amp;ipmmu_rtl 12&gt;, &lt;&amp;ipmmu_rtl 13&gt;,     &lt;&amp;ipmmu_rtl 14&gt;, &lt;&amp;ipmmu_rtl 15&gt;; }; rt_dmac1: dma-controller@ffd61000 {     ...     iommu = &lt;&amp;ipmmu_rtl 16&gt;, &lt;&amp;ipmmu_rtl 17&gt;,     &lt;&amp;ipmmu_rtl 18&gt;, &lt;&amp;ipmmu_rtl 19&gt;,     &lt;&amp;ipmmu_rtl 20&gt;, &lt;&amp;ipmmu_rtl 21&gt;,     &lt;&amp;ipmmu_rtl 22&gt;, &lt;&amp;ipmmu_rtl 23&gt;,     &lt;&amp;ipmmu_rtl 24&gt;, &lt;&amp;ipmmu_rtl 25&gt;,     &lt;&amp;ipmmu_rtl 26&gt;, &lt;&amp;ipmmu_rtl 27&gt;,     &lt;&amp;ipmmu_rtl 28&gt;, &lt;&amp;ipmmu_rtl 29&gt;,     &lt;&amp;ipmmu_rtl 30&gt;, &lt;&amp;ipmmu_rtl 31&gt;; }; rt_dmac2: dma-controller@ffd62000 {     ...     iommu = &lt;&amp;ipmmu_rtl 32&gt;, &lt;&amp;ipmmu_rtl 33&gt;,     &lt;&amp;ipmmu_rtl 34&gt;, &lt;&amp;ipmmu_rtl 35&gt;,     &lt;&amp;ipmmu_rtl 36&gt;, &lt;&amp;ipmmu_rtl 37&gt;,     &lt;&amp;ipmmu_rtl 38&gt;, &lt;&amp;ipmmu_rtl 39&gt;,     &lt;&amp;ipmmu_rtl 40&gt;, &lt;&amp;ipmmu_rtl 41&gt;,     &lt;&amp;ipmmu_rtl 42&gt;, &lt;&amp;ipmmu_rtl 43&gt;,     &lt;&amp;ipmmu_rtl 44&gt;, &lt;&amp;ipmmu_rtl 45&gt;,     &lt;&amp;ipmmu_rtl 46&gt;, &lt;&amp;ipmmu_rtl 47&gt;; }; rt_dmac3: dma-controller@ffd63000 {     ...     iommu = &lt;&amp;ipmmu_rtl 48&gt;, &lt;&amp;ipmmu_rtl 49&gt;,     &lt;&amp;ipmmu_rtl 50&gt;, &lt;&amp;ipmmu_rtl 51&gt;,     &lt;&amp;ipmmu_rtl 52&gt;, &lt;&amp;ipmmu_rtl 53&gt;,     &lt;&amp;ipmmu_rtl 54&gt;, &lt;&amp;ipmmu_rtl 55&gt;,     &lt;&amp;ipmmu_rtl 56&gt;, &lt;&amp;ipmmu_rtl 57&gt;,     &lt;&amp;ipmmu_rtl 58&gt;, &lt;&amp;ipmmu_rtl 59&gt;,     &lt;&amp;ipmmu_rtl 60&gt;, &lt;&amp;ipmmu_rtl 61&gt;,     &lt;&amp;ipmmu_rtl 62&gt;, &lt;&amp;ipmmu_rtl 63&gt;; }; </pre> |
| Display                      | <pre> fcpvd0: fcp@fea10000 {     ...     iommu = &lt;&amp;ipmmu_vil 6&gt;; }; fcpvd1: fcp@fea11000 {     ...     iommu = &lt;&amp;ipmmu_vil 7&gt;; }; </pre>   |

| Drivers                                | r8a779a0.dtsi  |
|--|--|
| DMAC<br>(DMAC1/2),<br>I2C, SCIF, MSIOF | <pre> dma1: dma-controller@e7350000 {     ...     iommus = &lt;&amp;ipmmu_ds0 0&gt;, &lt;&amp;ipmmu_ds0 1&gt;,     &lt;&amp;ipmmu_ds0 2&gt;, &lt;&amp;ipmmu_ds0 3&gt;,     &lt;&amp;ipmmu_ds0 4&gt;, &lt;&amp;ipmmu_ds0 5&gt;,     &lt;&amp;ipmmu_ds0 6&gt;, &lt;&amp;ipmmu_ds0 7&gt;,     &lt;&amp;ipmmu_ds0 8&gt;, &lt;&amp;ipmmu_ds0 9&gt;,     &lt;&amp;ipmmu_ds0 10&gt;, &lt;&amp;ipmmu_ds0 11&gt;,     &lt;&amp;ipmmu_ds0 12&gt;, &lt;&amp;ipmmu_ds0 13&gt;,     &lt;&amp;ipmmu_ds0 14&gt;, &lt;&amp;ipmmu_ds0 15&gt;; }; dma2: dma-controller@e7351000 {     ...     iommus = &lt;&amp;ipmmu_ds0 16&gt;, &lt;&amp;ipmmu_ds0 17&gt;,     &lt;&amp;ipmmu_ds0 18&gt;, &lt;&amp;ipmmu_ds0 19&gt;,     &lt;&amp;ipmmu_ds0 20&gt;, &lt;&amp;ipmmu_ds0 21&gt;,     &lt;&amp;ipmmu_ds0 22&gt;, &lt;&amp;ipmmu_ds0 23&gt;; }; </pre> |
| MMC (SDHI0)                            | <pre> mmc0: mmc@ee140000 {     ...     iommus = &lt;&amp;ipmmu_ds0 32&gt;; }; </pre>   |
| Video capture<br>VIN0 (0 to 7)         | <pre> vin0: video@e6ef0000 {     ...     iommus = &lt;&amp;ipmmu_vi0 0&gt;; }; vin1: video@e6ef1000 {     ...     iommus = &lt;&amp;ipmmu_vi0 0&gt;; }; vin2: video@e6ef2000 {     ...     iommus = &lt;&amp;ipmmu_vi0 0&gt;; }; vin3: video@e6ef3000 {     ...     iommus = &lt;&amp;ipmmu_vi0 0&gt;; }; vin4: video@e6ef4000 {     ...     iommus = &lt;&amp;ipmmu_vi0 0&gt;; }; vin5: video@e6ef5000 {     ...     iommus = &lt;&amp;ipmmu_vi0 0&gt;; }; vin6: video@e6ef6000 {     ...     iommus = &lt;&amp;ipmmu_vi0 0&gt;; }; vin7: video@e6ef7000 {     ...     iommus = &lt;&amp;ipmmu_vi0 0&gt;; }; </pre>   |

| Drivers                          | r8a779a0.dtsi  |
|----------------------------------|--|
| Video capture<br>VIN1 (8 to 15)  | <pre> vin8: video@e6ef8000 {     ...     + iommus = &lt;&amp;ipmmu_vio 1&gt;; }; vin9: video@e6ef9000 {     ...     + iommus = &lt;&amp;ipmmu_vio 1&gt;; }; vin10: video@e6efa000 {     ...     + iommus = &lt;&amp;ipmmu_vio 1&gt;; }; vin11: video@e6efb000 {     ...     + iommus = &lt;&amp;ipmmu_vio 1&gt;; }; vin12: video@e6efc000 {     ...     + iommus = &lt;&amp;ipmmu_vio 1&gt;; }; vin13: video@e6efd000 {     ...     + iommus = &lt;&amp;ipmmu_vio 1&gt;; }; vin14: video@e6efe000 {     ...     + iommus = &lt;&amp;ipmmu_vio 1&gt;; }; vin15: video@e6eff000 {     ...     + iommus = &lt;&amp;ipmmu_vio 1&gt;; }; </pre>   |
| Video capture<br>VIN2 (16 to 23) | <pre> vin16: video@e6ed0000 {     ...     + iommus = &lt;&amp;ipmmu_vio 2&gt;; }; vin17: video@e6ed1000 {     ...     + iommus = &lt;&amp;ipmmu_vio 2&gt;; }; vin18: video@e6ed2000 {     ...     + iommus = &lt;&amp;ipmmu_vio 2&gt;; }; vin19: video@e6ed3000 {     ...     + iommus = &lt;&amp;ipmmu_vio 2&gt;; }; vin20: video@e6ed4000 {     ...     + iommus = &lt;&amp;ipmmu_vio 2&gt;; }; vin21: video@e6ed5000 {     ...     + iommus = &lt;&amp;ipmmu_vio 2&gt;; }; vin22: video@e6ed6000 {     ...     + iommus = &lt;&amp;ipmmu_vio 2&gt;; }; vin23: video@e6ed7000 {     ...     + iommus = &lt;&amp;ipmmu_vio 2&gt;; }; </pre> |

| Drivers                          | r8a779a0.dtsi  |
|----------------------------------|--|
| Video capture<br>VIN3 (24 to 31) | <pre> vin24: video@e6ed8000 {     ... +    iommus = &lt;&amp;ipmmu_v10 3&gt;; }; vin25: video@e6ed9000 {     ... +    iommus = &lt;&amp;ipmmu_v10 3&gt;; }; vin26: video@e6eda000 {     ... +    iommus = &lt;&amp;ipmmu_v10 3&gt;; }; vin27: video@e6edb000 {     ... +    iommus = &lt;&amp;ipmmu_v10 3&gt;; }; vin28: video@e6edc000 {     ... +    iommus = &lt;&amp;ipmmu_v10 3&gt;; }; vin29: video@e6edd000 {     ... +    iommus = &lt;&amp;ipmmu_v10 3&gt;; }; vin30: video@e6ede000 {     ... +    iommus = &lt;&amp;ipmmu_v10 3&gt;; }; vin31: video@e6edf000 {     ... +    iommus = &lt;&amp;ipmmu_v10 3&gt;; }; </pre> |

| Drivers     | r8a779a0.dtsi  |
|-------------|--|
| EthernetAVB | <pre> avb0: ethernet@e6800000 {     ...     + iommus = &lt;&amp;ipmmu_ds1 0&gt;; }; avb1: ethernet@e6810000 {     ... + iommus = &lt;&amp;ipmmu_ds1 1&gt;; }; avb2: ethernet@e6820000 {     ... + iommus = &lt;&amp;ipmmu_ds1 2&gt;; }; avb3: ethernet@e6830000 {     ... + iommus = &lt;&amp;ipmmu_ds1 3&gt;; }; avb4: ethernet@e6840000 {     ... + iommus = &lt;&amp;ipmmu_ds1 4&gt;; }; avb5: ethernet@e6850000 {     ... + iommus = &lt;&amp;ipmmu_ds1 11&gt;; }; </pre>  |
| PCIe        | <pre> pciec0: pcie@e65d0000 {     ... - dma-ranges = &lt;0x42000000 0 0x40000000 0 0x40000000 0 0x80000000&gt;; + dma-ranges = &lt;0x42000000 0 0x00000000 0 0x00000000 1 0x00000000&gt;;     ...     status = "disabled"; + iommus = &lt;&amp;ipmmu_ds1 5&gt;; + iommu-map = &lt;0x0 &amp;ipmmu_ds1 0x0 0x10000&gt;; + iommu-map-mask = &lt;0x0&gt;; }; pciec1: pcie@e65d8000 {     ... - dma-ranges = &lt;0x42000000 0 0x40000000 0 0x40000000 0 0x80000000&gt;; + dma-ranges = &lt;0x42000000 0 0x00000000 0 0x00000000 1 0x00000000&gt;;     ...     status = "disabled"; + iommus = &lt;&amp;ipmmu_ds1 6&gt;; + iommu-map = &lt;0x0 &amp;ipmmu_ds1 0x1 0x10000&gt;; + iommu-map-mask = &lt;0x0&gt;; }; pciec2: pcie@e65f0000 {     ... - dma-ranges = &lt;0x42000000 0 0x40000000 0 0x40000000 0 0x80000000&gt;; + dma-ranges = &lt;0x42000000 0 0x00000000 0 0x00000000 1 0x00000000&gt;;     ...     status = "disabled"; + iommus = &lt;&amp;ipmmu_ds1 7&gt;; + iommu-map = &lt;0x0 &amp;ipmmu_ds1 0x0 0x10000&gt;; + iommu-map-mask = &lt;0x0&gt;; }; pciec3: pcie@e65f8000 {     ... - dma-ranges = &lt;0x42000000 0 0x40000000 0 0x40000000 0 0x80000000&gt;; + dma-ranges = &lt;0x42000000 0 0x00000000 0 0x00000000 1 0x00000000&gt;;     ...     status = "disabled"; + iommus = &lt;&amp;ipmmu_ds1 8&gt;; + iommu-map = &lt;0x0 &amp;ipmmu_ds1 0x1 0x10000&gt;; + iommu-map-mask = &lt;0x0&gt;; }; </pre> |

### 5.3.2.7 For R-Car V3H Ver.2.0 (R8A77980)

Edit r8a77980.dtsi as below:

- a) Enable common IPMMU DT node

| Drivers | r8a77980.dtsi   |
|---------|---|
| All     | <pre> ipmmu_mm: iommu@e67b0000 {     ... -     status = "disabled"; }; </pre> |

- b) Enable corresponding IPMMU cache

| Drivers   | r8a77980.dtsi  |
|---|--|
| Video capture,<br>Display,<br>PCIe                        | <pre> ipmmu_vi0: iommu@febd0000 {     ... -     status = "disabled"; }; </pre> |
| DMAC (DMAC1/2),<br>GEther, SCIF, I2C,<br>SDHI/MMC (SDHI1) | <pre> ipmmu_ds1: iommu@e7740000 {     ... -     status = "disabled"; }; </pre> |

- c) Enable IPMMU translation for target master device

| Drivers                        | r8a77980.dtsi  |
|--------------------------------|--|
| Video capture<br>VIN0 (0 to 3) | <pre> vin0: vin_00@e6ef0000 {     ... +     iommus = &lt;&amp;ipmmu_vi0 0&gt;; }; vin1: vin_01@e6ef1000 {     ... +     iommus = &lt;&amp;ipmmu_vi0 0&gt;; }; vin2: vin_02@e6ef2000 {     ... +     iommus = &lt;&amp;ipmmu_vi0 0&gt;; }; vin3: vin_03@e6ef3000 {     ... +     iommus = &lt;&amp;ipmmu_vi0 0&gt;; }; </pre> |

| Drivers                          | r8a77980.dtsi   |
|----------------------------------|---|
| Video capture<br>VIN1 (4 to 7)   | <pre> vin4: vin_04@e6ef4000 {     ...     + iommus = &lt;&amp;ipmmu_vio 1&gt;; }; vin5: vin_05@e6ef5000 {     ...     + iommus = &lt;&amp;ipmmu_vio 1&gt;; }; vin6: vin_06@e6ef6000 {     ...     + iommus = &lt;&amp;ipmmu_vio 1&gt;; }; vin7: vin_07@e6ef7000 {     ...     + iommus = &lt;&amp;ipmmu_vio 1&gt;; }; </pre>                              |
| Video capture<br>VIN1 (8 to 11)  | <pre> vin8: vin_08@e6ef8000 {     ...     + iommus = &lt;&amp;ipmmu_vio 2&gt;; }; vin9: vin_09@e6ef9000 {     ...     + iommus = &lt;&amp;ipmmu_vio 2&gt;; }; vin10: vin_10@e6efa000 {     ...     + iommus = &lt;&amp;ipmmu_vio 2&gt;; }; vin11: vin_11@e6efb000 {     ...     + iommus = &lt;&amp;ipmmu_vio 2&gt;; }; </pre>                            |
| Video capture<br>VIN1 (12 to 15) | <pre> vin12: vin_12@e6efc000 {     ...     + iommus = &lt;&amp;ipmmu_vio 3&gt;; }; vin13: vin_13@e6efd000 {     ...     + iommus = &lt;&amp;ipmmu_vio 3&gt;; }; vin14: vin_14@e6efe000 {     ...     + iommus = &lt;&amp;ipmmu_vio 3&gt;; }; vin15: vin_15@e6eff000 {     ...     + iommus = &lt;&amp;ipmmu_vio 3&gt;; }; </pre>                          |
| Display                          | <pre> fcpvd0: fcp@fea27000 {     ...     + iommus = &lt;&amp;ipmmu_vio 8&gt;; }; </pre>   |
| PCIe                             | <pre> pciec: pcie@fe000000 {     ...     - dma-ranges = &lt;0x42000000 0 0x40000000 0 0x40000000 0 0x80000000&gt;;     + dma-ranges = &lt;0x42000000 0 0x00000000 0 0x00000000 1 0x00000000&gt;;     ...     + iommus = &lt;&amp;ipmmu_vio 5&gt;;     + iommu-map = &lt;0x0 &amp;ipmmu_vio 0x0 0x10000&gt;;     + iommu-map-mask = &lt;0x0&gt;; }; </pre> |

| Drivers                         | r8a77980.dtsi   |
|---------------------------------|---|
| DMAC<br>(DMAC1/2),<br>I2C, SCIF | <pre> dmacl: dma-controller@e7300000 {     ...     iommus = &lt;&amp;ipmmu_ds1 0&gt;, &lt;&amp;ipmmu_ds1 1&gt;,     &lt;&amp;ipmmu_ds1 2&gt;, &lt;&amp;ipmmu_ds1 3&gt;,     &lt;&amp;ipmmu_ds1 4&gt;, &lt;&amp;ipmmu_ds1 5&gt;,     &lt;&amp;ipmmu_ds1 6&gt;, &lt;&amp;ipmmu_ds1 7&gt;,     &lt;&amp;ipmmu_ds1 8&gt;, &lt;&amp;ipmmu_ds1 9&gt;,     &lt;&amp;ipmmu_ds1 10&gt;, &lt;&amp;ipmmu_ds1 11&gt;,     &lt;&amp;ipmmu_ds1 12&gt;, &lt;&amp;ipmmu_ds1 13&gt;,     &lt;&amp;ipmmu_ds1 14&gt;, &lt;&amp;ipmmu_ds1 15&gt;; };  dmac2: dma-controller@e7310000 {     ...     iommus = &lt;&amp;ipmmu_ds1 16&gt;, &lt;&amp;ipmmu_ds1 17&gt;,     &lt;&amp;ipmmu_ds1 18&gt;, &lt;&amp;ipmmu_ds1 19&gt;,     &lt;&amp;ipmmu_ds1 20&gt;, &lt;&amp;ipmmu_ds1 21&gt;,     &lt;&amp;ipmmu_ds1 22&gt;, &lt;&amp;ipmmu_ds1 23&gt;,     &lt;&amp;ipmmu_ds1 24&gt;, &lt;&amp;ipmmu_ds1 25&gt;,     &lt;&amp;ipmmu_ds1 26&gt;, &lt;&amp;ipmmu_ds1 27&gt;,     &lt;&amp;ipmmu_ds1 28&gt;, &lt;&amp;ipmmu_ds1 29&gt;,     &lt;&amp;ipmmu_ds1 30&gt;, &lt;&amp;ipmmu_ds1 31&gt;; }; </pre> |
| MMC (SDHI1)                     | <pre> mmc0: mmc@ee140000 {     ...     iommus = &lt;&amp;ipmmu_ds1 32&gt;; }; </pre>  |
| GEther                          | <pre> gether: ethernet@e7400000 {     ...     iommus = &lt;&amp;ipmmu_ds1 34&gt;; }; </pre>   |



## **5.4 Option Setting**

### **5.4.1 Module Parameters**

There are no module parameters.

### **5.4.2 Kernel Parameters**

There are no kernel parameters.