1. Overview

1.1 Overview

This manual explains the driver module (this module) that controls the MSIOF Interfaces on R-Car H3/M3/M3N/E3/D3/V3U/V3H.

1.2 Function

This module transmits/receives data to/from a device connected to MSIOF on the R-Car H3/M3/M3N/E3/D3/V3U/V3H. The following table lists the function of this module.

Table 1.1 Driver Function

Function	Support status (R-Car H3/M3/M3N/E3/D3/V3H)	Support status (R-Car V3U)
Number of channels	4	6
Channel	Ch0 ~ Ch3	Ch0 ~ Ch5
Master Mode	Support	
Slave Mode	Support	
DMA function	Support	
MSIOF Chip select signal	Hardware control	
Settable word size	8, 16, 32 bits	
Settable transfer size	Set multiple of the word size by byte unit.	
Module Clock	R-Car H3/M3/M3N/E3/D3/V3U/V3H: 12.5MHz (initial value) - 133.33MHz	
Max transfer frequency	For R-Car H3/M3/M3N/E3/D3/V3U/V3H: MSIOF_SCK clock cycle time (when master TX or slave RX): “Module Clock” / 4 MSIOF_SCK clock cycle time (when master RX or slave TX): “Module Clock” / 8 Please designate the set value which considered an electrical characteristic as the transfer rate designated by application. (refer to R-Car Series, “3rd Generation Additional Document for User’s Manual: Hardware”)	

When you would like to use DMA transfer, please set the transfer size to the value calculated by the following Equation1. Other sizes will transfer 256m by DMA and transfer the remainder by PIO.

DMA transfer size = 16 + 4n + 256m ・・・ (Equation1)

n: 0, 1, 2, ～ 60

m: 0, 1, 2, ...

Ex)

In case of 510 bytes, 256 bytes will be transferred by DMA and 254 bytes will be transferred by PIO.

In case of 568 bytes, 256 bytes and 256 bytes and 56 bytes will be transferred by 3 times DMA.

In case of 266 bytes, 256 bytes will be transferred by DMA and 10 bytes will be transferred by PIO.

1.3 Connected device

This chapter describes the connected device to MSIOF. Please refer to the following tables for each device.

Table 1.2 MSIOF Connected device (R-Car H3/M3/M3N)

MSIOF Channel	Connected device	Support Status	Note
Ch0	None	No	—
Ch1	None	No	—
Ch2	None	No	—
Ch3	None	No	—

Table 1.3 MSIOF Connected device (R-Car E3)

MSIOF Channel	Connected device	Support Status	Note
Ch0	LVDS Control Connector – CN41	No	—
Ch1	None	No	—
Ch2	None	No	—
Ch3	None	No	—

Table 1.4 MSIOF Connected device (R-Car D3)

MSIOF Channel	Connected device	Support Status	Note
Ch0	None	No	—
Ch1	None	No	—
Ch2	LVDS Control Connector – CN41	No	—
Ch3	None	No	—

Table 1.5 MSIOF Connected device (R-Car V3U)

MSIOF Channel	Connected device	Support Status	Note
Ch0	None	No	—
Ch1	None	No	—
Ch2	None	No	—
Ch3	None	No	—
Ch4	None	No	—
Ch5	None	No	—

Table 1.6 MSIOF Connected device (R-Car V3H)

MSIOF Channel	Connected device	Support Status	Note
Ch0	CN17 - Multiplexed with JTAG2 signals	No	—
Ch1	None	No	—
Ch2	None	No	—
Ch3	None	No	—

Note : The MSIOF0, and other functions (e.g. DU_DRGB[1:0] functions) are multiplexed on the same pins as the JTAG2 functions due to the specifications of the R-CarV3H's pin function controller. Accordingly, when the JTAG2 functions are in use, the MSIOF0 and other functions are not available. Due to the specifications of the R-CarV3H's JTAG2 interface, the power-supply voltage to the VDDQ_DU pins must be 1.8 V when that interface is to be used. If you will be using the Condor-I board with an expansion board that requires a 3.3 V power supply voltage, the JTAG2 connector (CN26) will not be usable because of the difference in the power-supply voltage.

1.4 Reference

1.4.1 Standard

There are no reference documents on standards.

1.4.2 Related documents

The following table shows the document related to this module.

Table 1.7 Related documents (R-Car H3/M3/M3N/E3/D3/V3U/V3H)

Number	Issue	Title	Edition	Data
-	Renesas Electronics	R-Car Series, 3rd Generation User's Manual: Hardware	Rev.2.20	Jun. 30, 2020
-	Renesas Electronics	R-CarH3-SiP System Evaluation Board Salvator-X Hardware Manual RTP0RC7795SIPB0011S	Rev.1.09	May. 11, 2017
-	Renesas Electronics	R-CarM3-SiP System Evaluation Board Salvator-X Hardware Manual RTP0RC7796SIPB0011S	Rev.0.04	Oct. 3, 2016
-	Renesas Electronics	R-CarH3-SiP/M3-SiP/M3N-SiP System Evaluation Board Salvator-XS Hardware Manual	Rev.2.04	Jul. 17, 2018
-	Renesas Electronics	R-CarE3 System Evaluation Board Ebisu Hardware Manual RTP0RC77990SEB0010S	Rev.0.03	Apr. 11, 2018
-	Renesas Electronics	R-CarE3 System Evaluation Board Ebisu-4D (E3 board 4xDRAM) Hardware Manual	Rev.1.01	Jul. 19, 2018
-	Renesas Electronics	R-Car V3U Series User's Manual	Rev.0.5	Jul. 31, 2020
-	Renesas Electronics	R-CarV3U System Evaluation Board Falcon Hardware Manual	Rev.0.01	Sep. 11, 2020
-	Renesas Electronics	R-Car V3H_2 Additional Document for User's Manual: Hardware	Rev.0.50	Jul. 31, 2020
-	Renesas Electronics	R-CarV3H System Evaluation Board Condor-I Hardware Manual	Rev.0.02	Nov. 11, 2020
-	Renesas Electronics	R-CarD3 System Evaluation Board Hardware Manual RTP0RC77995SEB0010S	Rev.1.20	Jul. 25, 2017

1.5 Restriction

There is no restriction in this module.

1.6 Notice

When once of transmission exceeds 256 byte, it's possible to transfer with 2 group. (But present driver is not supported.)

When being used in 256 byte x 2group, a SS signal is asserted by the 512 byte unit.

When an asserting period of a SS signal requires more than 512 bytes, control by GPIO is needed.

The DTDL of SITMDR1/SIRMDR1 is set the fixed value (2 clock cycle delay) in case of R-Car H3 Ver.3.0 by the H/W specification.

2. Operating Environment

2.1 Hardware Environment

The following table lists the hardware needed to use this module.

Table 2.1 Hardware specification (R-Car H3/M3/M3N/E3/D3/V3U/V3H)

Name	Version	Manufacture
R-CarH3-SiP System Evaluation Board Salvator-X	-	Renesas Electronics
R-CarM3-SiP System Evaluation Board Salvator-X	-	Renesas Electronics
R-CarH3-SiP/M3-SiP/M3N-SiP System Evaluation Board Salvator-XS	-	Renesas Electronics
R-CarE3 System Evaluation Board Ebisu	-	Renesas Electronics
R-CarE3 System Evaluation Board Ebisu-4D	-	Renesas Electronics
R-CarV3U System Evaluation Board Falcon	-	Renesas Electronics
R-CarV3H System Evaluation Board Condor-I	-	Renesas Electronics
R-CarD3 System Evaluation Board Draak	-	Renesas Electronics

2.2 Module Configuration

The following figure shows the configuration of this module.

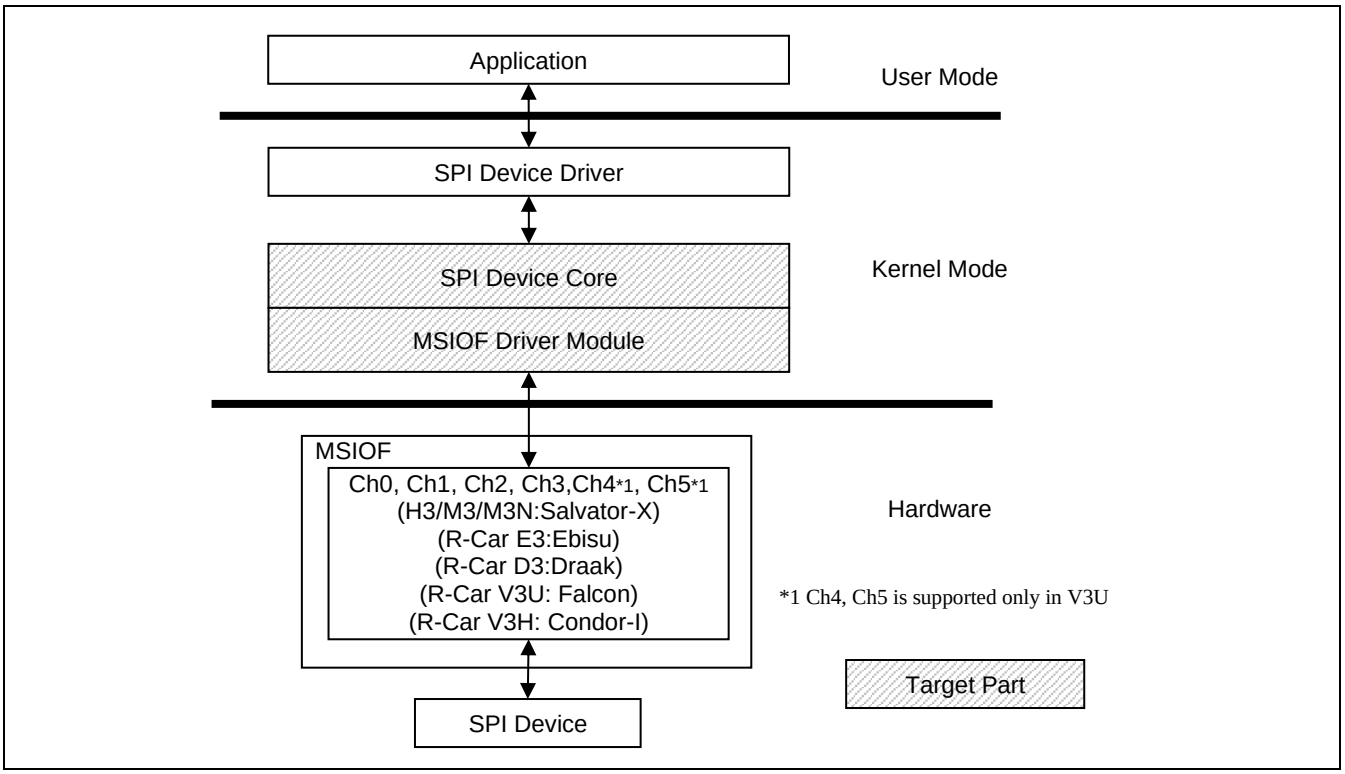

Figure 2.1 Module configuration (R-Car H3/M3/M3N/E3/D3/V3U/V3H)

2.3 State Transition Diagram

There is no state transition diagram for this module.

3. External Interface

Detailed explanation is skipped because the external interface of this module is based on Linux.

4. Integration

4.1 Directory Configuration

The directory configuration is shown below.

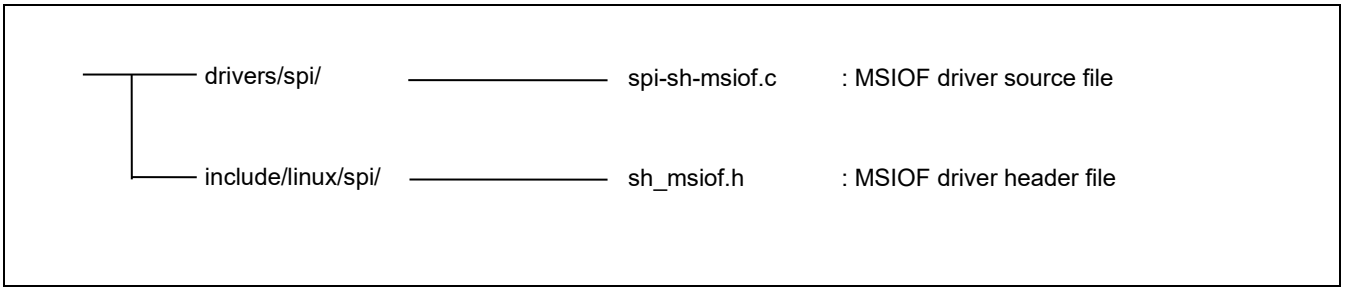

Figure 4-1 Directory Configuration (R-Car H3/M3/M3N/E3/D3/V3U/V3H)

4.2 Integration Procedure

Add the setting of the channel to be used.
Add "Pin Function", "Clock setting", "Channel Node setting", "sub node setting" to the device tree and add the compatible value of the sub node to spidev.c.

4.2.1 Device tree setting

Typical editing examples are shown below. The device tree file name varies depending on the board to be used. Please refer to the user's manual of Kernel Core for the device tree file name.

・Example for R-Car H3 Ver.3.0 or later(In case of Salvator-XS board)
File path: arch/arm64/boot/dts/renesas/r8a77951-salvator-xs-4x2g.dts

・Example for R-Car E3(In case of Ebisu board)
File path: arch/arm64/boot/dts/renesas/r8a77990-ebisu.dts

・Example for R-Car D3 (In case of Draak board)
File path: arch/arm64/boot/dts/renesas/r8a77995-draak.dts

・Example for R-Car V3U (In case of Falcon board)
File path: arch/arm64/boot/dts/renesas/r8a779a0-falcon.dts

・Example for R-Car V3H (In case of Condor-I board)
File path: arch/arm64/boot/dts/renesas/r8a77980-condor.dts

Edit the device tree as follows.
- 4.2.1.1 Pin Function setting
- 4.2.1.2 Clock setting
- 4.2.1.3 Channel Node setting
- 4.2.1.4 sub node setting

4.2.1.1 Pin Function setting

The editing contents are shown in Figure 4-2 (Example for r8a77951-salvator-xs-4x2g.dts).

```
&pfc {
        msiof0_pins: spi0 {
                groups = "msiof0_clk", "msiof0_sync",
                         "msiof0_rxd",    "msiof0_txd";
                function = "msiof0";
        };

        msiof1_pins: spi1 {
                groups = "msiof1_clk_c", "msiof1_sync_c",
                         "msiof1_rxd_c",    "msiof1_txd_c";
                function = "msiof1";
        };

        msiof2_pins: spi2 {
                groups = "msiof2_clk_b", "msiof2_sync_b",
                         "msiof2_rxd_b",    "msiof2_txd_b";
                function = "msiof2";
        };

        msiof3_pins: spi3 {
                groups = "msiof3_clk_d", "msiof3_sync_d",
                         "msiof3_rxd_d",    "msiof3_txd_d";
                function = "msiof3";
        };
};
```

Figure 4-2 Pin Function setting (Example for r8a77951-salvator-xs-4x2g.dts)

The editing contents are shown in Figure 4-3 (Example for r8a77990-ebisu.dts).

```
&pfc {
        msiof0_pins: spi0 {
                groups = "msiof0_clk", "msiof0_sync",
                         "msiof0_rxd", "msiof0_txd";
                function = "msiof0";
        };
};
```

Figure 4-3 Pin Function setting (Example for r8a77990-ebisu.dts)

The editing contents are shown in Figure 4-4 (Example for r8a77995-draak.dts).

```
&pfc {
        msiof0_pins: spi0 {
                groups = "msiof0_clk", "msiof0_sync",
                         "msiof0_rxd", "msiof0_txd";
                function = "msiof0";
        };

        msiof2_pins: spi2 {
                groups = "msiof2_clk", "msiof2_sync_b",
                         "msiof2_rxd", "msiof2_txd";
                function = "msiof2";
        };
};
```

Figure 4-4 Pin Function setting (Example for r8a77995-draak.dts)

The editing contents are shown in Figure 4-5 (Example for r8a779a0-falcon.dts).

```
&pfc {
        msiof0_pins: spi0 {
                groups = "msiof0_clk", "msiof0_sync",
                         "msiof0_rxd", "msiof0_txd";
                function = "msiof0";
                power-source = <1800>;
        };

        msiof1_pins: spi1 {
                groups = "msiof1_clk", "msiof1_sync",
                         "msiof1_rxd", "msiof1_txd";
                function = "msiof1";
                power-source = <1800>;
        };

        msiof2_pins: spi2 {
                groups = "msiof2_clk", "msiof2_sync",
                         "msiof2_rxd", "msiof2_txd";
                function = "msiof2";
                power-source = <1800>;
        };
};
```

Figure 4-5 Pin Function setting (Example for r8a779a0-falcon.dts)

The editing contents shown in Figure 4-6 (Example for r8a77980-condor.dts)

```
&pfc {
        msiof0_pins: spi0 {
                groups = "msiof_clk", "msiof0_sync",
                         "msiof0_rxd",    "msiof0_txd";
                function = "msiof0";
        };
        msiof1_pins: spi1 {
                groups = "msiof1_clk", "msiof1_sync",
                         "msiof1_rxd",    "msiof1_txd";
                function = "msiof1";
        };
        msiof2_pins: spi2 {
                groups = "msiof2_clk", "msiof2_sync",
                         "msiof2_rxd",    "msiof2_txd";
                function = "msiof2";
        };
        msiof3_pins: spi3 {
                groups = "msiof3_clk", "msiof3_sync",
                         "msiof3_rxd",    "msiof3_txd";
                function = "msiof3";
        };
};
```

Figure 4-6 Pin Function setting (Example for r8a77980-condor.dts)

4.2.1.2 Clock setting

Define the original clock for generating the bus speed.

```
/* module clock */
&msiof_ref_clk {
        clock-frequency = <133333333>; *1
};

*1 Please set a value based on electrical characteristics.
```

Figure 4-7 Clock setting

4.2.1.3 Channel Node setting

Enable status property.

```
&msiof0 {
        pinctrl-0 = <&msiof0_pins>;
        pinctrl-names = "default";
        /* Please use exclusively to the rcar_sound node */
        /* status = "okay"; */

        /* Add a subnode. */
};

&msiof1 {
        pinctrl-0 = <&msiof1_pins>;
        pinctrl-names = "default";
        /* In case of using this node, please enable this property */
        /* status = "okay"; */

        /* Add a subnode. */
};

&msiof2 {
        pinctrl-0 = <&msiof2_pins>;
        pinctrl-names = "default";
        /* In case of using this node, please enable this property */
        /* status = "okay"; */

        /* Add a subnode. */
};

&msiof3 {
        pinctrl-0 = <&msiof3_pins>;
        pinctrl-names = "default";
        /* In case of using this node, please enable this property */
        /* status = "okay"; */

        /* Add a subnode. */
};
```

Figure 4-8 Channel Node setting

4.2.1.4 sub node setting

Add a subnode to the channel node in Figure 4-8. Subnode is partially defined in master mode and slave mode.

Use the slave device name of the connection destination as the compatible value. The following form is ideal.
Maker name, slave device name

The editing contents sample for master mode are shown in Figure 4-9.

```
/* Add a subnode. */
slavedev {
        compatible = "maker,slavedev";
        reg = <0>;
        spi-max-frequency = <16666666>;
        spi-cpha;
        spi-cpol;
};
```

Figure 4-9 Subnode definition for master mode

The subnode name in slave mode is "slave".
The editing contents sample for slave mode are shown in Figure 4-10.

```
spi-slave;

/* Add a subnode. */
slave {
        compatible = "maker,slavedev";
        spi-cpha;
        spi-cpol;
};
```

Figure 4-10 Subnode definition for slave mode

4.2.2 Add userspace interface

Add the compatible value of the subnode to the next file.
file : drivers/spi/spidev.c

```
static const struct of_device_id spidev_dt_ids[] = {
        . . .
        { .compatible = "maker,slavedev" },        <-- Add this line.
        {},
};
```

Figure 4-11 User space interface

4.2.3 Kernel configuration

To enable the function of this module, make the following setting with Kernel Configuration. The changes affect after re-building the kernel.

```
Device Drivers    --->
        [*] SPI support    -->
                --- SPI support
                  <*>   SuperH MSIOF SPI Controller
                        ...
                        *** SPI Protocol Masters ***
                  <*>   User mode SPI device driver support
                        ...
                  [ ]   SPI slave protocol handlers *1
```

Figure 4-12 Kernel configuration (R-Car H3/M3/M3N/E3/D3/V3U/V3H)

Notes: *1: Please set if you want to enable SPI Slave mode.

4.3 Option Setting

4.3.1 Module Parameters

There are no module parameters.

4.3.2 Kernel Parameters

There are no module parameters.