R-Car Series, 3rd Generation

Energy Aware Scheduling

Introduction

[Background]

Third-generation R-Car series products have two types of CPU: Cortex-A57 and Cortex-A53 cores (eight in total for the R-Car H3 and six in total for the R-Car M3-W/R-Car M3-W+). In-vehicle information systems require several applications, such as for navigation, the playback of music or video, and the display of information on meters, to run at the same time. A multi-core environment, which includes multiple CPUs, is generally more suitable for such cases. Accordingly, R-Car H3, R-Car M3-W and R-Car M3-W+ products are suitable in such cases.

On the other hand, booting up the Cortex-A57 and Cortex-A53 cores with their different performances at the same time creates problems that we must take into account. Namely, since the Linux scheduler assigns tasks to CPUs such that the load on each of the CPUs is equal across the environment, the CPU by which a task is executed may switch between a Cortex-A57 and a Cortex-A53 during its execution. This leads to a problem of applications behaving unstably, including changes of operating speed on the user’s side. For example, this may lead to skipping of music during playback or video playback being interrupted.

Two methods can serve as solutions to this problem. One is applying processor affinity\* in the static assignment of tasks. This allows binding a task to a specified type of CPU to prevent another type of CPU from unexpectedly having to handle the task. The other is applying energy aware scheduling (EAS) in the dynamic assignment of tasks. This is provided as an enhanced function of the standard scheduler of the Linux OS and allows the scheduler to automatically judge the processing loads given tasks impose (which depend on the behavior of applications) and assign each task to an optimal CPU. This prevents unstable behavior by applications. This document describes EAS, the latter solution.

Note: \* For details on processor affinity, see the separate application note “R-Car Series, 3rd Generation Application Note Processor Affinity”.

[Purpose]

At the time of writing (as of October in 2016), EAS is a work in progress by the Linux community. Renesas will not formally support EAS until it’s officially posted by the upstream parties. Therefore, on the assumption that users will request an environment to evaluate EAS in advance, we provide this document as a guide to the advance evaluation of EAS. For this reason, the document only covers the EAS operations in outline, how to apply the patch set, and examples of applying EAS.

[Target Readers]

Readers of this document are assumed to have general knowledge in the fields and specific technologies listed below.

* Engineering, logic circuits, microcontrollers, and Linux.
* The functionality of the multiple processor cores of R-Car H3, R-Car M3-W and R-Car M3-W+ products.
* The electrical specifications of the multiple processor cores of R-Car H3, R-Car M3-W and R-Car M3-W+ products.
* The functions of the BSP drivers for R-Car H3, R-Car M3-W and R-Car M3-W+ products.

[Notes]

* Statements in relation to operating systems in this document only apply to Yocto v2.12.0 from Renesas (for the R-Car H3, R-Car M3-W) and not to any other versions of Yocto.
* As EAS is a prototype which the Linux community is developing at the time of writing (as of October of 2016), it may have problems. It may also be subject to change, depending on the thinking of the Linux community.
* The environment in which EAS is applied in the descriptions of this document was built in order to evaluate EAS in advance and its quality is thus equivalent to that of a prototype. In addition, Renesas does not support the application of EAS in your environment. If you do so, it is at your own responsibility.

Target Device

・R-Car H3

・R-Car M3-W/ R-Car M3-W+

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# Energy Aware Scheduling (EAS)

## Overview

### Overview of EAS

EAS is an enhanced scheduler based on the completely fair scheduler (CFS)\* and is for obtaining lower power consumption. It supports environments in which Cortex-A57 and Cortex-A53 cores are booted up at the same time. The major difference between CFS and EAS is the method of scheduling. The CFS assigns tasks to CPUs such that the load on each CPU is equal, while EAS assigns heavy-load tasks to the Cortex-A57s and low-load tasks to the Cortex-A53s. Furthermore, EAS applies control so that only the Cortex-A53 cores operate and places the Cortex-A57 cores in the idle state while no heavy-load tasks are running. This reduces power consumption. Namely, EAS handles a kind of low power consumption mode for multi-core processing.

A comparison of scheduling methods applicable in environments where the Cortex-A57 and Cortex-A53 cores are booted up at the same time is given in table 1-1.

Note: \* The completely fair scheduler (CFS) is the standard scheduler for the Linux OS.

Table 1‑1 Three Approaches to Scheduling

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Method | | Advantages | Disadvantages | Recommendation from Renesas |
| CFS  (the standard Linux scheduler) | The scheduler assigns tasks to CPUs such that the load on each CPU is equal. | Available for use with the standard board support package  (BSP) from Renesas. | Operation of the CFS is on the assumption of a symmetric multiprocessing (SMP) architecture, so its operation is not suitable in an environment where the Cortex-A57 and Cortex-A53 cores are operating at the same time. | We do not recommend its use in an environment in which Cortex-A57 and Cortex-A53 cores are operating at the same time. |
| Processor affinity | Processor affinity binds tasks to specified CPUs. | Available for use with the standard board support package  (BSP) from Renesas. | The assignment of tasks requires consideration and design from the viewpoint of the system as a whole. | We recommend applying this as a solution if you are able to design and control the assignment of tasks from the viewpoint of the system as a whole. |
| EAS | EAS allows the scheduler to automatically assign tasks to CPUs that are suitable for the loads of the respective tasks. | The dynamic assignment of tasks in an environment where the Cortex-A57 and Cortex-A53 cores are booted up at the same time is possible. | Continuous maintenance, such as continuously obtaining the latest code under development, is required to secure quality approaching suitability for commercial use. | You can only apply EAS as a solution with its support and maintenance as your own responsibility. |

### State of EAS Development

EAS was investigated and is under development by the Linux community. The latest patch set (as of October in 2016) is EAS v5.2. Forthcoming version updates and their timing depend on the Linux community.   
Note that Renesas does not formally support EAS during its development, but plan to formally support it after a mature version is posted upstream.

**2014**

**2015**

**2016**

**2017**

EAS RFC v2.0

Jul 2014

EAS RFC v1.0

May 2014

EAS RFC v5.0

Jul 2015

EAS RFC v4.0

May 2015

EAS RFC v3.0

Feb 2015

**EAS RFC v5.2**

**Dec 2015**

Figure 1‑1 Progress of EAS Development

### Potential Problems with EAS

* Even if the system as a whole imposes a heavy load, tasks may not be assigned to some of the CPUs.\*
* When a heavy-load task is awakened, the task may be temporarily assigned to a Cortex-A53 core. This is likely to result in overly long times for processing.\*

Note: \* These restrictions apply to EAS v5.2. Resolution of these potential problems depends on the Linux community.

## Operation in Outline

EAS when applied to assigning tasks handles the following functions, including some that are incidental to EAS.

* Monitoring how much load is being imposed on each of the CPU cores
* Dynamically assigning tasks that have been awakened and can be executed to suitable CPU cores
* Assigning tasks that have been recognized as low-load to low-power-consumption CPU cores as far as possible so that high-performance and high-power-consumption CPU cores can be placed in the idle state. This reduces power consumption of the system as a whole.

An outline of the principle of operation is given below.

EAS assigns tasks as follows. The design of EAS is based on a concept that scheduling proceeds so as to minimize power consumption while securing the specified processing performance of the system. Assigning tasks with the processing speed and power consumption of CPUs taken into account is a different approach from previous concepts. Accordingly, this enables scheduling that is appropriate in a system that runs with a combination of two types of CPU (the Cortex-A57 and Cortex-A53 cores) with their asymmetrical processing speeds and levels of power consumption.

* Basic algorithm used to assign tasks

Step 1: Select the CPUs that are currently idle and have the processing speed to suit the load that a given task imposes.

Step 2: Assign the task to the CPU with the lowest power consumption from among the CPUs selected in step 1.

* Processing speed and power consumption of CPUs

In EAS, a description of the processing speed and power consumption of the CPUs is referred to as an energy model. An energy model consists of the parameters required in scheduling and must be defined for each CPU configuration. For details, see section 1.4.

Figure 1-2 is a schematic view of the application of EAS to the dynamic assignment of tasks.

Note: The values in the figure are for reference, so do not have particular meanings.

Task B

Task A

Task C

Cortex-A57 (**1400**)

Cortex-A53 (**400**)

Linux kernel

Heavy   
load

Low load

Medium   
load

User

CPU 0

CPU 1

CPU 2

CPU 3

Scheduler

**EAS**

Processing speeds of the CPUs

1024

800

200

400

1024

512

512

Values: Loads imposed by the tasks

Values in plain type: Processing speeds of the CPUs

Values in bold type: Power consumption by the CPUs

Energy

models

Figure 1‑2 Schematic View of Applying EAS to the Assignment of Tasks

## Configuration of Modules

1. Block Diagram of Configuration of Software Modules

Linux kernel (4.6)

Hardware

Cortex-A57s

(big CPUs)

Scheduler

: Modules and processes modified for EAS

CPU

topology

Setting voltages

(2) Assignment of tasks

(3) Notification

(1) Energy

models

CPU freq

EAS

ARM-specific framework

Power-management framework

Cortex-A53s

(little CPUs)

PMIC

Clock

Setting   
operating frequencies

Figure 1‑3 Configuration of Modules in an Environment where EAS is Applied

2. Overview of Software Modules

* CPU topology: Controls information on the CPU configuration.
* EAS: An enhanced scheduler for configurations with combinations of Cortex-A57 and Cortex-A53 cores
* CPU freq: Changes the operating frequency and voltage of the CPUs (through the schedutil gov).

3. Processing in Outline

(1) An energy model is a table of information on the processing speeds (in DMIPS) and levels of power consumption (in mW) of the individual CPUs. It is created at initialization of the kernel and used to make judgements on scheduling.

(2) EAS uses the energy model to assign tasks to CPUs as to minimize power consumption while still securing the specified processing performance of the system.

(3) EAS notifies the “CPU freq” module of events each time scheduling proceeds. The “CPU freq” module uses information on the load on the given CPU in dynamically changing its operating frequency. This processing is part of the standard way the Linux OS operates.

## Energy Model

An energy model is an information table including definitions of the processing speeds (in DMIPS) and levels of power consumption (in mW) of the individual CPUs in an SoC and thus depend on the characteristics of the SoC. This information table is used to schedule tasks. Accordingly, appropriate values must be specified in the table. Note that the patch set described in section 2 includes correction patch files for the energy models for use in version 1.1 of the R-Car H3 and version 1.0 of the R-Car M3-W. Use the settings in these files in your environment.

For reference, sample settings (for version 1.1 of the R-Car H3) are given below. Values here are not measured values, but are relative values derived from measurements.

<1> Definitions of power consumption in the idle state for each cluster

static struct idle\_state idle\_states\_cluster\_h3\_a53[] = {

{ .power = 17 }, /\* arch\_cpu\_idle() = WFI \*/

{ .power = 17 }, /\* WFI \*/

{ .power = 0 }, /\* cpu-sleep-0 \*/

{ .power = 0 }, /\* cluster-sleep-0 \*/

};

static struct idle\_state idle\_states\_cluster\_h3\_a57[] = {

{ .power = 98 }, /\* arch\_cpu\_idle() = WFI \*/

{ .power = 98 }, /\* WFI \*/

{ .power = 0 }, /\* cpu-sleep-0 \*/

{ .power = 0 }, /\* cluster-sleep-0 \*/

};

<2> Definitions of processing capacity usage and levels of power consumption in the active state for each cluster

static struct capacity\_state cap\_states\_cluster\_h3\_a53[] = {

/\* Power per cluster \*/

{ .cap = 383, .power = 17, }, /\* 1200 MHz \*/

};

static struct capacity\_state cap\_states\_cluster\_h3\_a57[] = {

/\* Power per cluster \*/

{ .cap = 310, .power = 66, }, /\* 500 MHz \*/

{ .cap = 560, .power = 82, }, /\* 1000 MHz \*/

{ .cap = 903, .power = 98, }, /\* 1500 MHz \*/

{ .cap = 964, .power = 126, }, /\* 1600 MHz \*/

{ .cap = 1024, .power = 154, }, /\* 1700 MHz \*/

};

<3> Definitions of power consumption in the idle state for each CPU

static struct idle\_state idle\_states\_core\_h3\_a53[] = {

{ .power = 17 }, /\* arch\_cpu\_idle() = WFI \*/

{ .power = 17 }, /\* WFI \*/

{ .power = 0 }, /\* cpu-sleep-0 \*/

{ .power = 0 }, /\* cluster-sleep-0 \*/

};

static struct idle\_state idle\_states\_core\_h3\_a57[] = {

{ .power = 148}, /\* arch\_cpu\_idle() = WFI \*/

{ .power = 148 }, /\* WFI \*/

{ .power = 0 }, /\* cpu-sleep-0 \*/

{ .power = 0 }, /\* cluster-sleep-0 \*/

};

<4> Definitions of processing capacity usage and levels of power consumption in the active state for each CPU

static struct capacity\_state cap\_states\_core\_h3\_a53[] = {

/\* Power per cpu \*/

{ .cap = 383, .power = 85, }, /\* 1200 MHz \*/

};

static struct capacity\_state cap\_states\_core\_h3\_a57[] = {

/\* Power per cpu \*/

{ .cap = 310, .power = 361, }, /\* 500 MHz \*/

{ .cap = 560, .power = 590, }, /\* 1000 MHz \*/

{ .cap = 903, .power = 820, }, /\* 1500 MHz \*/

{ .cap = 964, .power = 1116, }, /\* 1600 MHz \*/

{ .cap = 1024, .power = 1344, }, /\* 1700 MHz \*/

};

Notes: 1. This table is set according to the frequency table of the CPUs. Accordingly, changes to parts of the frequency table require updating of this table.

2. This table is defined in a statement in the arch/arm64/kernel/topology.c file for the kernel.

### Calculating Values for Use in Energy Models

Calculating values for these information tables requires the advance measurement of values for performance and current. Renesas has measured these in accord with guidelines from Linaro (refer to the Web page at the URL below).

<http://www.slideshare.net/linaroorg/bkk16tr08-how-to-generate-power-models-for-eas-and-ipa>

## Further Items to Consider

Applying EAS may require further considerations to be taken into account to suit the use case in which you are to apply it. Examples of such items are given in section 1.5.1.

### Giving Higher Priority to the Execution of Desired Applications

As described in section 1.2, EAS involves examining the processing speeds and levels of power consumption of the CPUs to determine which type of CPU is suitable for the load that a given task imposes. EAS then assigns the task to the selected type of CPU. It does this with reference to the state of the load of the task to be executed. Note that the states of loads change, such as due to temporarily being lowered. In some actual use cases, however, users may wish to give a task higher priority throughout its execution, or to have it run solely on Cortex-A57 cores independently of the state of the load. In such cases, consider additional countermeasures for this in the environment where you are applying EAS. Table 1-2 lists some use cases and measures in response for reference.

Table 1‑2 Additional Measures when EAS is being Applied

|  |  |  |
| --- | --- | --- |
| Use Case | Countermeasure | Remarks |
| Executing a given task solely on Cortex-A57 cores | Bind the task to the Cortex-A57 cores through any of the following methods: setting up cgroup, issuing the taskset command, or calling the sched\_setaffinity function | For more details on cgroup, the taskset command, and the sched\_setaffinity function, see the separate application note with the filename “R-Car series 3rd Genenation Application Note Processor Affinity”. |
| Always giving the highest priority to a particular task for execution | Changing the attribute of the task to a realtime process\* | Note that creating too many realtime processes in the system may lead to the other processes not being executed. |

Note: \* Realtime processes are always given higher priority in scheduling than normal processes.

The pthread\_create system call or the chrt command, etc. can be used to make a process realtime at the time of its generation, and the sched\_setscheduler system call or the chrt command, etc. can be used to give a process the realtime attribute after its creation.

# Building an Environment in which EAS is Applied

## Patch Set

1. URL for Downloading the EAS Patch Set

The EAS patch set being evaluated by Renesas is released on the git repository\* below.

git://github.com/renesas-rcar/meta-renesas-power.git

Note: \* This EAS patch set was created by porting the git repository at the URL below for use on R-Car H3 and R-Car M3-W products.

<http://www.linux-arm.org/git?p=linux-power.git> (branch: energy\_model\_rfc\_v5.2)

1. Functions in the EAS Patch Set that Have been Evaluated by Renesas for Use on R-Car H3 and R-Car M3-W Products

Table 2‑1 EAS Functions

**√: Functions Evaluated by Renesas**

**―: Functions not Evaluated by Renesas**

|  |  |  |  |
| --- | --- | --- | --- |
| Function Name | Function Evaluated or Not? | Description | Remarks |
| EAS core | √ | Controls the assignment of tasks by EAS. |  |
| Capacity awareness | √ | When a task is awakened, if it imposed a heavy load while it was previously running, it will be assigned to a CPU with higher processing capacity (a Cortex-A57). |  |
| CPU topology for aarch32 | ― | Defines the configuration of the CPUs of the AArch32 platform. | Third-generation R-Car series products do not support AArch32. |
| CPU topology for aarch64 | √ | Defines the configuration of the CPUs of the AArch64 platform. |  |
| Sched governor | ― | The Sched governor is the CPU freq governor for v5.2 of EAS. This is different from the new CPU freq governor, Schedutil, which has already been merged with the BSP for third-generation R-Car series products. | Sched governor is old and no longer necessary. |
| Sched tune | ― | Sched tune is for boosting the performance of the Sched governor as CPU freq. | This does not work with the schedutil governor. |
| Dynamic capacity scaling | ― | Adjusting the processing capacities of CPUs by controlling the operating frequency | This does not work with the schedutil governor. |

## Procedure for Building

1. Preparation in Advance

Step 1: Proceed with all build processes according to the procedure in the separate guidelines with the filename “RENESAS\_RCH3M3\_YoctoStartupGuide”.

Step 2: Change the settings according to the procedure in the separate application note with the filename “R-CarGen3\_ApplicationNote\_Processoraffinity” to boot all CPUs up.

1. Instructions for Building EAS

Step 1: Download the EAS patch set and load it into the working directory for building the Yocto environment you have created in the advance preparations above, and check it out.

$ cd $WORK

$ git clone git://github.com/renesas-rcar/meta-renesas-power.git

$ cd $WORK/meta-renesas-power

Step 2: Execute the source command.

$ cd $WORK

$ source poky/oe-init-build-env

Step 3: Add the meta-renesas-power line as a statement in the $WORK/build/conf/bblayers.conf file.

BBLAYERS ?= " \

${TOPDIR}/../poky/meta \

${TOPDIR}/../poky/meta-yocto \

${TOPDIR}/../poky/meta-yocto-bsp \

${TOPDIR}/../meta-renesas/meta-rcar-gen3 \

${TOPDIR}/../meta-linaro/meta-linaro-toolchain \

${TOPDIR}/../meta-openembedded/meta-oe \

${TOPDIR}/../meta-renesas-power \ <--- Add this line.

Step 4: Build by using bitbake.

$ cd $WORK/build

[For Wayland]

bitbake core-image-weston

[For BSP only]

bitbake core-image-minimal

Path for image output: $WORK/build/tmp/deploy/images/salvator-x/ directory.

# Appendix

# Examples of Applying EAS

## Overview

The result of applying EAS in an in-vehicle infotainment (IVI) use case in a demonstration (in a demonstration with three monitors) is described here as an example. In this use case, several applications are running at the same, so the load is heavy. In addition, the use case is close in configuration to an integrated cockpit, which is the target use case for the R-Car H3. These are the two reasons why we selected the triple monitor demo as a sample use case. The results of evaluation, including the differences between the existing environment (i.e., one where EAS was not applied) and an environment where EAS is applied, are given on the following pages.

1. Configuration

R-Car H3



Video

Map

Menu

Center display (for the navigation system)

Instrument cluster

Display for entertainment

LVDS

HDMI

HDMI

Figure A1‑1 Schematic View of the Connection of Three Monitors for the Demonstration

1. Comparison of Environments

Table A1‑1 Comparison of Specifications

|  |  |  |  |
| --- | --- | --- | --- |
|  | | Existing Environment | Environment where EAS is Applied |
| SoC | | R-Car H3 (version 1.1) | R-Car H3 (version 1.1) |
| CPU | | Cortex-A57 × 4, 1.5 GHz | Cortex-A57 × 4, 1.5 GHz  Cortex-A53 × 4, 1.2 GHz |
| RAM | | DDR4-2400, 2-ch. split | DDR4-2400, 2-ch. split |
| GPU | | PowerVR GX6650, 600 MHz | PowerVR GX6650, 600 MHz |
| Display | Center | LVDS, 1024 × 768 | LVDS, 1024 × 768 |
| Instruments | HDMI, 1920 × 1080 | HDMI, 1920 × 1080 |
| Video | HDMI, 1920 × 1080  MP4 (H.264) VCP decoding | HDMI, 1920 × 1080  MP4 (H.264) VCP decoding |

## Effects of EAS in Changing the Assignment of Tasks

The changes to the CPU utilization and task assignment after applying EAS are given in table A1-2.

Table A1‑2 Comparison of CPU Utilization and Task Assignment

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
|  | Existing Environment | | | Environment where EAS is Applied | |
| CPU Utilization | | Task Name | CPU Utilization | Task Name |
| CPU0 (Cortex-A57) | 48.3% | ivi\_infotainment, etc | | 10.1% | ivi\_infotainment, etc |
| CPU1 (Cortex-A57) | 44.2% | ivi\_instrument\_cluster | | 8.9% |  |
| CPU2 (Cortex-A57) | 43.2% | ivi\_camera\_daemon | | 9.4% |  |
| CPU3 (Cortex-A57) | 44.0% | ivi\_passenger,  weston, ivi\_daemon | | 9.6% |  |
| CPU4 (Cortex-A53) | ― | ― | | 52.2% | weston, ivi\_daemon |
| CPU5 (Cortex-A53) | ― | ― | | 40.8% | ivi\_instrument\_cluster |
| CPU6 (Cortex-A53) | ― | ― | | 39.9% | ivi\_camera\_daemon |
| CPU7 (Cortex-A53) | ― | ― | | 44.7% | ivi\_passenger |

Note: The values given here are for reference.

This result indicates that low-load tasks, which were judged to be able to run sufficiently well on Cortex-A53 cores, have automatically been assigned to Cortex-A53 cores in an environment with task assignment controlled by EAS.

## Summary of Results

The results in terms of the levels of CPU utilization and values for current drawn are given in table A1-3.

Table A1‑3 Comparison of Levels of CPU Utilization and Values for Current

|  |  |  |  |
| --- | --- | --- | --- |
|  | Existing Environment | Environment where EAS is Applied | Difference |
| Zϕ (for Cortex-A57s) | 1500 MHz | 1500 MHz |  |
| Z2ϕ (for Cortex-A53s) | ― | 1200 MHz |  |
| Cortex-A57 utilization | 44.9% | 11.1% | - 33.8% |
| Cortex-A53 utilization | 0% | 44.4% | + 44.4% |
| GPU utilization | 60% to 70% | 60% to 70% | ±0% |
| DVFS 0.8 V (Cortex-A57s + GPU) | 3000 mA | 2340 mA | - 660 mA |
| VDD 0.8 V (Cortex-A53s + other modules) | 4980 mA | 5380 mA | + 400 mA |
| Current (DVFS 1.0 + VDD 1.0) | 7980 mA | 7720 mA | - 260 mA |

Note: The values given here are for reference.

The result of this example indicates that applying EAS in an existing environment allows applications from the existing environment to run normally in an environment where the Cortex-A57 and Cortex-A53 cores are booted up at the same time. It also indicates that applying EAS only produced a small reduction in current drawn, but increased the spare processing capacities of the Cortex-A57 cores. This may allow additional applications to run.

# Times for Task Switching between the Cortex-A57 and Cortex-A53 Cores

Table A2-1 shows the times for task switching.

Table A2‑1 Times for Task Switching

|  |  |  |  |
| --- | --- | --- | --- |
|  | Cortex-A57  -> Cortex-A57 | Cortex-A57  -> Cortex-A53 | Cortex-A53  -> Cortex-A57 |
| Straddling of clusters | Same cluster, so none | Yes | Yes |
| Switching time | 28 µs | 33 µs | 35 µs |

<Measurement environment>

* Software: Yocto v2.12.0 (Linux BSP 3.3.2)
* SoC: R-Car H3 version 1.1 (on a Salvator-X board)
* Measurement method

1. Awaken any executable process (process A) which endlessly loops on CPU1.

2. Use the taskset command\* to switch the CPU on which process A runs to CPU2.

Note: \* taskset is a command used to change the settings for assigning processes to CPUs.

: Suspended

Measurement period

: Operating

１．CPU1 is running process A.

２．Process A is suspended.

３．The CPU to run process A is switched to CPU2.

４．Process A is awakened on CPU2.

A

CPU1

Run queue

CPU2

Run queue

A

A

Run queue

Run queue

CPU2

Run queue

CPU1

Run queue

CPU2

A

Run queue

CPU1

CPU1

CPU2

Run queue

Figure A2‑1 Flow of Task Switching

# Using EAS with Other Functions Related to Power Control

## Overview

This subsection describes how to use EAS with other functions related to power control at the same time for further lowering the power consumption in environments where EAS is being applied. Table A3-1 describes how each of the functions behaves in such an environment. All functions are able to operate with the Cortex-A57s, and can be used in the same way in the existing environment. On the other hand, some functions will only be made able to operate with the Cortex-A53s through individual extensions. In the first place, however, the Cortex-A53 is a low-power-consumption core in comparison with the Cortex-A57. Accordingly, even if we attempt to use any of the functions to save power on the Cortex-A53s, their effects may easily be assumed to be extremely small from the viewpoint of the system as a whole. For this reason, the functions related to power control, including “CPU idle”, “CPU freq”, intelligent power allocation (IPA), and emergency shutdown (EMS), are disabled for the Cortex-A53s in the EAS evaluation environment from Renesas.

Table A3‑1 Support for Functions Related to Power Control

**√: Able to operate.**

**∆: Only able to operate after extension of the given function.**

|  |  |  |  |
| --- | --- | --- | --- |
| Function\* | Cortex-A57 | Cortex-A53 | Remarks |
| CPU hotplug | √ | √ |  |
| CPU idle | √ | ∆ | This version does not support the “CPU idle” function because of a functional limitation. The function will be able to operate with later versions. |
| CPU freq | √ | ∆ | This version does not support the “CPU freq” function on the Cortex-A53 because it has not been evaluated. The function will be able to operate with later versions following individual extensions. |
| System Suspend to RAM | √ | √ |  |
| IPA | √ | ∆ | This version does not support the IPA function on the Cortex-A53 because it has not been evaluated. The function will be able to operate with later versions following individual extensions. |
| EMS | √ | ∆ |  |

Note: \* For details on each of the functions above, see the separate document with the filename “RENESAS\_RCH3M3\_PowerManagement\_UME”.

## Using the “CPU Idle” Function (T.B.D.)

## Using the “CPU Freq” Function (T.B.D.)

## Using Intelligent Power Allocation (IPA) and Emergency Shutdown (EMS)

### State of Support for IPA and EMS with EAS

The IPA and EMS functions change power to the CPUs to control the generation of heat in the SoC. For the Cortex-A57, both IPA and EMS are able to operate with EAS. For the Cortex-A53, IPA is not usable because it has not been evaluated and is not supported by the standard BSP. EMS may be made to operate by extending its functionality.

### Applying EMS on the Cortex-A53s

Define CPUs (Cortex-A53 cores) to be shut down when EMS starts in a statement in the device tree file of the kernel. An example of the settings is shown below.

arch/arm64/boot/dts/renesas/r8a7795.dtsi

emergency {

polling-delay = <1000>;

on-temperature = <110000>;

off-temperature = <95000>;

target\_cpus = <&a57\_1>,

<&a57\_2>,

<&a57\_3>,

<&a53\_0>, <---- CPU4 will be shut down when EMS starts.

<&a53\_1>, <---- CPU5 will be shut down when EMS starts.

<&a53\_2>, <---- CPU6 will be shut down when EMS starts.

<&a53\_3>; <---- CPU7 will be shut down when EMS starts.

status = "disabled";

};

Note: An individually extended function other than those of the standard Yocto package is used to change the settings in this case. Renesas does not support this extended function. Use it at your own responsibility.

Revision History

|  |  |  |  |
| --- | --- | --- | --- |
| Rev. | Date | Description | |
| Page | Summary |
| 1.01 | July, 2017 | — | First edition issued |
| 1.02 | March, 2019 | 1, 2 | Background, Target Readers, Target Device updated.(“R-Car M3-W+”) |
| 9,4 and 16 | HW device version word is changed from WS to version. |



**General Precautions in the Handling of Microprocessing Unit and Microcontroller Unit Products**

The following usage notes are applicable to all Microprocessing unit and Microcontroller unit products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Precaution against Electrostatic Discharge (ESD)

A strong electrical field, when exposed to a CMOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop the generation of static electricity as much as possible, and quickly dissipate it when it occurs. Environmental control must be adequate. When it is dry, a humidifier should be used. This is recommended to avoid using insulators that can easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors must be grounded. The operator must also be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions must be taken for printed circuit boards with mounted semiconductor devices.

2. Processing at power-on

The state of the product is undefined at the time when power is supplied. The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the time when power is supplied. In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the time when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the time when power is supplied until the power reaches the level at which resetting is specified.

3. Input of signal during power-off state

Do not input signals or an I/O pull-up power supply while the device is powered off. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Follow the guideline for input signal during power-off state as described in your product documentation.

4. Handling of unused pins

Handle unused pins in accordance with the directions given under handling of unused pins in the manual. The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of the LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible.

5. Clock signals

After applying a reset, only release the reset line after the operating clock signal becomes stable. When switching the clock signal during program execution, wait until the target clock signal is stabilized. When the clock signal is generated with an external resonator or from an external oscillator during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Additionally, when switching to a clock signal produced with an external resonator or by an external oscillator while program execution is in progress, wait until the target clock signal is stable.

6. Voltage application waveform at input pin

Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between VIL (Max.) and VIH (Min.) due to noise, for example, the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between VIL (Max.) and VIH (Min.).

7. Prohibition of access to reserved addresses

Access to reserved addresses is prohibited. The reserved addresses are provided for possible future expansion of functions. Do not access these addresses as the correct operation of the LSI is not guaranteed.

8. Differences between products

Before changing from one product to another, for example to a product with a different part number, confirm that the change will not lead to problems. The characteristics of a microprocessing unit or microcontroller unit products in the same group but having a different part number might differ in terms of internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

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