Raydium Semiconductor Corporation

RM690B0 User Guide

Single Chip Driver with 16.7M color for 480RGBx600 AMOLED

Preliminary Version

Date: Oct. 27, 2020

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On/Revision History

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1. Manufacture Command Set (MCS)

1.1 Command Control

(FE00h): CMD Mode Switch

R/W	Addr	D7	D6	D5	D4	D3	D2	D1	D0	HEX
W	FE00h	CMD_Page[7:0]								00h

Description

This command is used to switch the Manufacture Command Pages and User Commands sets.

CMD_Page[7:0]	Description
00h (default)	User Command Set (UCS = CMD1)
10h	Manufacture Command Set Page Panel ID
12h	Manufacture Command Set Page SID
20h	Manufacture Command Set Page Panel
40h	Manufacture Command Set Page ABH Mode
82h	Manufacture Command Set Page Power
92h	Manufacture Command Set Page SD timing
50h	Manufacture Command Set Page Gamma1
60h	Manufacture Command Set Page Gamma2
30h	Manufacture Command Set Page Gamma3
52h	Manufacture Command Set Page Gamma4
70h	Manufacture Command Set Page GOA Timing 1
F0h	Manufacture Command Set Page GOA Timing 2
42h	Manufacture Command Set Page DBV
22h	Manufacture Command Set Page SES
80h	Manufacture Command Set Page APRC
90h	Manufacture Command Set Page ACL
62h	Manufacture Command Set Page CGM
C2h	Manufacture Command Set Page CGM LUT

Restriction

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(FF00h): Read CMD Status

R/W	Addr	D7	D6	D5	D4	D3	D2	D1	D0	HEX
R	FF00h	CMD_Status[7:0]								00h

Description	This command is used to read the status of Manufacture Command Pages. Please refer to FE00h
Restriction	-

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1.2 MTP Program Flow

1.2.1 CMD2 Program Flow

CMD2 MTP Summary Table
Programmed by Customer

CMD2 Page10_Panel ID: Panel ID

Total Program Count = 3

1st Enable Program => CMD2 Page40_ABH Reg 0xEF40h, D[2]=PID_PGM_EN
1st Program Done Flag => CMD2 Page40_ABH Reg 0xB840h, D[7]=PID_1st_Done

2nd Enable Program => CMD2 Page40_ABH Reg 0xEF40h, D[2]=PID_PGM_EN
2nd Program Done Flag => CMD2 Page40_ABH Reg 0xB840h, D[6]=PID_2nd_Done

3rd Enable Program => CMD2 Page40_ABH Reg 0xEF40h, D[2]=PID_PGM_EN
3rd Program Done Flag => CMD2 Page40_ABH Reg 0xB840h, D[5]=PID_3rd_Done

CMD2 Page12_SID: Suppiler ID Code

Total Program Count = 3

1st Enable Program => CMD2 Page40_ABH Reg 0xF040h, D[7]=SID_PGM_EN
1st Program Done Flag => CMD2 Page40_ABH Reg 0xC240h, D[3]=SID_1st_Done

2nd Enable Program => CMD2 Page40_ABH Reg 0xF040h, D[7]=SID_PGM_EN
2nd Program Done Flag => CMD2 Page40_ABH Reg 0xC240h, D[2]=SID_2nd_Done

3rd Enable Program => CMD2 Page40_ABH Reg 0xF040h, D[7]=SID_PGM_EN
3rd Program Done Flag => CMD2 Page40_ABH Reg 0xC240h, D[1]=SID_3rd_Done

CMD2 Page20_Panel: Display Option etc.

Total Program Count = 2

1st Enable Program => CMD2 Page40_ABH Reg 0xEF40h, D[3]=Panel_PGM_EN
1st Program Done Flag => CMD2 Page40_ABH Reg 0xB940h, D[7]=Panel_1st_Done

2nd Enable Program => CMD2 Page40_ABH Reg 0xEF40h, D[3]=Panel_PGM_EN
2nd Program Done Flag => CMD2 Page40_ABH Reg 0xB940h, D[6]=Panel_2nd_Done

CMD2 Page40_ABH Mode: Display Mode and Frame Rate Control Option etc.

Total Program Count = 3

1st Enable Program => CMD2 Page40_ABH Reg 0xF040h, D[5]=ABH_PGM_EN
1st Program Done Flag => CMD2 Page40_ABH Reg 0xB840h, D[3]=ABH_1st_Done

2nd Enable Program => CMD2 Page40_ABH Reg 0xF040h, D[5]=ABH_PGM_EN
2nd Program Done Flag => CMD2 Page40_ABH Reg 0xB840h, D[2]=ABH_2nd_Done

3rd Enable Program => CMD2 Page40_ABH Reg 0xF040h, D[5]=ABH_PGM_EN
3rd Program Done Flag => CMD2 Page40_ABH Reg 0xB840h, D[1]=ABH_3rd_Done

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CMD2 Page82_power: Power etc.

Total Program Count = 2

1st Enable Program => CMD2 Page40_ABH Reg 0xEE40h, D[2]=power_PGM_EN
1st Program Done Flag => CMD2 Page40_ABH Reg 0xC040h, D[3]=power_1st_Done

2nd Enable Program => CMD2 Page40_ABH Reg 0xEE40h, D[2]=power_PGM_EN
2nd Program Done Flag => CMD2 Page40_ABH Reg 0xC040h, D[2]=power_2nd_Done

CMD2 Page92_SD timing: Source setting etc.

Total Program Count = 2

1st Enable Program => CMD2 Page40_ABH Reg 0xEE40h, D[1]=SD_timing_PGM_EN
1st Program Done Flag => CMD2 Page40_ABH Reg 0xC040h, D[7]=SD_timing_1st_Done

2nd Enable Program => CMD2 Page40_ABH Reg 0xEE40h, D[1]=SD_timing_PGM_EN
2nd Program Done Flag => CMD2 Page40_ABH Reg 0xC040h, D[6]=SD_timing_2nd_Done

CMD2 Page50_Gamma1: Gamma1 etc.

Total Program Count = 3

1st Enable Program => CMD2 Page40_ABH Reg 0xF040h, D[4]=gm1_PGM_EN
1st Program Done Flag => CMD2 Page40_ABH Reg 0xB940h, D[3]=gm1_1st_Done

2nd Enable Program => CMD2 Page40_ABH Reg 0xF040h, D[4]=gm1_PGM_EN
2nd Program Done Flag => CMD2 Page40_ABH Reg 0xB940h, D[2]=gm1_2nd_Done

3rd Enable Program => CMD2 Page40_ABH Reg 0xF040h, D[4]=gm1_PGM_EN
3rd Program Done Flag => CMD2 Page40_ABH Reg 0xB940h, D[1]=gm1_3rd_Done

CMD2 Page60_Gamma2: Gamma2 etc.

Total Program Count = 3

1st Enable Program => CMD2 Page40_ABH Reg 0xF040h, D[3]=gm2_PGM_EN
1st Program Done Flag => CMD2 Page40_ABH Reg 0xBA40h, D[7]=gm2_1st_Done

2nd Enable Program => CMD2 Page40_ABH Reg 0xF040h, D[3]=gm2_PGM_EN
2nd Program Done Flag => CMD2 Page40_ABH Reg 0xBA40h, D[6]=gm2_2nd_Done

3rd Enable Program => CMD2 Page40_ABH Reg 0xF040h, D[3]=gm2_PGM_EN
3rd Program Done Flag => CMD2 Page40_ABH Reg 0xBA40h, D[5]=gm2_3rd_Done

CMD2 Page30_Gamma3: Gamma3 etc.

Total Program Count = 3

1st Enable Program => CMD2 Page40_ABH Reg 0xEF40h, D[4]=gm3_PGM_EN
1st Program Done Flag => CMD2 Page40_ABH Reg 0xBA40h, D[3]=gm3_1st_Done

2nd Enable Program => CMD2 Page40_ABH Reg 0xEF40h, D[4]=gm3_PGM_EN
2nd Program Done Flag => CMD2 Page40_ABH Reg 0xBA40h, D[2]=gm3_2nd_Done

3rd Enable Program => CMD2 Page40_ABH Reg 0xEF40h, D[4]=gm3_PGM_EN
3rd Program Done Flag => CMD2 Page40_ABH Reg 0xBA40h, D[1]=gm3_3rd_Done

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CMD2 Page52_Gamma4: Gamma4 etc.

Total Program Count = 3

1st Enable Program => CMD2 Page40_ABH Reg 0xF040h, D[6]=gm4_PGM_EN
1st Program Done Flag => CMD2 Page40_ABH Reg 0xBB40h, D[7]=gm4_1st_Done

2nd Enable Program => CMD2 Page40_ABH Reg 0xF040h, D[6]=gm4_PGM_EN
2nd Program Done Flag => CMD2 Page40_ABH Reg 0xBB40h, D[6]=gm4_2nd_Done

3rd Enable Program => CMD2 Page40_ABH Reg 0xF040h, D[6]=gm4_PGM_EN
3rd Program Done Flag => CMD2 Page40_ABH Reg 0xBB40h, D[5]=gm4_3rd_Done

CMD2 Page70_GOA Timing 1: VSR.

Total Program Count = 2

1st Enable Program => CMD2 Page40_ABH Reg 0xF040h, D[2]=VSR_PGM_EN
1st Program Done Flag => CMD2 Page40_ABH Reg 0xBC40h, D[7]=VSR_1st_Done

2nd Enable Program => CMD2 Page40_ABH Reg 0xF040h, D[2]=VSR_PGM_EN
2nd Program Done Flag => CMD2 Page40_ABH Reg 0xBC40h, D[6]=VSR_2nd_Done

CMD2 PageF0_GOA Timing 2: VSR.

Total Program Count = 2

1st Enable Program => CMD2 Page40_ABH Reg 0xEF40h, D[5]=VSRB_PGM_EN
1st Program Done Flag => CMD2 Page40_ABH Reg 0xBC40h, D[3]=VSRB_1st_Done

2nd Enable Program => CMD2 Page40_ABH Reg 0xEF40h, D[5]=VSRB_PGM_EN
2nd Program Done Flag => CMD2 Page40_ABH Reg 0xBC40h, D[2]=VSRB_2nd_Done

CMD2 Page42_DBV: DBV.

Total Program Count = 2

1st Enable Program => CMD2 Page40_ABH Reg 0xEE40h, D[5]=DBV_PGM_EN
1st Program Done Flag => CMD2 Page40_ABH Reg 0xBF40h, D[7]=DBV_1st_Done

2nd Enable Program => CMD2 Page40_ABH Reg 0xEE40h, D[5]=DBV_PGM_EN
2nd Program Done Flag => CMD2 Page40_ABH Reg 0xBF40h, D[6]=DBV_2nd_Done

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CMD2 Page22_SES: SES.

Total Program Count = 2

1st Enable Program => CMD2 Page40_ABH Reg 0xF040h, D[0]=SES_PGM_EN
1st Program Done Flag => CMD2 Page40_ABH Reg 0xC140h, D[7]=SES_1st_Done

2nd Enable Program => CMD2 Page40_ABH Reg 0xF040h, D[0]=SES_PGM_EN
2nd Program Done Flag => CMD2 Page40_ABH Reg 0xC140h, D[6]=SES_2nd_Done

CMD2 Page80_APRC: APRC.

Total Program Count = 2

1st Enable Program => CMD2 Page40_ABH Reg 0xF040h, D[1]=APRC_PGM_EN
1st Program Done Flag => CMD2 Page40_ABH Reg 0xC140h, D[3]=APRC_1st_Done

2nd Enable Program => CMD2 Page40_ABH Reg 0xF040h, D[1]=APRC_PGM_EN
2nd Program Done Flag => CMD2 Page40_ABH Reg 0xC140h, D[2]=APRC_2nd_Done

CMD2 Page90_ACL: ACL

Total Program Count = 2

1st Enable Program => CMD2 Page40_ABH Reg 0xEF40h, D[6]=ACL_PGM_EN
1st Program Done Flag => CMD2 Page40_ABH Reg 0xBE40h, D[7]=ACL_1st_Done

2nd Enable Program => CMD2 Page40_ABH Reg 0xEF40h, D[6]=ACL_PGM_EN
2nd Program Done Flag => CMD2 Page40_ABH Reg 0xBE40h, D[6]=ACL_2nd_Done

CMD2 Page62_CGM: CGM.

Total Program Count = 2

1st Enable Program => CMD2 Page40_ABH Reg 0xEE40h, D[4]=CGM_PGM_EN
1st Program Done Flag => CMD2 Page40_ABH Reg 0xBF40h, D[3]=CGM_1st_Done

2nd Enable Program => CMD2 Page40_ABH Reg 0xEE40h, D[4]=CGM_PGM_EN
2nd Program Done Flag => CMD2 Page40_ABH Reg 0xBF40h, D[2]=CGM_2nd_Done

CMD2 PageC2_CGM LUT: CGM LUT

Total Program Count = 2

1st Enable Program => CMD2 Page40_ABH Reg 0xEE40h, D[0]=CGM_gm_PGM_EN
1st Program Done Flag => CMD2 Page40_ABH Reg 0xC240h, D[7]=CGM_gm_1st_Done

2nd Enable Program => CMD2 Page40_ABH Reg 0xEE40h, D[0]=CGM_gm_PGM_EN
2nd Program Done Flag => CMD2 Page40_ABH Reg 0xC240h, D[6]=CGM_gm_2nd_Done

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1.3 MCS: CMD2 Page10, Panel ID

Instruction	R/W	Addr	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Panel ID	R/W	0010h	Panel_ID1[7:0]								00h
Panel ID	R/W	0110h	Panel_ID2[7:0]								00h
Panel ID	R/W	0210h	Panel_ID3[7:0]								00h
Panel ID	R/W	0310h	Panel_ID4[7:0]								00h
Panel ID	R/W	0410h	Panel_ID5[7:0]								00h
Panel ID	R/W	0510h	Panel_ID6[7:0]								00h
Panel ID	R/W	0610h	Panel_ID7[7:0]								00h
Panel ID	R/W	0710h	Panel_ID8[7:0]								00h
Panel ID	R/W	0810h	Panel_ID9[7:0]								00h
Panel ID	R/W	0910h	Panel_ID10[7:0]								00h
Panel ID	R/W	0A10h	Panel_ID11[7:0]								00h
Panel ID	R/W	0B10h	Panel_ID12[7:0]								00h
Panel ID	R/W	0C10h	Panel_ID13[7:0]								00h
Panel ID	R/W	0D10h	Panel_ID14[7:0]								00h
Panel ID	R/W	0E10h	Panel_ID15[7:0]								00h
Panel ID	R/W	0F10h	Panel_ID16[7:0]								00h
Panel ID	R/W	1010h	Panel_ID17[7:0]								00h
Panel ID	R/W	1110h	Panel_ID18[7:0]								00h
Panel ID	R/W	1210h	Panel_ID19[7:0]								00h
Panel ID	R/W	1310h	Panel_ID20[7:0]								00h
Panel ID	R/W	1410h	Panel_ID21[7:0]								00h
Panel ID	R/W	1510h	Panel_ID22[7:0]								00h
Panel ID	R/W	1610h	Panel_ID23[7:0]								00h
Panel ID	R/W	1710h	Panel_ID24[7:0]								00h
Panel ID	R/W	1810h	Panel_ID25[7:0]								00h
Panel ID	R/W	1910h	Panel_ID26[7:0]								00h
Panel ID	R/W	1A10h	Panel_ID27[7:0]								00h
Panel ID	R/W	1B10h	Panel_ID28[7:0]								00h
Panel ID	R/W	1C10h	Panel_ID29[7:0]								00h
Panel ID	R/W	1D10h	Panel_ID30[7:0]								00h
Panel ID	R/W	1E10h	Panel_ID31[7:0]								00h
Panel ID	R/W	1F10h	Panel_ID32[7:0]								00h
CMD Mode Switch	W	FE10h	CMD_Page [7:0]								00h
RD CMD Status	R	FF10h	CMD_Status[7:0]								00h

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(0010h ~1F10h) Panel ID

R/W	Addr	D7	D6	D5	D4	D3	D2	D1	D0	HEX
R/W	0010h	Panel ID1[7:0]								00h
R/W	0110h	Panel ID2[7:0]								00h
R/W	0210h	Panel ID3[7:0]								00h
R/W	0310h	Panel ID4[7:0]								00h
R/W	0410h	Panel ID5[7:0]								00h
R/W	0510h	Panel ID6[7:0]								00h
R/W	0610h	Panel ID7[7:0]								00h
R/W	0710h	Panel ID8[7:0]								00h
R/W	0810h	Panel ID9[7:0]								00h
R/W	0910h	Panel ID10[7:0]								00h
R/W	0A10h	Panel ID11[7:0]								00h
R/W	0B10h	Panel ID12[7:0]								00h
R/W	0C10h	Panel ID13[7:0]								00h
R/W	0D10h	Panel ID14[7:0]								00h
R/W	0E10h	Panel ID15[7:0]								00h
R/W	0F10h	Panel ID16[7:0]								00h
R/W	1010h	Panel ID17[7:0]								00h
R/W	1110h	Panel ID18[7:0]								00h
R/W	1210h	Panel ID19[7:0]								00h
R/W	1310h	Panel ID20[7:0]								00h
R/W	1410h	Panel ID21[7:0]								00h
R/W	1510h	Panel ID22[7:0]								00h
R/W	1610h	Panel ID23[7:0]								00h
R/W	1710h	Panel ID24[7:0]								00h
R/W	1810h	Panel ID25[7:0]								00h
R/W	1910h	Panel ID26[7:0]								00h
R/W	1A10h	Panel ID27[7:0]								00h
R/W	1B10h	Panel ID28[7:0]								00h
R/W	1C10h	Panel ID29[7:0]								00h

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R/W	1D10h	Panel ID30[7:0]	00h
R/W	1E10h	Panel ID31[7:0]	00h
R/W	1F10h	Panel ID32[7:0]	00h

Description	To define Panel ID1 ~ Panel ID32
Restriction	

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(FE10h): CMD Mode Switch

R/W	Addr	D7	D6	D5	D4	D3	D2	D1	D0	HEX
W	FE10h	CMD_Page[7:0]								00h

Description

This command is used to switch the Manufacture Command Pages and User Commands sets.

CMD_Page[7:0]	Description
00h (default)	User Command Set (UCS = CMD1)
10h	Manufacture Command Set Page Panel ID
12h	Manufacture Command Set Page SID
20h	Manufacture Command Set Page Panel
40h	Manufacture Command Set Page ABH Mode
82h	Manufacture Command Set Page Power
92h	Manufacture Command Set Page SD timing
50h	Manufacture Command Set Page Gamma1
60h	Manufacture Command Set Page Gamma2
30h	Manufacture Command Set Page Gamma3
52h	Manufacture Command Set Page Gamma4
70h	Manufacture Command Set Page GOA Timing 1
F0h	Manufacture Command Set Page GOA Timing 2
42h	Manufacture Command Set Page DBV
22h	Manufacture Command Set Page SES
80h	Manufacture Command Set Page APRC
90h	Manufacture Command Set Page ACL
62h	Manufacture Command Set Page CGM
C2h	Manufacture Command Set Page CGM LUT

Restriction

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(FF10h): Read CMD Status

R/W	Addr	D7	D6	D5	D4	D3	D2	D1	D0	HEX
R	FF10h	CMD_Status[7:0]								00h

Description	This command is used to read the status of Manufacture Command Pages. Please refer to FE00h
Restriction	-

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1.4 MCS: CMD2 Page12, SID Code

Instruction	R/W	Addr	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Supplier ID Code information	R/W	0012h	SID[15:8]								01h
Supplier ID Code information	R/W	0112h	SID[7:0]								D0h
Supplier ID Code information	R/W	0212h	MID[15:8]								90h
Supplier ID Code information	R/W	0312h	MID[7:0]								80h
Supplier ID Code information	R/W	0412h	ID1[7:0]								00h
Supplier ID Code information	R/W	0512h	ID2[7:0]								80h
Supplier ID Code infomation	R/W	0612h	ID3[7:0]								00h
CMD Mode Switch		FE12h	CMD_Page [7:0]								00h
RD CMD Status	R	FF12h	CMD_Status[7:0]								00h

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(0012h~0612h) Supplier ID Code Information

R/W	Addr	D7	D6	D5	D4	D3	D2	D1	D0	HEX
R/W	0012h	SID[15:8]								01h
R/W	0112h	SID[7:0]								D0h
R/W	0212h	MID[15:8]								90h
R/W	0312h	MID[7:0]								80h
R/W	0412h	ID1[7:0]								00h
R/W	0512h	ID2[7:0]								80h
R/W	0612h	ID3[7:0]								00h

Description

This command is for Supplier ID Code

Bit	Description	Data
SID[15:0]	Supplier ID	01D0h

This command is for Supplier Elective data such as module number

Bit	Description	Data
MID[15:0]	Supplier Elective Data	9080h

This command is for Module Manufacture Number

Bit	Description	Data
ID1[7:0]	Module Manufactor Number	00h

This command is for Module/Driver Version Number

Bit	Description	Data
ID2[7:0]	Module/Driver Version Number	80h

This command is for Module / Driver ID

Bit	Description	Data
ID3[7:0]	Module /Driver ID	00h

Restriction

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(FE12h): CMD Mode Switch

R/W	Addr	D7	D6	D5	D4	D3	D2	D1	D0	HEX
W	FE12h	CMD_Page[7:0]								00h

Description

This command is used to switch the Manufacture Command Pages and User Commands sets.

CMD_Page[7:0]	Description
00h (default)	User Command Set (UCS = CMD1)
10h	Manufacture Command Set Page Panel ID
12h	Manufacture Command Set Page SID
20h	Manufacture Command Set Page Panel
40h	Manufacture Command Set Page ABH Mode
82h	Manufacture Command Set Page Power
92h	Manufacture Command Set Page SD timing
50h	Manufacture Command Set Page Gamma1
60h	Manufacture Command Set Page Gamma2
30h	Manufacture Command Set Page Gamma3
52h	Manufacture Command Set Page Gamma4
70h	Manufacture Command Set Page GOA Timing 1
F0h	Manufacture Command Set Page GOA Timing 2
42h	Manufacture Command Set Page DBV
22h	Manufacture Command Set Page SES
80h	Manufacture Command Set Page APRC
90h	Manufacture Command Set Page ACL
62h	Manufacture Command Set Page CGM
C2h	Manufacture Command Set Page CGM LUT

Restriction

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(FF12h): Read CMD Status

R/W	Addr	D7	D6	D5	D4	D3	D2	D1	D0	HEX
R	FF12h	CMD_Status[7:0]								00h

Description	This command is used to read the status of Manufacture Command Pages. Please refer to FE00h
Restriction	-

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1.5 MCS: CMD2 Page20, Panel Settings

Instruction	R/W	Addr	D7	D6	D5	D4	D3	D2	D1	D0	HEX
PANEL_SET	R/W	0020h	-	-	CRL[1:0]		-	SDCH_SEL[2:0]			00h
PANEL_SET	R/W	0120h	NL[7:0]								F0h
PANEL_SET	R/W	0220h	-	-	-	-	-	-	NL[9:8]		00h
PANEL_SET	R/W	0320h	-	-	1	-	-	-	MUX_num_sel[1:0]		40h
PANEL_SET	R/W	0420h	x_new_resol[7:0]								00h
PANEL_SET	R/W	0520h	x_new_en	-	-	-	-	-	x_new_resol[9:8]		00h
PANEL_SET	R/W	0620h	-	data_shift[6:0]							00h
PCD	R/W	0920h	-	-	-	PCD_EN	-	-	-	-	00h
PCD	R/W	0A20h	-	-	PCD_RES_TR[5:0]						02h
SAR	R/W	0B20h	-	-	-	-	-	disp_abnor_err	-	lcd_chksum_err	00h
SAR	R/W	0C20h	-	-	-	-	-	lv_flag_en	-	-	00h
SAR	R/W	0D20h					TE1_MODE[1:0]				00h
MIPI	R/W	2520h	-	DIS_EoTp_HS	DSIG	N565	DSIM	-	-	-	68h
	R/W	2620h	-	-	-	-	MIPI_dis_key[3:0]				00h
EQ	R/W	2820h	-	-	GREQ_SW[5:0]						00h
EQ	R/W	2920h	-	-	GFEQ_SW[5:0]						00h
VSR EQ	R/W	2A20h	-	-	GREQ_VSR[5:0]						00h
VSR EQ	R/W	2B20h	-	-	GFEQ_VSR[5:0]						00h
PD_SET	R/W	2D20h	-	-	-	-	PTD	-	-	-	00h
TE1 Output Setting	R/W	3620h	TE1_POSE_SEL[7:0]								00h
	R/W	3720h	TE1_period[7:0]								00h
	R/W	3820h	TE1_POSE_SEL[9:8]		TE1_period[9:8]		TE1_pol	TE1_EN	-		00h
HBM	R/W	4820h	HBM_auto_exit	-	-	-	-	-	HBM_auto_exit_pos[9:8]		00h
HBM	R/W	4920h	HBM_auto_exit_pos[7:0]								96h
HBM	R/W	4A20h	hbm_gidx_type	-	hbm_in_dim	hbm_out_dim	-	-	-	-	30h
SWIRE_CTRL	R/W	5220h	OLED_PWR_Sel	ext_oled_pwr_off[6:0]							10h
SWIRE_CTRL	R/W	5320h	int_oled_pwr_off_frame[1:0]		int_oled_pwr_off[5:0]						40h

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SWIRE_CTRL	R/W	5520h	swire_idle_pus_p[7:0]								00h
SWIRE_CTRL	R/W	5620h	swire_idle_pus_n[7:0]								00h
SWIRE_CTRL	R/W	5720h	swire_hbm_pus_p[7:0]								00h
SWIRE_CTRL	R/W	5820h	swire_hbm_pus_n[7:0]								00h
SWIRE Control	R/W	5920h	-	swire_off	idle_pwr_pus_en	hbm_pwr_pus_en	-	pwr_ic_update_sel	pwr_ic_sel	-	00h
OVSS Control	R/W	5A20h	APRC_ovss_def[7:0]								00h
P_PWR_ST	R/W	5B20h	P_PWR_ST0[7:0]								00h
MIPI	R/W	7C20h	lptx_freq_sel[1:0]		lptx_TAGETD_sel[1:0]		lptx_TAGOD_sel[1:0]		-	-	00h
MIPI	R/W	7D20h	-		tato_en	lptxto_en	hsrxto_en	-	vcid[1:0]		38h
MIPI	R/W	7E20h	dswap_sw	dswap	pswap_sw	pswap	-	-	-	lansel	00h
PCD	R	F320h	-	-	-	-	-	-	-	PCD_FLAG	00h
CMD Mode Switch	W	FE20h	CMD_Page [7:0]								00h
RD CMD Status	R	FF20h	CMD_Status[7:0]								00h

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(0020h) Panel Display Setting

R/W	Addr	D7	D6	D5	D4	D3	D2	D1	D0	HEX
R/W	0020h	-	-	CRL[1:0]		-	SDCH_SEL[2:0]			00h
R/W	0120h	NL[7:0]								F0h
R/W	0220h	-	-	-	-	-	-	NL[9:8]		00h
R/W	0320h	-	-	1	-	-	-	MUX_num_sel[1:0]		40h

Description

These commands area used to set panel option:

Bit	Description	Data
CRL[1:0]	CRL[1]: 1st pixel position is at right side or left side. . CRL[0]: 1st Source pad position is at right side or left side.	CRL[1]: 0: 1st pixel at left side 1: 1st pixel at right side CRL[0]: 0: 1st source pad at left side 1: 1st source pad at right side

Display H-resolution and MUX number of panel setting is as the following:

MUX_num_sel [1:0]	MUX Description	SDCH_SEL[2:0]	H-Resolution Description
0	MUX6	000	480RGB
		001	400RGB
		010	360RGB
		011	320RGB
		100	272RGB
		101	240RGB
		110	180RGB
		111	128RGB
3	MUX9	000	Reserved
		001	Reserved
		010	540RGB
		011	480RGB
		100	408RGB
		101	360RGB
		110	270RGB
		111	192RGB
Others	Reserved		

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	This command is used to vertical scan line for Display.

Bit	Value		Display Scan Line Number
NL[9:0]	00h	Reserved	Reserved
	01h	1	2 lines
	02h	2	4 lines
	:	:	= 2*NL[7:0]
	12Bh	299	598 lines
	12Ch	300	600 lines
	Others	Reserved	Reserved

Restriction	

	Left side								Right side							
OP_group	240~209	208~195	194~181	180~173	172~161	160~151	150~141	140~121	120~101	100~91	90~81	80~69	68~61	60~45	44~33	32~1
SDCH_SEL	0 is disable , 1 is enable								0 is disable , 1 is enable							
0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
1	1	1	1	1	1	1	1	0	0	1	1	1	1	1	1	1
2	1	1	1	1	1	1	0	0	0	0	1	1	1	1	1	1
3	1	1	1	1	1	0	0	0	0	0	0	1	1	1	1	1
4	1	1	1	1	0	0	0	0	0	0	0	0	1	1	1	1
5	1	1	1	0	0	0	0	0	0	0	0	0	0	1	1	1
6	1	1	0	0	0	0	0	0	0	0	0	0	0	0	1	1
7	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

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(0420h~0620h) Resolution New Setting

R/W	Addr	D7	D6	D5	D4	D3	D2	D1	D0	HEX
R/W	0420h	x_new_resol[7:0]								00h
R/W	0520h	x_new_en	-	-	-	-	-	x_new_resol[9:8]		00h
R/W	0620h	-	data_shift[6:0]							00h

Description	This command is used to set horizontal resolution when it is not in the above SDCH_SEL H-resolution list Bit: x_new_en — Enable control for new x-resolution Bit: data_shift[6:0] — Data-shift for the new x-resolution Bit: x_new_resol[9:0] — Set the new x-resolution
Restriction	xnew_resol/data_shift shall be divisible by 2 xnew_resol shall set to the value less than SDCH_SEL H-resolution

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(0920h, 0C20h, F320h) Panel Crack Detection

R/W	Addr	D7	D6	D5	D4	D3	D2	D1	D0	HEX
R/W	0920h	-	-	-	PCD_EN	-	-	-	-	00h
R/W	0A20h	-	-	PCD_RES_TR[5:0]						02h
R	F320h	-	-	-	-	-	-	-	PCD_FLAG	00h

Description

This command is used to set PCD detection enable and read the crack detection flag.

Bit	Description	Data
PCD_EN	PCD enable control	0 : Disable PCD function 1 : Enable PCD function
PCD_FLAG	PCD detection status	0 : Panel is OK 1 : Panel crack is detected

This command is used to set the detect range of panel resistance.

PCD_RES_TR[5:0]	Panel resistance	Unit
000000	20	Kohm
000001	30	Kohm
000010	40 (default)	Kohm
…	…	…
100000	340	Kohm
100001	350	Kohm
…	…	…
111111	650	Kohm

Restriction

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(0B20h~0C20h) Status Active Report Control

R/W	Addr	D7	D6	D5	D4	D3	D2	D1	D0	HEX
R/W	0B20h	-	-	-	-	-	disp_abnor_err	-	lcd_chksum_err	00h
R/W	0C20h	err_arise	-	-	-	-	lv_flag_err	-	-	00h
R/W	0D20h	-	-	-	-	TE1_MODE[1:0]		-	-	00h

Description

This command is to enable the status reporting function in addition to register checksum comparison.

Bit	Description
disp_abnor_err	1: Enable display abnormal error report 0: Disable display abnormal error report.
lcd_chksum_err	1: Enable display read cheksum error report 0: Disable display read cheksum error report
lv_flag_err	1: Enable low-voltage detection error report 0: Disable low-voltage detection error report
err_arise	1: enable error status record 0: disable error status record Error status includes: lcd_chksum, cmd_chksum and low-voltage detection flag.
TE1_MODE[1:0]	0: Disable status active reporting function. 2: Enable status active reporting function, TE1 output IC status active reporting. others: reserved.

Restriction

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(2520h) MIPI Packet Option Control

R/W	Addr	D7	D6	D5	D4	D3	D2	D1	D0	HEX
R/W	2520h	-	DIS_EoTp_HS	DSIG	N565	DSIM	-	-	-	68h

Description

This command is used to setup MIPI options for customer's application.

Bit	Description	Data
DSIG	Generic read/write data type enable/disable for MIPI DSI	0: Generic read/write disable 1: Generic read/write enable
DSIM	Video mode data type enable/disable for MIPI DSI	0: Disable 1: Enable
DIS_EoTP_HS	"DSI Protocol Violation" error reporting enable/disable control	0: Enable report function 1: Disable report function
N565	16-bit/pixel format (MSB to LSB) selection in MIPI command mode	"0": G[2:0]+R[4:0] & B[4:0]+G[5:3]
		"1": R[4:0]+G[5:3] & G[2:0]+B[4:0]

Restriction

(2620h) MIPI Interface Turn Off

R/W	Addr	D7	D6	D5	D4	D3	D2	D1	D0	HEX
R/W	2620h	-	-	-	-	MIPI_dis_key[3:0]				00h

Description

This command is used set turn off MIPI interface

Bit	Description	Value
MIPI_dis_key[3:0]	MIPI interface turn off	MIPI_dis_key[3:0]=1010: MIPI interface turn off Others setting: MIPI interface is active at IM=[00~10]

Restriction

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(2820h~2920h) SWITCH EQ Control

R/W	Addr	D7	D6	D5	D4	D3	D2	D1	D0	HEX
R/W	2820h	-	-	GREQ_SW[5:0]						00h
R/W	2920h	-	-	GFEQ_SW[5:0]						00h

Description

This command is used to control the EQ function for gate signals SW.

rb_GREQ_SW_XX[5:0]: time setting of EQ step for rising edge.

rb_GFEQ_SW_XX[5:0]: time setting of EQ step for falling edge.

rb_GREQ_SW_xxx[5:0]/ rb_GREQ_SW_xxx[5:0]	NO. of pixel clock	SW EQ time (us)
00h	0	0
01h	1	0.0417
02h	2	0.0833
:	:	:
3Fh	63	2.625

Notes: SW EQ time is calculated by pixel clock = 24MHz

Restriction

pixel clock frequency refers to PSELA/PSELB/PSELH setting description

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(2A20h~2B20h) VSR EQ Control

R/W	Addr	D7	D6	D5	D4	D3	D2	D1	D0	HEX
R/W	2A20h	-	-	GREQ_VSR[5:0]						00h
R/W	2B20h	-	-	GFEQ_VSR[5:0]						00h

Description

This command is used to control the EQ function for gate signals VSR.

rb_GREQ_VSR_XX[5:0]: time setting of EQ step for rising edge.

rb_GFEQ_VSR_XX[5:0]: time setting of EQ step for falling edge.

rb_GREQ_VSR_xxx[5:0]/ rb_GREQ_VSR_xxx[5:0]	NO. of pixel clock	SW EQ time (us)
00h	0	0
01h	1	0.0417
02h	2	0.0833
:	:	:
3Fh	63	2.625

Notes: SW EQ time is calculated by pixel clock = 24MHz

Restriction

pixel clock frequency refers to PSELA/PSELB/PSELH setting description

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(2D20h) Partial Display Non-display Setting

R/W	Addr	D7	D6	D5	D4	D3	D2	D1	D0	HEX
R/W	2D20h	-	-	-	-	PTD	-	-	-	00h

Description	This command is used to set non-display area of partial display. PTD: 0 = Black; 1 = White (Non-display area)
Restriction	

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(3620h~3820h) TE1 Output Setting

R/W	Addr	D7	D6	D5	D4	D3	D2	D1	D0	HEX
R/W	3620h	TE1_POSE_SEL[7:0]								00h
R/W	3720h	TE1_period[7:0]								00h
R/W	3820h	TE1_POSE_SEL[9:8]		TE1_period[9:8]		TE1_pol	TE1_EN	-	-	00h

Description

This command is to select the transient edge of TE1 signal. The timing reference start point is internal Hsync, and one unit is a pixel clock.

Bit	Value		Description
TE1_POSE_SEL[9:0]	0	000h	0 Clocks
	1	001h	1 Clock ~ 41.67ns
	:	:	41.67 ns / Clock
	512	200h	512 Clocks ~ 21335 ns
	Reserved		Reserved

Notes: Above table is calculated when pixel clock = 24MHz

This command is to select the period of TE1 signal. The timing reference start point is TE1 transient edge, and one unit is a pixel clock.

Bit	Value		Description
TE1_period[9:0]	0	000h	0 pixel clocks
	1	001h	1 pixel clock = 41.67ns
	:	:	41.67 ns / clock
	512	200h	512 clocks = 21335 ns
	Reserved		Reserved

Notes: Above table is calculated when pixel clock = 24MHz

TE1_pol/TE1_EN are used to set TE1 enable and polarity

Bit	Description	Value
TE1_pol	TE1 Output Polarity	0: Low Actve 1: Hi Active
TE1_EN	TE1 Output Control	0: Disable FTE1 Output 1: Enable FTE1 Output

Restriction

TE1_POSE_SEL + TE1_period < T1A/T1B/T1H

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(4820h ~ 4920h) HBM Auto Exit

R/W	Addr	D7	D6	D5	D4	D3	D2	D1	D0	HEX
R/W	4820h	HBM_auto_exit	-	-	-	-	-	HBM_auto_exit_pos[9:8]		00h
R/W	4920h	HBM_auto_exit_pos[7:0]								96h

Description	HBM_auto_exit: HBM exit automatically when timeout. HBM_auto_exit_pos: the HBM timeout setting. (Unit: 4frames)
Restriction	

(4A20h) HBM Type Selection

R/W	Addr	D7	D6	D5	D4	D3	D2	D1	D0	HEX
R/W	4A20h	hbm_gidx_type	-	hbm_in_dim	hbm_out_dim	-	-	-	-	30h

Description	hbm_gidx_type: 1: The brightness of HBM is controlled by 0x6300 and IC provides the HBM dimming. 0: To implement HBM by gamma setting only. hbm_in_dim: 1: To enable brightness dimming when into HBM mode 0: To disable brightness dimming when into HBM mode hbm_out_dim: 1: To enable brightness dimming when exit HBM mode 0: To disable brightness dimming when exit HBM mode
Restriction	

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(5220h~5320h) Swire Control

R/W	Addr	D7	D6	D5	D4	D3	D2	D1	D0	HEX
R/W	5220h	OLED_PWR_Sel	ext_oled_pwr_off[6:0]							10h
R/W	5320h	int_oled_pwr_off_frame[1:0]		int_oled_pwr_off[5:0]						40h

Description

This command is used to set internal/external OLED power control via swire as below,

Bit	Description	Value
OLED_PWR_Sel	Internal/external OVDD/OVSS selection at IDLE mode	0: external 1: internal
ext_oled_pwr_off[6:0]	Line number to leave extenal power	0~127: line number
int_oled_pwr_off_frame[1:0]	Frame number to leave internal power	0~2: frame number
int_oled_pwr_off[5:0]	Line number to leave internal power	0: 0*32 = 0 line 1: 1*32 = 32 lines … 63: 63*32 = 2016 lines

Restriction

1. int_oled_pwr_off[5:0] setting value < NL*2.
2. int_oled_pwr_off_frame[1:0]+ int_oled_pwr_off[5:0] setting value ≦ 2 frame

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(5520h~5820h) SWIRE Pulse Setting

R/W	Addr	D7	D6	D5	D4	D3	D2	D1	D0	HEX
R/W	5520h	swire_idle_pus_p[7:0]								00h
R/W	5620h	swire_idle_pus_n[7:0]								00h
R/W	5720h	swire_hbm_pus_p[7:0]								00h
R/W	5820h	swire_hbm_pus_n[7:0]								00h

Description

This command is for SWIRE output control

Bit	Description	Data
swire_idle_pus_p	The IDLE mode swire default setting of positive voltage	0~255 Enable when idle_pwr_pus_en=1
swire_idle_pus_n	The IDLE mode swire default setting of negative voltage	0~255 Enable when idle_pwr_pus_en=1
swire_hbm_pus_p	The HBM mode swire default setting of positive voltage	0~255 Enable when hbm_pwr_pus_en =1
swire_hbm_pus_n	The HBM mode swire default setting of negative voltage	0~255 Enable when hbm_pwr_pus_en =1

Restriction

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(5920h) SWIRE Control

R/W	Addr	D7	D6	D5	D4	D3	D2	D1	D0	HEX
R/W	5920h	-	swire_off	idle_pwr_pus_en	hbm_pwr_pus_en	-	pwr_ic_update_sel	pwr_ic_sel	-	00h

Description

This command is for SWIRE output control

Bit	Description	Data
pwr_ic_sel	PWR IC type selection	0: negative volt type only 1: positive and negative voltages type
idle_pwr_pus_en	Enable/Disable IDLE mode swire pulse	0: disable 1: enable
hbm_pwr_pus_en	Enable/Disable HBM mode swire pulse	0: disable 1: enable
swire_off	Swire function turn on/off	0: turn ON 1: turn OFF
pwr_ic_update_sel	Swire update method	0: update on target changed 1: update every frame

Restriction

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(5A20h) OVSS Control

R/W	Addr	D7	D6	D5	D4	D3	D2	D1	D0	HEX
R/W	5A20h	ovss_def[7:0]								00h

Description	This command is used for setting OVSS default pulse number Bit: ovss_def[7:0]; Description: The default value of negative pulse; Data: 0~255
Restriction	

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(5B20h) P_PWR_ST

R/W	Addr	D7	D6	D5	D4	D3	D2	D1	D0	HEX
R/W	5B20h	P_PWR_ST0[7:0]								00h

Description	Normal mode swire pulse number of positive voltages
Restriction	This command is activated when pwr_ic_sel=1

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(7C20h~7D20h) MIPI Timing Option Control

R/W	Addr	D7	D6	D5	D4	D3	D2	D1	D0	HEX
R/W	7C20h	lptx_freq_sel[1:0]		lptx_TAGETD_sel[1:0]		lptx_TAGOD_sel[1:0]		-	-	00h
R/W	7D20h	-	-	tato_en	lptxo_en	hsrxto_en	-	vcid[1:0]		38h

Description

This command is used to setup MIPI options for customer's application.

lptx_freq_sel[1:0]	LP-TX Frequency
00h	7 MHz
01h	3.5 MHz
02h	1.75 MHz
03h	0.875 MHz

This command is used to setup MIPI BTA timing for customer's application.

lptx_TAGETD_sel[1:0]	Periods
00h	5*T_{LPX}
01h	4*T_{LPX}
02h	6*T_{LPX}
03h	7*T_{LPX}

This command is used to setup MIPI BTA timing for customer's application.

lptx_TAGOD_sel[1:0]	Periods
00h	2.5*T_{LPX}
01h	1.5*T_{LPX}
02h	3.5*T_{LPX}
03h	4.5*T_{LPX}

This command is used to setup MIPI options for customer's application.

Bit	Description
tato_en	Enable TA timer
lptxo_en	Enable LPDT Timer
hsrxto_en	Enable HSRX Timer

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<table>
<tr><td></td><td>This command is used to setup virtual channel for customer’s application.
<table>
<tr><th>vcid[1:0]</th><th>Description</th></tr>
<tr><td>00h</td><td>Virtual Channel = 00h</td></tr>
<tr><td>01h</td><td>Virtual Channel = 01h</td></tr>
<tr><td>02h</td><td>Virtual Channel = 02h</td></tr>
<tr><td>03h</td><td>Virtual Channel = 03h</td></tr>
</table></td></tr>
<tr><td>Restriction</td><td>Please don’t trim or change vcid[1:0] if only one display driver is used.</td></tr>
</table>

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(7E20h) MIPI LANE Configuration Control

R/W	Addr	D7	D6	D5	D4	D3	D2	D1	D0	HEX
R/W	7E20h	dswap_sw	dswap	pswap_sw	pswap	-	-	-	lansel	00h

Description

This command is used to dswap input selection

dswap_sw	Description
0	from pad: DSWAP
1	from bit6: dswap

This command is used to pswap input selection

pswap_sw	Description
0	from pad: PSWAP
1	from bit4: pswap

Dswap/pswap combinations are to select HSSI_D0/D1 data lane sequence and polarity in high speed interface only

Register	HSSI_D0_P	HSSI_D0_N	HSSI_CLK_P	HSSI_CLK_N	HSSI_D1_P	HSSI_D1_N
dswao=0 pswap=0	DSI D0+	DSI D0-	DSI CLK+	DSI CLK-	DSI D1+	DSI D1-
dswap=0 pswap=1	DSI D0-	DSI D0+	DSI CLK-	DSI CLK+	DSI D1-	DSI D1+
dswap=1 pswap=0	DSI D1+	DSI D1-	DSI CLK+	DSI CLK-	DSI D0+	DSI D0-
dswap=1 pswap=1	DSI D1-	DSI D1+	DSI CLK-	DSI CLK+	DSI D0-	DSI D0+

This command is used to set MIPI lane number

lansel	Description
0	1 lane
1	2 lane

Restriction

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(FE20h): CMD Mode Switch

R/W	Addr	D7	D6	D5	D4	D3	D2	D1	D0	HEX
W	FE20h	CMD_Page[7:0]								00h

Description

This command is used to switch the Manufacture Command Pages and User Commands sets.

CMD_Page[7:0]	Description
00h (default)	User Command Set (UCS = CMD1)
10h	Manufacture Command Set Page Panel ID
12h	Manufacture Command Set Page SID
20h	Manufacture Command Set Page Panel
40h	Manufacture Command Set Page ABH Mode
82h	Manufacture Command Set Page Power
92h	Manufacture Command Set Page SD timing
50h	Manufacture Command Set Page Gamma1
60h	Manufacture Command Set Page Gamma2
30h	Manufacture Command Set Page Gamma3
52h	Manufacture Command Set Page Gamma4
70h	Manufacture Command Set Page GOA Timing 1
F0h	Manufacture Command Set Page GOA Timing 2
42h	Manufacture Command Set Page DBV
22h	Manufacture Command Set Page SES
80h	Manufacture Command Set Page APRC
90h	Manufacture Command Set Page ACL
62h	Manufacture Command Set Page CGM
C2h	Manufacture Command Set Page CGM LUT

Restriction

-

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(FF20h): Read CMD Status

R/W	Addr	D7	D6	D5	D4	D3	D2	D1	D0	HEX
R	FF20h	CMD_Status[7:0]								00h

Description	This command is used to read the status of Manufacture Command Pages. Please refer to FE00h
Restriction	-

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1.6 MCS: CMD2 Page40, ABH Mode

Instruction	R/W	Addr	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Frame Rate Control Normal Mode	R/W	0040h	T1A[7:0]								20h
	R/W	0140h	D_CM_A[1:0]		PSELA[1:0]		-	-	T1A[9:8]		03h
	R/W	0240h	VBPDA[7:0]								12h
	R/W	0340h	-	-	-	-	-	-	VFPDA[9:8]		00h
	R/W	0440h	VFPDA[7:0]								12h
	R/W	0540h	F_SKIP_A[7:0]								01h
	R/W	0640h	-	F_SKIP_EN_A	-	-	-	-	F_SKIP_A[9:8]		00h
Set Display Time	R/W	0840h	T1A1[7:0]								20h
	R/W	0940h	T1A2[7:0]								20h
	R/W	0A40h	-	-	T1A2[9:8]		-	-	T1A1[9:8]		33h
	R/W	0B40h	T1A3[7:0]								20h
	R/W	0D40h	-	-	-		-	-	T1A3[9:8]		33h
Display Front Porch Setting	R/W	0E40h	VFPDA1[7:0]								12h
	R/W	0F40h	VFPDA2[7:0]								12h
	R/W	1040h	-	-	VFPDA2[9:8]		-	-	VFPDA1[9:8]		00h
	R/W	1140h	VFPDA3[7:0]								12h
	R/W	1340h	-	-	-		-	-	VFPDA3[9:8]		00h
Skip Frame Level Setting	R/W	1440h	F_SKIP_A1[7:0]								01h
	R/W	1540h	F_SKIP_A2[7:0]								01h
	R/W	1640h	-	-	F_SKIP_A2[9:8]		-	-	F_SKIP_A1[9:8]		00h
	R/W	1740h	F_SKIP_A3[7:0]								01h
Gamma Selection in Normal Mode	R/W	1E40h	2BAND_GMA_EN_A	2BAND_GMA_SEL_A[2:0]			-	GMA_SEL_A[2:0]			00h
	R/W	1F40h	2BAND_GMA_EN_A1	2BAND_GMA_SEL_A1[2:0]			-	GMA_SEL_A1[2:0]			00h
	R/W	2040h	2BAND_GMA_EN_A2	2BAND_GMA_SEL_A2[2:0]			-	GMA_SEL_A2[2:0]			00h
	R/W	2140h	2BAND_GMA_EN_A3	2BAND_GMA_SEL_A3[2:0]			-	GMA_SEL_A3[2:0]			00h
GOA timing parameter selection	R/W	2840h	VSR_A_A3_SEL[1:0]		VSR_A_A2_SEL[1:0]		VSR_A_A1_SEL[1:0]		VSR_A_A_SEL[1:0]		00h
	R/W	2940h	-	-	-	-	VSR_S_A_SEL[1:0]		-		00h
Switch timing parameter selection	R/W	2A40h	SW_A_A3_SEL[1:0]		SW_A_A2_SEL[1:0]		SW_A_A1_SEL[1:0]		SW_A_A_SEL[1:0]		00h
DFRS	R/W	3640h	DFR_PAR1								01h
	R/W	3740h	DFR_PAR2								00h
Frame Rate Control IDLE mode	R/W	3F40h	T1B[7:0]								20h
	R/W	4040h	D_CM_B[1:0]		PSELB[1:0]		-	-	T1B[9:8]		03h
	R/W	4140h	VBPDB[7:0]								12h
	R/W	4240h	-	-	-	-	-	-	VFPDB[9:8]		00h

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	R/W	4340h	VFPDB[7:0]							12h
	R/W	4440h	F_SKIP_B[7:0]							01h
	R/W	4540h	-	F_SKIP_EN_B	-	-	-	-	F_SKIP_B[9:8]	00h
Set Display Time of One Scan Line in IDLE mode	R/W	4740h	T1B1[7:0]							20h
	R/W	4840h	T1B2[7:0]							20h
	R/W	4940h	-	-	T1B2[9:8]		-	-	T1B1[9:8]	33h
Display Front Porch Setting in IDLE mode	R/W	4A40h	VFPDB1[7:0]							12h
	R/W	4B40h	VFPDB2[7:0]							12h
	R/W	4C40h	-	-	VFPDB2[9:8]		-	-	VFPDB1[9:8]	00h
Skip Frame Level Setting for IDLE mode	R/W	4D40h	F_SKIP_B1[7:0]							01h
	R/W	4E40h	F_SKIP_B2[7:0]							01h
	R/W	4F40h	-	-	F_SKIP_B2[9:8]		-	-	F_SKIP_B1[9:8]	00h
Gamma Selection	R/W	5340h	-	-	-	-	-	GMA_SEL_B[2:0]		00h
	R/W	5440h	-	-	-	-	-	GMA_SEL_B1[2:0]		00h
	R/W	5540h	-	-	-	-	-	GMA_SEL_B2[2:0]		00h
GOA	R/W	5940h	VSR_S_B_SEL[1:0]		VSR_A_B2_SEL[1:0]		VSR_A_B1_SEL[1:0]		VSR_A_B_SEL[1:0]	00h
Source	R/W	5A40h	-	-	SW_A_B2_SEL[1:0]		SW_A_B1_SEL[1:0]		SW_A_B_SEL[1:0]	00h
Display Color	R/W	6040h	-	-	-	-	D_CM_B2[1:0]		D_CM_B1[1:0]	00h
DFRS	R/W	6140h	DFR_PAR3							01h
Frame Rate Control HBM Mode	R/W	6640h	T1H[7:0]							20h
	R/W	6740h	D_CM_HBM[1:0]		PSELH[1:0]		-	-	T1H[9:8]	03h
	R/W	6840h	VBPDH[7:0]							12h
	R/W	6940h	-	-	-	-	-	-	VFPDH[9:8]	00h
	R/W	6A40h	VFPDH[7:0]							12h
	R/W	6B40h	F_SKIP_HBM[7:0]							01h
	R/W	6C40h	-	F_SKIP_EN_H	-	-	-	-	F_SKIP_HBM[9:8]	00h
Gamma Selection in HDM mode	R/W	7540h	-	-	-	-	-	GMA_SEL_H[2:0]		00h
GOA	R/W	7940h	VSR_S_H_SEL[1:0]		-	-	-		VSR_A_H_SEL[1:0]	00h
Source timing parameter selection at HBM mode	R/W	7A40h	-	-	-	-	-		SW_A_H_SEL[1:0]	00h
DFRS	R/W	8140h	DFR_PAR5							00h
DFRS	R/W	8240h	DFR_PAR6							00h
DFRS	R/W	8A40h	DFR_PAR7							00h

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Page Check sum Enable	R/W	AC40h	-	PID_chksum_en	ABH_chksum_en	PANEL_chksum_en	gm1_chksum_en	gm2_chksum_en	gm3_chksum_en	gm4_chksum_en	00h
	R/W	AD40h	VSR_chksum_en	VSRB_chksum_en	APRC_chksum_en	ACL_chksum_en	SES_chksum_en	-	DBV_chksum_en	CGM_chksum_en	00h
	R/W	AE40h	-	CGM_gm_chksum_en	SID_chksum_en	-	-	SD_timing_chksum_en	power_chksum_en	-	00h
MTP Comparsion	R	B240h	PID_chksum_cmp	ABH_chksum_cmp	PANEL_chksum_cmp	gm1_chksum_cmp	gm2_chksum_cmp	gm3_chksum_cmp	gm4_chksum_cmp	VSR_chksum_cmp	00h
	R	B340h	VSRB_chksum_cmp	APRC_chksum_cmp	-	ACL_chksum_cmp	SES_chksum_cmp	DBV_chksum_cmp	CGM_chksum_cmp	OTP_cmp_check_sum	00h
	R	B440h	-	CGM_gm_chksum_cmp	SID_chksum_cmp	-	-	SD_timing_chksum_cmp	power_chksum_cmp	-	00h
MTP Flag Check	R	B840h	PID_1st_Done	PID_2nd_Done	PID_3rd_Done	-	ABH_1st_Done	ABH_2nd_Done	ABH_3rd_Done	-	00h
	R	B940h	PANEL_1st_Done	PANEL_2nd_Done	-	-	gm1_1st_Done	gm1_2nd_Done	gm1_3rd_Done	-	00h
	R	BA40h	gm2_1st_Done	gm2_2nd_Done	gm2_3rd_Done	-	gm3_1st_Done	gm3_2nd_Done	gm3_3rd_Done	-	00h
	R	BB40h	gm4_1st_Done	gm4_2nd_Done	gm4_3rd_Done	-	-	-	-	-	00h
MTP Flag Check	R	BC40h	VSR_1st_Done	VSR_2nd_Done	-	-	VSRB_1st_Done	VSRB_2nd_Done	-	-	00h
	R	BE40h	ACL_1st_Done	ACL_2nd_Done	-	-	-	-	-	-	00h
	R	BF40h	DBV_1st_Done	DBV_2nd_Done	-	-	CGM_1st_Done	CGM_2nd_Done	-	-	00h
	R	C040h	SD_timing_1st_Done	SD_timing_2nd_Done	-	-	power_1st_Done	power_2nd_Done	-	-	00h
	R	C140h	SES_1st_Done	SES_2nd_Done	-	-	APRC_1st_Done	APRC_2nd_Done	-	-	00h
	R	C240h	CGM_gm_1st_Done	CGM_gm_2nd_Done	-	-	SID_1st_Done	SID_2nd_Done	SID_3rd_Done	-	00h
Version Code	R	DE40h	ID41[7:0]								69h
	R	DF40h	ID42[7:0]								0Bh
	R	E040h	IC_VERSION_Customer[7:0]								00h
OTP PROGRM EN	R/W	EE40h	-	-	DBV_PGM_EN	CGM_PGM_EN	-	power_PGM_EN	SD_timing_PGM_EN	CGM_gm_PGM_EN	00h
OTP PROGRM EN	R/W	EF40h	-	ACL_PGM_EN	VSRB_PGM_EN	gm3_PGM_EN	PANEL_PGM_EN	PID_PGM_EN	-	-	00h

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OTP PROGRM EN	R/W	F040h	SID_PGM_EN	gm4_PGM_EN	ABH_PGM_EN	gm1_PGM_EN	gm2_PGM_EN	VSR_PGM_EN	APRC_PGM_EN	SES_PGM_EN	00h
WMTP	R/W	F240h	-	-	-	-	-	-	1	MTP_W	02h
MTPW	R/W	F340h	0	0	0	0	0	0	0	0	00h
MTPW	R/W	F440h	0	0	0	0	0	0	0	0	00h
MTPW	R/W	F540h	0	0	0	0	0	0	0	0	00h
CMD Mode Switch		FE40h	CMD_Page[7:0]								00h
RD CMD Status	R	FF40h	CMD_Status[7:0]								00h

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(0040h ~ 0640h) Normal Mode Frame Rate Control

R/W	Addr	D7	D6	D5	D4	D3	D2	D1	D0	HEX
R/W	0040h	T1A[7:0]								20h
R/W	0140h	D_CM_A[1:0]		PSELA[1:0]		-	-	-	-	03h
R/W	0240h	VBPDA[7:0]								12h
R/W	0340h	-	-	-	-	-	-	VFPDA[9:8]		00h
R/W	0440h	VFPDA[7:0]								12h
R/W	0540h	F_SKIP_A[7:0]								01h
R/W	0640h	-	F_SKIP_EN_A	-	-	-	-	F_SKIP_A[9:8]		00h

Description

This command is used to set display time of one scan line in normal mode.

T1A[9:0]	Number of clock
0h~FFh	0~255
…	…
3FEh	1022
3FFh	1023

D_CM_A: This command is used to set display color mode in normal mode.

D_CM_A[1:0]	Display color bit
00	24 bit
01	12 bit
10	3 bit (8 color)
11	reserved

PSELA: This command is used to select pixel clock frequency in normal mode.

PSELA[1:0]	Divisor	Pixel Clock Frequency
00	1	24MHz
01	2	12MHz
10	4	6MHz
11	8	3MHz

Notes: PSELA will affect some register setting in pixel clock unit.
(ex: T1A, GOA, MUX and Switch EQ timing setting)

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VBPDA: This command is used to set vertical back porch lines in normal mode.

VBPDA[7:0]	Number of line
0h~7h	reserved
8h	8
9h	9
…	…
12h	18
…	…
FEh	254
FFh	255

VBPDA: This command is used to set vertical front porch lines in normal mode.

VFPDA[9:0]	Number of line
0h~7h	reserved
8h	8
9h	9
…	…
12h	18
…	…
3FEh	1022
3FFh	1023

These commands are used to set skip frame mode in normal mode.

Parameter	Number of line
F_SKIP_EN_A	0: Disable skip frame function in normal mode 1: Enable skip frame function in normal mode
F_SKIP_A	The number of the skip frame

Restriction	

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(0840h ~ 0D40h) Normal Mode Scan Line Time

R/W	Addr	D7	D6	D5	D4	D3	D2	D1	D0	HEX
R/W	0840h	T1A1[7:0]								20h
R/W	0940h	T1A2[7:0]								20h
R/W	0A40h	-	-	T1A2[9:8]		-	-	T1A1[9:8]		33h
R/W	0B40h	T1A3[7:0]								20h
R/W	0D40h	-	-	1	1	-	-	T1A3[9:8]		33h

Description	T1A1: This command is used to set display time of one scan line in normal mode level 1. T1A2: This command is used to set display time of one scan line in normal mode level 2. T1A3: This command is used to set display time of one scan line in normal mode level 3
Restriction	

(0E40h ~ 1340h) Normal Mode VFP

R/W	Addr	D7	D6	D5	D4	D3	D2	D1	D0	HEX
R/W	0E40h	VFPDA1[7:0]								12h
R/W	0F40h	VFPDA2[7:0]								12h
R/W	1040h	-	-	VFPDA2[9:8]		-	-	VFPDA1[9:8]		00h
R/W	1140h	VFPDA3[7:0]								12h
R/W	1340h	-	-	-	-	-	-	VFPDA3[9:8]		00h

Description	VFPDA1: This command is used to set display front porch line in normal mode level 1. VFPDA2: This command is used to set display front porch line in normal mode level 2. VFPDA3: This command is used to set display front porch line in normal mode level 3.
Restriction	

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(1440h ~ 1740h) Normal Mode Skip Frame

R/W	Addr	D7	D6	D5	D4	D3	D2	D1	D0	HEX
R/W	1440h	F_SKIP_A1[7:0]								01h
R/W	1540h	F_SKIP_A2[7:0]								01h
R/W	1640h	-	-	F_SKIP_A2[9:8]		-	-	F_SKIP_A1[9:8]		00h
R/W	1740h	F_SKIP_A3[7:0]								01h

Description

These commands are used to set skip frame mode in normal mode.

Parameter	Number of line
F_SKIP_A1	The number of the skip frame for normal mode level1
F_SKIP_A2	The number of the skip frame for normal mode level2
F_SKIP_A3	The number of the skip frame for normal mode level3

Restriction

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(1E40h ~ 2240h) Normal Mode Gamma Selection

R/W	Addr	D7	D6	D5	D4	D3	D2	D1	D0	HEX
R/W	1E40h	2Band_GMA_EN_A	2Band _GMA_SEL_A[2:0]			-	GMA_SEL_A[2:0]			00h
R/W	1F40h	2Band_GMA_EN_A1	2Band _GMA_SEL_A12:0]			-	GMA_SEL_A1[2:0]			00h
R/W	2040h	2Band_GMA_EN_A2	2Band _GMA_SEL_A2[2:0]			-	GMA_SEL_A2[2:0]			00h
R/W	2140h	2Band_GMA_EN_A3	2Band _GMA_SEL_A3[2:0]			-	GMA_SEL_A3[2:0]			00h

Description

This command is used to select normal mode Gamma in various level:

Bit	Description	Value
GMA_SEL_A[2:0]	Gamma selection for normal mode	0: Gamma1(Page50) 1: Gamma2(Page60), 2: Gamma3(Page30), 3: Gamma4(Page52) Other: Reserved
GMA_SEL_A1[2:0]	Gamma selection for normal mode level1	
GMA_SEL_A2[2:0]	Gamma selection for normal mode level2	
GMA_SEL_A3[2:0]	Gamma selection for normal mode level3	

This command is used to select normal mode 2nd band Gamma(low-brightness region) in various level:

Bit	Description	Value
2Band _GMA_SEL_A[2:0]	2band Gamma selection for normal mode	0: Gamma1(Page50) 1: Gamma2(Page60), 2: Gamma3(Page30), 3: Gamma4(Page52) Other: Reserved
2Band _GMA_SEL_A1[2:0]	2band Gamma selection for normal mode level1	
2Band _GMA_SEL_A2[2:0]	2band Gamma selection for normal mode level2	
2Band _GMA_SEL_A3[2:0]	2band Gamma selection for normal mode level3	

This command is used to select normal mode 2nd band Gamma enable in various level:

Bit	Description
2Band_GMA_EN_A	2band Gamma enable for normal mode
2Band_GMA_EN_A1	2band Gamma enable for normal mode level1
2Band_GMA_EN_A2	2band Gamma enable for normal mode level2
2Band_GMA_EN_A3	2band Gamma enable for normal mode level3

Restriction

If 2Band_GMA_EN_A/A1/A2/A3 are enable, the 2Band_GMA_SEL_A/A1/A2/A3 shall set to the same value (the same Gamma set).

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(2840h~2940h) Normal Mode GOA Timing Selection

R/W	Addr	D7	D6	D5	D4	D3	D2	D1	D0	HEX
R/W	2840h	VSR_A_A3_SEL[1:0]		VSR_A_A2_SEL[1:0]		VSR_A_A1_SEL[1:0]		VSR_A_A_SEL[1:0]		00h
R/W	2940h	-	-	-	-	VSR_S_A_SEL[1:0]		-	-	00h

Description

These commands are used to select GOA timing parameters:

Bit	Description	Value
VSR_A_A_SEL[1:0]	GOA timing selection for normal mode	0: GOA Timing1(Page70) 1: GOA Timing2(PageF0) Other: Reserved
VSR_A_A1_SEL[1:0]	GOA timing selection for normal mode level1	
VSR_A_A2_SEL[1:0]	GOA timing selection for normal mode level2	
VSR_A_A3_SEL[1:0]	GOA timing selection for normal mode level3	
VSR_S_A_SEL[1:0]	GOA timing selection for normal mode skip frame	

Restriction

(2A40h) Normal Mode Switch Timing Selection

R/W	Addr	D7	D6	D5	D4	D3	D2	D1	D0	HEX
R/W	2A40h	SW_A_A3_SEL[1:0]		SW_A_A2_SEL[1:0]		SW_A_A1_SEL[1:0]		SW_A_A_SEL[1:0]		00h

Description

These commands are used to set switch timing parameters:

Bit	Description	Value
SW_A_A_SEL[1:0]	switch timing selection for normal mode	0: Switch Timing1 (0892h~0D92h) 1: Switch Timing2 (0E92h~1392h) Other: Reserved
SW_A_A1_SEL[1:0]	switch timing selection for normal mode level1	
SW_A_A2_SEL[1:0]	switch timing selection for normal mode level2	
SW_A_A3_SEL[1:0]	switch timing selection for normal mode level3	

Restriction

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(3F40h ~ 4540h) IDLE mode Frame Rate Control

R/W	Addr	D7	D6	D5	D4	D3	D2	D1	D0	HEX
R/W	3F40h	T1B[7:0]								20h
R/W	4040h	D_CM_B[1:0]		PSELB[1:0]		-	-	T1B[9:8]		03h
R/W	4140h	VBPDB[7:0]								12h
R/W	4240h	-	-	-	-	-	-	VFPDB[9:8]		00h
R/W	4340h	VFPDB[7:0]								12h
R/W	4440h	F_SKIP_B[7:0]								01h
R/W	4540h	-	F_SKIP_EN_B	-	-	-	-	F_SKIP_B[9:8]		00h

Description

This command is used to set display time of one scan line in IDLE mode.

T1B[9:0]	Number of clock
0h~FFh	0~255
…	…
3FEh	1022
3FFh	1023

D_CM_B: This command is used to set display color mode in IDLE mode.

D_CM_B[1:0]	Display color bit
00	24 bit
01	12 bit
10	3 bit (8 color)
11	reserved

PSELB: This command is used to select pixel clock frequency in normal mode.

PSELB[1:0]	Divisor	Pixel Clock Frequency
00	1	24MHz
01	2	12MHz
10	4	6MHz
11	8	3MHz

Notes: PSELB will affect some register setting in pixel clock unit.
(ex: T1B, GOA, MUX and Switch EQ timing setting)

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VBPDB: This command is used to set vertical back porch lines in IDLE mode.

VBPDB[7:0]	Number of line
0h~7h	reserved
8h	8
9h	9
…	…
12h	18
…	…
FEh	254
FFh	255

VFPDB: This command is used to set vertical front porch lines in IDLE mode.

VFPDB[9:0]	Number of line
0h~7h	reserved
8h	8
9h	9
…	…
12h	18
…	…
3FEh	1022
3FFh	1023

These commands are used to set skip frame mode in IDLE mode.

Parameter	Number of line
F_SKIP_EN_B	0: Disable skip frame function in IDLE mode 1: Enable skip frame function in IDLE mode
F_SKIP_B	The number of the skip frame

Restriction	

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(4740h ~ 4940h) IDLE Mode Scan Line Time

R/W	Addr	D7	D6	D5	D4	D3	D2	D1	D0	HEX
R/W	4740h	T1B1[7:0]								20h
R/W	4840h	T1B2[7:0]								20h
R/W	4940h	-	-	T1B2[9:8]		-	-	T1B1[9:8]		33h

Description	T1B1: This command is used to set display time of one scan line in IDLE mode level 1. T1B2: This command is used to set display time of one scan line in IDLE mode level 2.
Restriction	

(4A40h ~ 4C40h) IDLE Mode VFP

R/W	Addr	D7	D6	D5	D4	D3	D2	D1	D0	HEX
R/W	4A40h	VFPDB1[7:0]								12h
R/W	4B40h	VFPDB2[7:0]								12h
R/W	4C40h	-	-	VFPDB2[9:8]		-	-	VFPDB1[9:8]		00h

Description	VFPDB1: This command is used to set display front porch line in IDLE mode level 1. VFPDB2: This command is used to set display front porch line in IDLE mode level 2.
Restriction	

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(4D40h ~ 4F40h) IDLE Mode Skip Frame

R/W	Addr	D7	D6	D5	D4	D3	D2	D1	D0	HEX
R/W	4D40h	F_SKIP_B1[7:0]								01h
R/W	4E40h	F_SKIP_B2[7:0]								01h
R/W	4F40h	-	-	F_SKIP_B2[9:8]		-	-	F_SKIP_B1[9:8]		00h

Description	These commands are used to set skip frame mode in normal mode. Parameter: Number of line F_SKIP_B1: The number of the skip frame for IDLE mode level1 F_SKIP_B2: The number of the skip frame for IDLE mode level2
Restriction	

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(5340h ~ 5540h) IDLE Mode Gamma Selection

R/W	Addr	D7	D6	D5	D4	D3	D2	D1	D0	HEX
R/W	5340h	-	-	-	-	-	GMA_SEL_B[2:0]			00h
R/W	5440h	-	-	-	-	-	GMA_SEL_B1[2:0]			00h
R/W	5540h	-	-	-	-	-	GMA_SEL_B2[2:0]			00h

Description

This command is used to select Gamma in various level:

Bit	Description	Value
GMA_SEL_B[2:0]	Gamma selection for IDLE mode	0: Gamma1(Page50) 1: Gamma2(Page60), 2: Gamma3(Page30), 3: Gamma4(Page52) Other: Reserved
GMA_SEL_B1[2:0]	Gamma selection for IDLE mode level1	
GMA_SEL_B2[2:0]	Gamma selection for IDLE mode level2	

Restriction

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(5940h) IDLE Mode GOA Timing Selection

R/W	Addr	D7	D6	D5	D4	D3	D2	D1	D0	HEX
R/W	5940h	VSR_S_B_SEL[1:0]		VSR_A_B2_SEL[1:0]		VSR_A_B1_SEL[1:0]		VSR_A_B_SEL[1:0]		00h

Description

These commands are used to select GOA timing parameters:

Bit	Description	Value
VSR_A_B_SEL[1:0]	GOA timing selection for IDLE mode	0: GOA Timing1(Page70) 1: GOA Timing2(PageF0) Other: Reserved
VSR_A_B1_SEL[1:0]	GOA timing selection for IDLE mode level1	
VSR_A_B2_SEL[1:0]	GOA timing selection for IDLE mode level2	
VSR_S_B_SEL[1:0]	GOA timing selection for IDLE mode skip frame	

Restriction

(5A40h) IDLE Mode Switch Timing Selection

R/W	Addr	D7	D6	D5	D4	D3	D2	D1	D0	HEX
R/W	5A40h	-	-	SW_A_B2_SEL[1:0]		SW_A_B1_SEL[1:0]		SW_A_B_SEL[1:0]		00h

Description

These commands are used to set switch timing parameters:

Bit	Description	Value
SW_A_B_SEL[1:0]	switch timing selection for IDLE mode	0: Switch Timing1 (0892h~0D92h) 1: Switch Timing2 (0E92h~1392h) Other: Reserved
SW_A_B1_SEL[1:0]	switch timing selection for IDLE mode level1	
SW_A_B2_SEL[1:0]	switch timing selection for IDLE mode level2	

Restriction

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(6040h) IDLE Mode Display Color Mode

R/W	Addr	D7	D6	D5	D4	D3	D2	D1	D0	HEX
R/W	6040h	-	-	-	-	D_CM_B2[1:0]		D_CM_B1[1:0]		00h

Description	D_CM_B1: This command is used to set display color mode in IDLE mode level 1 D_CM_B2: This command is used to set display color mode in IDLE mode level 2
Restriction	

D_CM_B[1:0]	Display color bit
00	24 bit
01	12 bit
10	3 bit (8 color)
11	reserved

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(6640h ~ 6C40h) HBM Mode Frame Rate Control

R/W	Addr	D7	D6	D5	D4	D3	D2	D1	D0	HEX
R/W	6640h	T1H[7:0]								20h
R/W	6740h	D_CM_HBM[1:0]		PSELH[1:0]		-	-	T1H[9:8]		03h
R/W	6840h	VBPDH[7:0]								12h
R/W	6940h	-	-	-	-	-	-	VFPDH[9:8]		00h
R/W	6A40h	VFPDH[7:0]								12h
R/W	6B40h	F_SKIP_H[7:0]								01h
R/W	6C40h	-	F_SKIP_EN_H	-	-	-	-	F_SKIP_H[9:8]		00h

Description

This command is used to set display time of one scan line in HBM mode.

T1H[9:0]	Number of clock
0h~FFh	0~255
…	…
3FEh	1022
3FFh	1023

D_CM_HBM: This command is used to set display color mode in HBM mode.

D_CM_HBM[1:0]	Display color bit
00	24 bit
01	12 bit
10	3 bit (8 color)
11	reserved

PSELH: This command is used to select pixel clock frequency in normal mode.

PSELH[1:0]	Divisor	Pixel Clock Frequency
00	1	24MHz
01	2	12MHz
10	4	6MHz
11	8	3MHz

Notes: PSELH will affect some register setting in pixel clock unit.
(ex: T1H, GOA, MUX and Switch EQ timing setting)

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VBPDH: This command is used to set vertical back porch lines in HBM mode.

VBPDH[7:0]	Number of line
0h~7h	reserved
8h	8
9h	9
…	…
12h	18
…	…
FEh	254
FFh	255

VFPDH: This command is used to set vertical front porch lines in HBM mode.

VFPDH[9:0]	Number of line
0h~7h	reserved
8h	8
9h	9
…	…
12h	18
…	…
3FEh	1022
3FFh	1023

These commands are used to set skip frame mode in HBM mode.

Parameter	Number of line
F_SKIP_EN_H	0: Disable skip frame function in HBM mode 1: Enable skip frame function in HBM mode
F_SKIP_H	The number of the skip frame

Restriction

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(7540h) HBM Mode Gamma Selection

R/W	Addr	D7	D6	D5	D4	D3	D2	D1	D0	HEX
R/W	7540h	-	-	-	-	-	GMA_SEL_H[2:0]			00h

Description	This command is used to select HBM mode Gamma: Bit: GMA_SEL_H[2:0] Description: Gamma selection for HBM mode Value: 0: Gamma1(Page50) 1: Gamma2(Page60), 2: Gamma3(Page30), 3: Gamma4(Page52) Other: Reserved
Restriction	

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(7940h) HBM Mode GOA Timing Selection

R/W	Addr	D7	D6	D5	D4	D3	D2	D1	D0	HEX
R/W	7940h	VSR_S_H_SEL[1:0]		-		-		VSR_A_H_SEL[1:0]		00h

Description	These commands are used to select GOA timing parameters: Bit: VSR_A_H_SEL[1:0] — Description: GOA timing selection for HBM mode Bit: VSR_S_H_SEL[1:0] — Description: GOA timing selection for HBM mode skip frame Value: 0: GOA Timing1(Page70) 1: GOA Timing2(PageF0) Other: Reserved
Restriction	

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(7A40h) HBM Mode Switch Timing Selection

R/W	Addr	D7	D6	D5	D4	D3	D2	D1	D0	HEX
R/W	7A40h	-	-	-	-	-	-	SW_A_H_SEL[1:0]		00h

Description	These commands are used to set switch timing parameters: Bit: SW_A_H_SEL[1:0] Description: switch timing selection for HBM mode Value: 0: Switch Timing1 (0892h~0D92h) 1: Switch Timing2 (0E92h~1392h) Other: Reserved
Restriction	

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(3640h~3740h, 6140h, 8140h~8240h, 8A40h) Dynamic Frame Rate Parameter

R/W	Address	D7	D6	D5	D4	D3	D2	D1	D0	HEX
R/W	3640h	DFR_PAR1								00h
R/W	3740h	DFR_PAR2								00h
R/W	6140h	DFR_PAR3								00h
R/W	8140h	DFR_PAR5								00h
R/W	8240h	DFR_PAR6								00h
R/W	8A40h	DFR_PAR7								00h

Description	These commands are used to set dynamic frame rate switching function parameters. Please provide the requirement and contact with Raydium for detailed information
Restriction	

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(AC40h~AE40h) Page Checksum Enable

R/W	Addr	D7	D6	D5	D4	D3	D2	D1	D0	HEX
R/W	AC40h	-	PID_chksum_en	ABH_chksum_en	PANEL_chksum_en	gm1_chksum_en	gm2_chksum_en	gm3_chksum_en	gm4_chksum_en	00h
R/W	AD40h	VSR_chksum_en	VSRB_chksum_en	APRC_chksum_en	ACL_chksum_en	SES_chksum_en	-	DBV_chksum_en	CGM_chksum_en	00h
R/W	AE40h	-	CGM_gm_chksum_en	SID_chksum_en	-	-	SD_timing_chksum_en	power_chksum_en	-	00h

Description

These commands are used to enable FCS/CCS calculation for individual page.

Bit	Description
PID_chksum_en	The value of FCS(0xAA00) and CCS(0xAF00) calculated by Page Panel ID only
ABH_chksum_en	The value of FCS(0xAA00) and CCS(0xAF00) calculated by Page ABH Mode only
PANEL_chksum_en	The value of FCS(0xAA00) and CCS(0xAF00) calculated by Page Panel only
Gm1_chksum_en	The value of FCS(0xAA00) and CCS(0xAF00) calculated by Page Gamma1 only
Gm2_chksum_en	The value of FCS(0xAA00) and CCS(0xAF00) calculated by Page Gamma2 only
Gm3_chksum_en	The value of FCS(0xAA00) and CCS(0xAF00) calculated by Page Gamma3 only
Gm4_chksum_en	The value of FCS(0xAA00) and CCS(0xAF00) calculated by Page Gamma4 only
VSR_chksum_en	The value of FCS(0xAA00) and CCS(0xAF00) calculated by Page GOA Timing1 only
VSRB_chksum_en	The value of FCS(0xAA00) and CCS(0xAF00) calculated by Page GOA Timing2 only
APRC_chksum_en	The value of FCS(0xAA00) and CCS(0xAF00) calculated by Page APRC only
ACL_chksum_en	The value of FCS(0xAA00) and CCS(0xAF00) calculated by Page ACL only
SES_chksum_en	The value of FCS(0xAA00) and CCS(0xAF00) calculated by Page SES only
DBV_chksum_en	The value of FCS(0xAA00) and CCS(0xAF00) calculated by Page DBV only
CGM_chksum_en	The value of FCS(0xAA00) and CCS(0xAF00) calculated by Page CGM only
CGM_gm_chksum_en	The value of FCS(0xAA00) and CCS(0xAF00) calculated by Page CGM LUT only
SID_chksum_en	The value of FCS(0xAA00) and CCS(0xAF00) calculated by Page SID
SD_timing_chksum_en	The value of FCS(0xAA00) and CCS(0xAF00) calculated by Page SD timing
power_chksum_en	The value of FCS(0xAA00) and CCS(0xAF00) calculated by Page Power

Restriction

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(B240h~B440h) MTP Comparsion

R/W	Addr	D7	D6	D5	D4	D3	D2	D1	D0	HEX
R	B240h	PID_chksum_cmp	ABH_chksum_cmp	PANEL_chksum_cmp	gm1_chksum_cmp	gm2_chksum_cmp	gm3_chksum_cmp	gm4_chksum_cmp	VSR_chksum_cmp	00h
R	B340h	VSRB_chksum_cmp	APRC_chksum_cmp	-	ACL_chksum_cmp	SES_chksum_cmp	DBV_chksum_cmp	CGM_chksum_cmp	OTP_cmp_check_sum	00h
R	B440h	-	CGM_gm_chksum_cmp	SID_chksum_cmp	-	-	SD_timing_chksum_cmp	power_chksum_cmp	-	00h

Description	This command are used to check MTP compared result while loading PID_chksum_cmp: MTP load compared status of Page Panel ID. ABH_chksum_cmp: MTP load compared status of Page ABH Mode PANEL_chksum_cmp: MTP load compared status of Page Panel Gm1_chksum_cmp: MTP load compared status of Page Gamma1 Gm2_chksum_cmp: MTP load compared status of Page Gamma2 Gm3_chksum_cmp: MTP load compared status of Page Gamma3 Gm4_chksum_cmp: MTP load compared status of Page Gamma4 VSR_chksum_cmp: MTP load compared status of Page GOA Timing 1 VSRB_chksum_cmp: MTP load compared status of Page GOA Timing 2 APRC_chksum_cmp: MTP load compared status of Page APRC ACL_chksum_cmp: MTP load compared status of Page ACL SES_chksum_cmp: MTP load compared status of Page SES DBV_chksum_cmp: MTP load compared status of Page DBV CGM_chksum_cmp: MTP load compared status of Page CGM CGM_gm_chksum_cmp: MTP load compared status of Page CGM LUT SID_chksum_cmp: MTP load compared status of Page SID SD_timing_ chksum_cmp: MTP load compared status of Page SD Timing power_ chksum_cmp: MTP load compared status of Page Power OTP_cmp_check_sum: Compared status of all above status check
Restriction	

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(B840h~C240h) MTP Flag Check

R/W	Addr	D7	D6	D5	D4	D3	D2	D1	D0	HEX
R	B840h	PID_1st_Done	PID_2nd_Done	PID_3rd_Done	-	ABH_1st_Done	ABH_2nd_Done	ABH_3rd_Done	-	00h
R	B940h	PANEL_1st_Done	PANEL_2nd_Done	-	-	gm1_1st_Done	gm1_2nd_Done	gm1_3rd_Done	-	00h
R	BA40h	gm2_1st_Done	gm2_2nd_Done	gm2_3rd_Done	-	gm3_1st_Done	gm3_2nd_Done	gm3_3rd_Done	-	00h
R	BB40h	gm4_1st_Done	gm4_2nd_Done	gm4_3rd_Done	-	-	-	-	-	00h
R	BC40h	VSR_1st_Done	VSR_2nd_Done	-	-	VSRB_1st_Done	VSRB_2nd_Done	-	-	00h
R	BD40h	-	-	-	-	-	-	-	-	00h
R	BE40h	ACL_1st_Done	ACL_2nd_Done	-	-	-	-	-	-	00h
R	BF40h	DBV_1st_Done	DBV_2nd_Done	-	-	CGM_1st_Done	CGM_2nd_Done	-	-	00h
R	C040h	SD_timing_1st_Done	SD_timing_2nd_Done	-	-	power_1st_Done	power_2nd_Done	-	-	00h
R	C140h	SES_1st_Done	SES_2nd_Done	-	-	APRC_1st_Done	APRC_2nd_Done	-	-	00h
R	C240h	CGM_gm_1st_Done	CGM_gm_2nd_Done	-	-	SID_1st_Done	SID_2nd_Done	SID_3rd_Done	-	00h

Description

These command are used to check MTP programming status of corresponding page

Bit	Description	Data
PID_1st_Done	Page Panel ID: 1st MTP status	0: Not programmed 1: Programmed
PID_2nd_Done	Page Panel ID: 2nd MTP status	
PID_3rd_Done	Page Panel ID: 3rd MTP status	
ABH_1st_Done	Page ABH Mode: 1st MTP status	
ABH_2nd_Done	Page ABH Mode: 2nd MTP status	
ABH_3rd_Done	Page ABH Mode: 3rd MTP status	
PANEL_1st_Done	Page Panel: 1st MTP status	
PANEL_2nd_Done	Page Panel: 2nd MTP status	
gm1_1st_Done	Page Gamma1: 1st MTP status	
gm1_2nd_Done	Page Gamma1: 2nd MTP status	
gm1_3rd_Done	Page Gamma1: 3rd MTP status	
gm2_1st_Done	Page Gamma2: 1st MTP status	
gm2_2nd_Done	Page Gamma2: 2nd MTP status	
gm2_3rd_Done	Page Gamma2: 3rd MTP status	
gm3_1st_Done	Page Gamma3: 1st MTP status	
gm3_2nd_Done	Page Gamma3: 2nd MTP status	
gm3_3rd_Done	Page Gamma3: 3rd MTP status	
gm4_1st_Done	Page Gamma4: 1st MTP status	

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	gm4_2nd_Done	Page Gamma4: 2nd MTP status	0: Not programmed 1: Programmed
	gm4_3rd_Done	Page Gamma4: 3rd MTP status	
	VSR_1st_Done	Page GOA Timing1: 1st MTP status	
	VSR_2nd_Done	Page GOA Timing1: 2nd MTP status	
	VSRB_1st_Done	Page GOA Timing2: 1st MTP status	
	VSRB_2nd_Done	Page GOA Timing2: 2nd MTP status	
	ACL_1st_Done	Page ACL: 1st MTP status	
	ACL_2nd_Done	Page ACL: 2nd MTP status	
	DBV_1st_Done	Page DBV: 1st MTP status	
	DBV_2nd_Done	Page DBV: 2nd MTP status	
	CGM_1st_Done	Page CGM: 1st MTP status	
	CGM_2nd_Done	Page CGM: 2nd MTP status	
	SD_timing_1st_Done	Page SD Timing: 1st MTP status	
	SD_timing_2nd_Done	Page SD Timing: 2nd MTP status	
	power_1st_Done	Page Power Setting: 1st MTP status	
	power_2nd_Done	Page Power Setting: 2nd MTP status	
	SES_1st_Done	Page SES: 1st MTP status	
	SES_2nd_Done	Page SES: 2nd MTP status	
	APRC_1st_Done	Page APRC: 1st MTP status	
	APRC_2nd_Done	Page APRC: 2nd MTP status	
	CGM_gm_1st_Done	Page CGM LUT: 1st MTP status	
	CGM_gm_2nd_Done	Page CGM LUT: 2nd MTP status	
	SID_1st_Done	Page SID: 1st MTP status	
	SID_2nd_Done	Page SID: 2nd MTP status	
	SID_3rd_Done	Page SID: 3rd MTP status	
Restriction			

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(DE40h~E040) IC Chip Code/Version Code

R/W	Addr	D7	D6	D5	D4	D3	D2	D1	D0	HEX
R	DE40h	ID41[7:0]								69h
R	DF40h	ID42[7:0]								0Bh
R	E040h	IC_VERSION_Customer[7:0]								00h

Description	This command is for Chip ID Code: RM690B00 Bit / Description / Data ID41[7:0] / Chip ID Code / 0x69 ID42[7:0] / Chip ID Code / 0x0B IC_VERSION_Customer[7:0] / Chip Version / 0x00
Restriction	

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(EE40h~F040h) MTP Program Page Enable

R/W	Addr	D7	D6	D5	D4	D3	D2	D1	D0	HEX
R/W	EE40h	-	-	DBV_PGM_EN	CGM_PGM_EN	-	power_PGM_EN	SD_timing_PGM_EN	CGM_gm_PGM_EN	00h
R/W	EF40h	-	ACL_PGM_EN	VSRB_PGM_EN	gm3_PGM_EN	PANEL_PGM_EN	PID_PGM_EN	-	-	00h
R/W	F040h	SID_PGM_EN	gm4_PGM_EN	ABH_PGM_EN	gm1_PGM_EN	gm2_PGM_EN	VSR_PGM_EN	APRC_PGM_EN	SES_PGM_EN	00h

Description

Bit	Description	Data
DBV_PGM_EN	Page DBV: Enable program function	0: Enable 1: Disable
CGM_PGM_EN	Page CGM: Enable program function	
power_PGM_EN	Page Power: Enable program function	
SD_timing_PGM_EN	Page SD Timing: Enable program function	
CGM_gm_PGM_EN	Page CGM LUT: Enable program function	
ACL_PGM_EN	Page ACL: Enable program function	
VSRB_PGM_EN	Page GOA Timing2: Enable program function	
gm3_PGM_EN	Page Gamma3: Enable program function	
PANEL_PGM_EN	Page Panel: Enable program function	
PID_PGM_EN	Page Panel ID: Enable program function	
SID_PGM_EN	Page SID: Enable program function	
gm4_PGM_EN	Page Gamma4: Enable program function	
ABH_PGM_EN	Page ABH Mode: Enable program function	
gm1_PGM_EN	Page Gamma1: Enable program function	
gm2_PGM_EN	Page Gamma2: Enable program function	
VSR_PGM_EN	Page GOA Timing1: Enable program function	
APRC_PGM_EN	Page APRC: Enable program function	
SES_PGM_EN	Page SES: Enable program function	

Restriction

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(F240h) MTP Function Control

R/W	Addr	D7	D6	D5	D4	D3	D2	D1	D0	HEX
R/W	F240h	-	-	-	-	-	-	1	MTP_W	02h

Description	This command is to control MTP Program function. Bit: MTP_W Description: MTP Program function control Data: 0: No Programming 1: Execute Programming
Restriction	

(F340h~F540h) MTP Program Control

R/W	Addr	D7	D6	D5	D4	D3	D2	D1	D0	HEX
W	F340h	0	0	0	0	0	0	0	0	00h
W	F440h	0	0	0	0	0	0	0	0	00h
W	F540h	0	0	0	0	0	0	0	0	00h

Description	MTP Program Write Command should follow the sequence: Address [0xF340h] write 0xA5h -> Address [0xF440h] write 0x5Ah -> Address [0xF540h] write 0x3Ch
Restriction	

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(FE40h): CMD Mode Switch

R/W	Addr	D7	D6	D5	D4	D3	D2	D1	D0	HEX
W	FE40h	CMD_Page[7:0]								00h

Description

This command is used to switch the Manufacture Command Pages and User Commands sets.

CMD_Page[7:0]	Description
00h (default)	User Command Set (UCS = CMD1)
10h	Manufacture Command Set Page Panel ID
12h	Manufacture Command Set Page SID
20h	Manufacture Command Set Page Panel
40h	Manufacture Command Set Page ABH Mode
82h	Manufacture Command Set Page Power
92h	Manufacture Command Set Page SD timing
50h	Manufacture Command Set Page Gamma1
60h	Manufacture Command Set Page Gamma2
30h	Manufacture Command Set Page Gamma3
52h	Manufacture Command Set Page Gamma4
70h	Manufacture Command Set Page GOA Timing 1
F0h	Manufacture Command Set Page GOA Timing 2
42h	Manufacture Command Set Page DBV
22h	Manufacture Command Set Page SES
80h	Manufacture Command Set Page APRC
90h	Manufacture Command Set Page ACL
62h	Manufacture Command Set Page CGM
C2h	Manufacture Command Set Page CGM LUT

Restriction

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(FF40h): Read CMD Status

R/W	Addr	D7	D6	D5	D4	D3	D2	D1	D0	HEX
R	FF40h	CMD_Status[7:0]								00h

Description	This command is used to read the status of Manufacture Command Pages. Please refer to FE00h
Restriction	-

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1.7 MCS: CMD2 Page82, Power Settings

Instruction	R/W	Addr	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Source Sequence Control	R/W	0582h	-	-	DC2DC_idle_sd[1:0]		-	-	DC2DC_sd	STB_sd	00h
	R/W	0682h	DSIPOFF_frame2_sd[1:0]		DSIPOFF_frame1_sd[1:0]		DSIPON_frame2_sd[1:0]		DSIPON_frame1_sd[1:0]		00h
SD	R/W	0882h	-	-	-	-	SDPWR_DDVDH_A	SDPWR_DDVDH_B	-	-	0Ch
SD	R/W	0982h	-	AP_B[2:0]			-	AP_A[2:0]			33h
SD	R/W	0A82h	-	-	-	-	-	AP_H[2:0]			03h
SD	R/W	0C82h	-	-	-	-	HZOPOFF2_A	HZOPOFF2_B	HZOPOFF2_H	-	00h
charge pump	R/W	0D82h	-	ENB_PUMP_DDVDHREG_A	ENB_PUMP_DDVDHREG_B	ENB_PUMP_DDVDHREG_H	-	-	-	-	00h
charge pump	R/W	1282h	DVCLA[1:0]		-	VDHA[4:0]					85h
charge pump	R/W	1382h	BT_VGLIA	BT_DHIA	BT_DHA	BT_VCLA	BT_VGHA[1:0]		BT_VGLA[1:0]		01h
charge pump	R/W	1482h	-	DC1A[2:0]			-	DC3A[2:0]			44h
charge pump	R/W	1582h	-	DC4A[2:0]			-	DC5A[2:0]			44h
charge pump	R/W	1682h	DVCLB[1:0]		-	VDHB[4:0]					85h
charge pump	R/W	1782h	BT_VGLIB	BT_DHIB	BT_DHB	BT_VCLB	BT_VGHB[1:0]		BT_VGLB[1:0]		01h
charge pump	R/W	1882h	-	DC1B[2:0]			-	DC3B[2:0]			44h
charge pump	R/W	1982h	-	DC4B[2:0]			-	DC5B[2:0]			44h
charge pump	R/W	1A82h	DVCL_HBM[1:0]		-	VDHH[4:0]					85h
charge pump	R/W	1B82h	BT_VGLIH	BT_DHIH	BT_DHH	BT_VCLH	BT_VGHH[1:0]		BT_VGL_HBM[1:0]		01h
charge pump	R/W	1C82h	-	DC1H[2:0]			-	DC3_HBM[2:0]			44h
charge pump	R/W	1D82h	-	DC4_HBM[2:0]			-	DC5_HBM[2:0]			44h
SRAM_PWR_SAV	R/W	2182h	-	-	-	-	-	-	-	PSDseq_en	00h
VP5/VN5	R/W	2682h	VP5_on[1:0]		VP5_off[1:0]		VN5_on[1:0]		VN5_off[1:0]		55h
VP5/VN5	R/W	2A82h	-	-	-	VREFN5EN	-	-	-	VREFP5EN	01h
VP5/VN5	R/W	2B82h	-	-	-	-	VN5_PGND	-	-	VP5_PGND	09h
VP5/VN5	R/W	3082h	-	-	-	-	-	-	HBM_AIPset	HBM_is_VPN5	00h
VP5/VN5	R/W	3182h	-	-	VP5REGA[5:0]						0Dh
VP5/V	R/W	3282h	-	-	VN5REGA[5:0]						05h

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N5											
VP5/VN5	R/W	3382h	-	-	VP5REGB[5:0]						0Dh
VP5/VN5	R/W	3482h	-	-	VN5REGB[5:0]						05h
VP5/VN5	R/W	3582h	-	-	VP5REG_HBM[5:0]						0Dh
VP5/VN5	R/W	3682h	-	-	VN5REG_HBM[5:0]						05h
VP5/VN5	R/W	3782h	VP5REG_SKIP_sel	-	VP5REG_SKIP[5:0]						0Dh
VP5/VN5	R/W	3882h	VN5REG_SKIP_sel	-	VN5REG_SKIP[5:0]						05h
OVDD_OVSS	R/W	3F82h	-	-	OVDD_REG[5:0]						0Dh
OVDD_OVSS	R/W	4082h	-	-	OVSS_REG[5:0]						1Eh
OVDD_OVSS	R/W	4382h	-	-	-	-	-	OVDDPWR_VCI_H	OVDDPWR_VCI_B	OVDDPWR_VCI_A	00h
VGMP/VGSP	R/W	4482h	-	-	-	VGMPREG_OFF_SKIP	VGSPREG_OFF_SKIP	-	-	-	00h
VGMP/VGSP	R/W	4682h	-	-	-	-		VGSPPWR_VCI_H	VGSPPWR_VCI_B	VGSPPWR_VCI_A	00h
VGHR/VGLR	R/W	5582h	-	-	-	VGHREGA[4:0]					04h
VGHR/VGLR	R/W	5682h	-	-	-	VGHREGB[4:0]					04h
VGHR/VGLR	R/W	5782h	-	-	-	VGHREGH[4:0]					04h
VGHR/VGLR	R/W	5882h	-	-	-	VGLREGA[4:0]					06h
VGHR/VGLR	R/W	5982h	-	-	-	VGLREGB[4:0]					06h
VGHR/VGLR	R/W	5A82h	-	-	-	VGLREG_HBM[4:0]					06h
CMD Mode Switch	W	FE82h	CMD_Page[7:0]								00h
RD CMD Status	R	FF82h	CMD_Status[7:0]								00h

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(0582h~0682h) Source Sequence Control

R/W	Addr	D7	D6	D5	D4	D3	D2	D1	D0	HEX
R/W	0582h	-	-	DC2DC_idle_sd[1:0]		-	-	DC2DC_sd	STB_sd	00h
R/W	0682h	DSIPOFF_frame2_sd [1:0]		DSIPOFF_frame1_sd [1:0]		DSIPON_frame2_sd[1:0]		DSIPON_frame1_sd[1:0]		00h

Description

This command is used to set Source Timing Status on each region of power seq

Bit	Description	Data
DC2DC_idle_sd	Source status on DC2DC idle region	0: SD to AGND 1: SD to SD Power
DC2DC_sd	Source status on DC2DC region	0: AGND 1: SD Power
STB_sd	Source status on STB region	0: AGND 1: SD Power
DSIPOFF_frame2_sd	Source status on Display OFF 2nd blanking frame region	0: AGND 1: SD Power 2: VGMP 3: VGSP
DSIPOFF_frame1_sd	Source status on Display OFF 1st blanking frame region	
DSIPON_frame2_sd	Source status on Display ON 2nd blanking frame region	
DSIPON_frame1_sd	Source status on Display ON 1st blanking frame region	

Restriction

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(0882h) Source Power Selection

R/W	Addr	D7	D6	D5	D4	D3	D2	D1	D0	HEX
R/W	0882h	-	-	-	-	SDPWR_DDVDH_A	SDPWR_DDVDH_B	-	-	0Ch

Description	This command is for select source circuit power source is AVDD or VCI. Bit: SDPWR_DDVDH_A — Description: Normal mode source power selection — Data: 0:VCI 1:AVDD Bit: SDPWR_DDVDH_B — Description: IDLE mode source power selection — Data: 0:VCI 1:AVDD
Restriction	

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(0982h~0A82h) Source Power Selection

R/W	Addr	D7	D6	D5	D4	D3	D2	D1	D0	HEX
R/W	0982h	-	AP_B[2:0]			-	AP_A[2:0]			33h
R/W	0A82h	-	-	-	-	-	AP_H[2:0]			03h

Description

This command is used to set source driver driving condition in normal/IDLE/HBM mode.

AP_A/B/H[2:0]	OPAMP power consumption
000	-48%
001	-32%
010	-16%
011	default
100	+16%
101	+32%
110	+48%
111	+63%

These commands are used to set source channel OP driving capability

Bit	Description
AP_A	Normal mode OP driving capability
AP_B	IDLE mode OP driving capability
AP_H	HBM mode OP driving capability

Restriction

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(0C82h) Gamma OP Power Saving

R/W	Addr	D7	D6	D5	D4	D3	D2	D1	D0	HEX
R/W	0C82h	-	-	-	-	HZOPOFF2_A	HZOPOFF2_B	HZOPOFF2_H	-	00h

Description	These commands are used to set GAMMA OP power saving Bit / Description / Data HZOPOFF2_A / Normal mode GAMMA OP power saving / 0:OP normal driving 1:OP power saving HZOPOFF2_B / IDLE mode GAMMA OP power saving / 0:OP normal driving 1:OP power saving HZOPOFF2_H / HBM mode GAMMA OP power saving / 0:OP normal driving 1:OP power saving
Restriction	

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(0D82h) Pump Regulation Control

R/W	Addr	D7	D6	D5	D4	D3	D2	D1	D0	HEX
R/W	0D82h	-	ENB_PUMP_DDVDHREG_A	ENB_PUMP_DDVDHREG_B	ENB_PUMP_DDVDHREG_H	-	-	-	-	00h

Description	These commands are used to control DVDDH regulation function. Bit / Description / Data ENB_PUMP_DDVDHREG_A / Normal mode DDVDH regulator control / 0:enable 1:disable ENB_PUMP_DDVDHREG_B / IDLE mode DDVDH regulator control / 0:enable 1:disable ENB_PUMP_DDVDHREG_H / HBM mode DDVDH regulator control / 0:enable 1:disable .
Restriction	If BT_DHIA =1, ENB_PUMP_DDHDHREG_A need to set “1”. If BT_DHIB =1, ENB_PUMP_DDHDHREG_B need to set “1”. If BT_DHIH =1, ENB_PUMP_DDHDHREG_H need to set “1”. Otherwise, ENB_PUMP_DDHDHREG_A/B/H shall keep “0”

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(1282h~1382h) Normal Mode Pump Control

R/W	Addr	D7	D6	D5	D4	D3	D2	D1	D0	HEX
R/W	1282h	DVCLA[1:0]		-	VDHA[4:0]					85h
R/W	1382h	BT_VGLIA	BT_DHIA	BT_DHA	BT_VCLA	BT_VGHA[1:0]		BT_VGLA[1:0]		01h

Description

This command is used to control AVDD voltage in normal mode.

VDHA[4:0]	AVDD
00h	6.5v
01h	6.4V
02h	6.3V
:	0.1V /step
05h	6V
:	0.1V /step
14h	4.5V
15h~	reserved

This command is used to control VCL output level in normal mode.

DVCLA[1:0]	VCL
00h	-3.5v
01h	-4.0V
02h	-4.5V
03h	-5.0V

This command is used to set VCL level

Bit	Description	Data
BT_VCLA	VCL Pump control	0: VCL=VCIx-1 1: VCL=VCIx-2

These commands are used to set AVDD level

BT_DHIA	BT_DHA	AVDD
0	0	VCI x 2.0
0	1	VCI x 3.0
1	0	VCI+VDDI
1	1	VCI+VDDI

If BT_DHIA =1 (AVDD=VCI+VDDI), AVDD has no regulation function and ENB_PUMP_DDVDHREG_A must set to “1”

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This command is used to set VGH

BT_VGHA[1:0]	VGH
00h	DDVDH
01h	DDVDH+VCI
10h	2xDDVDH
11h	DDVDH+VDDI

These commands are used to set VGL level

BT_VGLIA	BT_VGLA[1:0]	VGL
0	00h	VCL
0	01h	VCL-VCI
0	10h	VCL-DDVDH
0	11h	2xVCL-DDVDH
1	X	-DDVDH

Restriction	If BT_DHA is equal to 1, the Normal Mode output range of AVDD is from 6.5v to (2*VCI – 0.5).

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(1482h~1582h) Normal Mode Pump Frequency

R/W	Addr	D7	D6	D5	D4	D3	D2	D1	D0	HEX
R/W	1482h	-	DC1A[2:0]			-	DC3A[2:0]			44h
R/W	1582h	-	DC4A[2:0]			-	DC5A[2:0]			44h

Description

These commands are used to set charge pump frequency

DC1 for AVDD pump control
DC3 for VCL pump control
DC4 for VGH pump control
DC5 for VGL pump control

DC*[2:0]	Pump Clock Frequency
3'h0	Hsync / 16
3'h1	Hsync / 8
3'h2	Hsync / 4
3'h3	Hsync / 2
3'h4	Hsync
3'h5	Hsync * 2
3'h6	Hsync * 3
3'h7	Hsync * 4

Note: Hsync = Frame Rate x (display + vporch) Lines, ex: 60Hz x (400+36) LINE=26.16KHz.

Restriction

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(1682h~1782h) IDLE Mode Pump Control

R/W	Addr	D7	D6	D5	D4	D3	D2	D1	D0	HEX
R/W	1682h	DVCLB[1:0]		-	VDHB[4:0]					85h
R/W	1782h	BT_VGLIB	BT_DHIB	BT_DHB	BT_VCLB	BT_VGHB[1:0]		BT_VGLB[1:0]		01h

Description

This command is used to control AVDD voltage in IDLE mode.

VDHB[4:0]	AVDD
00h	6.5v
01h	6.4V
02h	6.3V
:	0.1V /step
05h	6V
:	0.1V /step
14h	4.5V
15h~	reserved

This command is used to control VCL output level in IDLE mode.

DVCLB[1:0]	VCL
00h	-3.5v
01h	-4.0V
02h	-4.5V
03h	-5.0V

This command is used to set VCL level

Bit	Description	Data
BT_VCLB	VCL Pump control	0: VCL=VCIx-1 1: VCL=VCIx-2

These commands are used to set AVDD level

BT_DHIB	BT_DHB	AVDD
0	0	VCI x 2.0
0	1	VCI x 3.0
1	0	VCI+VDDI
1	1	VCI+VDDI

If BT_DHIB =1 (AVDD=VCI+VDDI), AVDD has no regulation function and ENB_PUMP_DDVDHREG_B must set to “1”

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This command is used to set VGH

BT_VGHB[1:0]	VGH
00h	DDVDH
01h	DDVDH+VCI
10h	2xDDVDH
11h	DDVDH+VDDI

These commands are used to set VGL level

BT_VGLIB	BT_VGLB[1:0]	VGL
0	00h	VCL
0	01h	VCL-VCI
0	10h	VCL-DDVDH
0	11h	2xVCL-DDVDH
1	X	-DDVDH

Restriction	If BT_DHB is equal to 1, the IDLE mode output range of AVDD is from 6.5v to (2*VCI – 0.5).

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(1882h~1982h) IDLE Mode Pump Frequency

R/W	Addr	D7	D6	D5	D4	D3	D2	D1	D0	HEX
R/W	1882h	-	DC1B[2:0]			-	DC3B[2:0]			44h
R/W	1982h	-	DC4B[2:0]			-	DC5B[2:0]			44h

Description

These commands are used to set charge pump frequency

DC1 for AVDD pump control
DC3 for VCL pump control
DC4 for VGH pump control
DC5 for VGL pump control

DC*[2:0]	Pump Clock Frequency
3'h0	Hsync / 16
3'h1	Hsync / 8
3'h2	Hsync / 4
3'h3	Hsync / 2
3'h4	Hsync
3'h5	Hsync * 2
3'h6	Hsync * 3
3'h7	Hsync * 4

Note: Hsync = Frame Rate x (display + vporch) Lines, ex: 60Hz x (400+36) LINE=26.16KHz.

Restriction

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(1A82h~1B82h) HBM Mode Pump Control

R/W	Addr	D7	D6	D5	D4	D3	D2	D1	D0	HEX
R/W	1A82h	DVCL_HBM[1:0]		-	VDHH[4:0]					85h
R/W	1B82h	BT_VGLIH	BT_DHIH	BT_DHH	BT_VCLH	BT_VGHH[1:0]		BT_VGL_HBM[1:0]		01h

Description

This command is used to control AVDD voltage in HBM mode.

VDHH[4:0]	AVDD
00h	6.5v
01h	6.4V
02h	6.3V
:	0.1V /step
05h	6V
:	0.1V /step
14h	4.5V
15h~	reserved

This command is used to control VCL output level in HBM mode.

DVCL_HBM[1:0]	VCL
00h	-3.5v
01h	-4.0V
02h	-4.5V
03h	-5.0V

This command is used to set VCL level

Bit	Description	Data
BT_VCLH	VCL Pump control	0: VCL=VCIx-1 1: VCL=VCIx-2

These commands are used to set AVDD level

BT_DHIH	BT_DHH	AVDD
0	0	VCI x 2.0
0	1	VCI x 3.0
1	0	VCI+VDDI
1	1	VCI+VDDI

If BT_DHIH =1 (AVDD=VCI+VDDI), AVDD has no regulation function and ENB_PUMP_DDVDHREG_H must set to “1”

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This command is used to set VGH

BT_VGHH[1:0]	VGH
00h	DDVDH
01h	DDVDH+VCI
10h	2xDDVDH
11h	DDVDH+VDDI

These commands are used to set VGL level

BT_VGLIH	BT_VGL_HBM[1:0]	VGL
0	00h	VCL
0	01h	VCL-VCI
0	10h	VCL-DDVDH
0	11h	2xVCL-DDVDH
1	X	-DDVDH

Restriction	If BT_DHH is equal to 1, the HBM Mode output range of AVDD is from 6.5v to (2*VCI – 0.5).

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(1C82h~1D82h) HBM Mode Pump Frequency

R/W	Addr	D7	D6	D5	D4	D3	D2	D1	D0	HEX
R/W	1C82h	-	DC1H[2:0]			-	DC3_HBM[2:0]			44h
R/W	1D82h	-	DC4_HBM[2:0]			-	DC5_HBM[2:0]			44h

Description

These commands are used to set charge pump frequency

DC1 for AVDD pump control
DC3 for VCL pump control
DC4 for VGH pump control
DC5 for VGL pump control

DC*[2:0]	Pump Clock Frequency
3'h0	Hsync / 16
3'h1	Hsync / 8
3'h2	Hsync / 4
3'h3	Hsync / 2
3'h4	Hsync
3'h5	Hsync * 2
3'h6	Hsync * 3
3'h7	Hsync * 4

Note: Hsync = Frame Rate x (display + vporch) Lines, ex: 60Hz x (400+36) LINE=26.16KHz.

Restriction

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(2182h) Graphic RAM Power Saving Control

R/W	Addr	D7	D6	D5	D4	D3	D2	D1	D0	HEX
R/W	2182h	-	-	-	-	-	-	-	PSDseq_en	00h

Description	This command is used to control graphic RAM power saving function Bit: PSDseq_en Description: 1: power saving in SLPIN mode 0: normal
Restriction	When PSDseq_en=1, the graphic data in SRAM will lost in SLPIN, and host must update graphic after SLPOUT

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(2682h) VREFPN5 Sequence

R/W	Addr	D7	D6	D5	D4	D3	D2	D1	D0	HEX
R/W	2682h	VP5_on[1:0]		VP5_off[1:0]		VN5_on[1:0]		VN5_off[1:0]		55h

Description

This command is used to set VREFP5 and VREFN5 output status.

Bit	Description	Data
VP5_on[1:0]	VREFP5 output status from DC2DC frame 4 to Display ON blanking frame region.	00 : VP5 Power 01 : VREFP5 10 : Ground 11 : Reserved
VP5_off[1:0]	VREFP5 output status on Display OFF blanking frame region.	00 : VP5 Power 01 : VREFP5 10 : Ground 11 : Reserved
VN5_on[1:0]	VREFN5 output status from DC2DC frame 4 to Display ON blanking frame region.	00 : VCL 01 : VREFN5 10 : Ground 11 : Reserved
VN5_off[1:0]	VREFN5 output status on Display OFF blanking frame region.	00 : VCL 01 : VREFN5 10 : Ground 11 : Reserved

Restriction

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(2A82h) VREFPN5 control

R/W	Addr	D7	D6	D5	D4	D3	D2	D1	D0	HEX
R/W	2A82h	-		-	VREFN 5EN	-	-	-	VREFP 5EN	01h

<table>
<tr><td>Description</td><td>This command is to turn on/off VREFP5/VREFN5 regulator.
<table>
<tr><th>Bit</th><th>Description</th><th>Data</th></tr>
<tr><td>VREFP5EN</td><td>VREFP5 regulator on/off</td><td>0=regulator off, and the output is controlled by VP5_PGND (2B82h)
1=regulator on</td></tr>
<tr><td>VREFN5EN</td><td>VREFN5 regulator on/off</td><td>0=regulator off, and the output is controlled by VN5_PGND (2B82h)
1=regulator on</td></tr>
</table></td></tr>
<tr><td>Restriction</td><td></td></tr>
</table>

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(2B82h) VP5/VN5 OFF Setting

R/W	Addr	D7	D6	D5	D4	D3	D2	D1	D0	HEX
R/W	2B82h	-	-	-	-	VN5_PGND	-	-	VP5_PGND	09h

Description	VN5_PGND: to select VREFN5 is GND when VN5 is disable VP5_PGND: to select VREFP5 is GND when VP5 is disable
Restriction	

(3082h) HBM AIP Enable

R/W	Addr	D7	D6	D5	D4	D3	D2	D1	D0	HEX
R/W	3082h	-	-	-	-	-	-	HBM_AIPset	HBM_is_VPN5	00h

Description	HBM_AIPset: 1: The following setting change when RM690B0 is under HBM mode 0: The following setting are based on normal mode, not refer to HBM mode register. DC3_HBM, DVCL_HBM, DC5_HBM, BT_VCLH, BT_VGL_HBM, VGLREG_HBM (1A82h~1D82h, 5A82h~6082h) HBM_is_VPN5: 1: The following setting change when RM690B0 is under HBM mode 0: The following setting are based on normal mode, not refer to HBM mode register. VP5REG_HBM, VN5REG_HBM (3582h~3682h)
Restriction	

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(3182h~3882h) VP5 / VN5 voltage setting

R/W	Addr	D7	D6	D5	D4	D3	D2	D1	D0	HEX
R/W	3182h	-	-	VP5REGA[5:0]						0Dh
R/W	3282h	-	-	VN5REGA[5:0]						05h
R/W	3382h	-	-	VP5REGB[5:0]						0Dh
R/W	3482h	-	-	VN5REGB[5:0]						05h
R/W	3582h	-	-	VP5REG_HBM[5:0]						0Dh
R/W	3682h	-	-	VN5REG_HBM[5:0]						05h
R/W	3782h	VP5REG_SKIP_SEL	-	VP5REG_SKIP[5:0]						0Dh
R/W	3882h	VN5REG_SKIP_SEL	-	VN5REG_SKIP[5:0]						05h

Description

VP5REGA is for VP5 normal setting. Per-step is 0.1V
VP5REGB is for VP5 idle setting. Per-step is 0.1V
VP5REG_HBM is for VP5 HBM setting. Per-step is 0.1V
VP5REG_SKIP is for VP5 skip-frame setting when VP5REG_SKIP_SEL=1.

VP5REG_A/B/HBM[5:0]	VREFP5 (V)
000011	0.5
000100	0.6
000101	0.7
000110	0.8
…..	…..
001101	1.5 (default)
…..	…..
101101	4.7
101110	4.8
101111	4.9
110000	5.0
others	reserved

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<table>
<tr><td></td><td>VN5REGA is for VN5 normal setting. Per-step is 0.1V
VN5REGB is for VN5 idle setting. Per-step is 0.1V
VN5REG_HBM is for VN5 HBM setting. Per-step is 0.1V
VN5REG_SKIP is for VN5 skip-frame setting when VN5REG_SKIP_SEL=1.
<table>
<tr><th>VN5REG_A/B/HBM[5:0]</th><th>VREFN5 (V)</th></tr>
<tr><td>000000</td><td>-0.5</td></tr>
<tr><td>000001</td><td>-0.6</td></tr>
<tr><td>000010</td><td>-0.7</td></tr>
<tr><td>000011</td><td>-0.8</td></tr>
<tr><td>-----</td><td>…..</td></tr>
<tr><td>000101</td><td>-1.0 (default)</td></tr>
<tr><td>-----</td><td>…..</td></tr>
<tr><td>100101</td><td>-4.2</td></tr>
<tr><td>100110</td><td>-4.3</td></tr>
<tr><td>100111</td><td>-4.4</td></tr>
<tr><td>101000</td><td>-4.5</td></tr>
<tr><td>others</td><td>reserved</td></tr>
</table></td></tr>
<tr><td>Restriction</td><td></td></tr>
</table>

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(3F82h) OVDD Control

R/W	Addr	D7	D6	D5	D4	D3	D2	D1	D0	HEX
R/W	3F82h	-	-	OVDD_REG[5:0]						0Dh

Description

This command is used to set OVDD voltage level.

OVDD_REG[5:0]	OVDD voltage (V)
6'h00~03	reserved
6'h04	2.4
6'h05	2.5
6'h06	2.6
6'h07	2.7
6'h08	2.8
6'h09	2.9
6'h0A	3.0
6'h0B	3.1
6'h0C	3.2
6'h0D	3.3
:	0.1V/step
:	:
6'h1D	4.9
others	reserved

Restriction

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(4082h) OVSS Control

R/W	Addr	D7	D6	D5	D4	D3	D2	D1	D0	HEX
R/W	4082h	-	-	OVSS_REG[5:0]						1Eh

Description

This command is used to set OVSS voltage level.

OVSS_REG[5:0]	OVSS voltage (V)
6'h00	0
6'h01	-0.4
6'h02	-0.5
…	-0.1V/step
6'h1E	-3.3
…	-0.1V/step
6'h2B	-4.6
6'h2C	-4.7
6'h2D~6'h3F	Reserved

Restriction

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(4382h) OVDD Power Source Control

R/W	Addr	D7	D6	D5	D4	D3	D2	D1	D0	HEX
R/W	4382h	-	-	-	-	-	OVDDPWR_VCI_H	OVDDPWR_VCI_B	OVDDPWR_VCI_A	00h

<table>
<tr><td>Description</td><td>This command is for select OVDD regulator circuit power source is AVDD or VCI.
<table>
<tr><th>Bit</th><th>Description</th><th>Data</th></tr>
<tr><td>OVDDPWR_VCI_H</td><td>OVDD regulator source in normal mode</td><td rowspan="3">0: power source is AVDD
1: power source is VCI</td></tr>
<tr><td>OVDDPWR_VCI_B</td><td>OVDD regulator source in IDLE mode</td></tr>
<tr><td>OVDDPWR_VCI_A</td><td>OVDD regulator source in HBM mode</td></tr>
</table></td></tr>
<tr><td>Restriction</td><td></td></tr>
</table>

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(4482h) VGMP/VGSP Skip Frame Control

R/W	Addr	D7	D6	D5	D4	D3	D2	D1	D0	HEX
R/W	4482h	-	-	-	VGMPREG_OFF_SKIP	VGSPREG_OFF_SKIP	-	-	-	00h

Description	VGMPREG_OFF_SKIP=1, VGMP regulator is off at skip frame VGSPREG_OFF_SKIP=1, VGSP regulator is off at skip frame
Restriction	

(4682h) VGSP Power Source Control

R/W	Addr	D7	D6	D5	D4	D3	D2	D1	D0	HEX
R/W	4682h	-	-	-	-	-	VGSPPWR_VCI_H	VGSPPWR_VCI_B	VGSPPWR_VCI_A	00h

Description

This command is for select VGSP power source is AVDD or VCI.

Bit	Description	Data
VGSPPWR_VCI_H	VGSP power source in normal mode	0: power source is AVDD 1: power source is VCI
VGSPPWR_VCI_B	VGSP power source in IDLE mode	
VGSPPWR_VCI_A	VGSP power source in HBM mode	

Restriction

If VGSPPWR_VCI_A/B/H=1 (power source select to VCI), the VGSP output level must set to the value ≦ 2.5V .

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(5582h~5782h) VGHR Control

R/W	Addr	D7	D6	D5	D4	D3	D2	D1	D0	HEX
R/W	5582h	-	-	-	VGHREGA[4:0]					04h
R/W	5682h	-	-	-	VGHREGB[4:0]					04h
R/W	5782h	-	-	-	VGHREGH[4:0]					04h

Description

These commands are used to set VGHR Level
VGHREGA for normal mode, VGHREGB for IDLE mode, and VGHREGH for HBM mode.

VGHREG[4:0]	VGHR
00000	3V
00001	3.5V
00010	4V
00011	4.5V
00100 (Default)	5V
00101	5.5V
00110	6V
:	0.5V /step
10010	12.0V
others	reserved

Restriction

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(5882h~5A82h) VGLR Control

R/W	Addr	D7	D6	D5	D4	D3	D2	D1	D0	HEX
R/W	5882h	-	-	-	VGLREGA[4:0]					06h
R/W	5982h	-	-	-	VGLREGB[4:0]					06h
R/W	5A82h	-	-	-	VGLREGH[4:0]					06h

Description

These commands are used to set VGLR Level
VGLREGA for normal mode, VGLREGB for IDLE mode, and VGLREGH for HBM mode.

VGLREG[4:0]	VGLR [V]
00000	-2.0
00001	-2.5
:	0.5V /step
00100	-4.0
00101	-4.5
00110 (Default)	-5 (default)
00111	-5.5
01000	-6.0
:	0.5V /step
10100	-12.0
others	reserved

Restriction

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(FE82h): CMD Mode Switch

R/W	Addr	D7	D6	D5	D4	D3	D2	D1	D0	HEX
W	FE82h	CMD_Page[7:0]								00h

Description

This command is used to switch the Manufacture Command Pages and User Commands sets.

CMD_Page[7:0]	Description
00h (default)	User Command Set (UCS = CMD1)
10h	Manufacture Command Set Page Panel ID
12h	Manufacture Command Set Page SID
20h	Manufacture Command Set Page Panel
40h	Manufacture Command Set Page ABH Mode
82h	Manufacture Command Set Page Power
92h	Manufacture Command Set Page SD timing
50h	Manufacture Command Set Page Gamma1
60h	Manufacture Command Set Page Gamma2
30h	Manufacture Command Set Page Gamma3
52h	Manufacture Command Set Page Gamma4
70h	Manufacture Command Set Page GOA Timing 1
F0h	Manufacture Command Set Page GOA Timing 2
42h	Manufacture Command Set Page DBV
22h	Manufacture Command Set Page SES
80h	Manufacture Command Set Page APRC
90h	Manufacture Command Set Page ACL
62h	Manufacture Command Set Page CGM
C2h	Manufacture Command Set Page CGM LUT

Restriction

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(FF82h): Read CMD Status

R/W	Addr	D7	D6	D5	D4	D3	D2	D1	D0	HEX
R	FF82h	CMD_Status[7:0]								00h

Description	This command is used to read the status of Manufacture Command Pages. Please refer to FE00h
Restriction	-

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1.8 MCS: CMD2 Page92, SD Timing Settings

Instruction	R/W	Addr	D7	D6	D5	D4	D3	D2	D1	D0	HEX
SD_COPEN_OFF	R/W	0092h	-	-	-	-	-	-	SD_COPEN_OFF	SD_COPEN_H_opt	00h
Source control	R/W	0192h	-	-	1	GAMMA_SWAP	-	-	SW_POL	-	20h
SD	R/W	0392h	-	-	-	-	-	-	GAM_HZOPOFF_opt2	GAM_HZOPOFF_opt	00h
PRE-CHARGE selection	R/W	0592h	prechg_sel[1:0]		-	-	-	1	1	1	07h
Switch Timing 1 Control	R/W	0892h	T1_sd[7:0]								17h
	R/W	0992h	Tp_sd[7:0]								00h
	R/W	0A92h	Th_sd[7:0]								17h
	R/W	0B92h	Tsw_sd[7:0]								44h
	R/W	0C92h	Thsw_sd[7:0]								17h
	R/W	0D92h	Thsd_sd[7:0]								0Dh
Switch Timing 2 Control	R/W	0E92h	T1_sd_l[7:0]								00h
	R/W	0F92h	Tp_sd_l[7:0]								00h
	R/W	1092h	Th_sd_l[7:0]								00h
	R/W	1192h	Tsw_sd_l[7:0]								00h
	R/W	1292h	Thsw_sd_l[7:0]								00h
	R/W	1392h	Thsd_sd_l[7:0]								00h
Switch Output Selection	R/W	4692h	SW_step1_of_ol[3:0]				SW_step1_of_el[3:0]				11h
	R/W	4792h	SW_step2_of_ol[3:0]				SW_step2_of_el[3:0]				22h
	R/W	4892h	SW_step3_of_ol[3:0]				SW_step3_of_el[3:0]				33h
	R/W	4992h	SW_step4_of_ol[3:0]				SW_step4_of_el[3:0]				44h
	R/W	4A92h	SW_step5_of_ol[3:0]				SW_step5_of_el[3:0]				55h
	R/W	4B92h	SW_step6_of_ol[3:0]				SW_step6_of_el[3:0]				66h
	R/W	5392h	SW_step1_ef_ol[3:0]				SW_step1_ef_el[3:0]				11h
	R/W	5492h	SW_step2_ef_ol[3:0]				SW_step2_ef_el[3:0]				22h
	R/W	5592h	SW_step3_ef_ol[3:0]				SW_step3_ef_el[3:0]				33h
	R/W	5692h	SW_step4_ef_ol[3:0]				SW_step4_ef_el[3:0]				44h
	R/W	5792h	SW_step5_ef_ol[3:0]				SW_step5_ef_el[3:0]				55h
	R/W	5892h	SW_step6_ef_ol[3:0]				SW_step6_ef_el[3:0]				66h
Source Data Output Selection	R/W	5F92h	SD_step1_of_ol[3:0]				SD_step1_of_el[3:0]				11h
	R/W	6092h	SD_step2_of_ol[3:0]				SD_step2_of_el[3:0]				22h
	R/W	6192h	SD_step3_of_ol[3:0]				SD_step3_of_el[3:0]				33h
	R/W	6292h	SD_step4_of_ol[3:0]				SD_step4_of_el[3:0]				44h
	R/W	6392h	SD_step5_of_ol[3:0]				SD_step5_of_el[3:0]				55h
	R/W	6492h	SD_step6_of_ol[3:0]				SD_step6_of_el[3:0]				66h
	R/W	6B92h	SD_step1_ef_ol[3:0]				SD_step1_ef_el[3:0]				11h
	R/W	6C92h	SD_step2_ef_ol[3:0]				SD_step2_ef_el[3:0]				22h
	R/W	6D92h	SD_step3_ef_ol[3:0]				SD_step3_ef_el[3:0]				33h
	R/W	6E92h	SD_step4_ef_ol[3:0]				SD_step4_ef_el[3:0]				44h
	R/W	6F92h	SD_step5_ef_ol[3:0]				SD_step5_ef_el[3:0]				55h
	R/W	7092h	SD_step6_ef_ol[3:0]				SD_step6_ef_el[3:0]				66h

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SD	R/W	7C92h	-	-	-	T_ap_opt	-	-	-	-	10h
CMD Mode Switch	W	FE92h	CMD_Page[7:0]								00h
Read CMD Status	R	FF92h	CMD_Status[7:0]								00h

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(0092h) SD_COPEN_OFF

R/W	Addr	D7	D6	D5	D4	D3	D2	D1	D0	HEX
R/W	0092h	-	-	-	-	-	-	SD_COPEN_OFF	SD_COPEN_H_opt	00h

Description	These commands are used to set source power saving option Bit: SD_COPEN_OFF — Description: Source power saving option — Data: 0:Normal 1:Enable power saving Bit: SD_COPEN_H_opt — Description: Source even channel power saving option — Data: 0:Normal 1:Enable power saving
Restriction	If MUX_num_sel=0 (MUX6) or MUX_num_sel=3 (MUX9), the SD_COPEN_H_opt shall set to “0”.

(0192h) GAMA/Switch Option

R/W	Addr	D7	D6	D5	D4	D3	D2	D1	D0	HEX
R/W	0192h	-	-	1	GAMMA_SWAP	-	-	SW_POL	-	20h

Description	These commands are used to set source option Bit: GAMMA_SWAP — Description: gamma reference voltage selection — Data: 0:Normal operation 1:VGMP/VGSP swap Bit: SW_POL — Description: Polarity of panel switch — Data: 1’b0: Low active 1’b1: High active
Restriction	

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(0392h) Gamma OP Power Saving Control

R/W	Addr	D7	D6	D5	D4	D3	D2	D1	D0	HEX
R/W	0392h	-	-	-	-	-	-	GAM_HZOPOFF_opt2	GAM_HZOPOFF_opt	00h

Description	These commands are used to set gamma OP power saving option Bit: GAM_HZOPOFF_opt2 — Description: Gamma OP power saving option 2 — Data: 0:Normal, 1:Enable power saving Bit: GAM_HZOPOFF_opt — Description: Gamma OP power saving option 1 — Data: 0:Normal, 1:Enable power saving
Restriction	

(0592h) PRE-CHARGE Selection

R/W	Addr	D7	D6	D5	D4	D3	D2	D1	D0	HEX
R/W	0592h	prechg_sel[1:0]		-	-	-	1	1	1	07h

Description	This command is used to select source pre-charge level Bit: prechg_sel — Description: Pre-charge level selection — Data: 0:AGND, 1:SD Power, 2:VGMP, 3:VGSP
Restriction	

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(0892h~0D92h) Switch Timing1 Control

R/W	Addr	D7	D6	D5	D4	D3	D2	D1	D0	HEX
R/W	0892h	T1_sd[7:0]								17h
R/W	0992h	Tp_sd[7:0]								00h
R/W	0A92h	Th_sd[7:0]								17h
R/W	0B92h	Tsw_sd[7:0]								44h
R/W	0C92h	Thsw_sd[7:0]								17h
R/W	0D92h	Thsd_sd[7:0]								0Dh

Description

These commands are used to set SW timing. (unit: 41.667ns)

Bit	Description	Data
T1_sd	Time delay from Hsync to pre-charge start	1. Set Th_sd = Thsw_sd 2. Thsw_sd > Thsd_sd + 0.5us. 3. Thsd_sd > T(GREQ_ SW[5:0]) + SW transient time 4. Th_sd[7:0] and Tsw_sd[7:0] should be larger than GREQ_SW[5:0] or GFEQ_SW[5:0]
Tp_sd	Pulse width of pre-charge	
Th_sd	Time delay from pre-charge stop to SW1 start	
Tsw_sd	Pulse width of SW(n)	
Thsw_sd	Non overlap time between SW(n) to SW(n+1)	
Thsd_sd	Source data output hold time	

Restriction

These commands are activated when SW_A_A_SEL~ SW_A_A3_SEL or SW_A_B_SEL~ SW_A_B2_SEL or SW_A_H_SEL select to 0.

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(0E92h~1392h) Switch Timing2 Control

R/W	Addr	D7	D6	D5	D4	D3	D2	D1	D0	HEX
R/W	0E92h	T1_sd_I[7:0]								00h
R/W	0F92h	Tp_sd_I[7:0]								00h
R/W	1092h	Th_sd_I[7:0]								00h
R/W	1192h	Tsw_sd_I[7:0]								00h
R/W	1292h	Thsw_sd_I[7:0]								00h
R/W	1392h	Thsd_sd_I[7:0]								00h

Description

These commands are used to set SW timing parameter. (unit: 41.667ns)

Bit	Description	Data
T1_sd_I	Time delay from Hsync to pre-charge start	1. Set Th_sd = Thsw_sd 2. Thsw_sd > Thsd_sd + 0.5us. 3. Thsd_sd > T(GREQ_ SW[5:0]) + SW transient time 4. Th_sd[7:0] and Tsw_sd[7:0] should be larger than GREQ_SW[5:0] or GFEQ_SW[5:0]
Tp_sd_I	Pulse width of pre-charge	
Th_sd_I	Time delay from pre-charge stop to SW1 start	
Tsw_sd_I	Pulse width of SW(n)	
Thsw_sd_I	Non overlap time between SW(n) to SW(n+1)	
Thsd_sd_I	Source data output hold time	

Restriction

These commands are activated when SW_A_A_SEL~ SW_A_A3_SEL or SW_A_B_SEL~ SW_A_B2_SEL or SW_A_H_SEL select to 1.

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(4692h~4B92h,5392h~5892h) Switch Output Selection

R/W	Addr	D7	D6	D5	D4	D3	D2	D1	D0	HEX
R/W	4692h	SW_step1_of_ol[3:0]				SW_step1_of_el[3:0]				11h
R/W	4792h	SW_step2_of_ol[3:0]				SW_step2_of_el[3:0]				22h
R/W	4892h	SW_step3_of_ol[3:0]				SW_step3_of_el[3:0]				33h
R/W	4992h	SW_step4_of_ol[3:0]				SW_step4_of_el[3:0]				44h
R/W	4A92h	SW_step5_of_ol[3:0]				SW_step5_of_el[3:0]				55h
R/W	4B92h	SW_step6_of_ol[3:0]				SW_step6_of_el[3:0]				66h
R/W	5392h	SW_step1_ef_ol[3:0]				SW_step1_ef_el[3:0]				11h
R/W	5492h	SW_step2_ef_ol[3:0]				SW_step2_ef_el[3:0]				22h
R/W	5592h	SW_step3_ef_ol[3:0]				SW_step3_ef_el[3:0]				33h
R/W	5692h	SW_step4_ef_ol[3:0]				SW_step4_ef_el[3:0]				44h
R/W	5792h	SW_step5_ef_ol[3:0]				SW_step5_ef_el[3:0]				55h
R/W	5892h	SW_step6_ef_ol[3:0]				SW_step6_ef_el[3:0]				66h

Description

These commands area used to set the panel switch output sequence at odd/even line of odd/even frame

.

SW_step*_of_ol : SW output mapping at odd line of odd frame
SW_step*_of_el : SW output mapping at even line of odd frame
SW_step*_ef_ol : SW output mapping at odd line of even frame
SW_step*_ef_el : SW output mapping at even line of even frame

For example, SW_step3_of_ol[3:0]=4'h5, then the panel switch SW[5] will be active at STEP3 at odd frame and odd line.

Restriction

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(5F92h~6492h, 6B92h~7092h) Source Data Output Selection

R/W	Addr	D7	D6	D5	D4	D3	D2	D1	D0	HEX
R/W	5F92h	SD_step1_of_ol[3:0]				SD_step1_of_el[3:0]				11h
R/W	6092h	SD_step2_of_ol[3:0]				SD_step2_of_el[3:0]				22h
R/W	6192h	SD_step3_of_ol[3:0]				SD_step3_of_el[3:0]				33h
R/W	6292h	SD_step4_of_ol[3:0]				SD_step4_of_el[3:0]				44h
R/W	6392h	SD_step5_of_ol[3:0]				SD_step5_of_el[3:0]				55h
R/W	6492h	SD_step6_of_ol[3:0]				SD_step6_of_el[3:0]				66h
R/W	6B92h	SD_step1_ef_ol[3:0]				SD_step1_ef_el[3:0]				11h
R/W	6C92h	SD_step2_ef_ol[3:0]				SD_step2_ef_el[3:0]				22h
R/W	6D92h	SD_step3_ef_ol[3:0]				SD_step3_ef_el[3:0]				33h
R/W	6E92h	SD_step4_ef_ol[3:0]				SD_step4_ef_el[3:0]				44h
R/W	6F92h	SD_step5_ef_ol[3:0]				SD_step5_ef_el[3:0]				55h
R/W	7092h	SD_step6_ef_ol[3:0]				SD_step6_ef_el[3:0]				66h

Description

These commands used to set the source multiplex output sequence.
The following example illustrates how to set these parameters at MUX1-6 application

SW Tag	1	2	3	4	5	6
Odd Line	R1	G1	B1	R2	G2	B2
Even Line	B1	R1	G1	B2	R2	G2

SW tag	Panel Switch Setting				Source Data Setting			
Order	Order: R->G->B		Order: R->G->B		Order: R->G->B		Order: R->G->B	
1	SW step1_*_ol	1	SW step1_*_el	2	SD step1_*_ol	1	SD step1_*_el	1
2	SW step2_*_ol	4	SW step2_*_el	5	SD step2_*_ol	4	SD step2_*_el	4
3	SW step3_*_ol	2	SW step3_*_el	3	SD step3_*_ol	2	SD step3_*_el	2
4	SW step4_*_ol	5	SW step4_*_el	6	SD step4_*_ol	5	SD step4_*_el	5
5	SW step5_*_ol	3	SW step5_*_el	1	SD step5_*_ol	3	SD step5_*_el	3
6	SW step6_*_ol	6	SW step6_*_el	4	SD step6_*_ol	6	SD step6_*_el	6

SD_step*_of_ol : SD output data at odd line of odd frame
SD_step*_of_el : SD output data at even line of odd frame
SD_step*_ef_ol : SD output data at odd line of even frame
SD_step*_ef_el : SD output data at even line of even frame

Restriction

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(7C92h) SD Control Option

R/W	Addr	D7	D6	D5	D4	D3	D2	D1	D0	HEX
R/W	7C92h	-	-	-	T_ap_opt	-	-	-	-	10h

Description	These commands are used to set source power saving option Bit: T_ap_opt Description: Source power saving option Data: 0: Enable power saving 1: Normal
Restriction	

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(FE92h): CMD Mode Switch

R/W	Addr	D7	D6	D5	D4	D3	D2	D1	D0	HEX
W	FE92h	CMD_Page[7:0]								00h

Description

This command is used to switch the Manufacture Command Pages and User Commands sets.

CMD_Page[7:0]	Description
00h (default)	User Command Set (UCS = CMD1)
10h	Manufacture Command Set Page Panel ID
12h	Manufacture Command Set Page SID
20h	Manufacture Command Set Page Panel
40h	Manufacture Command Set Page ABH Mode
82h	Manufacture Command Set Page Power
92h	Manufacture Command Set Page SD timing
50h	Manufacture Command Set Page Gamma1
60h	Manufacture Command Set Page Gamma2
30h	Manufacture Command Set Page Gamma3
52h	Manufacture Command Set Page Gamma4
70h	Manufacture Command Set Page GOA Timing 1
F0h	Manufacture Command Set Page GOA Timing 2
42h	Manufacture Command Set Page DBV
22h	Manufacture Command Set Page SES
80h	Manufacture Command Set Page APRC
90h	Manufacture Command Set Page ACL
62h	Manufacture Command Set Page CGM
C2h	Manufacture Command Set Page CGM LUT

Restriction

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(FF92h): Read CMD Status

R/W	Addr	D7	D6	D5	D4	D3	D2	D1	D0	HEX
R	FF92h	CMD_Status[7:0]								00h

Description	This command is used to read the status of Manufacture Command Pages. Please refer to FE00h
Restriction	-

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1.9 MCS: CMD2 Page50, Gamma1 Settings

Instruction	R/W	Addr	D7	D6	D5	D4	D3	D2	D1	D0	HEX
GammaR_1	R/W	0050h	-	-	-	-	-	-	V0R1[9:8]		00h
GammaR_1	R/W	0150h	V0R1[7:0]								00h
GammaR_1	R/W	0250h	-	-	-	-	-	-	V1R1[9:8]		00h
GammaR_1	R/W	0350h	V1R1[7:0]								04h
GammaR_1	R/W	0450h	-	-	-	-	-	-	V2R1[9:8]		00h
GammaR_1	R/W	0550h	V2R1[7:0]								0Ch
GammaR_1	R/W	0650h	-	-	-	-	-	-	V3R1[9:8]		00h
GammaR_1	R/W	0750h	V3R1[7:0]								1Ch
GammaR_1	R/W	0850h	-	-	-	-	-	-	V4R1[9:8]		00h
GammaR_1	R/W	0950h	V4R1[7:0]								2Ch
GammaR_1	R/W	0A50h	-	-	-	-	-	-	V5R1[9:8]		00h
GammaR_1	R/W	0B50h	V5R1[7:0]								3Ch
GammaR_1	R/W	0C50h	-	-	-	-	-	-	V6R1[9:8]		00h
GammaR_1	R/W	0D50h	V6R1[7:0]								4Ch
GammaR_1	R/W	0E50h	-	-	-	-	-	-	V7R1[9:8]		00h
GammaR_1	R/W	0F50h	V7R1[7:0]								5Ch
GammaR_1	R/W	1050h	-	-	-	-	-	-	V8R1[9:8]		00h
GammaR_1	R/W	1150h	V8R1[7:0]								6Ch
GammaR_1	R/W	1250h	-	-	-	-	-	-	V9R1[9:8]		00h
GammaR_1	R/W	1350h	V9R1[7:0]								7Ch
GammaR_1	R/W	1450h	-	-	-	-	-	-	V10R1[9:8]		00h
GammaR_1	R/W	1550h	V10R1[7:0]								8Ch
GammaR_1	R/W	1650h	-	-	-	-	-	-	V11R1[9:8]		00h
GammaR_1	R/W	1750h	V11R1[7:0]								9Ch
GammaR_1	R/W	1850h	-	-	-	-	-	-	V12R1[9:8]		00h
GammaR_1	R/W	1950h	V12R1[7:0]								BCh
GammaR_1	R/W	1A50h	-	-	-	-	-	-	V13R1[9:8]		00h
GammaR_1	R/W	1B50h	V13R1[7:0]								DCh
GammaR_1	R/W	1C50h	-	-	-	-	-	-	V14R1[9:8]		00h
GammaR_1	R/W	1D50h	V14R1[7:0]								FCh
GammaR_1	R/W	1E50h	-	-	-	-	-	-	V15R1[9:8]		01h
GammaR_1	R/W	1F50h	V15R1[7:0]								3Ch
GammaR_1	R/W	2050h	-	-	-	-	-	-	V16R1[9:8]		01h
GammaR_1	R/W	2150h	V16R1[7:0]								7Ch
GammaR_1	R/W	2250h	-	-	-	-	-	-	V17R1[9:8]		01h
GammaR_1	R/W	2350h	V17R1[7:0]								BCh
GammaR_1	R/W	2450h	-	-	-	-	-	-	V18R1[9:8]		01h
GammaR_1	R/W	2550h	V18R1[7:0]								FCh
GammaR_1	R/W	2650h	-	-	-	-	-	-	V19R1[9:8]		02h
GammaR_1	R/W	2750h	V19R1[7:0]								3Ch
GammaR_1	R/W	2850h	-	-	-	-	-	-	V20R1[9:8]		02h
GammaR_1	R/W	2950h	V20R1[7:0]								7Ch
GammaR_1	R/W	2A50h	-	-	-	-	-	-	V21R1[9:8]		02h
GammaR_1	R/W	2B50h	V21R1[7:0]								BCh
GammaR_1	R/W	2D50h	-	-	-	-	-	-	V22R1[9:8]		02h
GammaR_1	R/W	2F50h	V22R1[7:0]								FCh
GammaR_1	R/W	3050h	-	-	-	-	-	-	V23R1[9:8]		03h

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GammaR_1	R/W	3150h	V23R1[7:0]							3Ch
GammaR_1	R/W	3250h	-	-	-	-	-	-	V24R1[9:8]	03h
GammaR_1	R/W	3350h	V24R1[7:0]							7Ch
GammaR_1	R/W	3450h	-	-	-	-	-	-	V25R1[9:8]	03h
GammaR_1	R/W	3550h	V25R1[7:0]							BCh
GammaR_1	R/W	3650h	-	-	-	-	-	-	V26R1[9:8]	03h
GammaR_1	R/W	3750h	V26R1[7:0]							FCh
GammaG_1	R/W	3850h	-	-	-	-	-	-	V0G1[9:8]	00h
GammaG_1	R/W	3950h	V0G1[7:0]							00h
GammaG_1	R/W	3A50h	-	-	-	-	-	-	V1G1[9:8]	00h
GammaG_1	R/W	3B50h	V1G1[7:0]							04h
GammaG_1	R/W	3D50h	-	-	-	-	-	-	V2G1[9:8]	00h
GammaG_1	R/W	3F50h	V2G1[7:0]							0Ch
GammaG_1	R/W	4050h	-	-	-	-	-	-	V3G1[9:8]	00h
GammaG_1	R/W	4150h	V3G1[7:0]							1Ch
GammaG_1	R/W	4250h	-	-	-	-	-	-	V4G1[9:8]	00h
GammaG_1	R/W	4350h	V4G1[7:0]							2Ch
GammaG_1	R/W	4450h	-	-	-	-	-	-	V5G1[9:8]	00h
GammaG_1	R/W	4550h	V5G1[7:0]							3Ch
GammaG_1	R/W	4650h	-	-	-	-	-	-	V6G1[9:8]	00h
GammaG_1	R/W	4750h	V6G1[7:0]							4Ch
GammaG_1	R/W	4850h	-	-	-	-	-	-	V7G1[9:8]	00h
GammaG_1	R/W	4950h	V7G1[7:0]							5Ch
GammaG_1	R/W	4A50h	-	-	-	-	-	-	V8G1[9:8]	00h
GammaG_1	R/W	4B50h	V8G1[7:0]							6Ch
GammaG_1	R/W	4C50h	-	-	-	-	-	-	V9G1[9:8]	00h
GammaG_1	R/W	4D50h	V9G1[7:0]							7Ch
GammaG_1	R/W	4E50h	-	-	-	-	-	-	V10G1[9:8]	00h
GammaG_1	R/W	4F50h	V10G1[7:0]							8Ch
GammaG_1	R/W	5050h	-	-	-	-	-	-	V11G1[9:8]	00h
GammaG_1	R/W	5250h	V11G1[7:0]							9Ch
GammaG_1	R/W	5350h	-	-	-	-	-	-	V12G1[9:8]	00h
GammaG_1	R/W	5450h	V12G1[7:0]							BCh
GammaG_1	R/W	5550h	-	-	-	-	-	-	V13G1[9:8]	00h
GammaG_1	R/W	5650h	V13G1[7:0]							DCh
GammaG_1	R/W	5750h	-	-	-	-	-	-	V14G1[9:8]	00h
GammaG_1	R/W	5850h	V14G1[7:0]							FCh
GammaG_1	R/W	5950h	-	-	-	-	-	-	V15G1[9:8]	01h
GammaG_1	R/W	5A50h	V15G1[7:0]							3Ch
GammaG_1	R/W	5B50h	-	-	-	-	-	-	V16G1[9:8]	01h
GammaG_1	R/W	5C50h	V16G1[7:0]							7Ch
GammaG_1	R/W	5D50h	-	-	-	-	-	-	V17G1[9:8]	01h
GammaG_1	R/W	5E50h	V17G1[7:0]							BCh
GammaG_1	R/W	5F50h	-	-	-	-	-	-	V18G1[9:8]	01h
GammaG_1	R/W	6050h	V18G1[7:0]							FCh
GammaG_1	R/W	6150h	-	-	-	-	-	-	V19G1[9:8]	02h
GammaG_1	R/W	6250h	V19G1[7:0]							3Ch
GammaG_1	R/W	6350h	-	-	-	-	-	-	V20G1[9:8]	02h
GammaG_1	R/W	6450h	V20G1[7:0]							7Ch
GammaG_1	R/W	6550h	-	-	-	-	-	-	V21G1[9:8]	02h
GammaG_1	R/W	6650h	V21G1[7:0]							BCh

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GammaG_1	R/W	6750h	-	-	-	-	-	-	V22G1[9:8]	02h
GammaG_1	R/W	6850h	V22G1[7:0]							FCh
GammaG_1	R/W	6950h	-	-	-	-	-	-	V23G1[9:8]	03h
GammaG_1	R/W	6A50h	V23G1[7:0]							3Ch
GammaG_1	R/W	6B50h	-	-	-	-	-	-	V24G1[9:8]	03h
GammaG_1	R/W	6C50h	V24G1[7:0]							7Ch
GammaG_1	R/W	6D50h	-	-	-	-	-	-	V25G1[9:8]	03h
GammaG_1	R/W	6E50h	V25G1[7:0]							BCh
GammaG_1	R/W	6F50h	-	-	-	-	-	-	V26G1[9:8]	03h
GammaG_1	R/W	7050h	V26G1[7:0]							FCh
GammaB_1	R/W	7150h	-	-	-	-	-	-	V0B1[9:8]	00h
GammaB_1	R/W	7250h	V0B1[7:0]							00h
GammaB_1	R/W	7350h	-	-	-	-	-	-	V1B1[9:8]	00h
GammaB_1	R/W	7450h	V1B1[7:0]							04h
GammaB_1	R/W	7550h	-	-	-	-	-	-	V2B1[9:8]	00h
GammaB_1	R/W	7650h	V2B1[7:0]							0Ch
GammaB_1	R/W	7750h	-	-	-	-	-	-	V3B1[9:8]	00h
GammaB_1	R/W	7850h	V3B1[7:0]							1Ch
GammaB_1	R/W	7950h	-	-	-	-	-	-	V4B1[9:8]	00h
GammaB_1	R/W	7A50h	V4B1[7:0]							2Ch
GammaB_1	R/W	7B50h	-	-	-	-	-	-	V5B1[9:8]	00h
GammaB_1	R/W	7C50h	V5B1[7:0]							3Ch
GammaB_1	R/W	7D50h	-	-	-	-	-	-	V6B1[9:8]	00h
GammaB_1	R/W	7E50h	V6B1[7:0]							4Ch
GammaB_1	R/W	7F50h	-	-	-	-	-	-	V7B1[9:8]	00h
GammaB_1	R/W	8050h	V7B1[7:0]							5Ch
GammaB_1	R/W	8150h	-	-	-	-	-	-	V8B1[9:8]	00h
GammaB_1	R/W	8250h	V8B1[7:0]							6Ch
GammaB_1	R/W	8350h	-	-	-	-	-	-	V9B1[9:8]	00h
GammaB_1	R/W	8450h	V9B1[7:0]							7Ch
GammaB_1	R/W	8550h	-	-	-	-	-	-	V10B1[9:8]	00h
GammaB_1	R/W	8650h	V10B1[7:0]							8Ch
GammaB_1	R/W	8750h	-	-	-	-	-	-	V11B1[9:8]	00h
GammaB_1	R/W	8850h	V11B1[7:0]							9Ch
GammaB_1	R/W	8950h	-	-	-	-	-	-	V12B1[9:8]	00h
GammaB_1	R/W	8A50h	V12B1[7:0]							BCh
GammaB_1	R/W	8B50h	-	-	-	-	-	-	V13B1[9:8]	00h
GammaB_1	R/W	8C50h	V13B1[7:0]							DCh
GammaB_1	R/W	8D50h	-	-	-	-	-	-	V14B1[9:8]	00h
GammaB_1	R/W	8E50h	V14B1[7:0]							FCh
GammaB_1	R/W	8F50h	-	-	-	-	-	-	V15B1[9:8]	01h
GammaB_1	R/W	9050h	V15B1[7:0]							3Ch
GammaB_1	R/W	9150h	-	-	-	-	-	-	V16B1[9:8]	01h
GammaB_1	R/W	9250h	V16B1[7:0]							7Ch
GammaB_1	R/W	9350h	-	-	-	-	-	-	V17B1[9:8]	01h
GammaB_1	R/W	9450h	V17B1[7:0]							BCh
GammaB_1	R/W	9550h	-	-	-	-	-	-	V18B1[9:8]	01h
GammaB_1	R/W	9650h	V18B1[7:0]							FCh
GammaB_1	R/W	9750h	-	-	-	-	-	-	V19B1[9:8]	02h
GammaB_1	R/W	9850h	V19B1[7:0]							3Ch
GammaB_1	R/W	9950h	-	-	-	-	-	-	V20B1[9:8]	02h

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GammaB_1	R/W	9A50h	V20B1[7:0]								7Ch
GammaB_1	R/W	9B50h	-	-	-	-	-	-	V21B1[9:8]		02h
GammaB_1	R/W	9C50h	V21B1[7:0]								BCh
GammaB_1	R/W	9D50h	-	-	-	-	-	-	V22B1[9:8]		02h
GammaB_1	R/W	9E50h	V22B1[7:0]								FCh
GammaB_1	R/W	9F50h	-	-	-	-	-	-	V23B1[9:8]		03h
GammaB_1	R/W	A050h	V23B1[7:0]								3Ch
GammaB_1	R/W	A250h	-	-	-	-	-	-	V24B1[9:8]		03h
GammaB_1	R/W	A350h	V24B1[7:0]								7Ch
GammaB_1	R/W	A450h	-	-	-	-	-	-	V25B1[9:8]		03h
GammaB_1	R/W	A550h	V25B1[7:0]								BCh
GammaB_1	R/W	A650h	-	-	-	-	-	-	V26B1[9:8]		03h
GammaB_1	R/W	A750h	V26B1[7:0]								FCh
VGMP/VGSP	R/W	A950h	VGMPTR1[7:0]								50h
VGMP/VGSP	R/W	AA50h	VGSPTR1[7:0]								18h
VGMP/VGSP	R/W	AB50h	GMA_13P1	-	-	VGSPTR1[8]	-	-	-	VGMPTR1[8]	00h
CMD Mode Switch	W	FE50h	CMD_Page[7:0]								00h
RD CMD Status	R	FF50h	CMD_Status[7:0]								00h

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(0050h~3750h)Gamma 2.2 Corrections Set 1 for Red

R/W	Addr	D7	D6	D5	D4	D3	D2	D1	D0	HEX
	0050h	-	-	-	-	-	-	V0R1[9:8]		00h
	0150h	V0R1[7:0]								00h
	0250h	-	-	-	-	-	-	V1R1[9:8]		00h
	0350h	V1R1[7:0]								04h
	0450h	-	-	-	-	-	-	V2R1[9:8]		00h
	0550h	V2R1[7:0]								0Ch
	0650h	-	-	-	-	-	-	V3R1[9:8]		00h
	0750h	V3R1[7:0]								1Ch
	0850h	-	-	-	-	-	-	V4R1[9:8]		00h
	0950h	V4R1[7:0]								2Ch
	0A50h	-	-	-	-	-	-	V5R1[9:8]		00h
	0B50h	V5R1[7:0]								3Ch
	0C50h	-	-	-	-	-	-	V6R1[9:8]		00h
	0D50h	V6R1[7:0]								4Ch
	0E50h	-	-	-	-	-	-	V7R1[9:8]		00h
	0F50h	V7R1[7:0]								5Ch
	1050h	-	-	-	-	-	-	V8R1[9:8]		00h
	1150h	V8R1[7:0]								6Ch
R/W	1250h	-	-	-	-	-	-	V9R1[9:8]		00h
	1350h	V9R1[7:0]								7Ch
	1450h	-	-	-	-	-	-	V10R1[9:8]		00h
	1550h	V10R1[7:0]								8Ch
	1650h	-	-	-	-	-	-	V11R1[9:8]		00h
	1750h	V11R1[7:0]								9Ch
	1850h	-	-	-	-	-	-	V12R1[9:8]		00h
	1950h	V12R1[7:0]								BCh
	1A50h	-	-	-	-	-	-	V13R1[9:8]		00h
	1B50h	V13R1[7:0]								DCh
	1C50h	-	-	-	-	-	-	V14R1[9:8]		00h
	1D50h	V14R1[7:0]								FCh
	1E50h	-	-	-	-	-	-	V15R1[9:8]		01h
	1F50h	V15R1[7:0]								3Ch
	2050h	-	-	-	-	-	-	V16R1[9:8]		01h
	2150h	V16R1[7:0]								7Ch
	2250h	-	-	-	-	-	-	V17R1[9:8]		01h
	2350h	V17R1[7:0]								BCh
	2450h	-	-	-	-	-	-	V18R1[9:8]		01h

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	2550h	V18R1[7:0]							FCh
	2650h	-	-	-	-	-	-	V19R1[9:8]	02h
	2750h	V19R1[7:0]							3Ch
	2850h	-	-	-	-	-	-	V20R1[9:8]	02h
	2950h	V20R1[7:0]							7Ch
	2A50h	-	-	-	-	-	-	V21R1[9:8]	02h
	2B50h	V21R1[7:0]							BCh
	2D50h	-	-	-	-	-	-	V22R1[9:8]	02h
	2F50h	V22R1[7:0]							FCh
	3050h	-	-	-	-	-	-	V23R1[9:8]	03h
	3150h	V23R1[7:0]							3Ch
	3250h	-	-	-	-	-	-	V24R1[9:8]	03h
	3350h	V24R1[7:0]							7Ch
	3450h	-	-	-	-	-	-	V25R1[9:8]	03h
	3550h	V25R1[7:0]							BCh
	3650h	-	-	-	-	-	-	V26R1[9:8]	03h
	3750h	V26R1[7:0]							FCh

Description	This command is used to adjust the gamma 2.2 correction for the red under normal display mode. For rb_GMA_13P1=0 Adjust R_0(darkest) via V0R1 Adjust R_1 via V1R1 Adjust R_3 via V2R1 Adjust R_7 via V3R1 Adjust R_11 via V4R1 Adjust R_15 via V5R1 Adjust R_19 via V6R1 Adjust R_23 via V7R1 Adjust R_27 via V8R1 Adjust R_31 via V9R1 Adjust R_35 via V10R1 Adjust R_39 via V11R1 Adjust R_47 via V12R1 Adjust R_55 via V13R1 Adjust R_63 via V14R1 Adjust R_79 via V15R1 Adjust R_95 via V16R1 Adjust R_111 via V17R1 Adjust R_127 via V18R1 Adjust R_143 via V19R1 Adjust R_159 via V20R1 Adjust R_175 via V21R1 Adjust R_191 via V22R1 Adjust R_207 via V23R1 Adjust R_223 via V24R1 Adjust R_239 via V25R1 Adjust R_255(brightest) via V26R1

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	For rb_GMA_13P1=1 Adjust R_0(darkest) via V0R1 Adjust R_1 via V1R1 Adjust R_3 via V2R1 Adjust R_7 via V3R1 Adjust R_11 via V4R1 Adjust R_15 via V5R1 Adjust R_31 via V9R1 Adjust R_63 via V14R1 Adjust R_95 via V16R1 Adjust R_127 via V18R1 Adjust R_159 via V20R1 Adjust R_191 via V22R1 Adjust R_255(brightest) via V26R1
Restriction	Set V0R1[9:0] < V1R1[9:0] < V2R1[9:0] < ... < V25R1[9:0] < V26R1[9:0], or V0R1[9:0] > V1R1[9:0] > V2R1[9:0] > ... > V25R1[9:0] > V26R1[9:0]

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(3850h~7050h) Gamma 2.2 Corrections Set 1 for Green

R/W	Addr	D7	D6	D5	D4	D3	D2	D1	D0	HEX
	3850h	-	-	-	-	-	-	V0G1[9:8]		00h
	3950h	V0G1[7:0]								00h
	3A50h	-	-	-	-	-	-	V1G1[9:8]		00h
	3B50h	V1G1[7:0]								04h
	3D50h	-	-	-	-	-	-	V2G1[9:8]		00h
	3F50h	V2G1[7:0]								0Ch
	4050h	-	-	-	-	-	-	V3G1[9:8]		00h
	4150h	V3G1[7:0]								1Ch
	4250h	-	-	-	-	-	-	V4G1[9:8]		00h
	4350h	V4G1[7:0]								2Ch
	4450h	-	-	-	-	-	-	V5G1[9:8]		00h
	4550h	V5G1[7:0]								3Ch
	4650h	-	-	-	-	-	-	V6G1[9:8]		00h
	4750h	V6G1[7:0]								4Ch
	4850h	-	-	-	-	-	-	V7G1[9:8]		00h
	4950h	V7G1[7:0]								5Ch
	4A50h	-	-	-	-	-	-	V8G1[9:8]		00h
	4B50h	V8G1[7:0]								6Ch
R/W	4C50h	-	-	-	-	-	-	V9G1[9:8]		00h
	4D50h	V9G1[7:0]								7Ch
	4E50h	-	-	-	-	-	-	V10G1[9:8]		00h
	4F50h	V10G1[7:0]								8Ch
	5050h	-	-	-	-	-	-	V11G1[9:8]		00h
	5250h	V11G1[7:0]								9Ch
	5350h	-	-	-	-	-	-	V12G1[9:8]		00h
	5450h	V12G1[7:0]								BCh
	5550h	-	-	-	-	-	-	V13G1[9:8]		00h
	5650h	V13G1[7:0]								DCh
	5750h	-	-	-	-	-	-	V14G1[9:8]		00h
	5850h	V14G1[7:0]								FCh
	5950h	-	-	-	-	-	-	V15G1[9:8]		01h
	5A50h	V15G1[7:0]								3Ch
	5B50h	-	-	-	-	-	-	V16G1[9:8]		01h
	5C50h	V16G1[7:0]								7Ch
	5D50h	-	-	-	-	-	-	V17G1[9:8]		01h
	5E50h	V17G1[7:0]								BCh
	5F50h	-	-	-	-	-	-	V18G1[9:8]		01h

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	6050h	V18G1[7:0]							FCh
	6150h	-	-	-	-	-	-	V19G1[9:8]	02h
	6250h	V19G1[7:0]							3Ch
	6350h	-	-	-	-	-	-	V20G1[9:8]	02h
	6450h	V20G1[7:0]							7Ch
	6550h	-	-	-	-	-	-	V21G1[9:8]	02h
	6650h	V21G1[7:0]							BCh
	6750h	-	-	-	-	-	-	V22G1[9:8]	02h
	6850h	V22G1[7:0]							FCh
	6950h	-	-	-	-	-	-	V23G1[9:8]	03h
	6A50h	V23G1[7:0]							3Ch
	6B50h	-	-	-	-	-	-	V24G1[9:8]	03h
	6C50h	V24G1[7:0]							7Ch
	6D50h	-	-	-	-	-	-	V25G1[9:8]	03h
	6E50h	V25G1[7:0]							BCh
	6F50h	-	-	-	-	-	-	V26G1[9:8]	03h
	7050h	V26G1[7:0]							FCh

Description	This command is used to adjust the gamma 2.2 correction for the red under normal display mode. For rb_GMA_13P1=0 Adjust G_0(darkest) via V0G1 Adjust G_1 via V1G1 Adjust G_3 via V2G1 Adjust G_7 via V3G1 Adjust G_11 via V4G1 Adjust G_15 via V5G1 Adjust G_19 via V6G1 Adjust G_23 via V7G1 Adjust G_27 via V8G1 Adjust G_31 via V9G1 Adjust G_35 via V10G1 Adjust G_39 via V11G1 Adjust G_47 via V12G1 Adjust G_55 via V13G1 Adjust G_63 via V14G1 Adjust G_79 via V15G1 Adjust G_95 via V16G1 Adjust G_111 via V17G1 Adjust G_127 via V18G1 Adjust G_143 via V19G1 Adjust G_159 via V20G1 Adjust G_175 via V21G1 Adjust G_191 via V22G1 Adjust G_207 via V23G1 Adjust G_223 via V24G1 Adjust G_239 via V25G1 Adjust G_255(brightest) via V26G1 For rb_GMA_13P1=1

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	Adjust G_0(darkest) via V0G1 Adjust G_1 via V1G1 Adjust G_3 via V2G1 Adjust G_7 via V3G1 Adjust G_11 via V4G1 Adjust G_15 via V5G1 Adjust G_31 via V9G1 Adjust G_63 via V14G1 Adjust G_95 via V16G1 Adjust G_127 via V18G1 Adjust G_159 via V20G1 Adjust G_191 via V22G1 Adjust G_255(brightest) via V26G1
Restriction	Set V0G1[9:0] < V1G1[9:0] < V2G1[9:0] < ... < V25G1[9:0] < V26G1[9:0], or V0G1[9:0] > V1G1[9:0] > V2G1[9:0] > ... > V25G1[9:0] > V26G1[9:0]

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(7150h~A750h) Gamma 2.2 Corrections Set 1 for Blue

R/W	Addr	D7	D6	D5	D4	D3	D2	D1	D0	HEX
R/W	7150h	-	-	-	-	-	-	V0B1[9:8]		00h
	7250h	V0B1[7:0]								00h
	7350h	-	-	-	-	-	-	V1B1[9:8]		00h
	7450h	V1B1[7:0]								04h
	7550h	-	-	-	-	-	-	V2B1[9:8]		00h
	7650h	V2B1[7:0]								0Ch
	7750h	-	-	-	-	-	-	V3B1[9:8]		00h
	7850h	V3B1[7:0]								1Ch
	7950h	-	-	-	-	-	-	V4B1[9:8]		00h
	7A50h	V4B1[7:0]								2Ch
	7B50h	-	-	-	-	-	-	V5B1[9:8]		00h
	7C50h	V5B1[7:0]								3Ch
	7D50h	-	-	-	-	-	-	V6B1[9:8]		00h
	7E50h	V6B1[7:0]								4Ch
	7F50h	-	-	-	-	-	-	V7B1[9:8]		00h
	8050h	V7B1[7:0]								5Ch
	8150h	-	-	-	-	-	-	V8B1[9:8]		00h
	8250h	V8B1[7:0]								6Ch
	8350h	-	-	-	-	-	-	V9B1[9:8]		00h
	8450h	V9B1[7:0]								7Ch
	8550h	-	-	-	-	-	-	V10B1[9:8]		00h
	8650h	V10B1[7:0]								8Ch
	8750h	-	-	-	-	-	-	V11B1[9:8]		00h
	8850h	V11B1[7:0]								9Ch
	8950h	-	-	-	-	-	-	V12B1[9:8]		00h
	8A50h	V12B1[7:0]								BCh
	8B50h	-	-	-	-	-	-	V13B1[9:8]		00h
	8C50h	V13B1[7:0]								DCh
	8D50h	-	-	-	-	-	-	V14B1[9:8]		00h
	8E50h	V14B1[7:0]								FCh
	8F50h	-	-	-	-	-	-	V15B1[9:8]		01h
	9050h	V15B1[7:0]								3Ch
	9150h	-	-	-	-	-	-	V16B1[9:8]		01h
	9250h	V16B1[7:0]								7Ch
	9350h	-	-	-	-	-	-	V17B1[9:8]		01h
	9450h	V17B1[7:0]								BCh
	9550h	-	-	-	-	-	-	V18B1[9:8]		01h
	9650h	V18B1[7:0]								FCh
	9750h	-	-	-	-	-	-	V19B1[9:8]		02h
	9850h	V19B1[7:0]								3Ch
	9950h	-	-	-	-	-	-	V20B1[9:8]		02h
	9A50h	V20B1[7:0]								7Ch
	9B50h	-	-	-	-	-	-	V21B1[9:8]		02h
	9C50h	V21B1[7:0]								BCh
	9D50h	-	-	-	-	-	-	V22B1[9:8]		02h
	9E50h	V22B1[7:0]								FCh
	9F50h	-	-	-	-	-	-	V23B1[9:8]		03h
	A050h	V23B1[7:0]								3Ch
	A250h	-	-	-	-	-	-	V24B1[9:8]		03h
	A350h	V24B1[7:0]								7Ch
	A450h	-	-	-	-	-	-	V25B1[9:8]		03h
	A550h	V25B1[7:0]								BCh
	A650h	-	-	-	-	-	-	V26B1[9:8]		03h

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	A750h	V26B1[7:0]	FCh

Description	This command is used to adjust the gamma 2.2 correction for the red under normal display mode. For rb_GMA_13P1=0 Adjust B_0(darkest) via V0B1 Adjust B_1 via V1B1 Adjust B_3 via V2B1 Adjust B_7 via V3B1 Adjust B_11 via V4B1 Adjust B_15 via V5B1 Adjust B_19 via V6B1 Adjust B_23 via V7B1 Adjust B_27 via V8B1 Adjust B_31 via V9B1 Adjust B_35 via V10B1 Adjust B_39 via V11B1 Adjust B_47 via V12B1 Adjust B_55 via V13B1 Adjust B_63 via V14B1 Adjust B_79 via V15B1 Adjust B_95 via V16B1 Adjust B_111 via V17B1 Adjust B_127 via V18B1 Adjust B_143 via V19B1 Adjust B_159 via V20B1 Adjust B_175 via V21B1 Adjust B_191 via V22B1 Adjust B_207 via V23B1 Adjust B_223 via V24B1 Adjust B_239 via V25B1 Adjust B_255(brightest) via V26B1 For rb_GMA_13P1=1 Adjust B_0(darkest) via V0B1 Adjust B_1 via V1B1 Adjust B_3 via V2B1 Adjust B_7 via V3B1 Adjust B_11 via V4B1 Adjust B_15 via V5B1 Adjust B_31 via V9B1 Adjust B_63 via V14B1 Adjust B_95 via V16B1 Adjust B_127 via V18B1 Adjust B_159 via V20B1 Adjust B_191 via V22B1 Adjust B_255(brightest) via V26B1
Restriction	Set V0B1[9:0] < V1B1[9:0] < V2B1[9:0] < ... < V25B1[9:0] < V26B1[9:0], or V0B1[9:0] > V1B1[9:0] > V2B1[9:0] > ... > V25B1[9:0] > V26B1[9:0]

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(A950h~AB50h) VGMP/VGSP Control

R/W	Addr	D7	D6	D5	D4	D3	D2	D1	D0	HEX
R/W	A950h	VGMPTR1[7:0]								50h
R/W	AA50h	VGSPTR1[7:0]								18h
R/W	AB50h	rb_GMA_13P1	-	-	VGSPTR1[8]	-	-	-	VGMPTR1[8]	00h

Description

This command is for VGMP output level selection.

Bit	Value	VGMP Output level
VGMPTR1[8:0]	000h	2.0000V
	001h	2.0125V
	:	0.0125V / Step
	050h	3.0000V
	:	0.0125V / Step
	157h	6.2875V
	158h	6.3000V
	159h~1FFh	Reserved

This command is for VGSP output level selection.

Bit	Value	VGSP Output level
VGSPTR1[8:0]	000h	0.0000V
	001h	0.2125V
	:	0.0125V / Step
	005h	0.2625V
	:	0.0125V / Step
	158h	4.5000V
	159h~1FFh	Reserved
	000h	0.0000V

Restriction

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(FE50h): CMD Mode Switch

R/W	Addr	D7	D6	D5	D4	D3	D2	D1	D0	HEX
W	FE50h	CMD_Page[7:0]								00h

Description

This command is used to switch the Manufacture Command Pages and User Commands sets.

CMD_Page[7:0]	Description
00h (default)	User Command Set (UCS = CMD1)
10h	Manufacture Command Set Page Panel ID
12h	Manufacture Command Set Page SID
20h	Manufacture Command Set Page Panel
40h	Manufacture Command Set Page ABH Mode
82h	Manufacture Command Set Page Power
92h	Manufacture Command Set Page SD timing
50h	Manufacture Command Set Page Gamma1
60h	Manufacture Command Set Page Gamma2
30h	Manufacture Command Set Page Gamma3
52h	Manufacture Command Set Page Gamma4
70h	Manufacture Command Set Page GOA Timing 1
F0h	Manufacture Command Set Page GOA Timing 2
42h	Manufacture Command Set Page DBV
22h	Manufacture Command Set Page SES
80h	Manufacture Command Set Page APRC
90h	Manufacture Command Set Page ACL
62h	Manufacture Command Set Page CGM
C2h	Manufacture Command Set Page CGM LUT

Restriction

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(FF50h): Read CMD Status

R/W	Addr	D7	D6	D5	D4	D3	D2	D1	D0	HEX
R	FF50h	CMD_Status[7:0]								00h

Description	This command is used to read the status of Manufacture Command Pages. Please refer to FE00h
Restriction	-

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1.10MCS: CMD2 Page60, Gamma2 Settings

Instruction	R/W	Addr	D7	D6	D5	D4	D3	D2	D1	D0	HEX
GammaR_2	R/W	0060h	-	-	-	-	-	-	V0R2[9:8]		00h
GammaR_2	R/W	0160h	V0R2[7:0]								00h
GammaR_2	R/W	0260h	-	-	-	-	-	-	V1R2[9:8]		00h
GammaR_2	R/W	0360h	V1R2[7:0]								04h
GammaR_2	R/W	0460h	-	-	-	-	-	-	V2R2[9:8]		00h
GammaR_2	R/W	0560h	V2R2[7:0]								0Ch
GammaR_2	R/W	0660h	-	-	-	-	-	-	V3R2[9:8]		00h
GammaR_2	R/W	0760h	V3R2[7:0]								1Ch
GammaR_2	R/W	0860h	-	-	-	-	-	-	V4R2[9:8]		00h
GammaR_2	R/W	0960h	V4R2[7:0]								2Ch
GammaR_2	R/W	0A60h	-	-	-	-	-	-	V5R2[9:8]		00h
GammaR_2	R/W	0B60h	V5R2[7:0]								3Ch
GammaR_2	R/W	0C60h	-	-	-	-	-	-	V6R2[9:8]		00h
GammaR_2	R/W	0D60h	V6R2[7:0]								4Ch
GammaR_2	R/W	0E60h	-	-	-	-	-	-	V7R2[9:8]		00h
GammaR_2	R/W	0F60h	V7R2[7:0]								5Ch
GammaR_2	R/W	1060h	-	-	-	-	-	-	V8R2[9:8]		00h
GammaR_2	R/W	1160h	V8R2[7:0]								6Ch
GammaR_2	R/W	1260h	-	-	-	-	-	-	V9R2[9:8]		00h
GammaR_2	R/W	1360h	V9R2[7:0]								7Ch
GammaR_2	R/W	1460h	-	-	-	-	-	-	V10R2[9:8]		00h
GammaR_2	R/W	1560h	V10R2[7:0]								8Ch
GammaR_2	R/W	1660h	-	-	-	-	-	-	V11R2[9:8]		00h
GammaR_2	R/W	1760h	V11R2[7:0]								9Ch
GammaR_2	R/W	1860h	-	-	-	-	-	-	V12R2[9:8]		00h
GammaR_2	R/W	1960h	V12R2[7:0]								BCh
GammaR_2	R/W	1A60h	-	-	-	-	-	-	V13R2[9:8]		00h
GammaR_2	R/W	1B60h	V13R2[7:0]								DCh
GammaR_2	R/W	1C60h	-	-	-	-	-	-	V14R2[9:8]		00h
GammaR_2	R/W	1D60h	V14R2[7:0]								FCh
GammaR_2	R/W	1E60h	-	-	-	-	-	-	V15R2[9:8]		01h
GammaR_2	R/W	1F60h	V15R2[7:0]								3Ch
GammaR_2	R/W	2060h	-	-	-	-	-	-	V16R2[9:8]		01h
GammaR_2	R/W	2160h	V16R2[7:0]								7Ch
GammaR_2	R/W	2260h	-	-	-	-	-	-	V17R2[9:8]		01h
GammaR_2	R/W	2360h	V17R2[7:0]								BCh
GammaR_2	R/W	2460h	-	-	-	-	-	-	V18R2[9:8]		01h
GammaR_2	R/W	2560h	V18R2[7:0]								FCh
GammaR_2	R/W	2660h	-	-	-	-	-	-	V19R2[9:8]		02h
GammaR_2	R/W	2760h	V19R2[7:0]								3Ch
GammaR_2	R/W	2860h	-	-	-	-	-	-	V20R2[9:8]		02h
GammaR_2	R/W	2960h	V20R2[7:0]								7Ch
GammaR_2	R/W	2A60h	-	-	-	-	-	-	V21R2[9:8]		02h
GammaR_2	R/W	2B60h	V21R2[7:0]								BCh
GammaR_2	R/W	2D60h	-	-	-	-	-	-	V22R2[9:8]		02h
GammaR_2	R/W	2F60h	V22R2[7:0]								FCh
GammaR_2	R/W	3060h	-	-	-	-	-	-	V23R2[9:8]		03h

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GammaR_2	R/W	3160h	V23R2[7:0]							3Ch
GammaR_2	R/W	3260h	-	-	-	-	-	-	V24R2[9:8]	03h
GammaR_2	R/W	3360h	V24R2[7:0]							7Ch
GammaR_2	R/W	3460h	-	-	-	-	-	-	V25R2[9:8]	03h
GammaR_2	R/W	3560h	V25R2[7:0]							BCh
GammaR_2	R/W	3660h	-	-	-	-	-	-	V26R2[9:8]	03h
GammaR_2	R/W	3760h	V26R2[7:0]							FCh
GammaG_2	R/W	3860h	-	-	-	-	-	-	V0G2[9:8]	00h
GammaG_2	R/W	3960h	V0G2[7:0]							00h
GammaG_2	R/W	3A60h	-	-	-	-	-	-	V1G2[9:8]	00h
GammaG_2	R/W	3B60h	V1G2[7:0]							04h
GammaG_2	R/W	3D60h	-	-	-	-	-	-	V2G2[9:8]	00h
GammaG_2	R/W	3F60h	V2G2[7:0]							0Ch
GammaG_2	R/W	4060h	-	-	-	-	-	-	V3G2[9:8]	00h
GammaG_2	R/W	4160h	V3G2[7:0]							1Ch
GammaG_2	R/W	4260h	-	-	-	-	-	-	V4G2[9:8]	00h
GammaG_2	R/W	4360h	V4G2[7:0]							2Ch
GammaG_2	R/W	4460h	-	-	-	-	-	-	V5G2[9:8]	00h
GammaG_2	R/W	4560h	V5G2[7:0]							3Ch
GammaG_2	R/W	4660h	-	-	-	-	-	-	V6G2[9:8]	00h
GammaG_2	R/W	4760h	V6G2[7:0]							4Ch
GammaG_2	R/W	4860h	-	-	-	-	-	-	V7G2[9:8]	00h
GammaG_2	R/W	4960h	V7G2[7:0]							5Ch
GammaG_2	R/W	4A60h	-	-	-	-	-	-	V8G2[9:8]	00h
GammaG_2	R/W	4B60h	V8G2[7:0]							6Ch
GammaG_2	R/W	4C60h	-	-	-	-	-	-	V9G2[9:8]	00h
GammaG_2	R/W	4D60h	V9G2[7:0]							7Ch
GammaG_2	R/W	4E60h	-	-	-	-	-	-	V10G2[9:8]	00h
GammaG_2	R/W	4F60h	V10G2[7:0]							8Ch
GammaG_2	R/W	5060h	-	-	-	-	-	-	V11G2[9:8]	00h
GammaG_2	R/W	5260h	V11G2[7:0]							9Ch
GammaG_2	R/W	5360h	-	-	-	-	-	-	V12G2[9:8]	00h
GammaG_2	R/W	5460h	V12G2[7:0]							BCh
GammaG_2	R/W	5560h	-	-	-	-	-	-	V13G2[9:8]	00h
GammaG_2	R/W	5660h	V13G2[7:0]							DCh
GammaG_2	R/W	5760h	-	-	-	-	-	-	V14G2[9:8]	00h
GammaG_2	R/W	5860h	V14G2[7:0]							FCh
GammaG_2	R/W	5960h	-	-	-	-	-	-	V15G2[9:8]	01h
GammaG_2	R/W	5A60h	V15G2[7:0]							3Ch
GammaG_2	R/W	5B60h	-	-	-	-	-	-	V16G2[9:8]	01h
GammaG_2	R/W	5C60h	V16G2[7:0]							7Ch
GammaG_2	R/W	5D60h	-	-	-	-	-	-	V17G2[9:8]	01h
GammaG_2	R/W	5E60h	V17G2[7:0]							BCh
GammaG_2	R/W	5F60h	-	-	-	-	-	-	V18G2[9:8]	01h
GammaG_2	R/W	6060h	V18G2[7:0]							FCh
GammaG_2	R/W	6160h	-	-	-	-	-	-	V19G2[9:8]	02h
GammaG_2	R/W	6260h	V19G2[7:0]							3Ch
GammaG_2	R/W	6360h	-	-	-	-	-	-	V20G2[9:8]	02h
GammaG_2	R/W	6460h	V20G2[7:0]							7Ch
GammaG_2	R/W	6560h	-	-	-	-	-	-	V21G2[9:8]	02h
GammaG_2	R/W	6660h	V21G2[7:0]							BCh

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GammaG_2	R/W	6760h	-	-	-	-	-	-	V22G2[9:8]	02h
GammaG_2	R/W	6860h	V22G2[7:0]							FCh
GammaG_2	R/W	6960h	-	-	-	-	-	-	V23G2[9:8]	03h
GammaG_2	R/W	6A60h	V23G2[7:0]							3Ch
GammaG_2	R/W	6B60h	-	-	-	-	-	-	V24G2[9:8]	03h
GammaG_2	R/W	6C60h	V24G2[7:0]							7Ch
GammaG_2	R/W	6D60h	-	-	-	-	-	-	V25G2[9:8]	03h
GammaG_2	R/W	6E60h	V25G2[7:0]							BCh
GammaG_2	R/W	6F60h	-	-	-	-	-	-	V26G2[9:8]	03h
GammaG_2	R/W	7060h	V26G2[7:0]							FCh
GammaB_2	R/W	7160h	-	-	-	-	-	-	V0B2[9:8]	00h
GammaB_2	R/W	7260h	V0B2[7:0]							00h
GammaB_2	R/W	7360h	-	-	-	-	-	-	V1B2[9:8]	00h
GammaB_2	R/W	7460h	V1B2[7:0]							04h
GammaB_2	R/W	7560h	-	-	-	-	-	-	V2B2[9:8]	00h
GammaB_2	R/W	7660h	V2B2[7:0]							0Ch
GammaB_2	R/W	7760h	-	-	-	-	-	-	V3B2[9:8]	00h
GammaB_2	R/W	7860h	V3B2[7:0]							1Ch
GammaB_2	R/W	7960h	-	-	-	-	-	-	V4B2[9:8]	00h
GammaB_2	R/W	7A60h	V4B2[7:0]							2Ch
GammaB_2	R/W	7B60h	-	-	-	-	-	-	V5B2[9:8]	00h
GammaB_2	R/W	7C60h	V5B2[7:0]							3Ch
GammaB_2	R/W	7D60h	-	-	-	-	-	-	V6B2[9:8]	00h
GammaB_2	R/W	7E60h	V6B2[7:0]							4Ch
GammaB_2	R/W	7F60h	-	-	-	-	-	-	V7B2[9:8]	00h
GammaB_2	R/W	8060h	V7B2[7:0]							5Ch
GammaB_2	R/W	8160h	-	-	-	-	-	-	V8B2[9:8]	00h
GammaB_2	R/W	8260h	V8B2[7:0]							6Ch
GammaB_2	R/W	8360h	-	-	-	-	-	-	V9B2[9:8]	00h
GammaB_2	R/W	8460h	V9B2[7:0]							7Ch
GammaB_2	R/W	8560h	-	-	-	-	-	-	V10B2[9:8]	00h
GammaB_2	R/W	8660h	V10B2[7:0]							8Ch
GammaB_2	R/W	8760h	-	-	-	-	-	-	V11B2[9:8]	00h
GammaB_2	R/W	8860h	V11B2[7:0]							9Ch
GammaB_2	R/W	8960h	-	-	-	-	-	-	V12B2[9:8]	00h
GammaB_2	R/W	8A60h	V12B2[7:0]							BCh
GammaB_2	R/W	8B60h	-	-	-	-	-	-	V13B2[9:8]	00h
GammaB_2	R/W	8C60h	V13B2[7:0]							DCh
GammaB_2	R/W	8D60h	-	-	-	-	-	-	V14B2[9:8]	00h
GammaB_2	R/W	8E60h	V14B2[7:0]							FCh
GammaB_2	R/W	8F60h	-	-	-	-	-	-	V15B2[9:8]	01h
GammaB_2	R/W	9060h	V15B2[7:0]							3Ch
GammaB_2	R/W	9160h	-	-	-	-	-	-	V16B2[9:8]	01h
GammaB_2	R/W	9260h	V16B2[7:0]							7Ch
GammaB_2	R/W	9360h	-	-	-	-	-	-	V17B2[9:8]	01h
GammaB_2	R/W	9460h	V17B2[7:0]							BCh
GammaB_2	R/W	9560h	-	-	-	-	-	-	V18B2[9:8]	01h
GammaB_2	R/W	9660h	V18B2[7:0]							FCh
GammaB_2	R/W	9760h	-	-	-	-	-	-	V19B2[9:8]	02h
GammaB_2	R/W	9860h	V19B2[7:0]							3Ch
GammaB_2	R/W	9960h	-	-	-	-	-	-	V20B2[9:8]	02h

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GammaB_2	R/W	9A60h	V20B2[7:0]								7Ch
GammaB_2	R/W	9B60h	-	-	-	-	-	-	V21B2[9:8]		02h
GammaB_2	R/W	9C60h	V21B2[7:0]								BCh
GammaB_2	R/W	9D60h	-	-	-	-	-	-	V22B2[9:8]		02h
GammaB_2	R/W	9E60h	V22B2[7:0]								FCh
GammaB_2	R/W	9F60h	-	-	-	-	-	-	V23B2[9:8]		03h
GammaB_2	R/W	A060h	V23B2[7:0]								3Ch
GammaB_2	R/W	A260h	-	-	-	-	-	-	V24B2[9:8]		03h
GammaB_2	R/W	A360h	V24B2[7:0]								7Ch
GammaB_2	R/W	A460h	-	-	-	-	-	-	V25B2[9:8]		03h
GammaB_2	R/W	A560h	V25B2[7:0]								BCh
GammaB_2	R/W	A660h	-	-	-	-	-	-	V26B2[9:8]		03h
GammaB_2	R/W	A760h	V26B2[7:0]								FCh
VGMP/VGSP	R/W	A960h	VGMPTR2[7:0]								50h
VGMP/VGSP	R/W	AA60h	VGSPTR2[7:0]								18h
VGMP/VGSP	R/W	AB60h	GMA_13P2	-	-	VGSPTR2[8]	-	-	-	VGMPTR2[8]	00h
CMD Mode Switch	W	FE60h	CMD_Page[7:0]								00h
RD CMD Status	R	FF60h	CMD_Status[7:0]								00h

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(0060h~3760h)Gamma 2.2 Corrections Set 2 for Red

R/W	Addr	D7	D6	D5	D4	D3	D2	D1	D0	HEX
R/W	0060h	-	-	-	-	-	-	V0R2[9:8]		00h
	0160h	V0R2[7:0]								00h
	0260h	-	-	-	-	-	-	V1R2[9:8]		00h
	0360h	V1R2[7:0]								04h
	0460h	-	-	-	-	-	-	V2R2[9:8]		00h
	0560h	V2R2[7:0]								0Ch
	0660h	-	-	-	-	-	-	V3R2[9:8]		00h
	0760h	V3R2[7:0]								1Ch
	0860h	-	-	-	-	-	-	V4R2[9:8]		00h
	0960h	V4R2[7:0]								2Ch
	0A60h	-	-	-	-	-	-	V5R2[9:8]		00h
	0B60h	V5R2[7:0]								3Ch
	0C60h	-	-	-	-	-	-	V6R2[9:8]		00h
	0D60h	V6R2[7:0]								4Ch
	0E60h	-	-	-	-	-	-	V7R2[9:8]		00h
	0F60h	V7R2[7:0]								5Ch
	1060h	-	-	-	-	-	-	V8R2[9:8]		00h
	1160h	V8R2[7:0]								6Ch
	1260h	-	-	-	-	-	-	V9R2[9:8]		00h
	1360h	V9R2[7:0]								7Ch
	1460h	-	-	-	-	-	-	V10R2[9:8]		00h
	1560h	V10R2[7:0]								8Ch
	1660h	-	-	-	-	-	-	V11R2[9:8]		00h
	1760h	V11R2[7:0]								9Ch
	1860h	-	-	-	-	-	-	V12R2[9:8]		00h
	1960h	V12R2[7:0]								BCh
	1A60h	-	-	-	-	-	-	V13R2[9:8]		00h
	1B60h	V13R2[7:0]								DCh
	1C60h	-	-	-	-	-	-	V14R2[9:8]		00h
	1D60h	V14R2[7:0]								FCh
	1E60h	-	-	-	-	-	-	V15R2[9:8]		01h
	1F60h	V15R2[7:0]								3Ch
	2060h	-	-	-	-	-	-	V16R2[9:8]		01h
	2160h	V16R2[7:0]								7Ch
	2260h	-	-	-	-	-	-	V17R2[9:8]		01h
	2360h	V17R2[7:0]								BCh
	2460h	-	-	-	-	-	-	V18R2[9:8]		01h
	2560h	V18R2[7:0]								FCh
	2660h	-	-	-	-	-	-	V19R2[9:8]		02h
	2760h	V19R2[7:0]								3Ch
	2860h	-	-	-	-	-	-	V20R2[9:8]		02h
	2960h	V20R2[7:0]								7Ch
	2A60h	-	-	-	-	-	-	V21R2[9:8]		02h
	2B60h	V21R2[7:0]								BCh
	2D60h	-	-	-	-	-	-	V22R2[9:8]		02h
	2F60h	V22R2[7:0]								FCh
	3060h	-	-	-	-	-	-	V23R2[9:8]		03h
	3160h	V23R2[7:0]								3Ch
	3260h	-	-	-	-	-	-	V24R2[9:8]		03h
	3360h	V24R2[7:0]								7Ch
	3460h	-	-	-	-	-	-	V25R2[9:8]		03h
	3560h	V25R2[7:0]								BCh
	3660h	-	-	-	-	-	-	V26R2[9:8]		03h

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	3760h	V26R2[7:0]	FCh

Description	This command is used to adjust the gamma 2.2 correction for the red under normal display mode. For rb_GMA_13P1=0 Adjust R_0(darkest) via V0R2 Adjust R_1 via V1R2 Adjust R_3 via V2R2 Adjust R_7 via V3R2 Adjust R_11 via V4R2 Adjust R_15 via V5R2 Adjust R_19 via V6R2 Adjust R_23 via V7R2 Adjust R_27 via V8R2 Adjust R_31 via V9R2 Adjust R_35 via V10R2 Adjust R_39 via V11R2 Adjust R_47 via V12R2 Adjust R_55 via V13R2 Adjust R_63 via V14R2 Adjust R_79 via V15R2 Adjust R_95 via V16R2 Adjust R_111 via V17R2 Adjust R_127 via V18R2 Adjust R_143 via V19R2 Adjust R_159 via V20R2 Adjust R_175 via V21R2 Adjust R_191 via V22R2 Adjust R_207 via V23R2 Adjust R_223 via V24R2 Adjust R_239 via V25R2 Adjust R_255(brightest) via V26R2 For rb_GMA_13P1=1 Adjust R_0(darkest) via V0R2 Adjust R_1 via V1R2 Adjust R_3 via V2R2 Adjust R_7 via V3R2 Adjust R_11 via V4R2 Adjust R_15 via V5R2 Adjust R_31 via V9R2 Adjust R_63 via V14R2 Adjust R_95 via V16R2 Adjust R_127 via V18R2 Adjust R_159 via V20R2 Adjust R_191 via V22R2 Adjust R_255(brightest) via V26R2
Restriction	Set V0R2[9:0] < V1R2[9:0] < V2R2[9:0] < ... < V25R2[9:0] < V26R2[9:0], or V0R2[9:0] > V1R2[9:0] > V2R2[9:0] > ... > V25R2[9:0] > V26R2[9:0]

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(3860h~7060h) Gamma 2.2 Corrections Set 2 for Green

R/W	Addr	D7	D6	D5	D4	D3	D2	D1	D0	HEX
R/W	3860h	-	-	-	-	-	-	V0G2[9:8]		00h
	3960h	V0G2[7:0]								00h
	3A60h	-	-	-	-	-	-	V1G2[9:8]		00h
	3B60h	V1G2[7:0]								04h
	3D60h	-	-	-	-	-	-	V2G2[9:8]		00h
	3F60h	V2G2[7:0]								0Ch
	4060h	-	-	-	-	-	-	V3G2[9:8]		00h
	4160h	V3G2[7:0]								1Ch
	4260h	-	-	-	-	-	-	V4G2[9:8]		00h
	4360h	V4G2[7:0]								2Ch
	4460h	-	-	-	-	-	-	V5G2[9:8]		00h
	4560h	V5G2[7:0]								3Ch
	4660h	-	-	-	-	-	-	V6G2[9:8]		00h
	4760h	V6G2[7:0]								4Ch
	4860h	-	-	-	-	-	-	V7G2[9:8]		00h
	4960h	V7G2[7:0]								5Ch
	4A60h	-	-	-	-	-	-	V8G2[9:8]		00h
	4B60h	V8G2[7:0]								6Ch
	4C60h	-	-	-	-	-	-	V9G2[9:8]		00h
	4D60h	V9G2[7:0]								7Ch
	4E60h	-	-	-	-	-	-	V10G2[9:8]		00h
	4F60h	V10G2[7:0]								8Ch
	5060h	-	-	-	-	-	-	V11G2[9:8]		00h
	5260h	V11G2[7:0]								9Ch
	5360h	-	-	-	-	-	-	V12G2[9:8]		00h
	5460h	V12G2[7:0]								BCh
	5560h	-	-	-	-	-	-	V13G2[9:8]		00h
	5660h	V13G2[7:0]								DCh
	5760h	-	-	-	-	-	-	V14G2[9:8]		00h
	5860h	V14G2[7:0]								FCh
	5960h	-	-	-	-	-	-	V15G2[9:8]		01h
	5A60h	V15G2[7:0]								3Ch
	5B60h	-	-	-	-	-	-	V16G2[9:8]		01h
	5C60h	V16G2[7:0]								7Ch
	5D60h	-	-	-	-	-	-	V17G2[9:8]		01h
	5E60h	V17G2[7:0]								BCh
	5F60h	-	-	-	-	-	-	V18G2[9:8]		01h
	6060h	V18G2[7:0]								FCh
	6160h	-	-	-	-	-	-	V19G2[9:8]		02h
	6260h	V19G2[7:0]								3Ch
	6360h	-	-	-	-	-	-	V20G2[9:8]		02h
	6460h	V20G2[7:0]								7Ch
	6560h	-	-	-	-	-	-	V21G2[9:8]		02h
	6660h	V21G2[7:0]								BCh
	6760h	-	-	-	-	-	-	V22G2[9:8]		02h
	6860h	V22G2[7:0]								FCh
	6960h	-	-	-	-	-	-	V23G2[9:8]		03h
	6A60h	V23G2[7:0]								3Ch
	6B60h	-	-	-	-	-	-	V24G2[9:8]		03h
	6C60h	V24G2[7:0]								7Ch
	6D60h	-	-	-	-	-	-	V25G2[9:8]		03h
	6E60h	V25G2[7:0]								BCh
	6F60h	-	-	-	-	-	-	V26G2[9:8]		03h

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	7060h	V26G2[7:0]	FCh

Description	This command is used to adjust the gamma 2.2 correction for the red under normal display mode. For rb_GMA_13P1=0 Adjust G_0(darkest) via V0G2 Adjust G_1 via V1G2 Adjust G_3 via V2G2 Adjust G_7 via V3G2 Adjust G_11 via V4G2 Adjust G_15 via V5G2 Adjust G_19 via V6G2 Adjust G_23 via V7G2 Adjust G_27 via V8G2 Adjust G_31 via V9G2 Adjust G_35 via V10G2 Adjust G_39 via V11G2 Adjust G_47 via V12G2 Adjust G_55 via V13G2 Adjust G_63 via V14G2 Adjust G_79 via V15G2 Adjust G_95 via V16G2 Adjust G_111 via V17G2 Adjust G_127 via V18G2 Adjust G_143 via V19G2 Adjust G_159 via V20G2 Adjust G_175 via V21G2 Adjust G_191 via V22G2 Adjust G_207 via V23G2 Adjust G_223 via V24G2 Adjust G_239 via V25G2 Adjust G_255(brightest) via V26G2 For rb_GMA_13P1=1 Adjust G_0(darkest) via V0G2 Adjust G_1 via V1G2 Adjust G_3 via V2G2 Adjust G_7 via V3G2 Adjust G_11 via V4G2 Adjust G_15 via V5G2 Adjust G_31 via V9G2 Adjust G_63 via V14G2 Adjust G_95 via V16G2 Adjust G_127 via V18G2 Adjust G_159 via V20G2 Adjust G_191 via V22G2 Adjust G_255(brightest) via V26G2
Restriction	Set V0G2[9:0] < V1G2[9:0] < V2G2[9:0] < ... < V25G2[9:0] < V26G2[9:0], or V0G2[9:0] > V1G2[9:0] > V2G2[9:0] > ... > V25G2[9:0] > V26G2[9:0]

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(7160h~A760h) Gamma 2.2 Corrections Set 2 for Blue

R/W	Addr	D7	D6	D5	D4	D3	D2	D1	D0	HEX
R/W	7160h	-	-	-	-	-	-	V0B2[9:8]		00h
	7260h	V0B2[7:0]								00h
	7360h	-	-	-	-	-	-	V1B2[9:8]		00h
	7460h	V1B2[7:0]								04h
	7560h	-	-	-	-	-	-	V2B2[9:8]		00h
	7660h	V2B2[7:0]								0Ch
	7760h	-	-	-	-	-	-	V3B2[9:8]		00h
	7860h	V3B2[7:0]								1Ch
	7960h	-	-	-	-	-	-	V4B2[9:8]		00h
	7A60h	V4B2[7:0]								2Ch
	7B60h	-	-	-	-	-	-	V5B2[9:8]		00h
	7C60h	V5B2[7:0]								3Ch
	7D60h	-	-	-	-	-	-	V6B2[9:8]		00h
	7E60h	V6B2[7:0]								4Ch
	7F60h	-	-	-	-	-	-	V7B2[9:8]		00h
	8060h	V7B2[7:0]								5Ch
	8160h	-	-	-	-	-	-	V8B2[9:8]		00h
	8260h	V8B2[7:0]								6Ch
	8360h	-	-	-	-	-	-	V9B2[9:8]		00h
	8460h	V9B2[7:0]								7Ch
	8560h	-	-	-	-	-	-	V10B2[9:8]		00h
	8660h	V10B2[7:0]								8Ch
	8760h	-	-	-	-	-	-	V11B2[9:8]		00h
	8860h	V11B2[7:0]								9Ch
	8960h	-	-	-	-	-	-	V12B2[9:8]		00h
	8A60h	V12B2[7:0]								BCh
	8B60h	-	-	-	-	-	-	V13B2[9:8]		00h
	8C60h	V13B2[7:0]								DCh
	8D60h	-	-	-	-	-	-	V14B2[9:8]		00h
	8E60h	V14B2[7:0]								FCh
	8F60h	-	-	-	-	-	-	V15B2[9:8]		01h
	9060h	V15B2[7:0]								3Ch
	9160h	-	-	-	-	-	-	V16B2[9:8]		01h
	9260h	V16B2[7:0]								7Ch
	9360h	-	-	-	-	-	-	V17B2[9:8]		01h
	9460h	V17B2[7:0]								BCh
	9560h	-	-	-	-	-	-	V18B2[9:8]		01h
	9660h	V18B2[7:0]								FCh
	9760h	-	-	-	-	-	-	V19B2[9:8]		02h
	9860h	V19B2[7:0]								3Ch
	9960h	-	-	-	-	-	-	V20B2[9:8]		02h
	9A60h	V20B2[7:0]								7Ch
	9B60h	-	-	-	-	-	-	V21B2[9:8]		02h
	9C60h	V21B2[7:0]								BCh
	9D60h	-	-	-	-	-	-	V22B2[9:8]		02h
	9E60h	V22B2[7:0]								FCh
	9F60h	-	-	-	-	-	-	V23B2[9:8]		03h
	A060h	V23B2[7:0]								3Ch
	A260h	-	-	-	-	-	-	V24B2[9:8]		03h
	A360h	V24B2[7:0]								7Ch
	A460h	-	-	-	-	-	-	V25B2[9:8]		03h
	A560h	V25B2[7:0]								BCh
	A660h	-	-	-	-	-	-	V26B2[9:8]		03h

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	A760h	V26B2[7:0]	FCh

Description	This command is used to adjust the gamma 2.2 correction for the red under normal display mode. For rb_GMA_13P1=0 Adjust B_0(darkest) via V0B2 Adjust B_1 via V1B2 Adjust B_3 via V2B2 Adjust B_7 via V3B2 Adjust B_11 via V4B2 Adjust B_15 via V5B2 Adjust B_19 via V6B2 Adjust B_23 via V7B2 Adjust B_27 via V8B2 Adjust B_31 via V9B2 Adjust B_35 via V10B2 Adjust B_39 via V11B2 Adjust B_47 via V12B2 Adjust B_55 via V13B2 Adjust B_63 via V14B2 Adjust B_79 via V15B2 Adjust B_95 via V16B2 Adjust B_111 via V17B2 Adjust B_127 via V18B2 Adjust B_143 via V19B2 Adjust B_159 via V20B2 Adjust B_175 via V21B2 Adjust B_191 via V22B2 Adjust B_207 via V23B2 Adjust B_223 via V24B2 Adjust B_239 via V25B2 Adjust B_255(brightest) via V26B2 For rb_GMA_13P1=1 Adjust B_0(darkest) via V0B2 Adjust B_1 via V1B2 Adjust B_3 via V2B2 Adjust B_7 via V3B2 Adjust B_11 via V4B2 Adjust B_15 via V5B2 Adjust B_31 via V9B2 Adjust B_63 via V14B2 Adjust B_95 via V16B2 Adjust B_127 via V18B2 Adjust B_159 via V20B2 Adjust B_191 via V22B2 Adjust B_255(brightest) via V26B2
Restriction	Set V0B2[9:0] < V1B2[9:0] < V2B2[9:0] < ... < V25B2[9:0] < V26B2[9:0], or V0B2[9:0] > V1B2[9:0] > V2B2[9:0] > ... > V25B2[9:0] > V26B2[9:0]

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(A960h~AB60h) VGMP/VGSP Control

R/W	Addr	D7	D6	D5	D4	D3	D2	D1	D0	HEX
R/W	A960h	VGMPTR2[7:0]								50h
R/W	AA60h	VGSPTR2[7:0]								18h
R/W	AB60h	rb_GMA_13P2	-	-	VGSPTR2[8]	-	-	-	VGMPTR2[8]	00h

Description

This command is for VGMP output level selection.

Bit	Value	VGMP Output level
VGMPTR2[8:0]	000h	2.0000V
	001h	2.0125V
	:	0.0125V / Step
	050h	3.0000V
	:	0.0125V / Step
	157h	6.2875V
	158h	6.3000V
	159h~1FFh	Reserved

This command is for VGSP output level selection.

Bit	Value	VGSP Output level
VGSPTR2[8:0]	000h	0.0000V
	001h	0.2125V
	:	0.0125V / Step
	005h	0.2625V
	:	0.0125V / Step
	158h	4.5000V
	159h~1FFh	Reserved
	000h	0.0000V

Restriction

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(FE60h): CMD Mode Switch

R/W	Addr	D7	D6	D5	D4	D3	D2	D1	D0	HEX
W	FE60h	CMD_Page[7:0]								00h

Description

This command is used to switch the Manufacture Command Pages and User Commands sets.

CMD_Page[7:0]	Description
00h (default)	User Command Set (UCS = CMD1)
10h	Manufacture Command Set Page Panel ID
12h	Manufacture Command Set Page SID
20h	Manufacture Command Set Page Panel
40h	Manufacture Command Set Page ABH Mode
82h	Manufacture Command Set Page Power
92h	Manufacture Command Set Page SD timing
50h	Manufacture Command Set Page Gamma1
60h	Manufacture Command Set Page Gamma2
30h	Manufacture Command Set Page Gamma3
52h	Manufacture Command Set Page Gamma4
70h	Manufacture Command Set Page GOA Timing 1
F0h	Manufacture Command Set Page GOA Timing 2
42h	Manufacture Command Set Page DBV
22h	Manufacture Command Set Page SES
80h	Manufacture Command Set Page APRC
90h	Manufacture Command Set Page ACL
62h	Manufacture Command Set Page CGM
C2h	Manufacture Command Set Page CGM LUT

Restriction

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(FF60h): Read CMD Status

R/W	Addr	D7	D6	D5	D4	D3	D2	D1	D0	HEX
R	FF60h	CMD_Status[7:0]								00h

Description	This command is used to read the status of Manufacture Command Pages. Please refer to FE00h
Restriction	-

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1.11MCS: CMD2 Page30, Gamma3 Settings

Instruction	R/W	Addr	D7	D6	D5	D4	D3	D2	D1	D0	HEX
GammaR_3	R/W	0030h	-	-	-	-	-	-	V0R3[9:8]		00h
GammaR_3	R/W	0130h	V0R3[7:0]								00h
GammaR_3	R/W	0230h	-	-	-	-	-	-	V1R3[9:8]		00h
GammaR_3	R/W	0330h	V1R3[7:0]								04h
GammaR_3	R/W	0430h	-	-	-	-	-	-	V2R3[9:8]		00h
GammaR_3	R/W	0530h	V2R3[7:0]								0Ch
GammaR_3	R/W	0630h	-	-	-	-	-	-	V3R3[9:8]		00h
GammaR_3	R/W	0730h	V3R3[7:0]								1Ch
GammaR_3	R/W	0830h	-	-	-	-	-	-	V4R3[9:8]		00h
GammaR_3	R/W	0930h	V4R3[7:0]								2Ch
GammaR_3	R/W	0A30h	-	-	-	-	-	-	V5R3[9:8]		00h
GammaR_3	R/W	0B30h	V5R3[7:0]								3Ch
GammaR_3	R/W	0C30h	-	-	-	-	-	-	V6R3[9:8]		00h
GammaR_3	R/W	0D30h	V6R3[7:0]								4Ch
GammaR_3	R/W	0E30h	-	-	-	-	-	-	V7R3[9:8]		00h
GammaR_3	R/W	0F30h	V7R3[7:0]								5Ch
GammaR_3	R/W	1030h	-	-	-	-	-	-	V8R3[9:8]		00h
GammaR_3	R/W	1130h	V8R3[7:0]								6Ch
GammaR_3	R/W	1230h	-	-	-	-	-	-	V9R3[9:8]		00h
GammaR_3	R/W	1330h	V9R3[7:0]								7Ch
GammaR_3	R/W	1430h	-	-	-	-	-	-	V10R3[9:8]		00h
GammaR_3	R/W	1530h	V10R3[7:0]								8Ch
GammaR_3	R/W	1630h	-	-	-	-	-	-	V11R3[9:8]		00h
GammaR_3	R/W	1730h	V11R3[7:0]								9Ch
GammaR_3	R/W	1830h	-	-	-	-	-	-	V12R3[9:8]		00h
GammaR_3	R/W	1930h	V12R3[7:0]								BCh
GammaR_3	R/W	1A30h	-	-	-	-	-	-	V13R3[9:8]		00h
GammaR_3	R/W	1B30h	V13R3[7:0]								DCh
GammaR_3	R/W	1C30h	-	-	-	-	-	-	V14R3[9:8]		00h
GammaR_3	R/W	1D30h	V14R3[7:0]								FCh
GammaR_3	R/W	1E30h	-	-	-	-	-	-	V15R3[9:8]		01h
GammaR_3	R/W	1F30h	V15R3[7:0]								3Ch
GammaR_3	R/W	2030h	-	-	-	-	-	-	V16R3[9:8]		01h
GammaR_3	R/W	2130h	V16R3[7:0]								7Ch
GammaR_3	R/W	2230h	-	-	-	-	-	-	V17R3[9:8]		01h
GammaR_3	R/W	2330h	V17R3[7:0]								BCh
GammaR_3	R/W	2430h	-	-	-	-	-	-	V18R3[9:8]		01h
GammaR_3	R/W	2530h	V18R3[7:0]								FCh
GammaR_3	R/W	2630h	-	-	-	-	-	-	V19R3[9:8]		02h
GammaR_3	R/W	2730h	V19R3[7:0]								3Ch
GammaR_3	R/W	2830h	-	-	-	-	-	-	V20R3[9:8]		02h
GammaR_3	R/W	2930h	V20R3[7:0]								7Ch
GammaR_3	R/W	2A30h	-	-	-	-	-	-	V21R3[9:8]		02h
GammaR_3	R/W	2B30h	V21R3[7:0]								BCh
GammaR_3	R/W	2D30h	-	-	-	-	-	-	V22R3[9:8]		02h
GammaR_3	R/W	2F30h	V22R3[7:0]								FCh
GammaR_3	R/W	3030h	-	-	-	-	-	-	V23R3[9:8]		03h

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GammaR_3	R/W	3130h	V23R3[7:0]							3Ch
GammaR_3	R/W	3230h	-	-	-	-	-	-	V24R3[9:8]	03h
GammaR_3	R/W	3330h	V24R3[7:0]							7Ch
GammaR_3	R/W	3430h	-	-	-	-	-	-	V25R3[9:8]	03h
GammaR_3	R/W	3530h	V25R3[7:0]							BCh
GammaR_3	R/W	3630h	-	-	-	-	-	-	V26R3[9:8]	03h
GammaR_3	R/W	3730h	V26R3[7:0]							FCh
GammaG_3	R/W	3830h	-	-	-	-	-	-	V0G3[9:8]	00h
GammaG_3	R/W	3930h	V0G3[7:0]							00h
GammaG_3	R/W	3A30h	-	-	-	-	-	-	V1G3[9:8]	00h
GammaG_3	R/W	3B30h	V1G3[7:0]							04h
GammaG_3	R/W	3D30h	-	-	-	-	-	-	V2G3[9:8]	00h
GammaG_3	R/W	3F30h	V2G3[7:0]							0Ch
GammaG_3	R/W	4030h	-	-	-	-	-	-	V3G3[9:8]	00h
GammaG_3	R/W	4130h	V3G3[7:0]							1Ch
GammaG_3	R/W	4230h	-	-	-	-	-	-	V4G3[9:8]	00h
GammaG_3	R/W	4330h	V4G3[7:0]							2Ch
GammaG_3	R/W	4430h	-	-	-	-	-	-	V5G3[9:8]	00h
GammaG_3	R/W	4530h	V5G3[7:0]							3Ch
GammaG_3	R/W	4630h	-	-	-	-	-	-	V6G3[9:8]	00h
GammaG_3	R/W	4730h	V6G3[7:0]							4Ch
GammaG_3	R/W	4830h	-	-	-	-	-	-	V7G3[9:8]	00h
GammaG_3	R/W	4930h	V7G3[7:0]							5Ch
GammaG_3	R/W	4A30h	-	-	-	-	-	-	V8G3[9:8]	00h
GammaG_3	R/W	4B30h	V8G3[7:0]							6Ch
GammaG_3	R/W	4C30h	-	-	-	-	-	-	V9G3[9:8]	00h
GammaG_3	R/W	4D30h	V9G3[7:0]							7Ch
GammaG_3	R/W	4E30h	-	-	-	-	-	-	V10G3[9:8]	00h
GammaG_3	R/W	4F30h	V10G3[7:0]							8Ch
GammaG_3	R/W	5030h	-	-	-	-	-	-	V11G3[9:8]	00h
GammaG_3	R/W	5230h	V11G3[7:0]							9Ch
GammaG_3	R/W	5330h	-	-	-	-	-	-	V12G3[9:8]	00h
GammaG_3	R/W	5430h	V12G3[7:0]							BCh
GammaG_3	R/W	5530h	-	-	-	-	-	-	V13G3[9:8]	00h
GammaG_3	R/W	5630h	V13G3[7:0]							DCh
GammaG_3	R/W	5730h	-	-	-	-	-	-	V14G3[9:8]	00h
GammaG_3	R/W	5830h	V14G3[7:0]							FCh
GammaG_3	R/W	5930h	-	-	-	-	-	-	V15G3[9:8]	01h
GammaG_3	R/W	5A30h	V15G3[7:0]							3Ch
GammaG_3	R/W	5B30h	-	-	-	-	-	-	V16G3[9:8]	01h
GammaG_3	R/W	5C30h	V16G3[7:0]							7Ch
GammaG_3	R/W	5D30h	-	-	-	-	-	-	V17G3[9:8]	01h
GammaG_3	R/W	5E30h	V17G3[7:0]							BCh
GammaG_3	R/W	5F30h	-	-	-	-	-	-	V18G3[9:8]	01h
GammaG_3	R/W	6030h	V18G3[7:0]							FCh
GammaG_3	R/W	6130h	-	-	-	-	-	-	V19G3[9:8]	02h
GammaG_3	R/W	6230h	V19G3[7:0]							3Ch
GammaG_3	R/W	6330h	-	-	-	-	-	-	V20G3[9:8]	02h
GammaG_3	R/W	6430h	V20G3[7:0]							7Ch
GammaG_3	R/W	6530h	-	-	-	-	-	-	V21G3[9:8]	02h
GammaG_3	R/W	6630h	V21G3[7:0]							BCh

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GammaG_3	R/W	6730h	-	-	-	-	-	-	V22G3[9:8]	02h
GammaG_3	R/W	6830h	V22G3[7:0]							FCh
GammaG_3	R/W	6930h	-	-	-	-	-	-	V23G3[9:8]	03h
GammaG_3	R/W	6A30h	V23G3[7:0]							3Ch
GammaG_3	R/W	6B30h	-	-	-	-	-	-	V24G3[9:8]	03h
GammaG_3	R/W	6C30h	V24G3[7:0]							7Ch
GammaG_3	R/W	6D30h	-	-	-	-	-	-	V25G3[9:8]	03h
GammaG_3	R/W	6E30h	V25G3[7:0]							BCh
GammaG_3	R/W	6F30h	-	-	-	-	-	-	V26G3[9:8]	03h
GammaG_3	R/W	7030h	V26G3[7:0]							FCh
GammaB_3	R/W	7130h	-	-	-	-	-	-	V0B3[9:8]	00h
GammaB_3	R/W	7230h	V0B3[7:0]							00h
GammaB_3	R/W	7330h	-	-	-	-	-	-	V1B3[9:8]	00h
GammaB_3	R/W	7430h	V1B3[7:0]							04h
GammaB_3	R/W	7530h	-	-	-	-	-	-	V2B3[9:8]	00h
GammaB_3	R/W	7630h	V2B3[7:0]							0Ch
GammaB_3	R/W	7730h	-	-	-	-	-	-	V3B3[9:8]	00h
GammaB_3	R/W	7830h	V3B3[7:0]							1Ch
GammaB_3	R/W	7930h	-	-	-	-	-	-	V4B3[9:8]	00h
GammaB_3	R/W	7A30h	V4B3[7:0]							2Ch
GammaB_3	R/W	7B30h	-	-	-	-	-	-	V5B3[9:8]	00h
GammaB_3	R/W	7C30h	V5B3[7:0]							3Ch
GammaB_3	R/W	7D30h	-	-	-	-	-	-	V6B3[9:8]	00h
GammaB_3	R/W	7E30h	V6B3[7:0]							4Ch
GammaB_3	R/W	7F30h	-	-	-	-	-	-	V7B3[9:8]	00h
GammaB_3	R/W	8030h	V7B3[7:0]							5Ch
GammaB_3	R/W	8130h	-	-	-	-	-	-	V8B3[9:8]	00h
GammaB_3	R/W	8230h	V8B3[7:0]							6Ch
GammaB_3	R/W	8330h	-	-	-	-	-	-	V9B3[9:8]	00h
GammaB_3	R/W	8430h	V9B3[7:0]							7Ch
GammaB_3	R/W	8530h	-	-	-	-	-	-	V10B3[9:8]	00h
GammaB_3	R/W	8630h	V10B3[7:0]							8Ch
GammaB_3	R/W	8730h	-	-	-	-	-	-	V11B3[9:8]	00h
GammaB_3	R/W	8830h	V11B3[7:0]							9Ch
GammaB_3	R/W	8930h	-	-	-	-	-	-	V12B3[9:8]	00h
GammaB_3	R/W	8A30h	V12B3[7:0]							BCh
GammaB_3	R/W	8B30h	-	-	-	-	-	-	V13B3[9:8]	00h
GammaB_3	R/W	8C30h	V13B3[7:0]							DCh
GammaB_3	R/W	8D30h	-	-	-	-	-	-	V14B3[9:8]	00h
GammaB_3	R/W	8E30h	V14B3[7:0]							FCh
GammaB_3	R/W	8F30h	-	-	-	-	-	-	V15B3[9:8]	01h
GammaB_3	R/W	9030h	V15B3[7:0]							3Ch
GammaB_3	R/W	9130h	-	-	-	-	-	-	V16B3[9:8]	01h
GammaB_3	R/W	9230h	V16B3[7:0]							7Ch
GammaB_3	R/W	9330h	-	-	-	-	-	-	V17B3[9:8]	01h
GammaB_3	R/W	9430h	V17B3[7:0]							BCh
GammaB_3	R/W	9530h	-	-	-	-	-	-	V18B3[9:8]	01h
GammaB_3	R/W	9630h	V18B3[7:0]							FCh
GammaB_3	R/W	9730h	-	-	-	-	-	-	V19B3[9:8]	02h
GammaB_3	R/W	9830h	V19B3[7:0]							3Ch
GammaB_3	R/W	9930h	-	-	-	-	-	-	V20B3[9:8]	02h

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GammaB_3	R/W	9A30h	V20B3[7:0]								7Ch
GammaB_3	R/W	9B30h	-	-	-	-	-	-	V21B3[9:8]		02h
GammaB_3	R/W	9C30h	V21B3[7:0]								BCh
GammaB_3	R/W	9D30h	-	-	-	-	-	-	V22B3[9:8]		02h
GammaB_3	R/W	9E30h	V22B3[7:0]								FCh
GammaB_3	R/W	9F30h	-	-	-	-	-	-	V23B3[9:8]		03h
GammaB_3	R/W	A030h	V23B3[7:0]								3Ch
GammaB_3	R/W	A230h	-	-	-	-	-	-	V24B3[9:8]		03h
GammaB_3	R/W	A330h	V24B3[7:0]								7Ch
GammaB_3	R/W	A430h	-	-	-	-	-	-	V25B3[9:8]		03h
GammaB_3	R/W	A530h	V25B3[7:0]								BCh
GammaB_3	R/W	A630h	-	-	-	-	-	-	V26B3[9:8]		03h
GammaB_3	R/W	A730h	V26B3[7:0]								FCh
VGMP/VGSP	R/W	A930h	VGMPTR3[7:0]								50h
VGMP/VGSP	R/W	AA30h	VGSPTR3[7:0]								18h
VGMP/VGSP	R/W	AB30h	GMA_13P3	-	-	VGSPTR3[8]	-	-	-	VGMPTR3[8]	00h
CMD Mode Switch	W	FE30h	CMD_Page [7:0]								00h
RD CMD Status	R	FF30h	CMD_Status[7:0]								00h

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(0030h~3730h)Gamma 2.2 Corrections Set 3 for Red

R/W	Addr	D7	D6	D5	D4	D3	D2	D1	D0	HEX
R/W	0030h	-	-	-	-	-	-	V0R3[9:8]		00h
	0130h	V0R3[7:0]								00h
	0230h	-	-	-	-	-	-	V1R3[9:8]		00h
	0330h	V1R3[7:0]								04h
	0430h	-	-	-	-	-	-	V2R3[9:8]		00h
	0530h	V2R3[7:0]								0Ch
	0630h	-	-	-	-	-	-	V3R3[9:8]		00h
	0730h	V3R3[7:0]								1Ch
	0830h	-	-	-	-	-	-	V4R3[9:8]		00h
	0930h	V4R3[7:0]								2Ch
	0A30h	-	-	-	-	-	-	V5R3[9:8]		00h
	0B30h	V5R3[7:0]								3Ch
	0C30h	-	-	-	-	-	-	V6R3[9:8]		00h
	0D30h	V6R3[7:0]								4Ch
	0E30h	-	-	-	-	-	-	V7R3[9:8]		00h
	0F30h	V7R3[7:0]								5Ch
	1030h	-	-	-	-	-	-	V8R3[9:8]		00h
	1130h	V8R3[7:0]								6Ch
	1230h	-	-	-	-	-	-	V9R3[9:8]		00h
	1330h	V9R3[7:0]								7Ch
	1430h	-	-	-	-	-	-	V10R3[9:8]		00h
	1530h	V10R3[7:0]								8Ch
	1630h	-	-	-	-	-	-	V11R3[9:8]		00h
	1730h	V11R3[7:0]								9Ch
	1830h	-	-	-	-	-	-	V12R3[9:8]		00h
	1930h	V12R3[7:0]								BCh
	1A30h	-	-	-	-	-	-	V13R3[9:8]		00h
	1B30h	V13R3[7:0]								DCh
	1C30h	-	-	-	-	-	-	V14R3[9:8]		00h
	1D30h	V14R3[7:0]								FCh
	1E30h	-	-	-	-	-	-	V15R3[9:8]		01h
	1F30h	V15R3[7:0]								3Ch
	2030h	-	-	-	-	-	-	V16R3[9:8]		01h
	2130h	V16R3[7:0]								7Ch
	2230h	-	-	-	-	-	-	V17R3[9:8]		01h
	2330h	V17R3[7:0]								BCh
	2430h	-	-	-	-	-	-	V18R3[9:8]		01h
	2530h	V18R3[7:0]								FCh
	2630h	-	-	-	-	-	-	V19R3[9:8]		02h
	2730h	V19R3[7:0]								3Ch
	2830h	-	-	-	-	-	-	V20R3[9:8]		02h
	2930h	V20R3[7:0]								7Ch
	2A30h	-	-	-	-	-	-	V21R3[9:8]		02h
	2B30h	V21R3[7:0]								BCh
	2D30h	-	-	-	-	-	-	V22R3[9:8]		02h
	2F30h	V22R3[7:0]								FCh
	3030h	-	-	-	-	-	-	V23R3[9:8]		03h
	3130h	V23R3[7:0]								3Ch
	3230h	-	-	-	-	-	-	V24R3[9:8]		03h
	3330h	V24R3[7:0]								7Ch
	3430h	-	-	-	-	-	-	V25R3[9:8]		03h
	3530h	V25R3[7:0]								BCh
	3630h	-	-	-	-	-	-	V26R3[9:8]		03h

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	3730h	V26R3[7:0]	FCh

Description	This command is used to adjust the gamma 2.2 correction for the red under normal display mode. For rb_GMA_13P1=0 Adjust R_0(darkest) via V0R3 Adjust R_1 via V1R3 Adjust R_3 via V2R3 Adjust R_7 via V3R3 Adjust R_11 via V4R3 Adjust R_15 via V5R3 Adjust R_19 via V6R3 Adjust R_23 via V7R3 Adjust R_27 via V8R3 Adjust R_31 via V9R3 Adjust R_35 via V10R3 Adjust R_39 via V11R3 Adjust R_47 via V12R3 Adjust R_55 via V13R3 Adjust R_63 via V14R3 Adjust R_79 via V15R3 Adjust R_95 via V16R3 Adjust R_111 via V17R3 Adjust R_127 via V18R3 Adjust R_143 via V19R3 Adjust R_159 via V20R3 Adjust R_175 via V21R3 Adjust R_191 via V22R3 Adjust R_207 via V23R3 Adjust R_223 via V24R3 Adjust R_239 via V25R3 Adjust R_255(brightest) via V26R3 For rb_GMA_13P1=1 Adjust R_0(darkest) via V0R3 Adjust R_1 via V1R3 Adjust R_3 via V2R3 Adjust R_7 via V3R3 Adjust R_11 via V4R3 Adjust R_15 via V5R3 Adjust R_31 via V9R3 Adjust R_63 via V14R3 Adjust R_95 via V16R3 Adjust R_127 via V18R3 Adjust R_159 via V20R3 Adjust R_191 via V22R3 Adjust R_255(brightest) via V26R3
Restriction	Set V0R3[9:0] < V1R3[9:0] < V2R3[9:0] < ... < V25R3[9:0] < V26R3[9:0], or V0R3[9:0] > V1R3[9:0] > V2R3[9:0] > ... > V25R3[9:0] > V26R3[9:0]

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(3830h~7030h) Gamma 2.2 Corrections Set 3 for Green

R/W	Addr	D7	D6	D5	D4	D3	D2	D1	D0	HEX
R/W	3830h	-	-	-	-	-	-	V0G3[9:8]		00h
	3930h	V0G3[7:0]								00h
	3A30h	-	-	-	-	-	-	V1G3[9:8]		00h
	3B30h	V1G3[7:0]								04h
	3D30h	-	-	-	-	-	-	V2G3[9:8]		00h
	3F30h	V2G3[7:0]								0Ch
	4030h	-	-	-	-	-	-	V3G3[9:8]		00h
	4130h	V3G3[7:0]								1Ch
	4230h	-	-	-	-	-	-	V4G3[9:8]		00h
	4330h	V4G3[7:0]								2Ch
	4430h	-	-	-	-	-	-	V5G3[9:8]		00h
	4530h	V5G3[7:0]								3Ch
	4630h	-	-	-	-	-	-	V6G3[9:8]		00h
	4730h	V6G3[7:0]								4Ch
	4830h	-	-	-	-	-	-	V7G3[9:8]		00h
	4930h	V7G3[7:0]								5Ch
	4A30h	-	-	-	-	-	-	V8G3[9:8]		00h
	4B30h	V8G3[7:0]								6Ch
	4C30h	-	-	-	-	-	-	V9G3[9:8]		00h
	4D30h	V9G3[7:0]								7Ch
	4E30h	-	-	-	-	-	-	V10G3[9:8]		00h
	4F30h	V10G3[7:0]								8Ch
	5030h	-	-	-	-	-	-	V11G3[9:8]		00h
	5230h	V11G3[7:0]								9Ch
	5330h	-	-	-	-	-	-	V12G3[9:8]		00h
	5430h	V12G3[7:0]								BCh
	5530h	-	-	-	-	-	-	V13G3[9:8]		00h
	5630h	V13G3[7:0]								DCh
	5730h	-	-	-	-	-	-	V14G3[9:8]		00h
	5830h	V14G3[7:0]								FCh
	5930h	-	-	-	-	-	-	V15G3[9:8]		01h
	5A30h	V15G3[7:0]								3Ch
	5B30h	-	-	-	-	-	-	V16G3[9:8]		01h
	5C30h	V16G3[7:0]								7Ch
	5D30h	-	-	-	-	-	-	V17G3[9:8]		01h
	5E30h	V17G3[7:0]								BCh
	5F30h	-	-	-	-	-	-	V18G3[9:8]		01h
	6030h	V18G3[7:0]								FCh
	6130h	-	-	-	-	-	-	V19G3[9:8]		02h
	6230h	V19G3[7:0]								3Ch
	6330h	-	-	-	-	-	-	V20G3[9:8]		02h
	6430h	V20G3[7:0]								7Ch
	6530h	-	-	-	-	-	-	V21G3[9:8]		02h
	6630h	V21G3[7:0]								BCh
	6730h	-	-	-	-	-	-	V22G3[9:8]		02h
	6830h	V22G3[7:0]								FCh
	6930h	-	-	-	-	-	-	V23G3[9:8]		03h
	6A30h	V23G3[7:0]								3Ch
	6B30h	-	-	-	-	-	-	V24G3[9:8]		03h
	6C30h	V24G3[7:0]								7Ch
	6D30h	-	-	-	-	-	-	V25G3[9:8]		03h
	6E30h	V25G3[7:0]								BCh
	6F30h	-	-	-	-	-	-	V26G3[9:8]		03h

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	7030h	V26G3[7:0]	FCh

Description	This command is used to adjust the gamma 2.2 correction for the red under normal display mode. For rb_GMA_13P1=0 Adjust G_0(darkest) via V0G3 Adjust G_1 via V1G3 Adjust G_3 via V2G3 Adjust G_7 via V3G3 Adjust G_11 via V4G3 Adjust G_15 via V5G3 Adjust G_19 via V6G3 Adjust G_23 via V7G3 Adjust G_27 via V8G3 Adjust G_31 via V9G3 Adjust G_35 via V10G3 Adjust G_39 via V11G3 Adjust G_47 via V12G3 Adjust G_55 via V13G3 Adjust G_63 via V14G3 Adjust G_79 via V15G3 Adjust G_95 via V16G3 Adjust G_111 via V17G3 Adjust G_127 via V18G3 Adjust G_143 via V19G3 Adjust G_159 via V20G3 Adjust G_175 via V21G3 Adjust G_191 via V22G3 Adjust G_207 via V23G3 Adjust G_223 via V24G3 Adjust G_239 via V25G3 Adjust G_255(brightest) via V26G3 For rb_GMA_13P1=1 Adjust G_0(darkest) via V0G3 Adjust G_1 via V1G3 Adjust G_3 via V2G3 Adjust G_7 via V3G3 Adjust G_11 via V4G3 Adjust G_15 via V5G3 Adjust G_31 via V9G3 Adjust G_63 via V14G3 Adjust G_95 via V16G3 Adjust G_127 via V18G3 Adjust G_159 via V20G3 Adjust G_191 via V22G3 Adjust G_255(brightest) via V26G3
Restriction	Set V0G3[9:0] < V1G3[9:0] < V2G3[9:0] < ... < V25G3[9:0] < V26G3[9:0], or V0G3[9:0] > V1G3[9:0] > V2G3[9:0] > ... > V25G3[9:0] > V26G3[9:0]

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(7130h~A730h) Gamma 2.2 Corrections Set 3 for Blue

R/W	Addr	D7	D6	D5	D4	D3	D2	D1	D0	HEX
R/W	7130h	-	-	-	-	-	-	V0B3[9:8]		00h
	7230h	V0B3[7:0]								00h
	7330h	-	-	-	-	-	-	V1B3[9:8]		00h
	7430h	V1B3[7:0]								04h
	7530h	-	-	-	-	-	-	V2B3[9:8]		00h
	7630h	V2B3[7:0]								0Ch
	7730h	-	-	-	-	-	-	V3B3[9:8]		00h
	7830h	V3B3[7:0]								1Ch
	7930h	-	-	-	-	-	-	V4B3[9:8]		00h
	7A30h	V4B3[7:0]								2Ch
	7B30h	-	-	-	-	-	-	V5B3[9:8]		00h
	7C30h	V5B3[7:0]								3Ch
	7D30h	-	-	-	-	-	-	V6B3[9:8]		00h
	7E30h	V6B3[7:0]								4Ch
	7F30h	-	-	-	-	-	-	V7B3[9:8]		00h
	8030h	V7B3[7:0]								5Ch
	8130h	-	-	-	-	-	-	V8B3[9:8]		00h
	8230h	V8B3[7:0]								6Ch
	8330h	-	-	-	-	-	-	V9B3[9:8]		00h
	8430h	V9B3[7:0]								7Ch
	8530h	-	-	-	-	-	-	V10B3[9:8]		00h
	8630h	V10B3[7:0]								8Ch
	8730h	-	-	-	-	-	-	V11B3[9:8]		00h
	8830h	V11B3[7:0]								9Ch
	8930h	-	-	-	-	-	-	V12B3[9:8]		00h
	8A30h	V12B3[7:0]								BCh
	8B30h	-	-	-	-	-	-	V13B3[9:8]		00h
	8C30h	V13B3[7:0]								DCh
	8D30h	-	-	-	-	-	-	V14B3[9:8]		00h
	8E30h	V14B3[7:0]								FCh
	8F30h	-	-	-	-	-	-	V15B3[9:8]		01h
	9030h	V15B3[7:0]								3Ch
	9130h	-	-	-	-	-	-	V16B3[9:8]		01h
	9230h	V16B3[7:0]								7Ch
	9330h	-	-	-	-	-	-	V17B3[9:8]		01h
	9430h	V17B3[7:0]								BCh
	9530h	-	-	-	-	-	-	V18B3[9:8]		01h
	9630h	V18B3[7:0]								FCh
	9730h	-	-	-	-	-	-	V19B3[9:8]		02h
	9830h	V19B3[7:0]								3Ch
	9930h	-	-	-	-	-	-	V20B3[9:8]		02h
	9A30h	V20B3[7:0]								7Ch
	9B30h	-	-	-	-	-	-	V21B3[9:8]		02h
	9C30h	V21B3[7:0]								BCh
	9D30h	-	-	-	-	-	-	V22B3[9:8]		02h
	9E30h	V22B3[7:0]								FCh
	9F30h	-	-	-	-	-	-	V23B3[9:8]		03h
	A030h	V23B3[7:0]								3Ch
	A230h	-	-	-	-	-	-	V24B3[9:8]		03h
	A330h	V24B3[7:0]								7Ch
	A430h	-	-	-	-	-	-	V25B3[9:8]		03h
	A530h	V25B3[7:0]								BCh
	A630h	-	-	-	-	-	-	V26B3[9:8]		03h

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	A730h	V26B3[7:0]	FCh

Description	This command is used to adjust the gamma 2.2 correction for the red under normal display mode. For rb_GMA_13P1=0 Adjust B_0(darkest) via V0B3 Adjust B_1 via V1B3 Adjust B_3 via V2B3 Adjust B_7 via V3B3 Adjust B_11 via V4B3 Adjust B_15 via V5B3 Adjust B_19 via V6B3 Adjust B_23 via V7B3 Adjust B_27 via V8B3 Adjust B_31 via V9B3 Adjust B_35 via V10B3 Adjust B_39 via V11B3 Adjust B_47 via V12B3 Adjust B_55 via V13B3 Adjust B_63 via V14B3 Adjust B_79 via V15B3 Adjust B_95 via V16B3 Adjust B_111 via V17B3 Adjust B_127 via V18B3 Adjust B_143 via V19B3 Adjust B_159 via V20B3 Adjust B_175 via V21B3 Adjust B_191 via V22B3 Adjust B_207 via V23B3 Adjust B_223 via V24B3 Adjust B_239 via V25B3 Adjust B_255(brightest) via V26B3 For rb_GMA_13P1=1 Adjust B_0(darkest) via V0B3 Adjust B_1 via V1B3 Adjust B_3 via V2B3 Adjust B_7 via V3B3 Adjust B_11 via V4B3 Adjust B_15 via V5B3 Adjust B_31 via V9B3 Adjust B_63 via V14B3 Adjust B_95 via V16B3 Adjust B_127 via V18B3 Adjust B_159 via V20B3 Adjust B_191 via V22B3 Adjust B_255(brightest) via V26B3
Restriction	Set V0B3[9:0] < V1B3[9:0] < V2B3[9:0] < ... < V25B3[9:0] < V26B3[9:0], or V0B3[9:0] > V1B3[9:0] > V2B3[9:0] > ... > V25B3[9:0] > V26B3[9:0]

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(A930h~AB30h) VGMP/VGSP Control

R/W	Addr	D7	D6	D5	D4	D3	D2	D1	D0	HEX
R/W	A930h	VGMPTR3[7:0]								50h
R/W	AA30h	VGSPTR3[7:0]								18h
R/W	AB30h	rb_GMA_13P3	-	-	VGSPTR3[8]	-	-	-	VGMPTR3[8]	00h

Description

This command is for VGMP output level selection.

Bit	Value	VGMP Output level
VGMPTR3[8:0]	000h	2.0000V
	001h	2.0125V
	:	0.0125V / Step
	050h	3.0000V
	:	0.0125V / Step
	157h	6.2875V
	158h	6.3000V
	159h~1FFh	Reserved

This command is for VGSP output level selection.

Bit	Value	VGSP Output level
VGSPTR3[8:0]	000h	0.0000V
	001h	0.2125V
	:	0.0125V / Step
	005h	0.2625V
	:	0.0125V / Step
	158h	4.5000V
	159h~1FFh	Reserved
	000h	0.0000V

Restriction

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(FE30h): CMD Mode Switch

R/W	Addr	D7	D6	D5	D4	D3	D2	D1	D0	HEX
W	FE30h	CMD_Page[7:0]								00h

Description

This command is used to switch the Manufacture Command Pages and User Commands sets.

CMD_Page[7:0]	Description
00h (default)	User Command Set (UCS = CMD1)
10h	Manufacture Command Set Page Panel ID
12h	Manufacture Command Set Page SID
20h	Manufacture Command Set Page Panel
40h	Manufacture Command Set Page ABH Mode
82h	Manufacture Command Set Page Power
92h	Manufacture Command Set Page SD timing
50h	Manufacture Command Set Page Gamma1
60h	Manufacture Command Set Page Gamma2
30h	Manufacture Command Set Page Gamma3
52h	Manufacture Command Set Page Gamma4
70h	Manufacture Command Set Page GOA Timing 1
F0h	Manufacture Command Set Page GOA Timing 2
42h	Manufacture Command Set Page DBV
22h	Manufacture Command Set Page SES
80h	Manufacture Command Set Page APRC
90h	Manufacture Command Set Page ACL
62h	Manufacture Command Set Page CGM
C2h	Manufacture Command Set Page CGM LUT

Restriction

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(FF30h): Read CMD Status

R/W	Addr	D7	D6	D5	D4	D3	D2	D1	D0	HEX
R	FF30h	CMD_Status[7:0]								00h

Description	This command is used to read the status of Manufacture Command Pages. Please refer to FE00h
Restriction	-

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1.12MCS: CMD2 Page52, Gamma4 Settings

Instruction	R/W	Addr	D7	D6	D5	D4	D3	D2	D1	D0	HEX
GammaR_4	R/W	0052h	-	-	-	-	-	-	V0R4[9:8]		00h
GammaR_4	R/W	0152h	V0R4[7:0]								00h
GammaR_4	R/W	0252h	-	-	-	-	-	-	V1R4[9:8]		00h
GammaR_4	R/W	0352h	V1R4[7:0]								04h
GammaR_4	R/W	0452h	-	-	-	-	-	-	V2R4[9:8]		00h
GammaR_4	R/W	0552h	V2R4[7:0]								0Ch
GammaR_4	R/W	0652h	-	-	-	-	-	-	V3R4[9:8]		00h
GammaR_4	R/W	0752h	V3R4[7:0]								1Ch
GammaR_4	R/W	0852h	-	-	-	-	-	-	V4R4[9:8]		00h
GammaR_4	R/W	0952h	V4R4[7:0]								2Ch
GammaR_4	R/W	0A52h	-	-	-	-	-	-	V5R4[9:8]		00h
GammaR_4	R/W	0B52h	V5R4[7:0]								3Ch
GammaR_4	R/W	0C52h	-	-	-	-	-	-	V6R4[9:8]		00h
GammaR_4	R/W	0D52h	V6R4[7:0]								4Ch
GammaR_4	R/W	0E52h	-	-	-	-	-	-	V7R4[9:8]		00h
GammaR_4	R/W	0F52h	V7R4[7:0]								5Ch
GammaR_4	R/W	1052h	-	-	-	-	-	-	V8R4[9:8]		00h
GammaR_4	R/W	1152h	V8R4[7:0]								6Ch
GammaR_4	R/W	1252h	-	-	-	-	-	-	V9R4[9:8]		00h
GammaR_4	R/W	1352h	V9R4[7:0]								7Ch
GammaR_4	R/W	1452h	-	-	-	-	-	-	V10R4[9:8]		00h
GammaR_4	R/W	1552h	V10R4[7:0]								8Ch
GammaR_4	R/W	1652h	-	-	-	-	-	-	V11R4[9:8]		00h
GammaR_4	R/W	1752h	V11R4[7:0]								9Ch
GammaR_4	R/W	1852h	-	-	-	-	-	-	V12R4[9:8]		00h
GammaR_4	R/W	1952h	V12R4[7:0]								BCh
GammaR_4	R/W	1A52h	-	-	-	-	-	-	V13R4[9:8]		00h
GammaR_4	R/W	1B52h	V13R4[7:0]								DCh
GammaR_4	R/W	1C52h	-	-	-	-	-	-	V14R4[9:8]		00h
GammaR_4	R/W	1D52h	V14R4[7:0]								FCh
GammaR_4	R/W	1E52h	-	-	-	-	-	-	V15R4[9:8]		01h
GammaR_4	R/W	1F52h	V15R4[7:0]								3Ch
GammaR_4	R/W	2052h	-	-	-	-	-	-	V16R4[9:8]		01h
GammaR_4	R/W	2152h	V16R4[7:0]								7Ch
GammaR_4	R/W	2252h	-	-	-	-	-	-	V17R4[9:8]		01h
GammaR_4	R/W	2352h	V17R4[7:0]								BCh
GammaR_4	R/W	2452h	-	-	-	-	-	-	V18R4[9:8]		01h
GammaR_4	R/W	2552h	V18R4[7:0]								FCh
GammaR_4	R/W	2652h	-	-	-	-	-	-	V19R4[9:8]		02h
GammaR_4	R/W	2752h	V19R4[7:0]								3Ch
GammaR_4	R/W	2852h	-	-	-	-	-	-	V20R4[9:8]		02h
GammaR_4	R/W	2952h	V20R4[7:0]								7Ch
GammaR_4	R/W	2A52h	-	-	-	-	-	-	V21R4[9:8]		02h
GammaR_4	R/W	2B52h	V21R4[7:0]								BCh
GammaR_4	R/W	2D52h	-	-	-	-	-	-	V22R4[9:8]		02h
GammaR_4	R/W	2F52h	V22R4[7:0]								FCh
GammaR_4	R/W	3052h	-	-	-	-	-	-	V23R4[9:8]		03h
GammaR_4	R/W	3152h	V23R4[7:0]								3Ch

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GammaR_4	R/W	3252h	-	-	-	-	-	-	V24R4[9:8]	03h
GammaR_4	R/W	3352h	V24R4[7:0]							7Ch
GammaR_4	R/W	3452h	-	-	-	-	-	-	V25R4[9:8]	03h
GammaR_4	R/W	3552h	V25R4[7:0]							BCh
GammaR_4	R/W	3652h	-	-	-	-	-	-	V26R4[9:8]	03h
GammaR_4	R/W	3752h	V26R4[7:0]							FCh
GammaG_4	R/W	3852h	-	-	-	-	-	-	V0G4[9:8]	00h
GammaG_4	R/W	3952h	V0G4[7:0]							00h
GammaG_4	R/W	3A52h	-	-	-	-	-	-	V1G4[9:8]	00h
GammaG_4	R/W	3B52h	V1G4[7:0]							04h
GammaG_4	R/W	3D52h	-	-	-	-	-	-	V2G4[9:8]	00h
GammaG_4	R/W	3F52h	V2G4[7:0]							0Ch
GammaG_4	R/W	4052h	-	-	-	-	-	-	V3G4[9:8]	00h
GammaG_4	R/W	4152h	V3G4[7:0]							1Ch
GammaG_4	R/W	4252h	-	-	-	-	-	-	V4G4[9:8]	00h
GammaG_4	R/W	4352h	V4G4[7:0]							2Ch
GammaG_4	R/W	4452h	-	-	-	-	-	-	V5G4[9:8]	00h
GammaG_4	R/W	4552h	V5G4[7:0]							3Ch
GammaG_4	R/W	4652h	-	-	-	-	-	-	V6G4[9:8]	00h
GammaG_4	R/W	4752h	V6G4[7:0]							4Ch
GammaG_4	R/W	4852h	-	-	-	-	-	-	V7G4[9:8]	00h
GammaG_4	R/W	4952h	V7G4[7:0]							5Ch
GammaG_4	R/W	4A52h	-	-	-	-	-	-	V8G4[9:8]	00h
GammaG_4	R/W	4B52h	V8G4[7:0]							6Ch
GammaG_4	R/W	4C52h	-	-	-	-	-	-	V9G4[9:8]	00h
GammaG_4	R/W	4D52h	V9G4[7:0]							7Ch
GammaG_4	R/W	4E52h	-	-	-	-	-	-	V10G4[9:8]	00h
GammaG_4	R/W	4F52h	V10G4[7:0]							8Ch
GammaG_4	R/W	5052h	-	-	-	-	-	-	V11G4[9:8]	00h
GammaG_4	R/W	5252h	V11G4[7:0]							9Ch
GammaG_4	R/W	5352h	-	-	-	-	-	-	V12G4[9:8]	00h
GammaG_4	R/W	5452h	V12G4[7:0]							BCh
GammaG_4	R/W	5552h	-	-	-	-	-	-	V13G4[9:8]	00h
GammaG_4	R/W	5652h	V13G4[7:0]							DCh
GammaG_4	R/W	5752h	-	-	-	-	-	-	V14G4[9:8]	00h
GammaG_4	R/W	5852h	V14G4[7:0]							FCh
GammaG_4	R/W	5952h	-	-	-	-	-	-	V15G4[9:8]	01h
GammaG_4	R/W	5A52h	V15G4[7:0]							3Ch
GammaG_4	R/W	5B52h	-	-	-	-	-	-	V16G4[9:8]	01h
GammaG_4	R/W	5C52h	V16G4[7:0]							7Ch
GammaG_4	R/W	5D52h	-	-	-	-	-	-	V17G4[9:8]	01h
GammaG_4	R/W	5E52h	V17G4[7:0]							BCh
GammaG_4	R/W	5F52h	-	-	-	-	-	-	V18G4[9:8]	01h
GammaG_4	R/W	6052h	V18G4[7:0]							FCh
GammaG_4	R/W	6152h	-	-	-	-	-	-	V19G4[9:8]	02h
GammaG_4	R/W	6252h	V19G4[7:0]							3Ch
GammaG_4	R/W	6352h	-	-	-	-	-	-	V20G4[9:8]	02h
GammaG_4	R/W	6452h	V20G4[7:0]							7Ch
GammaG_4	R/W	6552h	-	-	-	-	-	-	V21G4[9:8]	02h
GammaG_4	R/W	6652h	V21G4[7:0]							BCh
GammaG_4	R/W	6752h	-	-	-	-	-	-	V22G4[9:8]	02h

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GammaG_4	R/W	6852h	V22G4[7:0]							FCh
GammaG_4	R/W	6952h	-	-	-	-	-	-	V23G4[9:8]	03h
GammaG_4	R/W	6A52h	V23G4[7:0]							3Ch
GammaG_4	R/W	6B52h	-	-	-	-	-	-	V24G4[9:8]	03h
GammaG_4	R/W	6C52h	V24G4[7:0]							7Ch
GammaG_4	R/W	6D52h	-	-	-	-	-	-	V25G4[9:8]	03h
GammaG_4	R/W	6E52h	V25G4[7:0]							BCh
GammaG_4	R/W	6F52h	-	-	-	-	-	-	V26G4[9:8]	03h
GammaG_4	R/W	7052h	V26G4[7:0]							FCh
GammaB_4	R/W	7152h	-	-	-	-	-	-	V0B4[9:8]	00h
GammaB_4	R/W	7252h	V0B4[7:0]							00h
GammaB_4	R/W	7352h	-	-	-	-	-	-	V1B4[9:8]	00h
GammaB_4	R/W	7452h	V1B4[7:0]							04h
GammaB_4	R/W	7552h	-	-	-	-	-	-	V2B4[9:8]	00h
GammaB_4	R/W	7652h	V2B4[7:0]							0Ch
GammaB_4	R/W	7752h	-	-	-	-	-	-	V3B4[9:8]	00h
GammaB_4	R/W	7852h	V3B4[7:0]							1Ch
GammaB_4	R/W	7952h	-	-	-	-	-	-	V4B4[9:8]	00h
GammaB_4	R/W	7A52h	V4B4[7:0]							2Ch
GammaB_4	R/W	7B52h	-	-	-	-	-	-	V5B4[9:8]	00h
GammaB_4	R/W	7C52h	V5B4[7:0]							3Ch
GammaB_4	R/W	7D52h	-	-	-	-	-	-	V6B4[9:8]	00h
GammaB_4	R/W	7E52h	V6B4[7:0]							4Ch
GammaB_4	R/W	7F52h	-	-	-	-	-	-	V7B4[9:8]	00h
GammaB_4	R/W	8052h	V7B4[7:0]							5Ch
GammaB_4	R/W	8152h	-	-	-	-	-	-	V8B4[9:8]	00h
GammaB_4	R/W	8252h	V8B4[7:0]							6Ch
GammaB_4	R/W	8352h	-	-	-	-	-	-	V9B4[9:8]	00h
GammaB_4	R/W	8452h	V9B4[7:0]							7Ch
GammaB_4	R/W	8552h	-	-	-	-	-	-	V10B4[9:8]	00h
GammaB_4	R/W	8652h	V10B4[7:0]							8Ch
GammaB_4	R/W	8752h	-	-	-	-	-	-	V11B4[9:8]	00h
GammaB_4	R/W	8852h	V11B4[7:0]							9Ch
GammaB_4	R/W	8952h	-	-	-	-	-	-	V12B4[9:8]	00h
GammaB_4	R/W	8A52h	V12B4[7:0]							BCh
GammaB_4	R/W	8B52h	-	-	-	-	-	-	V13B4[9:8]	00h
GammaB_4	R/W	8C52h	V13B4[7:0]							DCh
GammaB_4	R/W	8D52h	-	-	-	-	-	-	V14B4[9:8]	00h
GammaB_4	R/W	8E52h	V14B4[7:0]							FCh
GammaB_4	R/W	8F52h	-	-	-	-	-	-	V15B4[9:8]	01h
GammaB_4	R/W	9052h	V15B4[7:0]							3Ch
GammaB_4	R/W	9152h	-	-	-	-	-	-	V16B4[9:8]	01h
GammaB_4	R/W	9252h	V16B4[7:0]							7Ch
GammaB_4	R/W	9352h	-	-	-	-	-	-	V17B4[9:8]	01h
GammaB_4	R/W	9452h	V17B4[7:0]							BCh
GammaB_4	R/W	9552h	-	-	-	-	-	-	V18B4[9:8]	01h
GammaB_4	R/W	9652h	V18B4[7:0]							FCh
GammaB_4	R/W	9752h	-	-	-	-	-	-	V19B4[9:8]	02h
GammaB_4	R/W	9852h	V19B4[7:0]							3Ch
GammaB_4	R/W	9952h	-	-	-	-	-	-	V20B4[9:8]	02h
GammaB_4	R/W	9A52h	V20B4[7:0]							7Ch

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GammaB_4	R/W	9B52h	-	-	-	-	-	-	V21B4[9:8]	02h
GammaB_4	R/W	9C52h	V21B4[7:0]							BCh
GammaB_4	R/W	9D52h	-	-	-	-	-	-	V22B4[9:8]	02h
GammaB_4	R/W	9E52h	V22B4[7:0]							FCh
GammaB_4	R/W	9F52h	-	-	-	-	-	-	V23B4[9:8]	03h
GammaB_4	R/W	A052h	V23B4[7:0]							3Ch
GammaB_4	R/W	A252h	-	-	-	-	-	-	V24B4[9:8]	03h
GammaB_4	R/W	A352h	V24B4[7:0]							7Ch
GammaB_4	R/W	A452h	-	-	-	-	-	-	V25B4[9:8]	03h
GammaB_4	R/W	A552h	V25B4[7:0]							BCh
GammaB_4	R/W	A652h	-	-	-	-	-	-	V26B4[9:8]	03h
GammaB_4	R/W	A752h	V26B4[7:0]							FCh
VGMP/VGSP	R/W	A952h	VGMPTR4[7:0]							50h
VGMP/VGSP	R/W	AA52h	VGSPTR4[7:0]							18h
VGMP/VGSP	R/W	AB52h	GMA_13P4	-	-	VGSPTR4[8]	-	-	- | VGMPTR4[8]	00h
CMD Mode Switch	W	FE52h	-	-	-	CMD_Page_Selection[4:0]				01h
RD CMD Status	R	FF52h	-	-	-	Current_CMD_Page[4:0]				01h

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(0052h~3752h)Gamma 2.2 Corrections Set 4 for Red

R/W	Addr	D7	D6	D5	D4	D3	D2	D1	D0	HEX
R/W	0052h	-	-	-	-	-	-	V0R4[9:8]		00h
	0152h	V0R4[7:0]								00h
	0252h	-	-	-	-	-	-	V1R4[9:8]		00h
	0352h	V1R4[7:0]								04h
	0452h	-	-	-	-	-	-	V2R4[9:8]		00h
	0552h	V2R4[7:0]								0Ch
	0652h	-	-	-	-	-	-	V3R4[9:8]		00h
	0752h	V3R4[7:0]								1Ch
	0852h	-	-	-	-	-	-	V4R4[9:8]		00h
	0952h	V4R4[7:0]								2Ch
	0A52h	-	-	-	-	-	-	V5R4[9:8]		00h
	0B52h	V5R4[7:0]								3Ch
	0C52h	-	-	-	-	-	-	V6R4[9:8]		00h
	0D52h	V6R4[7:0]								4Ch
	0E52h	-	-	-	-	-	-	V7R4[9:8]		00h
	0F52h	V7R4[7:0]								5Ch
	1052h	-	-	-	-	-	-	V8R4[9:8]		00h
	1152h	V8R4[7:0]								6Ch
	1252h	-	-	-	-	-	-	V9R4[9:8]		00h
	1352h	V9R4[7:0]								7Ch
	1452h	-	-	-	-	-	-	V10R4[9:8]		00h
	1552h	V10R4[7:0]								8Ch
	1652h	-	-	-	-	-	-	V11R4[9:8]		00h
	1752h	V11R4[7:0]								9Ch
	1852h	-	-	-	-	-	-	V12R4[9:8]		00h
	1952h	V12R4[7:0]								BCh
	1A52h	-	-	-	-	-	-	V13R4[9:8]		00h
	1B52h	V13R4[7:0]								DCh
	1C52h	-	-	-	-	-	-	V14R4[9:8]		00h
	1D52h	V14R4[7:0]								FCh
	1E52h	-	-	-	-	-	-	V15R4[9:8]		01h
	1F52h	V15R4[7:0]								3Ch
	2052h	-	-	-	-	-	-	V16R4[9:8]		01h
	2152h	V16R4[7:0]								7Ch
	2252h	-	-	-	-	-	-	V17R4[9:8]		01h
	2352h	V17R4[7:0]								BCh
	2452h	-	-	-	-	-	-	V18R4[9:8]		01h
	2552h	V18R4[7:0]								FCh
	2652h	-	-	-	-	-	-	V19R4[9:8]		02h
	2752h	V19R4[7:0]								3Ch
	2852h	-	-	-	-	-	-	V20R4[9:8]		02h
	2952h	V20R4[7:0]								7Ch
	2A52h	-	-	-	-	-	-	V21R4[9:8]		02h
	2B52h	V21R4[7:0]								BCh
	2D52h	-	-	-	-	-	-	V22R4[9:8]		02h
	2F52h	V22R4[7:0]								FCh
	3052h	-	-	-	-	-	-	V23R4[9:8]		03h
	3152h	V23R4[7:0]								3Ch
	3252h	-	-	-	-	-	-	V24R4[9:8]		03h
	3352h	V24R4[7:0]								7Ch
	3452h	-	-	-	-	-	-	V25R4[9:8]		03h
	3552h	V25R4[7:0]								BCh
	3652h	-	-	-	-	-	-	V26R4[9:8]		03h

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	3752h	V26R4[7:0]	FCh

Description	This command is used to adjust the gamma 2.2 correction for the red under normal display mode. For rb_GMA_13P1=0 Adjust R_0(darkest) via V0R4 Adjust R_1 via V1R4 Adjust R_3 via V2R4 Adjust R_7 via V3R4 Adjust R_11 via V4R4 Adjust R_15 via V5R4 Adjust R_19 via V6R4 Adjust R_23 via V7R4 Adjust R_27 via V8R4 Adjust R_31 via V9R4 Adjust R_35 via V10R4 Adjust R_39 via V11R4 Adjust R_47 via V12R4 Adjust R_55 via V13R4 Adjust R_63 via V14R4 Adjust R_79 via V15R4 Adjust R_95 via V16R4 Adjust R_111 via V17R4 Adjust R_127 via V18R4 Adjust R_143 via V19R4 Adjust R_159 via V20R4 Adjust R_175 via V21R4 Adjust R_191 via V22R4 Adjust R_207 via V23R4 Adjust R_223 via V24R4 Adjust R_239 via V25R4 Adjust R_255(brightest) via V26R4 For rb_GMA_13P1=1 Adjust R_0(darkest) via V0R4 Adjust R_1 via V1R4 Adjust R_3 via V2R4 Adjust R_7 via V3R4 Adjust R_11 via V4R4 Adjust R_15 via V5R4 Adjust R_31 via V9R4 Adjust R_63 via V14R4 Adjust R_95 via V16R4 Adjust R_127 via V18R4 Adjust R_159 via V20R4 Adjust R_191 via V22R4 Adjust R_255(brightest) via V26R4
Restriction	Set V0R4[9:0] < V1R4[9:0] < V2R4[9:0] < ... < V25R4[9:0] < V26R4[9:0], or V0R4[9:0] > V1R4[9:0] > V2R4[9:0] > ... > V25R4[9:0] > V26R4[9:0]

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(3852h~7052h) Gamma 2.2 Corrections Set 4 for Green

R/W	Addr	D7	D6	D5	D4	D3	D2	D1	D0	HEX
R/W	3852h	-	-	-	-	-	-	V0G4[9:8]		00h
	3952h	V0G4[7:0]								00h
	3A52h	-	-	-	-	-	-	V1G4[9:8]		00h
	3B52h	V1G4[7:0]								04h
	3D52h	-	-	-	-	-	-	V2G4[9:8]		00h
	3F52h	V2G4[7:0]								0Ch
	4052h	-	-	-	-	-	-	V3G4[9:8]		00h
	4152h	V3G4[7:0]								1Ch
	4252h	-	-	-	-	-	-	V4G4[9:8]		00h
	4352h	V4G4[7:0]								2Ch
	4452h	-	-	-	-	-	-	V5G4[9:8]		00h
	4552h	V5G4[7:0]								3Ch
	4652h	-	-	-	-	-	-	V6G4[9:8]		00h
	4752h	V6G4[7:0]								4Ch
	4852h	-	-	-	-	-	-	V7G4[9:8]		00h
	4952h	V7G4[7:0]								5Ch
	4A52h	-	-	-	-	-	-	V8G4[9:8]		00h
	4B52h	V8G4[7:0]								6Ch
	4C52h	-	-	-	-	-	-	V9G4[9:8]		00h
	4D52h	V9G4[7:0]								7Ch
	4E52h	-	-	-	-	-	-	V10G4[9:8]		00h
	4F52h	V10G4[7:0]								8Ch
	5052h	-	-	-	-	-	-	V11G4[9:8]		00h
	5252h	V11G4[7:0]								9Ch
	5352h	-	-	-	-	-	-	V12G4[9:8]		00h
	5452h	V12G4[7:0]								BCh
	5552h	-	-	-	-	-	-	V13G4[9:8]		00h
	5652h	V13G4[7:0]								DCh
	5752h	-	-	-	-	-	-	V14G4[9:8]		00h
	5852h	V14G4[7:0]								FCh
	5952h	-	-	-	-	-	-	V15G4[9:8]		01h
	5A52h	V15G4[7:0]								3Ch
	5B52h	-	-	-	-	-	-	V16G4[9:8]		01h
	5C52h	V16G4[7:0]								7Ch
	5D52h	-	-	-	-	-	-	V17G4[9:8]		01h
	5E52h	V17G4[7:0]								BCh
	5F52h	-	-	-	-	-	-	V18G4[9:8]		01h
	6052h	V18G4[7:0]								FCh
	6152h	-	-	-	-	-	-	V19G4[9:8]		02h
	6252h	V19G4[7:0]								3Ch
	6352h	-	-	-	-	-	-	V20G4[9:8]		02h
	6452h	V20G4[7:0]								7Ch
	6552h	-	-	-	-	-	-	V21G4[9:8]		02h
	6652h	V21G4[7:0]								BCh
	6752h	-	-	-	-	-	-	V22G4[9:8]		02h
	6852h	V22G4[7:0]								FCh
	6952h	-	-	-	-	-	-	V23G4[9:8]		03h
	6A52h	V23G4[7:0]								3Ch
	6B52h	-	-	-	-	-	-	V24G4[9:8]		03h
	6C52h	V24G4[7:0]								7Ch
	6D52h	-	-	-	-	-	-	V25G4[9:8]		03h
	6E52h	V25G4[7:0]								BCh
	6F52h	-	-	-	-	-	-	V26G4[9:8]		03h

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	7052h	V26G4[7:0]	FCh

Description	This command is used to adjust the gamma 2.2 correction for the red under normal display mode. For rb_GMA_13P1=0 Adjust G_0(darkest) via V0G4 Adjust G_1 via V1G4 Adjust G_3 via V2G4 Adjust G_7 via V3G4 Adjust G_11 via V4G4 Adjust G_15 via V5G4 Adjust G_19 via V6G4 Adjust G_23 via V7G4 Adjust G_27 via V8G4 Adjust G_31 via V9G4 Adjust G_35 via V10G4 Adjust G_39 via V11G4 Adjust G_47 via V12G4 Adjust G_55 via V13G4 Adjust G_63 via V14G4 Adjust G_79 via V15G4 Adjust G_95 via V16G4 Adjust G_111 via V17G4 Adjust G_127 via V18G4 Adjust G_143 via V19G4 Adjust G_159 via V20G4 Adjust G_175 via V21G4 Adjust G_191 via V22G4 Adjust G_207 via V23G4 Adjust G_223 via V24G4 Adjust G_239 via V25G4 Adjust G_255(brightest) via V26G4 For rb_GMA_13P1=1 Adjust G_0(darkest) via V0G4 Adjust G_1 via V1G4 Adjust G_3 via V2G4 Adjust G_7 via V3G4 Adjust G_11 via V4G4 Adjust G_15 via V5G4 Adjust G_31 via V9G4 Adjust G_63 via V14G4 Adjust G_95 via V16G4 Adjust G_127 via V18G4 Adjust G_159 via V20G4 Adjust G_191 via V22G4 Adjust G_255(brightest) via V26G4
Restriction	Set V0G4[9:0] < V1G4[9:0] < V2G4[9:0] < ... < V25G4[9:0] < V26G4[9:0], or V0G4[9:0] > V1G4[9:0] > V2G4[9:0] > ... > V25G4[9:0] > V26G4[9:0]

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(7152h~A752h) Gamma 2.2 Corrections Set 4 for Blue

R/W	Addr	D7	D6	D5	D4	D3	D2	D1	D0	HEX
	7152h	-	-	-	-	-	-	V0B4[9:8]		00h
	7252h	V0B4[7:0]								00h
	7352h	-	-	-	-	-	-	V1B4[9:8]		00h
	7452h	V1B4[7:0]								04h
	7552h	-	-	-	-	-	-	V2B4[9:8]		00h
	7652h	V2B4[7:0]								0Ch
	7752h	-	-	-	-	-	-	V3B4[9:8]		00h
	7852h	V3B4[7:0]								1Ch
	7952h	-	-	-	-	-	-	V4B4[9:8]		00h
	7A52h	V4B4[7:0]								2Ch
	7B52h	-	-	-	-	-	-	V5B4[9:8]		00h
	7C52h	V5B4[7:0]								3Ch
	7D52h	-	-	-	-	-	-	V6B4[9:8]		00h
	7E52h	V6B4[7:0]								4Ch
	7F52h	-	-	-	-	-	-	V7B4[9:8]		00h
	8052h	V7B4[7:0]								5Ch
	8152h	-	-	-	-	-	-	V8B4[9:8]		00h
	8252h	V8B4[7:0]								6Ch
	8352h	-	-	-	-	-	-	V9B4[9:8]		00h
	8452h	V9B4[7:0]								7Ch
	8552h	-	-	-	-	-	-	V10B4[9:8]		00h
	8652h	V10B4[7:0]								8Ch
	8752h	-	-	-	-	-	-	V11B4[9:8]		00h
	8852h	V11B4[7:0]								9Ch
	8952h	-	-	-	-	-	-	V12B4[9:8]		00h
	8A52h	V12B4[7:0]								BCh
	8B52h	-	-	-	-	-	-	V13B4[9:8]		00h
	8C52h	V13B4[7:0]								DCh
	8D52h	-	-	-	-	-	-	V14B4[9:8]		00h
	8E52h	V14B4[7:0]								FCh
	8F52h	-	-	-	-	-	-	V15B4[9:8]		01h
	9052h	V15B4[7:0]								3Ch
	9152h	-	-	-	-	-	-	V16B4[9:8]		01h
R/W	9252h	V16B4[7:0]								7Ch
	9352h	-	-	-	-	-	-	V17B4[9:8]		01h
	9452h	V17B4[7:0]								BCh
	9552h	-	-	-	-	-	-	V18B4[9:8]		01h
	9652h	V18B4[7:0]								FCh
	9752h	-	-	-	-	-	-	V19B4[9:8]		02h
	9852h	V19B4[7:0]								3Ch
	9952h	-	-	-	-	-	-	V20B4[9:8]		02h
	9A52h	V20B4[7:0]								7Ch
	9B52h	-	-	-	-	-	-	V21B4[9:8]		02h
	9C52h	V21B4[7:0]								BCh
	9D52h	-	-	-	-	-	-	V22B4[9:8]		02h
	9E52h	V22B4[7:0]								FCh
	9F52h	-	-	-	-	-	-	V23B4[9:8]		03h
	A052h	V23B4[7:0]								3Ch
	A252h	-	-	-	-	-	-	V24B4[9:8]		03h
	A352h	V24B4[7:0]								7Ch
	A452h	-	-	-	-	-	-	V25B4[9:8]		03h
	A552h	V25B4[7:0]								BCh
	A652h	-	-	-	-	-	-	V26B4[9:8]		03h

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	A752h	V26B4[7:0]	FCh

Description	This command is used to adjust the gamma 2.2 correction for the red under normal display mode. For rb_GMA_13P1=0 Adjust B_0(darkest) via V0B4 Adjust B_1 via V1B4 Adjust B_3 via V2B4 Adjust B_7 via V3B4 Adjust B_11 via V4B4 Adjust B_15 via V5B4 Adjust B_19 via V6B4 Adjust B_23 via V7B4 Adjust B_27 via V8B4 Adjust B_31 via V9B4 Adjust B_35 via V10B4 Adjust B_39 via V11B4 Adjust B_47 via V12B4 Adjust B_55 via V13B4 Adjust B_63 via V14B4 Adjust B_79 via V15B4 Adjust B_95 via V16B4 Adjust B_111 via V17B4 Adjust B_127 via V18B4 Adjust B_143 via V19B4 Adjust B_159 via V20B4 Adjust B_175 via V21B4 Adjust B_191 via V22B4 Adjust B_207 via V23B4 Adjust B_223 via V24B4 Adjust B_239 via V25B4 Adjust B_255(brightest) via V26B4 For rb_GMA_13P1=1 Adjust B_0(darkest) via V0B4 Adjust B_1 via V1B4 Adjust B_3 via V2B4 Adjust B_7 via V3B4 Adjust B_11 via V4B4 Adjust B_15 via V5B4 Adjust B_31 via V9B4 Adjust B_63 via V14B4 Adjust B_95 via V16B4 Adjust B_127 via V18B4 Adjust B_159 via V20B4 Adjust B_191 via V22B4 Adjust B_255(brightest) via V26B4
Restriction	Set V0B4[9:0] < V1B4[9:0] < V2B4[9:0] < ... < V25B4[9:0] < V26B4[9:0], or V0B4[9:0] > V1B4[9:0] > V2B4[9:0] > ... > V25B4[9:0] > V26B4[9:0]

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(A952h~AB52h) VGMP/VGSP Control

R/W	Addr	D7	D6	D5	D4	D3	D2	D1	D0	HEX
R/W	A952h	VGMPTR4[7:0]								50h
R/W	AA52h	VGSPTR4[7:0]								18h
R/W	AB52h	rb_GMA_13P4	-	-	VGSPTR4[8]	-	-	-	VGMPTR4[8]	00h

Description

This command is for VGMP output level selection.

Bit	Value	VGMP Output level
VGMPTR4[8:0]	000h	2.0000V
	001h	2.0125V
	:	0.0125V / Step
	050h	3.0000V
	:	0.0125V / Step
	157h	6.2875V
	158h	6.3000V
	159h~1FFh	Reserved

This command is for VGSP output level selection.

Bit	Value	VGSP Output level
VGSPTR4[8:0]	000h	0.0000V
	001h	0.2125V
	:	0.0125V / Step
	005h	0.2625V
	:	0.0125V / Step
	158h	4.5000V
	159h~1FFh	Reserved
	000h	0.0000V

Restriction

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(FE52h): CMD Mode Switch

R/W	Addr	D7	D6	D5	D4	D3	D2	D1	D0	HEX
W	FE52h	CMD_Page[7:0]								00h

Description

This command is used to switch the Manufacture Command Pages and User Commands sets.

CMD_Page[7:0]	Description
00h (default)	User Command Set (UCS = CMD1)
10h	Manufacture Command Set Page Panel ID
12h	Manufacture Command Set Page SID
20h	Manufacture Command Set Page Panel
40h	Manufacture Command Set Page ABH Mode
82h	Manufacture Command Set Page Power
92h	Manufacture Command Set Page SD timing
50h	Manufacture Command Set Page Gamma1
60h	Manufacture Command Set Page Gamma2
30h	Manufacture Command Set Page Gamma3
52h	Manufacture Command Set Page Gamma4
70h	Manufacture Command Set Page GOA Timing 1
F0h	Manufacture Command Set Page GOA Timing 2
42h	Manufacture Command Set Page DBV
22h	Manufacture Command Set Page SES
80h	Manufacture Command Set Page APRC
90h	Manufacture Command Set Page ACL
62h	Manufacture Command Set Page CGM
C2h	Manufacture Command Set Page CGM LUT

Restriction

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(FF52h): Read CMD Status

R/W	Addr	D7	D6	D5	D4	D3	D2	D1	D0	HEX
R	FF52h	CMD_Status[7:0]								00h

Description	This command is used to read the status of Manufacture Command Pages. Please refer to FE00h
Restriction	-

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1.13MCS: CMD2 Page70, GOA Timing1 Control

Instruction	R/W	Addr	D7	D6	D5	D4	D3	D2	D1	D0	HEX
VSR1	R/W	0070h	VSR1_en	VSR1_rpt_en	VSR1_vrst_en	VSR1_wid_D_sel	VSR1_pwr_pol	VSR1_bk_pol	VSR1_pol	VSR1_SKIP_sel	08h
VSR1	R/W	0170h	-	VSR1_wid_L[10:8]			-	VSR1_prid[10:8]			00h
VSR1	R/W	0270h	VSR1_prid[7:0]								00h
VSR1	R/W	0370h	VSR1_wid_L[7:0]								00h
VSR1	R/W	0470h	VSR1_ofst1_ad_sel	VSR1_wid_D[9:8]		VSR1_ofst2[9:8]		VSR1_ofst1[10:8]			00h
VSR1	R/W	0570h	VSR1_ofst1[7:0]								00h
VSR1	R/W	0670h	VSR1_ofst2[7:0]								00h
VSR1	R/W	0770h	VSR1_wid_D[7:0]								00h
VSR2	R/W	0970h	VSR2_en	VSR2_rpt_en	VSR2_vrst_en	VSR2_wid_D_sel	VSR2_pwr_pol	VSR2_bk_pol	VSR2_pol	VSR2_SKIP_sel	08h
VSR2	R/W	0A70h	-	VSR2_wid_L[10:8]			-	VSR2_prid[10:8]			00h
VSR2	R/W	0B70h	VSR2_prid[7:0]								00h
VSR2	R/W	0C70h	VSR2_wid_L[7:0]								00h
VSR2	R/W	0D70h	VSR2_ofst1_ad_sel	VSR2_wid_D[9:8]		VSR2_ofst2[9:8]		VSR2_ofst1[10:8]			00h
VSR2	R/W	0E70h	VSR2_ofst1[7:0]								00h
VSR2	R/W	0F70h	VSR2_ofst2[7:0]								00h
VSR2	R/W	1070h	VSR2_wid_D[7:0]								00h
VSR3	R/W	1270h	VSR3_en	VSR3_rpt_en	VSR3_vrst_en	VSR3_wid_D_sel	VSR3_pwr_pol	VSR3_bk_pol	VSR3_pol	VSR3_SKIP_sel	08h
VSR3	R/W	1370h	-	VSR3_wid_L[10:8]			-	VSR3_prid[10:8]			00h
VSR3	R/W	1470h	VSR3_prid[7:0]								00h
VSR3	R/W	1570h	VSR3_wid_L[7:0]								00h
VSR3	R/W	1670h	VSR3_ofst1_ad_sel	VSR3_wid_D[9:8]		VSR3_ofst2[9:8]		VSR3_ofst1[10:8]			00h
VSR3	R/W	1770h	VSR3_ofst1[7:0]								00h
VSR3	R/W	1870h	VSR3_ofst2[7:0]								00h
VSR3	R/W	1970h	VSR3_wid_D[7:0]								00h
VSR4	R/W	1B70h	VSR4_e	VSR4_r	VSR4_vr	VSR4_wid	VSR4_p	VSR4_b	VSR4	VSR4_S	08

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			n	pt_en	st_en	_D_sel	wr_pol	k_pol	_pol	KIP_sel	h
VSR4	R/W	1C70h	-	VSR4_wid_L[10:8]			-	VSR4_prid[10:8]			00h
VSR4	R/W	1D70h	VSR4_prid[7:0]								00h
VSR4	R/W	1E70h	VSR4_wid_L[7:0]								00h
VSR4	R/W	1F70h	VSR4_ofst1_ad_sel	VSR4_wid_D[9:8]		VSR4_ofst2[9:8]		VSR4_ofst1[10:8]			00h
VSR4	R/W	2070h	VSR4_ofst1[7:0]								00h
VSR4	R/W	2170h	VSR4_ofst2[7:0]								00h
VSR4	R/W	2270h	VSR4_wid_D[7:0]								00h
VSR5	R/W	2470h	VSR5_en	VSR5_rpt_en	VSR5_vrst_en	VSR5_wid_D_sel	VSR5_pwr_pol	VSR5_bk_pol	VSR5_pol	VSR5_SKIP_sel	08h
VSR5	R/W	2570h	-	VSR5_wid_L[10:8]			-	VSR5_prid[10:8]			00h
VSR5	R/W	2670h	VSR5_prid[7:0]								00h
VSR5	R/W	2770h	VSR5_wid_L[7:0]								00h
VSR5	R/W	2870h	VSR5_ofst1_ad_sel	VSR5_wid_D[9:8]		VSR5_ofst2[9:8]		VSR5_ofst1[10:8]			00h
VSR5	R/W	2970h	VSR5_ofst1[7:0]								00h
VSR5	R/W	2A70h	VSR5_ofst2[7:0]								00h
VSR5	R/W	2B70h	VSR5_wid_D[7:0]								00h
VSR6	R/W	2F70h	VSR6_en	VSR6_rpt_en	VSR6_vrst_en	VSR6_wid_D_sel	VSR6_pwr_pol	VSR6_bk_pol	VSR6_pol	VSR6_SKIP_sel	08h
VSR6	R/W	3070h	-	VSR6_wid_L[10:8]			-	VSR6_prid[10:8]			00h
VSR6	R/W	3170h	VSR6_prid[7:0]								00h
VSR6	R/W	3270h	VSR6_wid_L[7:0]								00h
VSR6	R/W	3370h	VSR6_ofst1_ad_sel	VSR6_wid_D[9:8]		VSR6_ofst2[9:8]		VSR6_ofst1[10:8]			00h
VSR6	R/W	3470h	VSR6_ofst1[7:0]								00h
VSR6	R/W	3570h	VSR6_ofst2[7:0]								00h
VSR6	R/W	3670h	VSR6_wid_D[7:0]								00h
VSR7	R/W	3870h	VSR7_en	VSR7_rpt_en	VSR7_vrst_en	VSR7_wid_D_sel	VSR7_pwr_pol	VSR7_bk_pol	VSR7_pol	VSR7_SKIP_sel	08h
VSR7	R/W	3970h	-	VSR7_wid_L[10:8]			-	VSR7_prid[10:8]			00h
VSR7	R/W	3A70h	VSR7_prid[7:0]								00h
VSR7	R/W	3B70h	VSR7_wid_L[7:0]								00h

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VSR7	R/W	3D70h	VSR7_ofst1_ad_sel	VSR7_wid_D[9:8]		VSR7_ofst2[9:8]		VSR7_ofst1[10:8]			00h
VSR7	R/W	3F70h	VSR7_ofst1[7:0]								00h
VSR7	R/W	4070h	VSR7_ofst2[7:0]								00h
VSR7	R/W	4170h	VSR7_wid_D[7:0]								00h
VSR8	R/W	4370h	VSR8_en	VSR8_rpt_en	VSR8_vrst_en	VSR8_wid_D_sel	VSR8_pwr_pol	VSR8_bk_pol	VSR8_pol	VSR8_SKIP_sel	08h
VSR8	R/W	4470h	-	VSR8_wid_L[10:8]			-	VSR8_prid[10:8]			00h
VSR8	R/W	4570h	VSR8_prid[7:0]								00h
VSR8	R/W	4670h	VSR8_wid_L[7:0]								00h
VSR8	R/W	4770h	VSR8_ofst1_ad_sel	VSR8_wid_D[9:8]		VSR8_ofst2[9:8]		VSR8_ofst1[10:8]			00h
VSR8	R/W	4870h	VSR8_ofst1[7:0]								00h
VSR8	R/W	4970h	VSR8_ofst2[7:0]								00h
VSR8	R/W	4A70h	VSR8_wid_D[7:0]								00h
VST	R/W	4C70h	VST_en	-	-	VST_wid_D_sel	VST_pwr_pol	VST_ofst3	VST_pol	VST_SKIP_sel	08h
VST	R/W	4D70h	-	VST_wid_L[10:8]			-	-	-	-	00h
VST	R/W	4E70h	VST_wid_L[7:0]								00h
VST	R/W	4F70h	VST_ofst1_ad_sel	VST_wid_D[9:8]		VST_ofst2[9:8]		VST_ofst1[10:8]			00h
VST	R/W	5070h	VST_ofst1[7:0]								00h
VST	R/W	5270h	VST_wid_D[7:0]								00h
VEN	R/W	5370h	VEN_en	VEN_rpt_en	VEN_vrst_en	VEN_wid_D_sel	VEN_pwr_pol	VEN_bk_pol	VEN_pol	VEN_SKIP_sel	08h
VEN	R/W	5470h	VEN_ofst1_ad_sel	VEN_wid_D[9:8]		VEN_ofst2[9:8]		VEN_ofst1[10:8]			00h
VEN	R/W	5570h	VEN_ofst1[7:0]								00h
VEN	R/W	5670h	VEN_ofst2[7:0]								00h
VEN	R/W	5770h	VSTE_ofst3	-	-	-	-	-	-	-	00h
VEN	R/W	5870h	VEN_wid_D[7:0]								00h
VEN	R/W	5A70h	VSR_VRST_SEL[7:0]								00h
GOA_VST	R/W	5C70h	VST_ofst2[7:0]								00h
OUT_SEL	R/W	5F70h	VSTE_perid_exp[7:0]								00h

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OUT_SEL	R/W	6070h	VSTE_wid_L_exp[7:0]								00h
OUT_SEL	R/W	6170h	VSTE_user	VSTE_perid_exp[10:8]			-	VSTE_wid_L_exp[10:8]			00h
VSR9	R/W	6C70h	VSR9_en	VSR9_rpt_en	VSR9_vrst_en	VSR9_wid_D_sel	VSR9_pwr_pol	VSR9_bk_pol	VSR9_pol	VSR9_SKIP_sel	08h
VSR9	R/W	6D70h	VSR9_2_VSTE	VSR9_wid_L[10:8]			-	VSR9_prid[10:8]			00h
VSR9	R/W	6E70h	VSR9_prid[7:0]								00h
VSR9	R/W	6F70h	VSR9_wid_L[7:0]								00h
VSR9	R/W	7070h	VSR9_ofst1_ad_sel	VSR9_wid_D[9:8]		VSR9_ofst2[9:8]		VSR9_ofst1[10:8]			00h
VSR9	R/W	7170h	VSR9_ofst1[7:0]								00h
VSR9	R/W	7270h	VSR9_ofst2[7:0]								00h
VSR9	R/W	7370h	VSR9_wid_D[7:0]								00h
VSR10	R/W	7570h	VSR10_en	VSR10_rpt_en	VSR10_vrst_en	VSR10_wid_D_sel	VSR10_pwr_pol	VSR10_bk_pol	VSR10_pol	VSR10_SKIP_sel	08h
VSR10	R/W	7670h	VSR10_2_VSTE	VSR10_wid_L[10:8]			-	VSR10_prid[10:8]			00h
VSR10	R/W	7770h	VSR10_prid[7:0]								00h
VSR10	R/W	7870h	VSR10_wid_L[7:0]								00h
VSR10	R/W	7970h	VSR10_ofst1_ad_sel	VSR10_wid_D[9:8]		VSR10_ofst2[9:8]		VSR10_ofst1[10:8]			00h
VSR10	R/W	7A70h	VSR10_ofst1[7:0]								00h
VSR10	R/W	7B70h	VSR10_ofst2[7:0]								00h
VSR10	R/W	7C70h	VSR10_wid_D[7:0]								00h
VSR Keep Toggle	R/W	8670h	VSR1_kp_tg[7:0]								00h
VSR Keep Toggle	R/W	8770h	VSR2_kp_tg[7:0]								00h
VSR Keep Toggle	R/W	8870h	VSR3_kp_tg[7:0]								00h
VSR Keep Toggle	R/W	8970h	VSR4_kp_tg[7:0]								00h
VSR Keep Toggle	R/W	8A70h	VSR5_kp_tg[7:0]								00h
VSR Keep Toggle	R/W	8B70h	VSR6_kp_tg[7:0]								00h
VSR Keep Toggle	R/W	8C70h	VSR7_kp_tg[7:0]								00h
VSR Keep Toggle	R/W	8D70h	VSR8_kp_tg[7:0]								00h
VSR Keep Toggle	R/W	9070h	VEN_kp_tg[7:0]								00h

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VSR Keep Toggle	R/W	9170h	-	VSR2_kp_tg[10:8]			-	VSR1_kp_tg[10:8]	00h
VSR Keep Toggle	R/W	9270h	-	VSR4_kp_tg[10:8]			-	VSR3_kp_tg[10:8]	00h
VSR Keep Toggle	R/W	9370h	-	VSR6_kp_tg[10:8]			-	VSR5_kp_tg[10:8]	00h
VSR Keep Toggle	R/W	9470h	-	VSR8_kp_tg[10:8]			-	VSR7_kp_tg[10:8]	00h
VSR Keep Toggle	R/W	9570h	-	VSR10_kp_tg[10:8]			-	VSR9_kp_tg[10:8]	00h
VSR Keep Toggle	R/W	9670h	-	-	-	-	-	VEN_kp_tg[10:8]	00h
VSR & SW Output Selection	R/W	9870h	-	-	VSR_L01_map[5:0]				00h
VSR & SW Output Selection	R/W	9970h	-	-	VSR_L02_map[5:0]				00h
VSR & SW Output Selection	R/W	9A70h	-	-	VSR_L03_map[5:0]				00h
VSR & SW Output Selection	R/W	9B70h	-	-	VSR_L04_map[5:0]				00h
VSR & SW Output Selection	R/W	9C70h	-	-	VSR_L05_map[5:0]				00h
VSR & SW Output Selection	R/W	9D70h	-	-	VSR_L06_map[5:0]				00h
VSR & SW Output Selection	R/W	9E70h	-	-	VSR_L07_map[5:0]				00h
VSR & SW Output Selection	R/W	9F70h	-	-	VSR_L08_map[5:0]				00h
VSR & SW Output Selection	R/W	A070h	-	-	VSR_L09_map[5:0]				00h
VSR & SW Output Selection	R/W	A270h	-	-	VSR_L10_map[5:0]				00h
VSR & SW Output Selection	R/W	A370h	-	-	VSR_L11_map[5:0]				00h
VSR & SW Output Selection	R/W	A470h	-	-	VSR_L12_map[5:0]				00h
VSR & SW Output Selection	R/W	A570h	-	-	VSR_L13_map[5:0]				00h
VSR & SW Output Selection	R/W	A670h	-	-	VSR_L14_map[5:0]				00h
VSR & SW Output Selection	R/W	A770h	-	-	VSR_R01_map[5:0]				00h

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VSR & SW Output Selection	R/W	A970h	-	-	VSR_R02_map[5:0]			00h
VSR & SW Output Selection	R/W	AA70h	-	-	VSR_R03_map[5:0]			00h
VSR & SW Output Selection	R/W	AB70h	-	-	VSR_R04_map[5:0]			00h
VSR & SW Output Selection	R/W	AC70h	-	-	VSR_R05_map[5:0]			00h
VSR & SW Output Selection	R/W	AD70h	-	-	VSR_R06_map[5:0]			00h
VSR & SW Output Selection	R/W	AE70h	-	-	VSR_R07_map[5:0]			00h
VSR & SW Output Selection	R/W	AF70h	-	-	VSR_R08_map[5:0]			00h
VSR & SW Output Selection	R/W	B070h	-	-	VSR_R09_map[5:0]			00h
VSR & SW Output Selection	R/W	B170h	-	-	VSR_R10_map[5:0]			00h
VSR & SW Output Selection	R/W	B270h	-	-	VSR_R11_map[5:0]			00h
VSR & SW Output Selection	R/W	B370h	-	-	VSR_R12_map[5:0]			00h
VSR & SW Output Selection	R/W	B470h	-	-	VSR_R13_map[5:0]			00h
VSR & SW Output Selection	R/W	B570h	-	-	VSR_R14_map[5:0]			00h
VSR & SW Output Selection	R/W	B670h	LVSR_HZ[7:0]					00h
VSR & SW Output Selection	R/W	B770h	-	-	LVSR_HZ[13:8]			00h
VSR & SW Output Selection	R/W	B870h	RVSR_HZ[7:0]					00h
VSR & SW Output Selection	R/W	B970h	-	-	RVSR_HZ[13:8]			00h
VSR HDLY Control	R/W	C770h	VSR2_HDLAY[3:0]				VSR1_HDLAY[3:0]	00h
VSR HDLY Control	R/W	C870h	VSR4_HDLAY[3:0]				VSR3_HDLAY[3:0]	00h
VSR HDLY Control	R/W	C970h	VSR6_HDLAY[3:0]				VSR5_HDLAY[3:0]	00h
VSR HDLY Control	R/W	CA70h	-	-	-	-	VSTE_HDLAY[3:0]	00h

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CMD Mode Switch	W	FE70h	CMD_Page[7:0]	00h
RD CMD Status	R	FF70h	CMD_Status[7:0]	00h

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(0070h~0770h) GOA_VSR1

R/W	Addr	D7	D6	D5	D4	D3	D2	D1	D0	HEX
R/W	0070h	VSR1_en	VSR1_rpt_en	VSR1_vrst_en	VSR1_wid_D_sel	VSR1_pwr_pol	VSR1_bk_pol	VSR1_pol	VSR1_SKIP_sel	08h
	0170h	-	VSR1_wid_L[10:8]			-	VSR1_prid[10:8]			00h
	0270h	VSR1_prid[7:0]								00h
	0370h	VSR1_wid_L[7:0]								00h
	0470h	VSR1_ofst1_ad_sel	VSR1_wid_D[9:8]		VSR1_ofst2[9:8]		VSR1_ofst1[10:8]			00h
	0570h	VSR1_ofst1[7:0]								00h
	0670h	VSR1_ofst2[7:0]								00h
	0770h	VSR1_wid_D[7:0]								00h

Description

This command is GOA Timing Control for VSR1.

Bit	Description	Data
VSR1_en	VSR1 enable	0: VSR1 disable 1: VSR1 enable
VSR1_rpt_en	Enable the repeat function of VSR1	0: disable 1: enable
VSR1_vrst_en	Enable the Vsync reset function for VSR1	0: disable 1: enable
VSR1_wid_D_sel	The selection of count direction from Hsync for VSR1_wid_D	0: VSR1_wid_D seen as advance 1: VSR1_wid_D seen as delay
VSR1_pwr_pol	The Polarity of VSR1 during display off area	0: VSR1 negative polarity 1: VSR1 positive polarity
VSR1_bk_pol	The Polarity of VSR1 during blanking area	0: VSR1 negative polarity 1: VSR1 positive polarity
VSR1_pol	The Polarity of VSR1 during active area	0: VSR1 negative polarity 1: VSR1 positive polarity
VSR1_SKIP_sel	VSR1 status for skip frame	0: normal operation 1: keep the last state before skip frame

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Bit	Description	Data
VSR1_prid[10:0]	Period that VSR1 repeats (unit: Hsync)	Note: do not exceed vtotal.

Bit	Description	Data
VSR1_wid_L[10:0]	Low pulse width of VSR1 inside a period. (unit: Hsync)	Note: do not exceed VSR1_period.

Bit	Description	Data
VSR1_ofst1_ad_sel	The selection of count direction from Hsync for VSR1_oftst1	0: VSR1_ofst1 seen as advance 1: VSR1_ ofst1 seen as delay
VSR1_ofst1[10:0]	Time delay/advance from VSR1 to last back proch line each frame(unit: Hsync)	Note: do not exceed vtotal.

Bit	Description	Data
VSR1_ofst2[9:0]	Time delay from VSR1(falling) start to hsync. (unit: pixel clock)	Note: do not exceed htotal.

Bit	Description	Data
VSR1_wid_D[9:0]	Time delay from VSR1(rising) start to hsync. ((unit: pixel clock)	Note: do not exceed htotal.

Restriction	

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(0970h~1070h) GOA_VSR2

R/W	Addr	D7	D6	D5	D4	D3	D2	D1	D0	HEX
R/W	0970h	VSR2_en	VSR2_rpt_en	VSR2_vrst_en	VSR2_wid_D_sel	VSR2_pwr_pol	VSR2_bk_pol	VSR2_pol	VSR2_SKIP_sel	08h
	0A70h	-	VSR2_wid_L[10:8]			-	VSR2_prid[10:8]			00h
	0B70h	VSR2_prid[7:0]								00h
	0C70h	VSR2_wid_L[7:0]								00h
	0D70h	VSR2_ofst1_ad_sel	VSR2_wid_D[9:8]		VSR2_ofst2[9:8]		VSR2_ofst1[10:8]			00h
	0E70h	VSR2_ofst1[7:0]								00h
	0F70h	VSR2_ofst2[7:0]								00h
	1070h	VSR2_wid_D[7:0]								00h

Description

This command is GOA Timing Control for VSR2.

Bit	Description	Data
VSR2_en	VSR2 enable	0: VSR2 disable 1: VSR2 enable
VSR2_rpt_en	Enable the repeat function of VSR2	0: disable 1: enable
VSR2_vrst_en	Enable the Vsync reset function for VSR2	0: disable 1: enable
VSR2_wid_D_sel	The selection of count direction from Hsync for VSR2_wid_D	0: VSR2_wid_D seen as advance 1: VSR2_wid_D seen as delay
VSR2_pwr_pol	The Polarity of VSR2 during display off area	0: VSR2 negative polarity 1: VSR2 positive polarity
VSR2_bk_pol	The Polarity of VSR2 during blanking area	0: VSR2 negative polarity 1: VSR2 positive polarity
VSR2_pol	The Polarity of VSR2 during active area	0: VSR2 negative polarity 1: VSR2 positive polarity
VSR2_SKIP_sel	VSR2 status for skip frame	0: normal operation 1: keep the last state before skip frame

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Bit	Description	Data
VSR2_prid[10:0]	Period that VSR2 repeats (unit: Hsync)	Note: do not exceed vtotal.

Bit	Description	Data
VSR2_wid_L[10:0]	Low pulse width of VSR2 inside a period. (unit: Hsync)	Note: do not exceed VSR2_period.

Bit	Description	Data
VSR2_ofst1_ad_sel	The selection of count direction from Hsync for VSR2_oftst1	0: VSR2_ofst1 seen as advance 1: VSR2_ ofst1 seen as delay
VSR2_ofst1[10:0]	Time delay/advance from VSR2 to last back proch line each frame(unit: Hsync)	Note: do not exceed vtotal.

Bit	Description	Data
VSR2_ofst2[9:0]	Time delay from VSR2(falling) start to hsync. (unit: pixel clock)	Note: do not exceed htotal.

Bit	Description	Data
VSR2_wid_D[9:0]	Time delay from VSR2(rising) start to hsync. ((unit: pixel clock)	Note: do not exceed htotal.

Restriction	

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(1270h~1970h) GOA_VSR3

R/W	Addr	D7	D6	D5	D4	D3	D2	D1	D0	HEX
R/W	1270h	VSR3_en	VSR3_rpt_en	VSR3_vrst_en	VSR3_wid_D_sel	VSR3_pwr_pol	VSR3_bk_pol	VSR3_pol	VSR3_SKIP_sel	08h
	1370h	-	VSR3_wid_L[10:8]			-	VSR3_prid[10:8]			00h
	1470h	VSR3_prid[7:0]								00h
	1570h	VSR3_wid_L[7:0]								00h
	1670h	VSR3_ofst1_ad_sel	VSR3_wid_D[9:8]		VSR3_ofst2[9:8]		VSR3_ofst1[10:8]			00h
	1770h	VSR3_ofst1[7:0]								00h
	1870h	VSR3_ofst2[7:0]								00h
	1970h	VSR3_wid_D[7:0]								00h

Description

This command is GOA Timing Control for VSR3.

Bit	Description	Data
VSR3_en	VSR3 enable	0: VSR3 disable 1: VSR3 enable
VSR3_rpt_en	Enable the repeat function of VSR3	0: disable 1: enable
VSR3_vrst_en	Enable the Vsync reset function for VSR3	0: disable 1: enable
VSR3_wid_D_sel	The selection of count direction from Hsync for VSR3_wid_D	0: VSR3_wid_D seen as advance 1: VSR3_wid_D seen as delay
VSR3_pwr_pol	The Polarity of VSR3 during display off area	0: VSR3 negative polarity 1: VSR3 positive polarity
VSR3_bk_pol	The Polarity of VSR3 during blanking area	0: VSR3 negative polarity 1: VSR3 positive polarity
VSR3_pol	The Polarity of VSR3 during active area	0: VSR3 negative polarity 1: VSR3 positive polarity
VSR3_SKIP_sel	VSR3 status for skip frame	0: normal operation 1: keep the last state before skip frame

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Bit	Description	Data
VSR3_prid[10:0]	Period that VSR3 repeats (unit: Hsync)	Note: do not exceed vtotal.

Bit	Description	Data
VSR3_wid_L[10:0]	Low pulse width of VSR3 inside a period. (unit: Hsync)	Note: do not exceed VSR3_period.

Bit	Description	Data
VSR3_ofst1_ad_sel	The selection of count direction from Hsync for VSR3_oftst1	0: VSR3_ofst1 seen as advance 1: VSR3_ofst1 seen as delay
VSR3_ofst1[10:0]	Time delay/advance from VSR3 to last back proch line each frame(unit: Hsync)	Note: do not exceed vtotal.

Bit	Description	Data
VSR3_ofst2[9:0]	Time delay from VSR3(falling) start to hsync. (unit: pixel clock)	Note: do not exceed htotal.

Bit	Description	Data
VSR3_wid_D[9:0]	Time delay from VSR3(rising) start to hsync. ((unit: pixel clock)	Note: do not exceed htotal.

Restriction	

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(1B70h~2270h) GOA_VSR4

R/W	Addr	D7	D6	D5	D4	D3	D2	D1	D0	HEX
R/W	1B70h	VSR4_en	VSR4_rpt_en	VSR4_vrst_en	VSR4_wid_D_sel	VSR4_pwr_pol	VSR4_bk_pol	VSR4_pol	VSR4_SKIP_sel	08h
	1C70h	-	VSR4_wid_L[10:8]			-	VSR4_prid[10:8]			00h
	1D70h	VSR4_prid[7:0]								00h
	1E70h	VSR4_wid_L[7:0]								00h
	1F70h	VSR4_ofst1_ad_sel	VSR4_wid_D[9:8]		VSR4_ofst2[9:8]		VSR4_ofst1[10:8]			00h
	2070h	VSR4_ofst1[7:0]								00h
	2170h	VSR4_ofst2[7:0]								00h
	2270h	VSR4_wid_D[7:0]								00h

Description

This command is GOA Timing Control for VSR4.

Bit	Description	Data
VSR4_en	VSR4 enable	0: VSR4 disable 1: VSR4 enable
VSR4_rpt_en	Enable the repeat function of VSR4	0: disable 1: enable
VSR4_vrst_en	Enable the Vsync reset function for VSR4	0: disable 1: enable
VSR4_wid_D_sel	The selection of count direction from Hsync for VSR4_wid_D	0: VSR4_wid_D seen as advance 1: VSR4_wid_D seen as delay
VSR4_pwr_pol	The Polarity of VSR4 during display off area	0: VSR4 negative polarity 1: VSR4 positive polarity
VSR4_bk_pol	The Polarity of VSR4 during blanking area	0: VSR4 negative polarity 1: VSR4 positive polarity
VSR4_pol	The Polarity of VSR4 during active area	0: VSR4 negative polarity 1: VSR4 positive polarity
VSR4_SKIP_sel	VSR4 status for skip frame	0: normal operation 1: keep the last state before skip frame

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Bit	Description	Data
VSR4_prid[10:0]	Period that VSR4 repeats (unit: Hsync)	Note: do not exceed vtotal.

Bit	Description	Data
VSR4_wid_L[10:0]	Low pulse width of VSR4 inside a period. (unit: Hsync)	Note: do not exceed VSR4_period.

Bit	Description	Data
VSR4_ofst1_ad_sel	The selection of count direction from Hsync for VSR4_oftst1	0: VSR4_ofst1 seen as advance 1: VSR4_ ofst1 seen as delay
VSR4_ofst1[10:0]	Time delay/advance from VSR4 to last back proch line each frame(unit: Hsync)	Note: do not exceed vtotal.

Bit	Description	Data
VSR4_ofst2[9:0]	Time delay from VSR4(falling) start to hsync. (unit: pixel clock)	Note: do not exceed htotal.

Bit	Description	Data
VSR4_wid_D[9:0]	Time delay from VSR4(rising) start to hsync. ((unit: pixel clock)	Note: do not exceed htotal.

Restriction	

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(2470h~2B70h) GOA_VSR5

R/W	Addr	D7	D6	D5	D4	D3	D2	D1	D0	HEX
R/W	2470h	VSR5_en	VSR5_rpt_en	VSR5_vrst_en	VSR5_wid_D_sel	VSR5_pwr_pol	VSR5_bk_pol	VSR5_pol	VSR5_SKIP_sel	08h
	2570h	-	VSR5_wid_L[10:8]			-	VSR5_prid[10:8]			00h
	2670h	VSR5_prid[7:0]								00h
	2770h	VSR5_wid_L[7:0]								00h
	2870h	VSR5_ofst1_ad_sel	VSR5_wid_D[9:8]		VSR5_ofst2[9:8]		VSR5_ofst1[10:8]			00h
	2970h	VSR5_ofst1[7:0]								00h
	2A70h	VSR5_ofst2[7:0]								00h
	2B70h	VSR5_wid_D[7:0]								00h

Description

This command is GOA Timing Control for VSR5.

Bit	Description	Data
VSR5_en	VSR5 enable	0: VSR5 disable 1: VSR5 enable
VSR5_rpt_en	Enable the repeat function of VSR5	0: disable 1: enable
VSR5_vrst_en	Enable the Vsync reset function for VSR5	0: disable 1: enable
VSR5_wid_D_sel	The selection of count direction from Hsync for VSR5_wid_D	0: VSR5_wid_D seen as advance 1: VSR5_wid_D seen as delay
VSR5_pwr_pol	The Polarity of VSR5 during display off area	0: VSR5 negative polarity 1: VSR5 positive polarity
VSR5_bk_pol	The Polarity of VSR5 during blanking area	0: VSR5 negative polarity 1: VSR5 positive polarity
VSR5_pol	The Polarity of VSR5 during active area	0: VSR5 negative polarity 1: VSR5 positive polarity
VSR5_SKIP_sel	VSR5 status for skip frame	0: normal operation 1: keep the last state before skip frame

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Bit	Description	Data
VSR5_prid[10:0]	Period that VSR5 repeats (unit: Hsync)	Note: do not exceed vtotal.

Bit	Description	Data
VSR5_wid_L[10:0]	Low pulse width of VSR5 inside a period. (unit: Hsync)	Note: do not exceed VSR5_period.

Bit	Description	Data
VSR5_ofst1_ad_sel	The selection of count direction from Hsync for VSR5_oftst1	0: VSR5_ofst1 seen as advance 1: VSR5_ ofst1 seen as delay
VSR5_ofst1[10:0]	Time delay/advance from VSR5 to last back proch line each frame(unit: Hsync)	Note: do not exceed vtotal.

Bit	Description	Data
VSR5_ofst2[9:0]	Time delay from VSR5(falling) start to hsync. (unit: pixel clock)	Note: do not exceed htotal.

Bit	Description	Data
VSR5_wid_D[9:0]	Time delay from VSR5(rising) start to hsync. ((unit: pixel clock)	Note: do not exceed htotal.

Restriction	

CONFIDENTIAL

(2F70h~3670h) GOA_VSR6

R/W	Addr	D7	D6	D5	D4	D3	D2	D1	D0	HEX
R/W	2F70h	VSR6_en	VSR6_rpt_en	VSR6_vrst_en	VSR6_wid_D_sel	VSR6_pwr_pol	VSR6_bk_pol	VSR6_pol	VSR6_SKIP_sel	08h
	3070h	-	VSR6_wid_L[10:8]			-	VSR6_prid[10:8]			00h
	3170h	VSR6_prid[7:0]								00h
	3270h	VSR6_wid_L[7:0]								00h
	3370h	VSR6_ofst1_ad_sel	VSR6_wid_D[9:8]		VSR6_ofst2[9:8]		VSR6_ofst1[10:8]			00h
	3470h	VSR6_ofst1[7:0]								00h
	3570h	VSR6_ofst2[7:0]								00h
	3670h	VSR6_wid_D[7:0]								00h

Description

This command is GOA Timing Control for VSR6.

Bit	Description	Data
VSR6_en	VSR6 enable	0: VSR6 disable 1: VSR6 enable
VSR6_rpt_en	Enable the repeat function of VSR6	0: disable 1: enable
VSR6_vrst_en	Enable the Vsync reset function for VSR6	0: disable 1: enable
VSR6_wid_D_sel	The selection of count direction from Hsync for VSR6_wid_D	0: VSR6_wid_D seen as advance 1: VSR6_wid_D seen as delay
VSR6_pwr_pol	The Polarity of VSR6 during display off area	0: VSR6 negative polarity 1: VSR6 positive polarity
VSR6_bk_pol	The Polarity of VSR6 during blanking area	0: VSR6 negative polarity 1: VSR6 positive polarity
VSR6_pol	The Polarity of VSR6 during active area	0: VSR6 negative polarity 1: VSR6 positive polarity
VSR6_SKIP_sel	VSR6 status for skip frame	0: normal operation 1: keep the last state before skip frame

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Bit	Description	Data
VSR6_prid[10:0]	Period that VSR6 repeats (unit: Hsync)	Note: do not exceed vtotal.

Bit	Description	Data
VSR6_wid_L[10:0]	Low pulse width of VSR6 inside a period. (unit: Hsync)	Note: do not exceed VSR6_period.

Bit	Description	Data
VSR6_ofst1_ad_sel	The selection of count direction from Hsync for VSR6_oftst1	0: VSR6_ofst1 seen as advance 1: VSR6_ ofst1 seen as delay
VSR6_ofst1[10:0]	Time delay/advance from VSR6 to last back proch line each frame(unit: Hsync)	Note: do not exceed vtotal.

Bit	Description	Data
VSR6_ofst2[9:0]	Time delay from VSR6(falling) start to hsync. (unit: pixel clock)	Note: do not exceed htotal.

Bit	Description	Data
VSR6_wid_D[9:0]	Time delay from VSR6(rising) start to hsync. ((unit: pixel clock)	Note: do not exceed htotal.

Restriction	

CONFIDENTIAL

(3870h~4170h) GOA_VSR7

R/W	Addr	D7	D6	D5	D4	D3	D2	D1	D0	HEX
R/W	3870h	VSR7_en	VSR7_rpt_en	VSR7_vrst_en	VSR7_wid_D_sel	VSR7_pwr_pol	VSR7_bk_pol	VSR7_pol	VSR7_SKIP_sel	08h
	3970h	-	VSR7_wid_L[10:8]			-	VSR7_prid[10:8]			00h
	3A70h	VSR7_prid[7:0]								00h
	3B70h	VSR7_wid_L[7:0]								00h
	3D70h	VSR7_ofst1_ad_sel	VSR7_wid_D[9:8]		VSR7_ofst2[9:8]		VSR7_ofst1[10:8]			00h
	3F70h	VSR7_ofst1[7:0]								00h
	4070h	VSR7_ofst2[7:0]								00h
	4170h	VSR7_wid_D[7:0]								00h

Description

This command is GOA Timing Control for VSR7.

Bit	Description	Data
VSR7_en	VSR7 enable	0: VSR7 disable 1: VSR7 enable
VSR7_rpt_en	Enable the repeat function of VSR7	0: disable 1: enable
VSR7_vrst_en	Enable the Vsync reset function for VSR7	0: disable 1: enable
VSR7_wid_D_sel	The selection of count direction from Hsync for VSR7_wid_D	0: VSR7_wid_D seen as advance 1: VSR7_wid_D seen as delay
VSR7_pwr_pol	The Polarity of VSR7 during display off area	0: VSR7 negative polarity 1: VSR7 positive polarity
VSR7_bk_pol	The Polarity of VSR7 during blanking area	0: VSR7 negative polarity 1: VSR7 positive polarity
VSR7_pol	The Polarity of VSR7 during active area	0: VSR7 negative polarity 1: VSR7 positive polarity
VSR7_SKIP_sel	VSR7 status for skip frame	0: normal operation 1: keep the last state before skip frame

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Bit	Description	Data
VSR7_prid[10:0]	Period that VSR7 repeats (unit: Hsync)	Note: do not exceed vtotal.

Bit	Description	Data
VSR7_wid_L[10:0]	Low pulse width of VSR7 inside a period. (unit: Hsync)	Note: do not exceed VSR7_period.

Bit	Description	Data
VSR7_ofst1_ad_sel	The selection of count direction from Hsync for VSR7_oftst1	0: VSR7_ofst1 seen as advance 1: VSR7_ ofst1 seen as delay
VSR7_ofst1[10:0]	Time delay/advance from VSR7 to last back proch line each frame(unit: Hsync)	Note: do not exceed vtotal.

Bit	Description	Data
VSR7_ofst2[9:0]	Time delay from VSR7(falling) start to hsync. (unit: pixel clock)	Note: do not exceed htotal.

Bit	Description	Data
VSR7_wid_D[9:0]	Time delay from VSR7(rising) start to hsync. ((unit: pixel clock)	Note: do not exceed htotal.

Restriction	

CONFIDENTIAL

(4370h~4A70h) GOA_VSR8

R/W	Addr	D7	D6	D5	D4	D3	D2	D1	D0	HEX
R/W	4370h	VSR8_en	VSR8_rpt_en	VSR8_vrst_en	VSR8_wid_D_sel	VSR8_pwr_pol	VSR8_bk_pol	VSR8_pol	VSR8_SKIP_sel	08h
	4470h	-	VSR8_wid_L[10:8]			-	VSR8_prid[10:8]			00h
	4570h	VSR8_prid[7:0]								00h
	4670h	VSR8_wid_L[7:0]								00h
	4770h	VSR8_ofst1_ad_sel	VSR8_wid_D[9:8]		VSR8_ofst2[9:8]		VSR8_ofst1[10:8]			00h
	4870h	VSR8_ofst1[7:0]								00h
	4970h	VSR8_ofst2[7:0]								00h
	4A70h	VSR8_wid_D[7:0]								00h

Description

This command is GOA Timing Control for VSR8.

Bit	Description	Data
VSR8_en	VSR8 enable	0: VSR8 disable 1: VSR8 enable
VSR8_rpt_en	Enable the repeat function of VSR8	0: disable 1: enable
VSR8_vrst_en	Enable the Vsync reset function for VSR8	0: disable 1: enable
VSR8_wid_D_sel	The selection of count direction from Hsync for VSR8_wid_D	0: VSR8_wid_D seen as advance 1: VSR8_wid_D seen as delay
VSR8_pwr_pol	The Polarity of VSR8 during display off area	0: VSR8 negative polarity 1: VSR8 positive polarity
VSR8_bk_pol	The Polarity of VSR8 during blanking area	0: VSR8 negative polarity 1: VSR8 positive polarity
VSR8_pol	The Polarity of VSR8 during active area	0: VSR8 negative polarity 1: VSR8 positive polarity
VSR8_SKIP_sel	VSR8 status for skip frame	0: normal operation 1: keep the last state before skip frame

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Bit	Description	Data
VSR8_prid[10:0]	Period that VSR8 repeats (unit: Hsync)	Note: do not exceed vtotal.

Bit	Description	Data
VSR8_wid_L[10:0]	Low pulse width of VSR8 inside a period. (unit: Hsync)	Note: do not exceed VSR8_period.

Bit	Description	Data
VSR8_ofst1_ad_sel	The selection of count direction from Hsync for VSR8_oftst1	0: VSR8_ofst1 seen as advance 1: VSR8_ ofst1 seen as delay
VSR8_ofst1[10:0]	Time delay/advance from VSR8 to last back proch line each frame(unit: Hsync)	Note: do not exceed vtotal.

Bit	Description	Data
VSR8_ofst2[9:0]	Time delay from VSR8(falling) start to hsync. (unit: pixel clock)	Note: do not exceed htotal.

Bit	Description	Data
VSR8_wid_D[9:0]	Time delay from VSR8(rising) start to hsync. ((unit: pixel clock)	Note: do not exceed htotal.

Restriction	

CONFIDENTIAL

(4C70h~5270h, 5C70h) GOA_VST

R/W	Addr	D7	D6	D5	D4	D3	D2	D1	D0	HEX
R/W	4C70h	VST_en	-	-	VST_wid_D_sel	VST_pwr_pol	-	VST_pol	VST_SKIP_sel	08h
	4D70h	-	VST_wid_L[10:8]			-	-	-	-	00h
	4E70h	VST_wid_L[7:0]								00h
	4F70h	VST_ofst1_ad_sel	VST_wid_D[9:8]		VST_ofst2[9:8]		VST_ofst1[10:8]			00h
	5070h	VST_ofst1[7:0]								00h
	5270h	VST_wid_D[7:0]								00h
	5C70h	VST_ofst2[7:0]								00h

Description

This command is GOA Timing Control for VST.

Bit	Description	Data
VST_en	VST enable	0: VST disable 1: VST enable
VST_wid_D_sel	The selection of count direction from Hsync for VST_wid_D	0: VST_wid_D seen as advance 1: VST_wid_D seen as delay
VST_pwr_pol	The Polarity of VST during display off area	0: VST negative polarity 1: VST positive polarity
VST_pol	The Polarity of VST during active area	0: VST negative polarity 1: VST positive polarity
VST_SKIP_sel	VST status for skip frame	0: normal operation 1: keep the last state before skip frame

Bit	Description	Data
VST_wid_L[10:0]	Low pulse width of VST inside a period. (unit: Hsync)	Note: do not exceed VST_period.

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Bit	Description	Data
VST_ofst2[9:0]	Time delay from VST(falling) start to hsync. (unit: pixel clock)	Note: do not exceed htotal.

Bit	Description	Data
VST_ofst1_ad_sel	The selection of count direction from Hsync for VST_oftst1	0: VST_ofst1 seen as advance 1: VST_ ofst1 seen as delay
VST_ofst1[10:0]	Time delay/advance from VST to last back proch line each frame(unit: Hsync)	Note: do not exceed vtotal.

Bit	Description	Data
VST_wid_D[9:0]	Time delay from VST(rising) start to hsync. ((unit: pixel clock)	Note: do not exceed htotal.

Restriction	

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(5370h~5870h) GOA_VEN

R/W	Addr	D7	D6	D5	D4	D3	D2	D1	D0	HEX
R/W	5370h	VEN_en	VEN_rpt_en	VEN_vrst_en	VEN_wid_D_sel	VEN_pwr_pol	VEN_bk_pol	VEN_pol	VEN_SKIP_sel	08h
	5470h	VEN_ofst1_ad_sel	VEN_wid_D[9:8]		VEN_ofst2[9:8]		VEN_ofst1[10:8]			00h
	5570h	VEN_ofst1[7:0]								00h
	5670h	VEN_ofst2[7:0]								00h
	5870h	VEN_wid_D[7:0]								00h

Description

This command is GOA Timing Control for VEN.

Bit	Description	Data
VEN_en	VEN enable	0: VEN disable 1: VEN enable
VEN_rpt_en	Enable the repeat function of VEN	0: disable 1: enable
VEN_vrst_en	Enable the Vsync reset function for VEN	0: disable 1: enable
VEN_wid_D_sel	The selection of count direction from Hsync for VEN_wid_D	0: VEN_wid_D seen as advance 1: VEN_wid_D seen as delay
VEN_pwr_pol	The Polarity of VEN during display off area	0: VEN negative polarity 1: VEN positive polarity
VEN_bk_pol	The Polarity of VEN during blanking area	0: VEN negative polarity 1: VEN positive polarity
VEN_pol	The Polarity of VEN during active area	0: VEN negative polarity 1: VEN positive polarity
VEN_SKIP_sel	VEN status for skip frame	0: normal operation 1: keep the last state before skip frame

Bit	Description	Data
VEN_wid_D[10:0]	Time delay from VEN(rising) start to hsync. ((unit: pixel clock)	Note: do not exceed htotal.

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Bit	Description	Data
VEN_ofst2[10:0]	Time delay from VEN(falling) start to hsync. (unit: pixel clock)	Note: do not exceed htotal.

Bit	Description	Data
VEN_ofst1_ad_sel	The selection of count direction from Hsync for VEN_oftst1	0: VEN_ofst1 seen as advance 1: VEN_ ofst1 seen as delay
VEN_ofst1[10:0]	Time delay/advance from VEN to last back proch line each frame(unit: Hsync)	Note: do not exceed vtotal.

Restriction	

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(5A70h) GOA Reset Selection

R/W	Addr	D7	D6	D5	D4	D3	D2	D1	D0	HEX
R/W	5A70h	VSR_VRST_SEL[7:0]								00h

Description

This command is used to set VSRx reset position when VSRx toggle repetitively. Note that VSRx_vrst_en shall be equal to 0.

Bit	Description	Data
VSR_VRST_SET[7]	Set VSR8 reset position at back porch +/- VSR8_ofst1	0: ON 1: OFF
VSR_VRST_SET[6]	Set VSR7 reset position at back porch +/- VSR7_ofst1	
VSR_VRST_SET[5]	Set VSR6 reset position at back porch +/- VSR6_ofst1	
VSR_VRST_SET[4]	Set VSR5 reset position at back porch +/- VSR5_ofst1	
VSR_VRST_SET[3]	Set VSR4 reset position at back porch +/- VSR4_ofst1	
VSR_VRST_SET[2]	Set VSR3 reset position at back porch +/- VSR3_ofst1	
VSR_VRST_SET[1]	Set VSR2 reset position at back porch +/- VSR2_ofst1	
VSR_VRST_SET[0]	Set VSR1 reset position at back porch +/- VSR1_ofst1	

Restriction

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(5F70h~6170h) BC_Perid&Wid

R/W	Addr	D7	D6	D5	D4	D3	D2	D1	D0	HEX
R/W	5F70h	VSTE_perid_exp[7:0]								00h
	6070h	VSTE_wid_L_exp[7:0]								00h
	6170h	-	VSTE_perid_exp[10:8]			-	VSTE_wid_L_exp[10:8]			00h

Description	This command is used to set VSTE period and low duration. Bit: VSTE_perid_exp[10:0] — Description: VSTE period — Data: 0~2047 Bit: VSTE_wid_L_exp[10:0] — Description: VSTE low duration — Data: 0~2047
Restriction	

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(6C70h~7370h) GOA_VSR9

R/W	Addr	D7	D6	D5	D4	D3	D2	D1	D0	HEX
R/W	6C70h	VSR9_en	VSR9_rpt_en	VSR9_vrst_en	VSR9_wid_D_sel	VSR9_pwr_pol	VSR9_bk_pol	VSR9_pol	VSR9_SKIP_sel	08h
	6D70h	-	VSR9_wid_L[10:8]			-	VSR9_prid[10:8]			00h
	6E70h	VSR9_prid[7:0]								00h
	6F70h	VSR9_wid_L[7:0]								00h
	7070h	VSR9_ofst1_ad_sel	VSR9_wid_D[9:8]		VSR9_ofst2[9:8]		VSR9_ofst1[10:8]			00h
	7170h	VSR9_ofst1[7:0]								00h
	7270h	VSR9_ofst2[7:0]								00h
	7370h	VSR9_wid_D[7:0]								00h

Description

This command is GOA Timing Control for VSR9.

Bit	Description	Data
VSR9_en	VSR9 enable	0: VSR9 disable 1: VSR9 enable
VSR9_rpt_en	Enable the repeat function of VSR9	0: disable 1: enable
VSR9_vrst_en	Enable the Vsync reset function for VSR9	0: disable 1: enable
VSR9_wid_D_sel	The selection of count direction from Hsync for VSR9_wid_D	0: VSR9_wid_D seen as advance 1: VSR9_wid_D seen as delay
VSR9_pwr_pol	The Polarity of VSR9 during display off area	0: VSR9 negative polarity 1: VSR9 positive polarity
VSR9_bk_pol	The Polarity of VSR9 during blanking area	0: VSR9 negative polarity 1: VSR9 positive polarity
VSR9_pol	The Polarity of VSR9 during active area	0: VSR9 negative polarity 1: VSR9 positive polarity
VSR9_SKIP_sel	VSR9 status for skip frame	0: normal operation 1: keep the last state before skip frame

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Bit	Description	Data
VSR9_prid[10:0]	Period that VSR9 repeats (unit: Hsync)	Note: do not exceed vtotal.

Bit	Description	Data
VSR9_wid_L[10:0]	Low pulse width of VSR9 inside a period. (unit: Hsync)	Note: do not exceed VSR9_period.

Bit	Description	Data
VSR9_ofst1_ad_sel	The selection of count direction from Hsync for VSR9_oftst1	0: VSR9_ofst1 seen as advance 1: VSR9_ ofst1 seen as delay
VSR9_ofst1[10:0]	Time delay/advance from VSR9 to last back proch line each frame(unit: Hsync)	Note: do not exceed vtotal.

Bit	Description	Data
VSR9_ofst2[9:0]	Time delay from VSR9(falling) start to hsync. (unit: pixel clock)	Note: do not exceed htotal.

Bit	Description	Data
VSR9_wid_D[9:0]	Time delay from VSR9(rising) start to hsync. ((unit: pixel clock)	Note: do not exceed htotal.

Restriction	

CONFIDENTIAL

(7570h~7C70h) GOA_VSR10

R/W	Addr	D7	D6	D5	D4	D3	D2	D1	D0	HEX
R/W	7570h	VSR10_en	VSR10_rpt_en	VSR10_vrst_en	VSR10_wid_D_sel	VSR10_pwr_pol	VSR10_bk_pol	VSR10_pol	VSR10_SKIP_sel	08h
	7670h	-	VSR10_wid_L[10:8]			-	VSR10_prid[10:8]			00h
	7770h	VSR10_prid[7:0]								00h
	7870h	VSR10_wid_L[7:0]								00h
	7970h	VSR10_ofst1_ad_sel	VSR10_wid_D[9:8]		VSR10_ofst2[9:8]		VSR10_ofst1[10:8]			00h
	7A70h	VSR10_ofst1[7:0]								00h
	7B70h	VSR10_ofst2[7:0]								00h
	7C70h	VSR10_wid_D[7:0]								00h

Description

This command is GOA Timing Control for VSR10.

Bit	Description	Data
VSR10_en	VSR10 enable	0: VSR10 disable 1: VSR10 enable
VSR10_rpt_en	Enable the repeat function of VSR10	0: disable 1: enable
VSR10_vrst_en	Enable the Vsync reset function for VSR10	0: disable 1: enable
VSR10_wid_D_sel	The selection of count direction from Hsync for VSR10_wid_D	0: VSR10_wid_D seen as advance 1: VSR10_wid_D seen as delay
VSR10_pwr_pol	The Polarity of VSR10 during display off area	0: VSR10 negative polarity 1: VSR10 positive polarity
VSR10_bk_pol	The Polarity of VSR10 during blanking area	0: VSR10 negative polarity 1: VSR10 positive polarity
VSR10_pol	The Polarity of VSR10 during active area	0: VSR10 negative polarity 1: VSR10 positive polarity
VSR10_SKIP_sel	VSR10 status for skip frame	0: normal operation 1: keep the last state before skip frame

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Bit	Description	Data
VSR10_prid[10:0]	Period that VSR10 repeats (unit: Hsync)	Note: do not exceed vtotal.

Bit	Description	Data
VSR10_wid_L[10:0]	Low pulse width of VSR10 inside a period. (unit: Hsync)	Note: do not exceed VSR10_period.

Bit	Description	Data
VSR10_ofst1_ad_sel	The selection of count direction from Hsync for VSR10_oftst1	0: VSR10_ofst1 seen as advance 1: VSR10_ ofst1 seen as delay
VSR10_ofst1[10:0]	Time delay/advance from VSR10 to last back proch line each frame(unit: Hsync)	Note: do not exceed vtotal.

Bit	Description	Data
VSR10_ofst2[9:0]	Time delay from VSR10(falling) start to hsync. (unit: pixel clock)	Note: do not exceed htotal.

Bit	Description	Data
VSR10_wid_D[9:0]	Time delay from VSR10(rising) start to hsync. ((unit: pixel clock)	Note: do not exceed htotal.

Restriction	

CONFIDENTIAL

(8670h~9670h) VSR Keep Toggle Setting

R/W	Addr	D7	D6	D5	D4	D3	D2	D1	D0	HEX
R/W	8670h	VSR1_kp_tgl[7:0]								00h
R/W	8770h	VSR2_kp_tgl[7:0]								00h
R/W	8870h	VSR3_kp_tgl[7:0]								00h
R/W	8970h	VSR4_kp_tgl[7:0]								00h
R/W	8A70h	VSR5_kp_tgl[7:0]								00h
R/W	8B70h	VSR6_kp_tgl[7:0]								00h
R/W	8C70h	VSR7_kp_tgl[7:0]								00h
R/W	8D70h	VSR8_kp_tgl[7:0]								00h
R/W	9070h	VEN_kp_tgl[7:0]								00h
R/W	9170h	-	VSR2_kp_tgl[10:8]			-	VSR1_kp_tgl[10:8]			00h
R/W	9270h	-	VSR4_kp_tgl[10:8]			-	VSR3_kp_tgl[10:8]			00h
R/W	9370h	-	VSR6_kp_tgl[10:8]			-	VSR5_kp_tgl[10:8]			00h
R/W	9470h	-	VSR8_kp_tgl[10:8]			-	VSR7_kp_tgl[10:8]			00h
R/W	9570h	-	VSR10_kp_tgl[10:8]			-	VSR9_kp_tgl[10:8]			00h
R/W	9670h	-					VEN_kp_tgl[10:8]			00h

Description

Parameter	Description
VSR1_kp_tg[10:0]	Keep toggling line number of VSR1_kp_tgl from VSR1_ofst1 position (unit Hsync)
VSR2_kp_tg[10:0]	Keep toggling line number of VSR2_kp_tgl from VSR2_ofst1 position (unit Hsync)
VSR3_kp_tg[10:0]	Keep toggling line number of VSR3_kp_tgl from VSR3_ofst1 position (unit Hsync)
VSR4_kp_tg[10:0]	Keep toggling line number of VSR4_kp_tgl from VSR4_ofst1 position (unit Hsync)
VSR5_kp_tg[10:0]	Keep toggling line number of VSR5_kp_tgl from VSR5_ofst1 position (unit Hsync)
VSR6_kp_tg[10:0]	Keep toggling line number of VSR6_kp_tgl from VSR6_ofst1 position (unit Hsync)
VSR7_kp_tg[10:0]	Keep toggling line number of VSR7_kp_tgl from VSR7_ofst1 position (unit Hsync)
VSR8_kp_tg[10:0]	Keep toggling line number of VSR8_kp_tgl from VSR8_ofst1 position (unit Hsync)
VSR9_kp_tg[10:0]	Keep toggling line number of VSR9_kp_tgl from VSR9_ofst1 position (unit Hsync)
VSR10_kp_tg[10:0]	Keep toggling line number of VSR10_kp_tgl from VSR10_ofst1 position (unit Hsync)
VEN_kp_tg[10:0]	Keep toggling line number of VEN_kp_tgl from VEN_ofst1 position (unit Hsync)

Restriction

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(9870h~B970h) VSR and SW Output Selection

R/W	Addr	D7	D6	D5	D4	D3	D2	D1	D0	HEX
R/W	9870h	-	-	VSR_L01_map[5:0]						00h
R/W	9970h	-	-	VSR_L02_map[5:0]						00h
R/W	9A70h	-	-	VSR_L03_map[5:0]						00h
R/W	9B70h	-	-	VSR_L04_map[5:0]						00h
R/W	9C70h	-	-	VSR_L05_map[5:0]						00h
R/W	9D70h	-	-	VSR_L06_map[5:0]						00h
R/W	9E70h	-	-	VSR_L07_map[5:0]						00h
R/W	9F70h	-	-	VSR_L08_map[5:0]						00h
R/W	A070h	-	-	VSR_L09_map[5:0]						00h
R/W	A270h	-	-	VSR_L10_map[5:0]						00h
R/W	A370h	-	-	VSR_L11_map[5:0]						00h
R/W	A470h	-	-	VSR_L12_map[5:0]						00h
R/W	A570h	-	-	VSR_L13_map[5:0]						00h
R/W	A670h	-	-	VSR_L14_map[5:0]						00h
R/W	A770h	-	-	VSR_R01_map[5:0]						00h
R/W	A970h	-	-	VSR_R02_map[5:0]						00h
R/W	AA70h	-	-	VSR_R03_map[5:0]						00h
R/W	AB70h	-	-	VSR_R04_map[5:0]						00h
R/W	AC70h	-	-	VSR_R05_map[5:0]						00h
R/W	AD70h	-	-	VSR_R06_map[5:0]						00h
R/W	AE70h	-	-	VSR_R07_map[5:0]						00h
R/W	AF70h	-	-	VSR_R08_map[5:0]						00h
R/W	B070h	-	-	VSR_R09_map[5:0]						00h
R/W	B170h	-	-	VSR_R10_map[5:0]						00h
R/W	B270h	-	-	VSR_R11_map[5:0]						00h
R/W	B370h	-	-	VSR_R12_map[5:0]						00h
R/W	B470h	-	-	VSR_R13_map[5:0]						00h
R/W	B570h	-	-	VSR_R14_map[5:0]						00h
R/W	B670h	LVSR_HZ[7:0]								00h
R/W	B770h	-	-	LVSR_HZ[13:8]						00h
R/W	B870h	RVSR_HZ[7:0]								00h
R/W	B970h	-	-	RVSR_HZ[13:8]						00h

Description

VSR_L*_map[5:0]: to select VSR_L* pad output mapping as the following table
VSR_R*_map[5:0]: to select VSR_R* pad output mapping as the following table
LVSR_HZ[13:0]: to assign Hi-Z state to VSR_L* pad
RVSR_HZ[13:0]: to assign Hi-Z state to VSR_R* pad

VSR_L*_map[5:0] VSR_R*_map[5:0]	Description
0h	Pad keeps High
1h	Pad references to internal VSR1 timing
2h	Pad references to internal VSR2 timing
3h	Pad references to internal VSR3 timing
4h	Pad references to internal VSR4 timing
5h	Pad references to internal VSR5 timing

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6h	Pad references to internal VSR6 timing
7h	Pad references to internal VSR7 timing
8h	Pad references to internal VSR8 timing
9h	Pad references to internal VST timing
Ah	Pad references to internal VEN timing
Bh	Pad references to internal VSR9 timing
Ch	Pad references to internal VSR10 timing
Dh~1Fh	Reserved
20h	Pad keeps Low
21h	Pad references to internal SW1 timing
22h	Pad references to internal SW2 timing
23h	Pad references to internal SW3 timing
24h	Pad references to internal SW4 timing
25h	Pad references to internal SW5 timing
26h	Pad references to internal SW6 timing
27h	Pad references to internal SW7 timing
28h	Pad references to internal SW8 timing
29h	Pad references to internal SW9 timing
2Ah	Pad references to internal SW10 timing
2Bh	Pad references to internal SW11 timing
2Ch	Pad references to internal SW12 timing
other	Pad keeps High

Restriction	

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(C770h~CA70h) VSR HDLY Control

R/W	Addr	D7	D6	D5	D4	D3	D2	D1	D0	HEX
R/W	C770h	VSR2_HDLAY[3:0]				VSR1_HDLAY[3:0]				00h
R/W	C870h	VSR4_HDLAY[3:0]				VSR3_HDLAY[3:0]				00h
R/W	C970h	VSR6_HDLAY[3:0]				VSR5_HDLAY[3:0]				00h
R/W	CA70h	-	-			VSTE_HDLAY[3:0]				00h

Description	This command is used to set the H-delay of VSR1~VSR6/VSTE for VSR and SW Output Selection.

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(FE70h): CMD Mode Switch

R/W	Addr	D7	D6	D5	D4	D3	D2	D1	D0	HEX
W	FE70h	CMD_Page[7:0]								00h

Description

This command is used to switch the Manufacture Command Pages and User Commands sets.

CMD_Page[7:0]	Description
00h (default)	User Command Set (UCS = CMD1)
10h	Manufacture Command Set Page Panel ID
12h	Manufacture Command Set Page SID
20h	Manufacture Command Set Page Panel
40h	Manufacture Command Set Page ABH Mode
82h	Manufacture Command Set Page Power
92h	Manufacture Command Set Page SD timing
50h	Manufacture Command Set Page Gamma1
60h	Manufacture Command Set Page Gamma2
30h	Manufacture Command Set Page Gamma3
52h	Manufacture Command Set Page Gamma4
70h	Manufacture Command Set Page GOA Timing 1
F0h	Manufacture Command Set Page GOA Timing 2
42h	Manufacture Command Set Page DBV
22h	Manufacture Command Set Page SES
80h	Manufacture Command Set Page APRC
90h	Manufacture Command Set Page ACL
62h	Manufacture Command Set Page CGM
C2h	Manufacture Command Set Page CGM LUT

Restriction

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(FF70h): Read CMD Status

R/W	Addr	D7	D6	D5	D4	D3	D2	D1	D0	HEX
R	FF70h	CMD_Status[7:0]								00h

Description	This command is used to read the status of Manufacture Command Pages. Please refer to FE00h
Restriction	-

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1.14MCS: CMD2 PageF0, GOA Timing2 Control

Instruction	R/W	Addr	D7	D6	D5	D4	D3	D2	D1	D0	HEX
VSR1_B	R/W	00F0h	VSR1_B_en	VSR1_B_rpt_en	VSR1_B_vrst_en	VSR1_B_wid_D_sel	VSR1_B_pwr_pol	VSR1_B_bk_pol	VSR1_B_pol	VSR1_B_SKIP_sel	08h
VSR1_B	R/W	01F0h	-	VSR1_B_wid_L[10:8]			-	VSR1_B_prid[10:8]			00h
VSR1_B	R/W	02F0h	VSR1_B_prid[7:0]								00h
VSR1_B	R/W	03F0h	VSR1_B_wid_L[7:0]								00h
VSR1_B	R/W	04F0h	VSR1_B_ofst1_ad_sel	VSR1_B_wid_D[9:8]		VSR1_B_ofst2[9:8]		VSR1_B_ofst1[10:8]			00h
VSR1_B	R/W	05F0h	VSR1_B_ofst1[7:0]								00h
VSR1_B	R/W	06F0h	VSR1_B_ofst2[7:0]								00h
VSR1_B	R/W	07F0h	VSR1_B_wid_D[7:0]								00h
VSR2_B	R/W	09F0h	VSR2_B_en	VSR2_B_rpt_en	VSR2_B_vrst_en	VSR2_B_wid_D_sel	VSR2_B_pwr_pol	VSR2_B_bk_pol	VSR2_B_pol	VSR2_B_SKIP_sel	08h
VSR2_B	R/W	0AF0h	-	VSR2_B_wid_L[10:8]			-	VSR2_B_prid[10:8]			00h
VSR2_B	R/W	0BF0h	VSR2_B_prid[7:0]								00h
VSR2_B	R/W	0CF0h	VSR2_B_wid_L[7:0]								00h
VSR2_B	R/W	0DF0h	VSR2_B_ofst1_ad_sel	VSR2_B_wid_D[9:8]		VSR2_B_ofst2[9:8]		VSR2_B_ofst1[10:8]			00h
VSR2_B	R/W	0EF0h	VSR2_B_ofst1[7:0]								00h
VSR2_B	R/W	0FF0h	VSR2_B_ofst2[7:0]								00h
VSR2_B	R/W	10F0h	VSR2_B_wid_D[7:0]								00h
VSR3_B	R/W	12F0h	VSR3_B_en	VSR3_B_rpt_en	VSR3_B_vrst_en	VSR3_B_wid_D_sel	VSR3_B_pwr_pol	VSR3_B_bk_pol	VSR3_B_pol	VSR3_B_SKIP_sel	08h
VSR3_B	R/W	13F0h	-	VSR3_B_wid_L[10:8]			-	VSR3_B_prid[10:8]			00h
VSR3_B	R/W	14F0h	VSR3_B_prid[7:0]								00h
VSR3_B	R/W	15F0h	VSR3_B_wid_L[7:0]								00h
VSR3_B	R/W	16F0h	VSR3_B_ofst1_ad_sel	VSR3_B_wid_D[9:8]		VSR3_B_ofst2[9:8]		VSR3_B_ofst1[10:8]			00h
VSR3_B	R/W	17F0h	VSR3_B_ofst1[7:0]								00h
VSR3_B	R/W	18F0h	VSR3_B_ofst2[7:0]								00h
VSR3_B	R/W	19F0h	VSR3_B_wid_D[7:0]								00h
VSR4_B	R/W	1BF0h	VSR4_B_en	VSR4_B_rpt_en	VSR4_B_vrst_en	VSR4_B_wid_D_sel	VSR4_B_pwr_pol	VSR4_B_bk_pol	VSR4_B_pol	VSR4_B_SKIP_sel	08h
VSR4_B	R/W	1CF0h	-	VSR4_B_wid_L[10:8]			-	VSR4_B_prid[10:8]			00h
VSR4_B	R/W	1DF0h	VSR4_B_prid[7:0]								00h
VSR4_B	R/W	1EF0h	VSR4_B_wid_L[7:0]								00h
VSR4_B	R/W	1FF0h	VSR4_B_ofst1_ad_sel	VSR4_B_wid_D[9:8]		VSR4_B_ofst2[9:8]		VSR4_B_ofst1[10:8]			00h
VSR4_B	R/W	20F0h	VSR4_B_ofst1[7:0]								00h
VSR4_B	R/W	21F0h	VSR4_B_ofst2[7:0]								00h
VSR4_B	R/W	22F0h	VSR4_B_wid_D[7:0]								00h
VSR5_B	R/W	24F0h	VSR5_B_en	VSR5_B_rpt_en	VSR5_B_vrst_en	VSR5_B_wid_D_sel	VSR5_B_pwr_pol	VSR5_B_bk_pol	VSR5_B_pol	VSR5_B_SKIP_sel	08h

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VSR5_B	R/W	25F0h	-	VSR5_B_wid_L[10:8]			-	VSR5_B_prid[10:8]			00h
VSR5_B	R/W	26F0h	VSR5_B_prid[7:0]								00h
VSR5_B	R/W	27F0h	VSR5_B_wid_L[7:0]								00h
VSR5_B	R/W	28F0h	VSR5_B_ofst1_ad_sel	VSR5_B_wid_D[9:8]		VSR5_B_ofst2[9:8]		VSR5_B_ofst1[10:8]			00h
VSR5_B	R/W	29F0h	VSR5_B_ofst1[7:0]								00h
VSR5_B	R/W	2AF0h	VSR5_B_ofst2[7:0]								00h
VSR5_B	R/W	2BF0h	VSR5_B_wid_D[7:0]								00h
VSR6_B	R/W	2FF0h	VSR6_B_en	VSR6_B_rpt_en	VSR6_B_vrst_en	VSR6_B_wid_D_sel	VSR6_B_pwr_pol	VSR6_B_bk_pol	VSR6_B_pol	VSR6_B_SKIP_sel	08h
VSR6_B	R/W	30F0h	-	VSR6_B_wid_L[10:8]			-	VSR6_B_prid[10:8]			00h
VSR6_B	R/W	31F0h	VSR6_B_prid[7:0]								00h
VSR6_B	R/W	32F0h	VSR6_B_wid_L[7:0]								00h
VSR6_B	R/W	33F0h	VSR6_B_ofst1_ad_sel	VSR6_B_wid_D[9:8]		VSR6_B_ofst2[9:8]		VSR6_B_ofst1[10:8]			00h
VSR6_B	R/W	34F0h	VSR6_B_ofst1[7:0]								00h
VSR6_B	R/W	35F0h	VSR6_B_ofst2[7:0]								00h
VSR6_B	R/W	36F0h	VSR6_B_wid_D[7:0]								00h
VSR7_B	R/W	38F0h	VSR7_B_en	VSR7_B_rpt_en	VSR7_B_vrst_en	VSR7_B_wid_D_sel	VSR7_B_pwr_pol	VSR7_B_bk_pol	VSR7_B_pol	VSR7_B_SKIP_sel	08h
VSR7_B	R/W	39F0h	-	VSR7_B_wid_L[10:8]			-	VSR7_B_prid[10:8]			00h
VSR7_B	R/W	3AF0h	VSR7_B_prid[7:0]								00h
VSR7_B	R/W	3BF0h	VSR7_B_wid_L[7:0]								00h
VSR7_B	R/W	3DF0h	VSR7_B_ofst1_ad_sel	VSR7_B_wid_D[9:8]		VSR7_B_ofst2[9:8]		VSR7_B_ofst1[10:8]			00h
VSR7_B	R/W	3FF0h	VSR7_B_ofst1[7:0]								00h
VSR7_B	R/W	40F0h	VSR7_B_ofst2[7:0]								00h
VSR7_B	R/W	41F0h	VSR7_B_wid_D[7:0]								00h
VSR8_B	R/W	43F0h	VSR8_B_en	VSR8_B_rpt_en	VSR8_B_vrst_en	VSR8_B_wid_D_sel	VSR8_B_pwr_pol	VSR8_B_bk_pol	VSR8_B_pol	VSR8_B_SKIP_sel	08h
VSR8_B	R/W	44F0h	-	VSR8_B_wid_L[10:8]			-	VSR8_B_prid[10:8]			00h
VSR8_B	R/W	45F0h	VSR8_B_prid[7:0]								00h
VSR8_B	R/W	46F0h	VSR8_B_wid_L[7:0]								00h
VSR8_B	R/W	47F0h	VSR8_B_ofst1_ad_sel	VSR8_B_wid_D[9:8]		VSR8_B_ofst2[9:8]		VSR8_B_ofst1[10:8]			00h
VSR8_B	R/W	48F0h	VSR8_B_ofst1[7:0]								00h
VSR8_B	R/W	49F0h	VSR8_B_ofst2[7:0]								00h
VSR8_B	R/W	4AF0h	VSR8_B_wid_D[7:0]								00h
VSR9_B	R/W	4CF0h	VSR9_B_en	VSR9_B_rpt_en	VSR9_B_vrst_en	VSR9_B_wid_D_sel	VSR9_B_pwr_pol	VSR9_B_bk_pol	VSR9_B_pol	VSR9_B_SKIP_sel	08h
VSR9_B	R/W	4DF0h	-	VSR9_B_wid_L[10:8]			VSR9_B_ofst3	VSR9_B_prid[10:8]			00h
VSR9_B	R/W	4EF0h	VSR9_B_prid[7:0]								00h
VSR9_B	R/W	4FF0h	VSR9_B_wid_L[7:0]								00h
VSR9_B	R/W	50F0h	VSR9_B_ofst1_ad_sel	VSR9_B_wid_D[9:8]		VSR9_B_ofst2[9:8]		VSR9_B_ofst1[10:8]			00h
VSR9_B	R/W	52F0h	VSR9_B_ofst1[7:0]								00h

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VSR9_B	R/W	53F0h	VSR9_B_ofst2[7:0]								00h
VSR9_B	R/W	54F0h	VSR9_B_wid_D[7:0]								00h
VSR10_B	R/W	55F0h	VSR10_B_en	VSR10_B_rpt_en	VSR10_B_vrst_en	VSR10_B_wid_D_sel	VSR10_B_pwr_pol	VSR10_B_bk_pol	VSR10_B_pol	VSR10_B_SKIP_sel	08h
VSR10_B	R/W	56F0h	-	VSR10_B_wid_L[10:8]			-	VSR10_B_prid[10:8]			00h
VSR10_B	R/W	57F0h	VSR10_B_prid[7:0]								00h
VSR10_B	R/W	58F0h	VSR10_B_wid_L[7:0]								00h
VSR10_B	R/W	59F0h	VSR10_B_ofst1_ad_sel	VSR10_B_wid_D[9:8]		VSR10_B_ofst2[9:8]		VSR10_B_ofst1[10:8]			00h
VSR10_B	R/W	5AF0h	VSR10_B_ofst1[7:0]								00h
VSR10_B	R/W	5BF0h	VSR10_B_ofst2[7:0]								00h
VSR10_B	R/W	5CF0h	VSR10_B_wid_D[7:0]								00h
VST_B	R/W	5EF0h	VST_B_en	-	-	VST_B_wid_D_sel	VST_B_pwr_pol	-	VST_B_pol	VST_B_SKIP_sel	08h
VST_B	R/W	5FF0h	-	VST_B_wid_L[10:8]			-	-	-	-	00h
VST_B	R/W	60F0h	VST_B_wid_L[7:0]								00h
VST_B	R/W	61F0h	VST_B_ofst1_ad_sel	VST_B_wid_D[9:8]		VST_B_ofst2[9:8]		VST_B_ofst1[10:8]			00h
VST_B	R/W	62F0h	VST_B_ofst1[7:0]								00h
VST_B	R/W	63F0h	VST_B_ofst2[7:0]								00h
VST_B	R/W	64F0h	VST_B_wid_D[7:0]								00h
VEN_B	R/W	65F0h	VEN_B_en	VEN_B_rpt_en	VEN_B_vrst_en	VEN_B_wid_D_sel	VEN_B_pwr_pol	VEN_B_bk_pol	VEN_B_pol	VEN_B_SKIP_sel	08h
VEN_B	R/W	66F0h	-	VEN_B_wid_L[10:8]			-	VEN_B_prid[10:8]			00h
VEN_B	R/W	67F0h	VEN_B_prid[7:0]								00h
VEN_B	R/W	68F0h	VEN_B_wid_L[7:0]								00h
VEN_B	R/W	69F0h	VEN_B_ofst1_ad_sel	VEN_B_wid_D[9:8]		VEN_B_ofst2[9:8]		VEN_B_ofst1[10:8]			00h
VEN_B	R/W	6AF0h	VEN_B_ofst1[7:0]								00h
VEN_B	R/W	6BF0h	VEN_B_ofst2[7:0]								00h
VEN_B	R/W	6CF0h	VEN_B_wid_D[7:0]								00h
GOA Reset Selection	R/W	6EF0h	VSR_B_VRST_SEL[7:0]								00h
VSR Keep Toggle Setting	R/W	70F0h	VSR1_B_kp_tgl[7:0]								00h
	R/W	71F0h	VSR2_B_kp_tgl[7:0]								00h
	R/W	72F0h	VSR3_B_kp_tgl[7:0]								00h
	R/W	73F0h	VSR4_B_kp_tgl[7:0]								00h
	R/W	74F0h	VSR5_B_kp_tgl[7:0]								00h
	R/W	75F0h	VSR6_B_kp_tgl[7:0]								00h
	R/W	76F0h	VSR7_B_kp_tgl[7:0]								00h
	R/W	77F0h	VSR8_B_kp_tgl[7:0]								00h
	R/W	78F0h	VSR9_B_kp_tgl[7:0]								00h

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	R/W	79F0h	VSR10_B_kp_tgl[7:0]					00h
	R/W	7AF0h	VEN_B_kp_tgl[7:0]					00h
	R/W	7BF0h	-	VSR2_B_kp_tgl[10:8]		-	VSR1_B_kp_tgl[10:8]	00h
	R/W	7CF0h	-	VSR4_B_kp_tgl[10:8]		-	VSR3_B_kp_tgl[10:8]	00h
	R/W	7DF0h	-	VSR6_B_kp_tgl[10:8]		-	VSR5_B_kp_tgl[10:8]	00h
VSR HDLY Control	R/W	81F0h	VSR2_B_HDLAY[3:0]			VSR1_B_HDLAY[3:0]		00h
	R/W	82F0h	VSR4_B_HDLAY[3:0]			VSR3_B_HDLAY[3:0]		00h
	R/W	83F0h	VSR6_B_HDLAY[3:0]			VSR5_B_HDLAY[3:0]		00h
	R/W	84F0h	-	-	-	-	VSTE_B_HDLAY[3:0]	00h
CMD Mode Switch	W	FEF0h	CMD_Page[7:0]					00h
RD CMD Status	R	FFF0h	CMD_Status[7:0]					00h

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(00F0h~07F0h) GOA_VSR1_B

R/W	Addr	D7	D6	D5	D4	D3	D2	D1	D0	HEX
R/W	00F0h	VSR1_B_en	VSR1_B_rpt_en	VSR1_B_vrst_en	VSR1_B_wid_D_sel	VSR1_B_pwr_pol	VSR1_B_bk_pol	VSR1_B_pol	VSR1_B_SKIP_sel	08h
	01F0h	-	VSR1_B_wid_L[10:8]			-	VSR1_B_prid[10:8]			00h
	02F0h	VSR1_B_prid[7:0]								00h
	03F0h	VSR1_B_wid_L[7:0]								00h
	04F0h	VSR1_B_ofst1_ad_sel	VSR1_B_wid_D[9:8]		VSR1_B_ofst2[9:8]		VSR1_B_ofst1[10:8]			00h
	05F0h	VSR1_B_ofst1[7:0]								00h
	06F0h	VSR1_B_ofst2[7:0]								00h
	07F0h	VSR1_B_wid_D[7:0]								00h

Description

This command is GOA Timing Control for VSR1.

Bit	Description	Data
VSR1_B_en	VSR1 enable	0: VSR1 disable 1: VSR1 enable
VSR1_B_rpt_en	Enable the repeat function of VSR1	0: disable 1: enable
VSR1_B_vrst_en	Enable the Vsync reset function for VSR1	0: disable 1: enable
VSR1_B_wid_D_sel	The selection of count direction from Hsync for VSR1_B_wid_D	0: VSR1_B_wid_D seen as advance 1: VSR1_B_wid_D seen as delay
VSR1_B_pwr_pol	The Polarity of VSR1 during display off area	0: VSR1 negative polarity 1: VSR1 positive polarity
VSR1_B_bk_pol	The Polarity of VSR1 during blanking area	0: VSR1 negative polarity 1: VSR1 positive polarity
VSR1_B_pol	The Polarity of VSR1 during active area	0: VSR1 negative polarity 1: VSR1 positive polarity
VSR1_B_SKIP_sel	VSR1 status for skip frame	0: normal operation 1: keep the last state before skip frame

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Bit	Description	Data
VSR1_B_prid[10:0]	Period that VSR1 repeats (unit: Hsync)	Note: do not exceed vtotal.

Bit	Description	Data
VSR1_B_wid_L[10:0]	Low pulse width of VSR1 inside a period. (unit: Hsync)	Note: do not exceed VSR1_B_period.

Bit	Description	Data
VSR1_B_ofst1_ad_sel	The selection of count direction from Hsync for VSR1_B_oftst1	0: VSR1_B_ofst1 seen as advance 1: VSR1_B_ ofst1 seen as delay
VSR1_B_ofst1[10:0]	Time delay/advance from VSR1 to last back proch line each frame(unit: Hsync)	Note: do not exceed vtotal.

Bit	Description	Data
VSR1_B_ofst2[9:0]	Time delay from VSR1(falling) start to hsync. (unit: pixel clock)	Note: do not exceed htotal.

Bit	Description	Data
VSR1_B_wid_D[9:0]	Time delay from VSR1(rising) start to hsync. ((unit: pixel clock)	Note: do not exceed htotal.

Restriction	

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(09F0h~10F0h) GOA_VSR2_B_

R/W	Addr	D7	D6	D5	D4	D3	D2	D1	D0	HEX
R/W	09F0h	VSR2_B__en	VSR2_B__rpt_en	VSR2_B__vrst_en	VSR2_B__wid_D_sel	VSR2_B__pwr_pol	VSR2_B__bk_pol	VSR2_B__pol	VSR2_B__SKIP_sel	08h
	0AF0h	-	VSR2_B_wid_L[10:8]			-	VSR2_B_prid[10:8]			00h
	0BF0h	VSR2_B_prid[7:0]								00h
	0CF0h	VSR2_B_wid_L[7:0]								00h
	0DF0h	VSR2_B_ofst1_ad_sel	VSR2_B_wid_D[9:8]		VSR2_B_ofst2[9:8]		VSR2_B_ofst1[10:8]			00h
	0EF0h	VSR2_B_ofst1[7:0]								00h
	0FF0h	VSR2_B_ofst2[7:0]								00h
	10F0h	VSR2_B_wid_D[7:0]								00h

Description

This command is GOA Timing Control for VSR2_B

Bit	Description	Data
VSR2_B_en	VSR2_B_enable	0: VSR2_B_disable 1: VSR2_B_enable
VSR2_B_rpt_en	Enable the repeat function of VSR2_B_	0: disable 1: enable
VSR2_B_vrst_en	Enable the Vsync reset function for VSR2_B_	0: disable 1: enable
VSR2_B_wid_D_sel	The selection of count direction from Hsync for VSR2_B_wid_D	0: VSR2_B_wid_D seen as advance 1: VSR2_B_wid_D seen as delay
VSR2_B_pwr_pol	The Polarity of VSR2_B_during display off area	0: VSR2_B_negative polarity 1: VSR2_B_positive polarity
VSR2_B_bk_pol	The Polarity of VSR2_B_during blanking area	0: VSR2_B_negative polarity 1: VSR2_B_positive polarity
VSR2_B_pol	The Polarity of VSR2_B_during active area	0: VSR2_B_negative polarity 1: VSR2_B_positive polarity
VSR2_B_SKIP_sel	VSR2_B_status for skip frame	0: normal operation 1: keep the last state before skip frame

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Bit	Description	Data
VSR2_B_prid[10:0]	Period that VSR2_B_repeats (unit: Hsync)	Note: do not exceed vtotal.

Bit	Description	Data
VSR2_B_wid_L[10:0]	Low pulse width of VSR2_B_inside a period. (unit: Hsync)	Note: do not exceed VSR2_B_period.

Bit	Description	Data
VSR2_B_ofst1_ad_sel	The selection of count direction from Hsync for VSR2_B_oftst1	0: VSR2_B_ofst1 seen as advance 1: VSR2_B_ofst1 seen as delay
VSR2_B_ofst1[10:0]	Time delay/advance from VSR2_B_to last back proch line each frame(unit: Hsync)	Note: do not exceed vtotal.

Bit	Description	Data
VSR2_B_ofst2[9:0]	Time delay from VSR2_B_(falling) start to hsync. (unit: pixel clock)	Note: do not exceed htotal.

Bit	Description	Data
VSR2_B_wid_D[9:0]	Time delay from VSR2_B_(rising) start to hsync. ((unit: pixel clock)	Note: do not exceed htotal.

Restriction	

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(12F0h~19F0h) GOA_VSR3_B_

R/W	Addr	D7	D6	D5	D4	D3	D2	D1	D0	HEX
R/W	12F0h	VSR3_B__en	VSR3_B__rpt_en	VSR3_B_vrst_en	VSR3_B_wid_D_sel	VSR3_B_pwr_pol	VSR3_B_bk_pol	VSR3_B_pol	VSR3_B_SKIP_sel	08h
	13F0h	-	VSR3_B_wid_L[10:8]			-	VSR3_B_prid[10:8]			00h
	14F0h	VSR3_B_prid[7:0]								00h
	15F0h	VSR3_B_wid_L[7:0]								00h
	16F0h	VSR3_B_ofst1_ad_sel	VSR3_B_wid_D[9:8]		VSR3_B_ofst2[9:8]		VSR3_B_ofst1[10:8]			00h
	17F0h	VSR3_B_ofst1[7:0]								00h
	18F0h	VSR3_B_ofst2[7:0]								00h
	19F0h	VSR3_B_wid_D[7:0]								00h

Description

This command is GOA Timing Control for VSR3_B

Bit	Description	Data
VSR3_B_en	VSR3_B_enable	0: VSR3_B_disable 1: VSR3_B_enable
VSR3_B_rpt_en	Enable the repeat function of VSR3_B_	0: disable 1: enable
VSR3_B_vrst_en	Enable the Vsync reset function for VSR3_B_	0: disable 1: enable
VSR3_B_wid_D_sel	The selection of count direction from Hsync for VSR3_B_wid_D	0: VSR3_B_wid_D seen as advance 1: VSR3_B_wid_D seen as delay
VSR3_B_pwr_pol	The Polarity of VSR3_B_during display off area	0: VSR3_B_negative polarity 1: VSR3_B_positive polarity
VSR3_B_bk_pol	The Polarity of VSR3_B_during blanking area	0: VSR3_B_negative polarity 1: VSR3_B_positive polarity
VSR3_B_pol	The Polarity of VSR3_B_during active area	0: VSR3_B_negative polarity 1: VSR3_B_positive polarity
VSR3_B_SKIP_sel	VSR3_B_status for skip frame	0: normal operation 1: keep the last state before skip frame

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Bit	Description	Data
VSR3_B_prid[10:0]	Period that VSR3_B_repeats (unit: Hsync)	Note: do not exceed vtotal.

Bit	Description	Data
VSR3_B_wid_L[10:0]	Low pulse width of VSR3_B_inside a period. (unit: Hsync)	Note: do not exceed VSR3_B_period.

Bit	Description	Data
VSR3_B_ofst1_ad_sel	The selection of count direction from Hsync for VSR3_B_oftst1	0: VSR3_B_ofst1 seen as advance 1: VSR3_B_ofst1 seen as delay
VSR3_B_ofst1[10:0]	Time delay/advance from VSR3_B_to last back proch line each frame(unit: Hsync)	Note: do not exceed vtotal.

Bit	Description	Data
VSR3_B_ofst2[9:0]	Time delay from VSR3_B_(falling) start to hsync. (unit: pixel clock)	Note: do not exceed htotal.

Bit	Description	Data
VSR3_B_wid_D[9:0]	Time delay from VSR3_B_(rising) start to hsync. ((unit: pixel clock)	Note: do not exceed htotal.

Restriction	

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(1BF0h~22F0h) GOA_VSR4_B_

R/W	Addr	D7	D6	D5	D4	D3	D2	D1	D0	HEX
R/W	1BF0h	VSR4_B__en	VSR4_B__rpt_en	VSR4_B_vrst_en	VSR4_B_wid_D_sel	VSR4_B_pwr_pol	VSR4_B_bk_pol	VSR4_B_pol	VSR4_B_SKIP_sel	08h
	1CF0h	-	VSR4_B_wid_L[10:8]			-	VSR4_B_prid[10:8]			00h
	1DF0h	VSR4_B_prid[7:0]								00h
	1EF0h	VSR4_B_wid_L[7:0]								00h
	1FF0h	VSR4_B_ofst1_ad_sel	VSR4_B_wid_D[9:8]		VSR4_B_ofst2[9:8]		VSR4_B_ofst1[10:8]			00h
	20F0h	VSR4_B_ofst1[7:0]								00h
	21F0h	VSR4_B_ofst2[7:0]								00h
	22F0h	VSR4_B_wid_D[7:0]								00h

Description

This command is GOA Timing Control for VSR4_B

Bit	Description	Data
VSR4_B_en	VSR4_B_enable	0: VSR4_B_disable 1: VSR4_B_enable
VSR4_B_rpt_en	Enable the repeat function of VSR4_B_	0: disable 1: enable
VSR4_B_vrst_en	Enable the Vsync reset function for VSR4_B_	0: disable 1: enable
VSR4_B_wid_D_sel	The selection of count direction from Hsync for VSR4_B_wid_D	0: VSR4_B_wid_D seen as advance 1: VSR4_B_wid_D seen as delay
VSR4_B_pwr_pol	The Polarity of VSR4_B_during display off area	0: VSR4_B_negative polarity 1: VSR4_B_positive polarity
VSR4_B_bk_pol	The Polarity of VSR4_B_during blanking area	0: VSR4_B_negative polarity 1: VSR4_B_positive polarity
VSR4_B_pol	The Polarity of VSR4_B_during active area	0: VSR4_B_negative polarity 1: VSR4_B_positive polarity
VSR4_B_SKIP_sel	VSR4_B_status for skip frame	0: normal operation 1: keep the last state before skip frame

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Bit	Description	Data
VSR4_B_prid[10:0]	Period that VSR4_B_repeats (unit: Hsync)	Note: do not exceed vtotal.

Bit	Description	Data
VSR4_B_wid_L[10:0]	Low pulse width of VSR4_B_inside a period. (unit: Hsync)	Note: do not exceed VSR4_B_period.

Bit	Description	Data
VSR4_B_ofst1_ad_sel	The selection of count direction from Hsync for VSR4_B_oftst1	0: VSR4_B_ofst1 seen as advance 1: VSR4_B_ofst1 seen as delay
VSR4_B_ofst1[10:0]	Time delay/advance from VSR4_B_to last back proch line each frame(unit: Hsync)	Note: do not exceed vtotal.

Bit	Description	Data
VSR4_B_ofst2[9:0]	Time delay from VSR4_B_(falling) start to hsync. (unit: pixel clock)	Note: do not exceed htotal.

Bit	Description	Data
VSR4_B_wid_D[9:0]	Time delay from VSR4_B_(rising) start to hsync. ((unit: pixel clock)	Note: do not exceed htotal.

Restriction	

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(24F0h~2BF0h) GOA_VSR5_B_

R/W	Addr	D7	D6	D5	D4	D3	D2	D1	D0	HEX
R/W	24F0h	VSR5_B__en	VSR5_B_rpt_en	VSR5_B_vrst_en	VSR5_B_wid_D_sel	VSR5_B_pwr_pol	VSR5_B_bk_pol	VSR5_B_pol	VSR5_B_SKIP_sel	08h
	25F0h	-	VSR5_B_wid_L[10:8]			-	VSR5_B_prid[10:8]			00h
	26F0h	VSR5_B_prid[7:0]								00h
	27F0h	VSR5_B_wid_L[7:0]								00h
	28F0h	VSR5_B_ofst1_ad_sel	VSR5_B_wid_D[9:8]		VSR5_B_ofst2[9:8]		VSR5_B_ofst1[10:8]			00h
	29F0h	VSR5_B_ofst1[7:0]								00h
	2AF0h	VSR5_B_ofst2[7:0]								00h
	2BF0h	VSR5_B_wid_D[7:0]								00h

Description

This command is GOA Timing Control for VSR5_B

Bit	Description	Data
VSR5_B_en	VSR5_B_enable	0: VSR5_B_disable 1: VSR5_B_enable
VSR5_B_rpt_en	Enable the repeat function of VSR5_B_	0: disable 1: enable
VSR5_B_vrst_en	Enable the Vsync reset function for VSR5_B_	0: disable 1: enable
VSR5_B_wid_D_sel	The selection of count direction from Hsync for VSR5_B_wid_D	0: VSR5_B_wid_D seen as advance 1: VSR5_B_wid_D seen as delay
VSR5_B_pwr_pol	The Polarity of VSR5_B_during display off area	0: VSR5_B_negative polarity 1: VSR5_B_positive polarity
VSR5_B_bk_pol	The Polarity of VSR5_B_during blanking area	0: VSR5_B_negative polarity 1: VSR5_B_positive polarity
VSR5_B_pol	The Polarity of VSR5_B_during active area	0: VSR5_B_negative polarity 1: VSR5_B_positive polarity
VSR5_B_SKIP_sel	VSR5_B_status for skip frame	0: normal operation 1: keep the last state before skip frame

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Bit	Description	Data
VSR5_B_prid[10:0]	Period that VSR5_B_repeats (unit: Hsync)	Note: do not exceed vtotal.

Bit	Description	Data
VSR5_B_wid_L[10:0]	Low pulse width of VSR5_B_inside a period. (unit: Hsync)	Note: do not exceed VSR5_B_period.

Bit	Description	Data
VSR5_B_ofst1_ad_sel	The selection of count direction from Hsync for VSR5_B_oftst1	0: VSR5_B_ofst1 seen as advance 1: VSR5_B_ofst1 seen as delay
VSR5_B_ofst1[10:0]	Time delay/advance from VSR5_B_to last back proch line each frame(unit: Hsync)	Note: do not exceed vtotal.

Bit	Description	Data
VSR5_B_ofst2[9:0]	Time delay from VSR5_B_(falling) start to hsync. (unit: pixel clock)	Note: do not exceed htotal.

Bit	Description	Data
VSR5_B_wid_D[9:0]	Time delay from VSR5_B_(rising) start to hsync. ((unit: pixel clock)	Note: do not exceed htotal.

Restriction	

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(2FF0h~36F0h) GOA_VSR6_B

R/W	Addr	D7	D6	D5	D4	D3	D2	D1	D0	HEX
R/W	2FF0h	VSR6_B__en	VSR6_B_rpt_en	VSR6_B_vrst_en	VSR6_B_wid_D_sel	VSR6_B_pwr_pol	VSR6_B_bk_pol	VSR6_B_pol	VSR6_B_SKIP_sel	08h
	30F0h	-	VSR6_B_wid_L[10:8]			-	VSR6_B_prid[10:8]			00h
	31F0h	VSR6_B_prid[7:0]								00h
	32F0h	VSR6_B_wid_L[7:0]								00h
	33F0h	VSR6_B_ofst1_ad_sel	VSR6_B_wid_D[9:8]		VSR6_B_ofst2[9:8]		VSR6_B_ofst1[10:8]			00h
	34F0h	VSR6_B_ofst1[7:0]								00h
	35F0h	VSR6_B_ofst2[7:0]								00h
	36F0h	VSR6_B_wid_D[7:0]								00h

Description

This command is GOA Timing Control for VSR6_B

Bit	Description	Data
VSR6_B_en	VSR6_B_enable	0: VSR6_B_disable 1: VSR6_B_enable
VSR6_B_rpt_en	Enable the repeat function of VSR6_B_	0: disable 1: enable
VSR6_B_vrst_en	Enable the Vsync reset function for VSR6_B_	0: disable 1: enable
VSR6_B_wid_D_sel	The selection of count direction from Hsync for VSR6_B_wid_D	0: VSR6_B_wid_D seen as advance 1: VSR6_B_wid_D seen as delay
VSR6_B_pwr_pol	The Polarity of VSR6_B_during display off area	0: VSR6_B_negative polarity 1: VSR6_B_positive polarity
VSR6_B_bk_pol	The Polarity of VSR6_B_during blanking area	0: VSR6_B_negative polarity 1: VSR6_B_positive polarity
VSR6_B_pol	The Polarity of VSR6_B_during active area	0: VSR6_B_negative polarity 1: VSR6_B_positive polarity
VSR6_B_SKIP_sel	VSR6_B_status for skip frame	0: normal operation 1: keep the last state before skip frame

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Bit	Description	Data
VSR6_B_prid[10:0]	Period that VSR6_B_repeats (unit: Hsync)	Note: do not exceed vtotal.

Bit	Description	Data
VSR6_B_wid_L[10:0]	Low pulse width of VSR6_B_inside a period. (unit: Hsync)	Note: do not exceed VSR6_B_period.

Bit	Description	Data
VSR6_B_ofst1_ad_sel	The selection of count direction from Hsync for VSR6_B_oftst1	0: VSR6_B_ofst1 seen as advance 1: VSR6_B_ofst1 seen as delay
VSR6_B_ofst1[10:0]	Time delay/advance from VSR6_B_to last back proch line each frame(unit: Hsync)	Note: do not exceed vtotal.

Bit	Description	Data
VSR6_B_ofst2[9:0]	Time delay from VSR6_B_(falling) start to hsync. (unit: pixel clock)	Note: do not exceed htotal.

Bit	Description	Data
VSR6_B_wid_D[9:0]	Time delay from VSR6_B_(rising) start to hsync. ((unit: pixel clock)	Note: do not exceed htotal.

Restriction	

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(38F0h~41F0h) GOA_VSR7_B

R/W	Addr	D7	D6	D5	D4	D3	D2	D1	D0	HEX
R/W	38F0h	VSR7_B_en	VSR7_B_rpt_en	VSR7_B_vrst_en	VSR7_B_wid_D_sel	VSR7_B_pwr_pol	VSR7_B_bk_pol	VSR7_B_pol	VSR7_B_SKIP_sel	08h
	39F0h	-	VSR7_B_wid_L[10:8]			-	VSR7_B_prid[10:8]			00h
	3AF0h	VSR7_B_prid[7:0]								00h
	3BF0h	VSR7_B_wid_L[7:0]								00h
	3DF0h	VSR7_B_ofst1_ad_sel	VSR7_B_wid_D[9:8]		VSR7_B_ofst2[9:8]		VSR7_B_ofst1[10:8]			00h
	3FF0h	VSR7_B_ofst1[7:0]								00h
	40F0h	VSR7_B_ofst2[7:0]								00h
	41F0h	VSR7_B_wid_D[7:0]								00h

Description

This command is GOA Timing Control for VSR7_B_.

Bit	Description	Data
VSR7_B_en	VSR7_B_enable	0: VSR7_B_disable 1: VSR7_B_enable
VSR7_B_rpt_en	Enable the repeat function of VSR7_B_	0: disable 1: enable
VSR7_B_vrst_en	Enable the Vsync reset function for VSR7_B_	0: disable 1: enable
VSR7_B_wid_D_sel	The selection of count direction from Hsync for VSR7_B_wid_D	0: VSR7_B_wid_D seen as advance 1: VSR7_B_wid_D seen as delay
VSR7_B_pwr_pol	The Polarity of VSR7_B_during display off area	0: VSR7_B_negative polarity 1: VSR7_B_positive polarity
VSR7_B_bk_pol	The Polarity of VSR7_B_during blanking area	0: VSR7_B_negative polarity 1: VSR7_B_positive polarity
VSR7_B_pol	The Polarity of VSR7_B_during active area	0: VSR7_B_negative polarity 1: VSR7_B_positive polarity
VSR7_B_SKIP_sel	VSR7_B_status for skip frame	0: normal operation 1: keep the last state before skip frame

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Bit	Description	Data
VSR7_B_prid[10:0]	Period that VSR7_B_repeats (unit: Hsync)	Note: do not exceed vtotal.

Bit	Description	Data
VSR7_B_wid_L[10:0]	Low pulse width of VSR7_B_inside a period. (unit: Hsync)	Note: do not exceed VSR7_B_period.

Bit	Description	Data
VSR7_B_ofst1_ad_sel	The selection of count direction from Hsync for VSR7_B_oftst1	0: VSR7_B_ofst1 seen as advance 1: VSR7_B_ofst1 seen as delay
VSR7_B_ofst1[10:0]	Time delay/advance from VSR7_B_to last back proch line each frame(unit: Hsync)	Note: do not exceed vtotal.

Bit	Description	Data
VSR7_B_ofst2[9:0]	Time delay from VSR7_B_(falling) start to hsync. (unit: pixel clock)	Note: do not exceed htotal.

Bit	Description	Data
VSR7_B_wid_D[9:0]	Time delay from VSR7_B_(rising) start to hsync. ((unit: pixel clock)	Note: do not exceed htotal.

Restriction	

CONFIDENTIAL

(43F0h~4AF0h) GOA_VSR8_B

R/W	Addr	D7	D6	D5	D4	D3	D2	D1	D0	HEX
R/W	43F0h	VSR8_B_en	VSR8_B_rpt_en	VSR8_B_vrst_en	VSR8_B_wid_D_sel	VSR8_B_pwr_pol	VSR8_B_bk_pol	VSR8_B_pol	VSR8_B_SKIP_sel	08h
	44F0h	-	VSR8_B_wid_L[10:8]			-	VSR8_B_prid[10:8]			00h
	45F0h	VSR8_B_prid[7:0]								00h
	46F0h	VSR8_B_wid_L[7:0]								00h
	47F0h	VSR8_B_ofst1_ad_sel	VSR8_B_wid_D[9:8]		VSR8_B_ofst2[9:8]		VSR8_B_ofst1[10:8]			00h
	48F0h	VSR8_B_ofst1[7:0]								00h
	49F0h	VSR8_B_ofst2[7:0]								00h
	4AF0h	VSR8_B_wid_D[7:0]								00h

Description

This command is GOA Timing Control for VSR8_B

Bit	Description	Data
VSR8_B_en	VSR8_B_enable	0: VSR8_B_disable 1: VSR8_B_enable
VSR8_B_rpt_en	Enable the repeat function of VSR8_B_	0: disable 1: enable
VSR8_B_vrst_en	Enable the Vsync reset function for VSR8_B_	0: disable 1: enable
VSR8_B_wid_D_sel	The selection of count direction from Hsync for VSR8_B_wid_D	0: VSR8_B_wid_D seen as advance 1: VSR8_B_wid_D seen as delay
VSR8_B_pwr_pol	The Polarity of VSR8_B_during display off area	0: VSR8_B_negative polarity 1: VSR8_B_positive polarity
VSR8_B_bk_pol	The Polarity of VSR8_B_during blanking area	0: VSR8_B_negative polarity 1: VSR8_B_positive polarity
VSR8_B_pol	The Polarity of VSR8_B_during active area	0: VSR8_B_negative polarity 1: VSR8_B_positive polarity
VSR8_B_SKIP_sel	VSR8_B_status for skip frame	0: normal operation 1: keep the last state before skip frame

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Bit	Description	Data
VSR8_B_prid[10:0]	Period that VSR8_B_repeats (unit: Hsync)	Note: do not exceed vtotal.

Bit	Description	Data
VSR8_B_wid_L[10:0]	Low pulse width of VSR8_B_inside a period. (unit: Hsync)	Note: do not exceed VSR8_B_period.

Bit	Description	Data
VSR8_B_ofst1_ad_sel	The selection of count direction from Hsync for VSR8_B_oftst1	0: VSR8_B_ofst1 seen as advance 1: VSR8_B_ofst1 seen as delay
VSR8_B_ofst1[10:0]	Time delay/advance from VSR8_B_to last back proch line each frame(unit: Hsync)	Note: do not exceed vtotal.

Bit	Description	Data
VSR8_B_ofst2[9:0]	Time delay from VSR8_B_(falling) start to hsync. (unit: pixel clock)	Note: do not exceed htotal.

Bit	Description	Data
VSR8_B_wid_D[9:0]	Time delay from VSR8_B_(rising) start to hsync. ((unit: pixel clock)	Note: do not exceed htotal.

Restriction	

CONFIDENTIAL

(4CF0h~54F0h) GOA_VSR9_B

R/W	Addr	D7	D6	D5	D4	D3	D2	D1	D0	HEX
R/W	4CF0h	VSR9_B_en	VSR9_B_rpt_en	VSR9_B_vrst_en	VSR9_B_wid_D_sel	VSR9_B_pwr_pol	VSR9_B_bk_pol	VSR9_B_pol	VSR9_B_SKIP_sel	08h
	4DF0h	-	VSR9_B_wid_L[10:8]			-	VSR9_B_prid[10:8]			00h
	4EF0h	VSR9_B_prid[7:0]								00h
	4FF0h	VSR9_B_wid_L[7:0]								00h
	50F0h	VSR9_B_ofst1_ad_sel	VSR9_B_wid_D[9:8]		VSR9_B_ofst2[9:8]		VSR9_B_ofst1[10:8]			00h
	52F0h	VSR9_B_ofst1[7:0]								00h
	53F0h	VSR9_B_ofst2[7:0]								00h
	54F0h	VSR9_B_wid_D[7:0]								00h

Description

This command is GOA Timing Control for VSR9_B.

Bit	Description	Data
VSR9_B_en	VSR9_B enable	0: VSR9_B disable 1: VSR9_B enable
VSR9_B_rpt_en	Enable the repeat function of VSR9_B	0: disable 1: enable
VSR9_B_vrst_en	Enable the Vsync reset function for VSR9_B	0: disable 1: enable
VSR9_B_wid_D_sel	The selection of count direction from Hsync for VSR9_B_wid_D	0: VSR9_B_wid_D seen as advance 1: VSR9_B_wid_D seen as delay
VSR9_B_pwr_pol	The Polarity of VSR9_B during display off area	0: VSR9_B negative polarity 1: VSR9_B positive polarity
VSR9_B_bk_pol	The Polarity of VSR9_B during blanking area	0: VSR9_B negative polarity 1: VSR9_B positive polarity
VSR9_B_pol	The Polarity of VSR9_B during active area	0: VSR9_B negative polarity 1: VSR9_B positive polarity
VSR9_B_SKIP_sel	VSR9_B status for skip frame	0: normal operation 1: keep the last state before skip frame

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Bit	Description	Data
VSR9_B_prid[10:0]	Period that VSR9_B repeats (unit: Hsync)	Note: do not exceed vtotal.

Bit	Description	Data
VSR9_B_wid_L[10:0]	Low pulse width of VSR9_B inside a period. (unit: Hsync)	Note: do not exceed VSR9_B_period.

Bit	Description	Data
VSR9_B_ofst1_ad_sel	The selection of count direction from Hsync for VSR9_B_oftst1	0: VSR9_B_ofst1 seen as advance 1: VSR9_B_ ofst1 seen as delay
VSR9_B_ofst1[10:0]	Time delay/advance from VSR9_B to last back proch line each frame(unit: Hsync)	Note: do not exceed vtotal.

Bit	Description	Data
VSR9_B_ofst2[9:0]	Time delay from VSR9_B(falling) start to hsync. (unit: pixel clock)	Note: do not exceed htotal.

Bit	Description	Data
VSR9_B_wid_D[9:0]	Time delay from VSR9_B(rising) start to hsync. ((unit: pixel clock)	Note: do not exceed htotal.

Restriction	

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(55F0h~5CF0h) GOA_VSR10_B

R/W	Addr	D7	D6	D5	D4	D3	D2	D1	D0	HEX
R/W	55F0h	VSR10_B_en	VSR10_B_rpt_en	VSR10_B_vrst_en	VSR10_B_wid_D_sel	VSR10_B_pwr_pol	VSR10_B_bk_pol	VSR10_B_pol	VSR10_B_SKIP_sel	08h
	56F0h	-	VSR10_B_wid_L[10:8]			-	VSR10_B_prid[10:8]			00h
	57F0h	VSR10_B_prid[7:0]								00h
	58F0h	VSR10_B_wid_L[7:0]								00h
	59F0h	VSR10_B_ofst1_ad_sel	VSR10_B_wid_D[9:8]		VSR10_B_ofst2[9:8]		VSR10_B_ofst1[10:8]			00h
	5AF0h	VSR10_B_ofst1[7:0]								00h
	5BF0h	VSR10_B_ofst2[7:0]								00h
	5CF0h	VSR10_B_wid_D[7:0]								00h

Description

This command is GOA Timing Control for VSR10_B.

Bit	Description	Data
VSR10_B_en	VSR10_B enable	0: VSR10_B disable 1: VSR10_B enable
VSR10_B_rpt_en	Enable the repeat function of VSR10_B	0: disable 1: enable
VSR10_B_vrst_en	Enable the Vsync reset function for VSR10_B	0: disable 1: enable
VSR10_B_wid_D_sel	The selection of count direction from Hsync for VSR10_B_wid_D	0: VSR10_B_wid_D seen as advance 1: VSR10_B_wid_D seen as delay
VSR10_B_pwr_pol	The Polarity of VSR10_B during display off area	0: VSR10_B negative polarity 1: VSR10_B positive polarity
VSR10_B_bk_pol	The Polarity of VSR10_B during blanking area	0: VSR10_B negative polarity 1: VSR10_B positive polarity
VSR10_B_pol	The Polarity of VSR10_B during active area	0: VSR10_B negative polarity 1: VSR10_B positive polarity
VSR10_B_SKIP_sel	VSR10_B status for skip frame	0: normal operation 1: keep the last state before skip frame

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Bit	Description	Data
VSR10_B_prid[10:0]	Period that VSR10_B repeats (unit: Hsync)	Note: do not exceed vtotal.

Bit	Description	Data
VSR10_B_wid_L[10:0]	Low pulse width of VSR10_B inside a period. (unit: Hsync)	Note: do not exceed VSR10_B_period.

Bit	Description	Data
VSR10_B_ofst1_ad_sel	The selection of count direction from Hsync for VSR10_B_oftst1	0: VSR10_B_ofst1 seen as advance 1: VSR10_B_ ofst1 seen as delay
VSR10_B_ofst1[10:0]	Time delay/advance from VSR10_B to last back proch line each frame(unit: Hsync)	Note: do not exceed vtotal.

Bit	Description	Data
VSR10_B_ofst2[9:0]	Time delay from VSR10_B(falling) start to hsync. (unit: pixel clock)	Note: do not exceed htotal.

Bit	Description	Data
VSR10_B_wid_D[9:0]	Time delay from VSR10_B(rising) start to hsync. ((unit: pixel clock)	Note: do not exceed htotal.

Restriction	

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(5EF0h~64F0h) GOA_VST_B

R/W	Addr	D7	D6	D5	D4	D3	D2	D1	D0	HEX
R/W	5EF0h	VST_B_en	-	-	VST_B_wid_D_sel	VST_B_pwr_pol	-	VST_B_pol	VST_B_SKIP_sel	08h
	5FF0h	-	VST_B_wid_L[10:8]			-	-	-	-	00h
	60F0h	VST_B_wid_L[7:0]								00h
	61F0h	VST_B_ofst1_ad_sel	VST_B_wid_D[9:8]		VST_B_ofst2[9:8]		VST_B_ofst1[10:8]			00h
	62F0h	VST_B_ofst1[7:0]								00h
	63F0h	VST_B_ofst2[7:0]								00h
	64F0h	VST_B_wid_D[7:0]								00h

Description

This command is GOA Timing Control for VST_B.

Bit	Description	Data
VST_B_en	VST_B enable	0: VST_B disable 1: VST_B enable
VST_B_wid_D_sel	The selection of count direction from Hsync for VST_B_wid_D	0: VST_B_wid_D seen as advance 1: VST_B_wid_D seen as delay
VST_B_pwr_pol	The Polarity of VST_B during display off area	0: VST_B negative polarity 1: VST_B positive polarity
VST_B_pol	The Polarity of VST_B during active area	0: VST_B negative polarity 1: VST_B positive polarity
VST_B_SKIP_sel	VST_B status for skip frame	0: normal operation 1: keep the last state before skip frame

Bit	Description	Data
VST_B_wid_L[10:0]	Low pulse width of VST_B inside a period. (unit: Hsync)	Note: do not exceed VST_B_period.

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Bit	Description	Data
VST_B_ofst2[9:0]	Time delay from VST_B(falling) start to hsync. (unit: pixel clock)	Note: do not exceed htotal.

Bit	Description	Data
VST_B_ofst1_ad_sel	The selection of count direction from Hsync for VST_B_oftst1	0: VST_B_ofst1 seen as advance 1: VST_B_ ofst1 seen as delay
VST_B_ofst1[10:0]	Time delay/advance from VST_B to last back proch line each frame(unit: Hsync)	Note: do not exceed vtotal.

Bit	Description	Data
VST_B_wid_D[9:0]	Time delay from VST_B(rising) start to hsync. ((unit: pixel clock)	Note: do not exceed htotal.

Restriction	

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(65F0h~6CF0h) GOA_VEN_B

R/W	Addr	D7	D6	D5	D4	D3	D2	D1	D0	HEX
R/W	65F0h	VEN_B_en	VEN_B_rpt_en	VEN_B_vrst_en	VEN_B_wid_D_sel	VEN_B_pwr_pol	VEN_B_bk_pol	VEN_B_pol	VEN_B_SKIP_sel	08h
	66F0h	-	VEN_B_wid_L[10:8]			-	VEN_B_prid[10:8]			00h
	67F0h	VEN_B_prid[7:0]								00h
	68F0h	VEN_B_wid_L[7:0]								00h
	69F0h	VEN_B_ofst1_ad_sel	VEN_B_wid_D[9:8]		VEN_B_ofst2[9:8]		VEN_B_ofst1[10:8]			00h
	6AF0h	VEN_B_ofst1[7:0]								00h
	6BF0h	VEN_B_ofst2[7:0]								00h
	6CF0h	VEN_B_wid_D[7:0]								00h

Description

This command is GOA Timing Control for VEN_B.

Bit	Description	Data
VEN_B_en	VEN_B enable	0: VEN_B disable 1: VEN_B enable
VEN_B_rpt_en	Enable the repeat function of VEN_B	0: disable 1: enable
VEN_B_vrst_en	Enable the Vsync reset function for VEN_B	0: disable 1: enable
VEN_B_wid_D_sel	The selection of count direction from Hsync for VEN_B_wid_D	0: VEN_B_wid_D seen as advance 1: VEN_B_wid_D seen as delay
VEN_B_pwr_pol	The Polarity of VEN_B during display off area	0: VEN_B negative polarity 1: VEN_B positive polarity
VEN_B_bk_pol	The Polarity of VEN_B during blanking area	0: VEN_B negative polarity 1: VEN_B positive polarity
VEN_B_pol	The Polarity of VEN_B during active area	0: VEN_B negative polarity 1: VEN_B positive polarity
VEN_B_SKIP_sel	VEN_B status for skip frame	0: normal operation 1: keep the last state before skip frame

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Bit	Description	Data
VEN_B_prid[10:0]	Period that VEN_B repeats (unit: Hsync)	Note: do not exceed vtotal.

Bit	Description	Data
VEN_B_wid_L[10:0]	Low pulse width of VEN_B inside a period. (unit: Hsync)	Note: do not exceed VEN_B_period.

Bit	Description	Data
VEN_B_ofst1_ad_sel	The selection of count direction from Hsync for VEN_B_oftst1	0: VEN_B_ofst1 seen as advance 1: VEN_B_ ofst1 seen as delay
VEN_B_ofst1[10:0]	Time delay/advance from VEN_B to last back proch line each frame(unit: Hsync)	Note: do not exceed vtotal.

Bit	Description	Data
VEN_B_ofst2[9:0]	Time delay from VEN_B(falling) start to hsync. (unit: pixel clock)	Note: do not exceed htotal.

Bit	Description	Data
VEN_B_wid_D[9:0]	Time delay from VEN_B(rising) start to hsync. ((unit: pixel clock)	Note: do not exceed htotal.

Restriction	

CONFIDENTIAL

(6EF0h) GOA Reset Selection B

R/W	Addr	D7	D6	D5	D4	D3	D2	D1	D0	HEX
R/W	6EF0h	VSR_B_VRST_SEL[7:0]								00h

Description

This command is used to set VSR_Bx reset position when VSR_Bx toggle repetitively.

Note that VSR_Bx_vrst_en shall be equal to 0.

Bit	Description	Data
VSR_B_VRST_SET [7]	Set VSR_B8 reset position at back porch +/- VSR_B8_ofst1	0: ON 1: OFF
VSR_B_VRST_SET [6]	Set VSR_B7 reset position at back porch +/- VSR_B7_ofst1	
VSR_B_VRST_SET [5]	Set VSR_B6 reset position at back porch +/- VSR_B6_ofst1	
VSR_B_VRST_SET [4]	Set VSR_B5 reset position at back porch +/- VSR_B5_ofst1	
VSR_B_VRST_SET [3]	Set VSR_B4 reset position at back porch +/- VSR_B4_ofst1	
VSR_B_VRST_SET [2]	Set VSR_B3 reset position at back porch +/- VSR_B3_ofst1	
VSR_B_VRST_SET [1]	Set VSR_B2 reset position at back porch +/- VSR_B2_ofst1	
VSR_B_VRST_SET [0]	Set VSR_B1 reset position at back porch +/- VSR_B1_ofst1	

Restriction

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(70F0h~80F0h) VSR Keep Toggle Setting B

R/W	Addr	D7	D6	D5	D4	D3	D2	D1	D0	HEX
R/W	70F0h	VSR1_B_kp_tgl[7:0]								00h
R/W	71F0h	VSR2_B_kp_tgl[7:0]								00h
R/W	72F0h	VSR3_B_kp_tgl[7:0]								00h
R/W	73F0h	VSR4_B_kp_tgl[7:0]								00h
R/W	74F0h	VSR5_B_kp_tgl[7:0]								00h
R/W	75F0h	VSR6_B_kp_tgl[7:0]								00h
R/W	76F0h	VSR7_B_kp_tgl[7:0]								00h
R/W	77F0h	VSR8_B_kp_tgl[7:0]								00h
R/W	78F0h	VEN_kp_tgl[7:0]								00h
R/W	79F0h	-	VSR2_B_kp_tgl[10:8]			-	VSR1_B_kp_tgl[10:8]			00h
R/W	7AF0h	-	VSR4_B_kp_tgl[10:8]			-	VSR3_B_kp_tgl[10:8]			00h
R/W	7BF0h	-	VSR6_B_kp_tgl[10:8]			-	VSR5_B_kp_tgl[10:8]			00h
R/W	7CF0h	-	VSR8_B_kp_tgl[10:8]			-	VSR7_B_kp_tgl[10:8]			00h
R/W	7DF0h	-					VEN_kp_tgl[10:8]			00h

Description

Parameter	Description
VSR1_B_kp_tg[10:0]	Keep toggling line number of VSR1_B_kp_tgl from VSR1_B_ofst1 position (unit Hsync)
VSR2_B_kp_tg[10:0]	Keep toggling line number of VSR2_B_kp_tgl from VSR2_B_ofst1 position (unit Hsync)
VSR3_B_kp_tg[10:0]	Keep toggling line number of VSR3_B_kp_tgl from VSR3_B_ofst1 position (unit Hsync)
VSR4_B_kp_tg[10:0]	Keep toggling line number of VSR4_B_kp_tgl from VSR4_B_ofst1 position (unit Hsync)
VSR5_B_kp_tg[10:0]	Keep toggling line number of VSR5_B_kp_tgl from VSR5_B_ofst1 position (unit Hsync)
VSR6_B_kp_tg[10:0]	Keep toggling line number of VSR6_B_kp_tgl from VSR6_B_ofst1 position (unit Hsync)
VSR7_B_kp_tg[10:0]	Keep toggling line number of VSR7_B_kp_tgl from VSR7_B_ofst1 position (unit Hsync)
VSR8_B_kp_tg[10:0]	Keep toggling line number of VSR8_B_kp_tgl from VSR8_B_ofst1 position (unit Hsync)
VEN_kp_tg[10:0]	Keep toggling line number of VEN_kp_tgl from VEN_ofst1 position (unit Hsync)

Restriction

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(81F0h~84F0h) VSR HDLY Control B

R/W	Addr	D7	D6	D5	D4	D3	D2	D1	D0	HEX
R/W	81F0h	VSR2_B_HDLAY[3:0]				VSR1_B_HDLAY[3:0]				00h
R/W	82F0h	VSR4_B_HDLAY[3:0]				VSR3_B_HDLAY[3:0]				00h
R/W	83F0h	VSR6_B_HDLAY[3:0]				VSR5_B_HDLAY[3:0]				00h
R/W	84F0h	-	-			VSTE_B_HDLAY[3:0]				00h

Description	This command is used to set the H-delay of VSR1~VSR6_B_, VSTE for VSR and SW Output Selection.

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(FEF0h): CMD Mode Switch

R/W	Addr	D7	D6	D5	D4	D3	D2	D1	D0	HEX
W	FEF0h	CMD_Page[7:0]								00h

Description

This command is used to switch the Manufacture Command Pages and User Commands sets.

CMD_Page[7:0]	Description
00h (default)	User Command Set (UCS = CMD1)
10h	Manufacture Command Set Page Panel ID
12h	Manufacture Command Set Page SID
20h	Manufacture Command Set Page Panel
40h	Manufacture Command Set Page ABH Mode
82h	Manufacture Command Set Page Power
92h	Manufacture Command Set Page SD timing
50h	Manufacture Command Set Page Gamma1
60h	Manufacture Command Set Page Gamma2
30h	Manufacture Command Set Page Gamma3
52h	Manufacture Command Set Page Gamma4
70h	Manufacture Command Set Page GOA Timing 1
F0h	Manufacture Command Set Page GOA Timing 2
42h	Manufacture Command Set Page DBV
22h	Manufacture Command Set Page SES
80h	Manufacture Command Set Page APRC
90h	Manufacture Command Set Page ACL
62h	Manufacture Command Set Page CGM
C2h	Manufacture Command Set Page CGM LUT

Restriction

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(FFF0h): Read CMD Status

R/W	Addr	D7	D6	D5	D4	D3	D2	D1	D0	HEX
R	FFF0h	CMD_Status[7:0]								00h

Description	This command is used to read the status of Manufacture Command Pages. Please refer to FE00h
Restriction	-

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1.15MCS: CMD2 Page42, DBV Settings

Instruction	R/W	Addr	D7	D6	D5	D4	D3	D2	D1	D0	HEX
2Band gama control	R/W	0142h	2BAND_PAR1[7:0]								00h
HBM_Swap Ratio	R/W	0442h	G_ratio_HBM_swap[7:0]								00h
2Band gama Control	R/W	0842h	2BAND_PAR2[7:0]								00h
2Band gama control	R/W	0942h	2BAND_PAR3[7:0]								00h
BC Curve Control	R/W	1442h	BC_curve	-	-	-	-	-	-	-	00h
BC curve remap	R/W	1542h	BC_remap_0[7:0]								00h
BC curve remap	R/W	1642h	BC_remap_1[7:0]								01h
BC curve remap	R/W	1742h	BC_remap_3[7:0]								03h
BC curve remap	R/W	1842h	BC_remap_7[7:0]								07h
BC curve remap	R/W	1942h	BC_remap_15[7:0]								0Fh
BC curve remap	R/W	1A42h	BC_remap_31[7:0]								1Fh
BC curve remap	R/W	1B42h	BC_remap_47[7:0]								2Fh
BC curve remap	R/W	1C42h	BC_remap_63[7:0]								3Fh
BC curve remap	R/W	1D42h	BC_remap_79[7:0]								4Fh
BC curve remap	R/W	1E42h	BC_remap_95[7:0]								5Fh
BC curve remap	R/W	1F42h	BC_remap_111[7:0]								6Fh
BC curve remap	R/W	2042h	BC_remap_127[7:0]								7Fh
BC curve remap	R/W	2142h	BC_remap_143[7:0]								8Fh
BC curve remap	R/W	2242h	BC_remap_159[7:0]								9Fh
BC curve remap	R/W	2342h	BC_remap_175[7:0]								AFh
BC curve remap	R/W	2442h	BC_remap_191[7:0]								BFh
BC curve remap	R/W	2542h	BC_remap_207[7:0]								CFh
BC curve remap	R/W	2642h	BC_remap_223[7:0]								DFh
BC curve remap	R/W	2742h	BC_remap_239[7:0]								EFh
BC curve remap	R/W	2842h	BC_remap_255[7:0]								FFh
CMD Mode Switch	W	FE42h	CMD_Page [7:0]								01h
RD CMD Status	R	FF42h	CMD_Status[7:0]								01h

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(0142h, 0842h~0942h) 2band Gamma Control Parameter

R/W	Addr	D7	D6	D5	D4	D3	D2	D1	D0	HEX
R/W	0142h	2band_PAR1								00h
R/W	0842h	2band_PAR2								00h
R/W	0942h	2band_PAR3								00h

Description	This command is used to set the parameter of 2band gamma function These parameters control the seamless switching between normal mode GAMA and 2band GAMA in low – brightness region.
Restriction	

(0442h) HBM_swap Ratio

R/W	Addr	D7	D6	D5	D4	D3	D2	D1	D0	HEX
R/W	0442h	G_ratio_HBM_swap[7:0]								00h

Description	This command is used to set the HBM start brightness ratio The brightness of HBM gamma at code “G_ratio_HBM_swap” is equal to code 255 under the normal gamma.
Restriction	

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(1442h) BC Curve Control

R/W	Addr	D7	D6	D5	D4	D3	D2	D1	D0	HEX
R/W	1442h	BC_curve	-	-	-	-	-	-	-	00h

Description	BC_curve: 1: Enable BC gamma curve remapping 0: Disable BC gamma curve remapping
Restriction	

(1542h ~ 2842h) BC Curve Remap

R/W	Addr	D7	D6	D5	D4	D3	D2	D1	D0	HEX
R/W	1542h	BC_remap_0[7:0]								00h
R/W	1642h	BC_remap_1[7:0]								01h
R/W	1742h	BC_remap_3[7:0]								03h
R/W	1842h	BC_remap_7[7:0]								07h
R/W	1942h	BC_remap_15[7:0]								0Fh
R/W	1A42h	BC_remap_31[7:0]								1Fh
R/W	1B42h	BC_remap_47[7:0]								2Fh
R/W	1C42h	BC_remap_63[7:0]								3Fh
R/W	1D42h	BC_remap_79[7:0]								4Fh
R/W	1E42h	BC_remap_95[7:0]								5Fh
R/W	1F42h	BC_remap_111[7:0]								6Fh
R/W	2042h	BC_remap_127[7:0]								7Fh
R/W	2142h	BC_remap_143[7:0]								8Fh
R/W	2242h	BC_remap_159[7:0]								9Fh
R/W	2342h	BC_remap_175[7:0]								AFh
R/W	2442h	BC_remap_191[7:0]								BFh
R/W	2542h	BC_remap_207[7:0]								CFh
R/W	2642h	BC_remap_223[7:0]								DFh
R/W	2742h	BC_remap_239[7:0]								EFh
R/W	2842h	BC_remap_255[7:0]								FFh

Description	This command is for Gamma to linear lookup table remapping points.
Restriction	

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(FE42h): CMD Mode Switch

R/W	Addr	D7	D6	D5	D4	D3	D2	D1	D0	HEX
W	FE42h	CMD_Page[7:0]								00h

Description

This command is used to switch the Manufacture Command Pages and User Commands sets.

CMD_Page[7:0]	Description
00h (default)	User Command Set (UCS = CMD1)
10h	Manufacture Command Set Page Panel ID
12h	Manufacture Command Set Page SID
20h	Manufacture Command Set Page Panel
40h	Manufacture Command Set Page ABH Mode
82h	Manufacture Command Set Page Power
92h	Manufacture Command Set Page SD timing
50h	Manufacture Command Set Page Gamma1
60h	Manufacture Command Set Page Gamma2
30h	Manufacture Command Set Page Gamma3
52h	Manufacture Command Set Page Gamma4
70h	Manufacture Command Set Page GOA Timing 1
F0h	Manufacture Command Set Page GOA Timing 2
42h	Manufacture Command Set Page DBV
22h	Manufacture Command Set Page SES
80h	Manufacture Command Set Page APRC
90h	Manufacture Command Set Page ACL
62h	Manufacture Command Set Page CGM
C2h	Manufacture Command Set Page CGM LUT

Restriction

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(FF42h): Read CMD Status

R/W	Addr	D7	D6	D5	D4	D3	D2	D1	D0	HEX
R	FF42h	CMD_Status[7:0]								00h

Description	This command is used to read the status of Manufacture Command Pages. Please refer to FE00h
Restriction	-

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1.16MCS: CMD2 Page22, SES Settings

Instruction	R/W	Addr	D7	D6	D5	D4	D3	D2	D1	D0	HEX
SES	R/W	0022h	SES_PAR1[7:0]								00h
SES	R/W	0122h	SES_PAR2[7:0]								00h
SES	R/W	0222h	SES_PAR3[7:0]								00h
SES	R/W	0322h	SES_PAR4[7:0]								00h
SES	R/W	0422h	SES_PAR5[7:0]								00h
SES	R/W	0522h	SES_PAR6[7:0]								00h
SES	R/W	0622h	SES_PAR7[7:0]								00h
SES	R/W	0722h	SES_PAR8[7:0]								00h
SES	R/W	0822h	SES_PAR9[7:0]								00h
SES	R/W	0922h	SES_PAR10[7:0]								00h
SES	R/W	0A22h	SES_PAR11[7:0]								00h
SES	R/W	0B22h	SES_PAR12[7:0]								00h
SES	R/W	0C22h	SES_PAR13[7:0]								00h
SES	R/W	0D22h	SES_PAR14[7:0]								00h
SES	R/W	0E22h	SES_PAR15[7:0]								00h
SES	R/W	0F22h	SES_PAR16[7:0]								00h
SES	R/W	1022h	SES_PAR17[7:0]								00h
SES	R/W	1122h	SES_PAR18[7:0]								00h
SES	R/W	1222h	SES_PAR19[7:0]								00h
SES	R/W	1322h	SES_PAR20[7:0]								00h
SES	R/W	1422h	SES_PAR21[7:0]								00h
SES	R/W	1522h	SES_PAR22[7:0]								00h
SES	R/W	1622h	SES_PAR23[7:0]								00h
SES	R/W	1722h	SES_PAR24[7:0]								00h
SES	R/W	1822h	SES_PAR25[7:0]								00h
SES	R/W	1922h	SES_PAR26[7:0]								00h
SES	R/W	1A22h	SES_PAR27[7:0]								00h
SES	R/W	1B22h	SES_PAR28[7:0]								00h
SES	R/W	1C22h	SES_PAR29[7:0]								00h
SES	R/W	1D22h	SES_PAR30[7:0]								00h
SES	R/W	1E22h	SES_PAR31[7:0]								00h
SES	R/W	1F22h	SES_PAR32[7:0]								00h
SES	R/W	2022h	SES_PAR33[7:0]								00h
SES	R/W	2122h	SES_PAR34[7:0]								00h
SES	R/W	2222h	SES_PAR35[7:0]								00h
SES	R/W	2322h	SES_PAR36[7:0]								00h
SES	R/W	2422h	SES_PAR37[7:0]								00h
SES	R/W	2522h	SES_PAR38[7:0]								00h
SES	R/W	2622h	SES_PAR39[7:0]								00h
SES	R/W	2722h	SES_PAR40[7:0]								00h
SES	R/W	2822h	SES_PAR41[7:0]								00h
SES	R/W	2922h	SES_PAR42[7:0]								00h
SES	R/W	2A22h	SES_PAR43[7:0]								00h
SES	R/W	2B22h	SES_PAR44[7:0]								00h
SES	R/W	2D22h	SES_PAR45[7:0]								00h
SES	R/W	2F22h	SES_PAR46[7:0]								00h
SES	R/W	3022h	SES_PAR47[7:0]								00h
SES	R/W	3122h	SES_PAR48[7:0]								00h

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SES	R/W	3222h	SES_PAR49[7:0]	00h
SES	R/W	3322h	SES_PAR50[7:0]	00h
SES	R/W	3422h	SES_PAR51[7:0]	00h
SES	R/W	3522h	SES_PAR52[7:0]	00h
SES	R/W	3622h	SES_PAR53[7:0]	00h
SES	R/W	3722h	SES_PAR54[7:0]	00h
SES	R/W	3822h	SES_PAR55[7:0]	00h
SES	R/W	3922h	SES_PAR56[7:0]	0Fh
SES	R/W	3A22h	SES_PAR57[7:0]	00h
SES	R/W	3B22h	SES_PAR58[7:0]	00h
SES	R/W	3D22h	SES_PAR59[7:0]	00h
SES	R/W	3F22h	SES_PAR60[7:0]	00h
SES	R/W	4022h	SES_PAR61[7:0]	00h
SES	R/W	4122h	SES_PAR62[7:0]	00h
SES	R/W	4222h	SES_PAR63[7:0]	00h
SES	R/W	4322h	SES_PAR64[7:0]	00h
SES	R/W	4422h	SES_PAR65[7:0]	00h
SES	R/W	4522h	SES_PAR66[7:0]	00h
SES	R/W	4622h	SES_PAR67[7:0]	00h
SES	R/W	4722h	SES_PAR68[7:0]	00h
SES	R/W	4822h	SES_PAR69[7:0]	00h
SES	R/W	4922h	SES_PAR70[7:0]	00h
SES	R/W	4A22h	SES_PAR71[7:0]	00h
SES	R/W	4B22h	SES_PAR72[7:0]	00h
SES	R/W	4C22h	SES_PAR73[7:0]	00h
SES	R/W	4D22h	SES_PAR74[7:0]	00h
SES	R/W	4E22h	SES_PAR75[7:0]	00h
SES	R/W	4F22h	SES_PAR76[7:0]	00h
SES	R/W	5022h	SES_PAR77[7:0]	00h
SES	R/W	5222h	SES_PAR78[7:0]	00h
SES	R/W	5322h	SES_PAR79[7:0]	00h
SES	R/W	5422h	SES_PAR80[7:0]	00h
SES	R/W	5522h	SES_PAR81[7:0]	00h
SES	R/W	5622h	SES_PAR82[7:0]	00h
SES	R/W	5722h	SES_PAR83[7:0]	00h
SES	R/W	5822h	SES_PAR84[7:0]	00h
SES	R/W	5922h	SES_PAR85[7:0]	00h
SES	R/W	5A22h	SES_PAR86[7:0]	00h
SES	R/W	5B22h	SES_PAR87[7:0]	00h
SES	R/W	5C22h	SES_PAR88[7:0]	00h
SES	R/W	5D22h	SES_PAR89[7:0]	00h
SES	R/W	5E22h	SES_PAR90[7:0]	00h
SES	R/W	5F22h	SES_PAR91[7:0]	00h
SES	R/W	6022h	SES_PAR92[7:0]	00h
SES	R/W	6122h	SES_PAR93[7:0]	00h
SES	R/W	6222h	SES_PAR94[7:0]	00h
SES	R/W	6322h	SES_PAR95[7:0]	00h
SES	R/W	6422h	SES_PAR96[7:0]	00h
SES	R/W	6522h	SES_PAR97[7:0]	00h
SES	R/W	6622h	SES_PAR98[7:0]	00h
SES	R/W	6722h	SES_PAR99[7:0]	00h

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SES	R/W	6822h	SES_PAR100[7:0]	00h
SES	R/W	6922h	SES_PAR101[7:0]	00h
SES	R/W	6A22h	SES_PAR102[7:0]	00h
SES	R/W	6B22h	SES_PAR103[7:0]	00h
SES	R/W	6C22h	SES_PAR104[7:0]	00h
SES	R/W	6D22h	SES_PAR105[7:0]	00h
SES	R/W	6E22h	SES_PAR106[7:0]	00h
SES	R/W	6F22h	SES_PAR107[7:0]	00h
SES	R/W	7022h	SES_PAR108[7:0]	00h
SES	R/W	7122h	SES_PAR109[7:0]	00h
SES	R/W	7222h	SES_PAR110[7:0]	00h
SES	R/W	7322h	SES_PAR111[7:0]	00h
SES	R/W	7422h	SES_PAR112[7:0]	00h
SES	R/W	7522h	SES_PAR113[7:0]	00h
SES	R/W	7622h	SES_PAR114[7:0]	00h
SES	R/W	7722h	SES_PAR115[7:0]	00h
SES	R/W	7822h	SES_PAR116[7:0]	00h
SES	R/W	7922h	SES_PAR117[7:0]	00h
SES	R/W	7A22h	SES_PAR118[7:0]	00h
SES	R/W	7B22h	SES_PAR119[7:0]	00h
SES	R/W	7C22h	SES_PAR120[7:0]	00h
SES	R/W	7D22h	SES_PAR121[7:0]	00h
SES	R/W	7E22h	SES_PAR122[7:0]	00h
SES	R/W	7F22h	SES_PAR123[7:0]	00h
SES	R/W	8022h	SES_PAR124[7:0]	00h
SES	R/W	8122h	SES_PAR125[7:0]	00h
SES	R/W	8222h	SES_PAR126[7:0]	00h
SES	R/W	8322h	SES_PAR127[7:0]	00h
SES	R/W	8422h	SES_PAR128[7:0]	00h
SES	R/W	8522h	SES_PAR129[7:0]	00h
SES	R/W	8622h	SES_PAR130[7:0]	00h
SES	R/W	8722h	SES_PAR131[7:0]	00h
SES	R/W	8822h	SES_PAR132[7:0]	00h
SES	R/W	8922h	SES_PAR133[7:0]	00h
SES	R/W	8A22h	SES_PAR134[7:0]	00h
SES	R/W	8B22h	SES_PAR135[7:0]	00h
SES	R/W	8C22h	SES_PAR136[7:0]	00h
SES	R/W	8D22h	SES_PAR137[7:0]	00h
SES	R/W	8E22h	SES_PAR138[7:0]	00h
SES	R/W	8F22h	SES_PAR139[7:0]	00h
SES	R/W	9022h	SES_PAR140[7:0]	00h
SES	R/W	9122h	SES_PAR141[7:0]	00h
SES	R/W	9222h	SES_PAR142[7:0]	00h
SES	R/W	9322h	SES_PAR143[7:0]	00h
SES	R/W	9422h	SES_PAR144[7:0]	00h
SES	R/W	9522h	SES_PAR145[7:0]	00h
SES	R/W	9622h	SES_PAR146[7:0]	00h
CMD Mode Switch	W	FE22h	CMD_Page[7:0]	00h
RD CMD Status	R	FF22h	CMD_Status[7:0]	00h

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(0022h~9722h) SES Parameter

R/W	Addr	D7	D6	D5	D4	D3	D2	D1	D0	HEX
R/W	0022h	SES_PAR1[7:0]								00h
R/W	0122h	SES_PAR2[7:0]								00h
R/W	0222h	SES_PAR3[7:0]								00h
R/W	0322h	SES_PAR4[7:0]								00h
R/W	0422h	SES_PAR5[7:0]								00h
R/W	0522h	SES_PAR6[7:0]								00h
R/W	0622h	SES_PAR7[7:0]								00h
R/W	0722h	SES_PAR8[7:0]								00h
R/W	0822h	SES_PAR9[7:0]								00h
R/W	0922h	SES_PAR10[7:0]								00h
R/W	0A22h	SES_PAR11[7:0]								00h
R/W	0B22h	SES_PAR12[7:0]								00h
R/W	0C22h	SES_PAR13[7:0]								00h
R/W	0D22h	SES_PAR14[7:0]								00h
R/W	0E22h	SES_PAR15[7:0]								00h
R/W	0F22h	SES_PAR16[7:0]								00h
R/W	1022h	SES_PAR17[7:0]								00h
R/W	1122h	SES_PAR18[7:0]								00h
R/W	1222h	SES_PAR19[7:0]								00h
R/W	1322h	SES_PAR20[7:0]								00h
R/W	1422h	SES_PAR21[7:0]								00h
R/W	1522h	SES_PAR22[7:0]								00h
R/W	1622h	SES_PAR23[7:0]								00h
R/W	1722h	SES_PAR24[7:0]								00h
R/W	1822h	SES_PAR25[7:0]								00h
R/W	1922h	SES_PAR26[7:0]								00h
R/W	1A22h	SES_PAR27[7:0]								00h
R/W	1B22h	SES_PAR28[7:0]								00h
R/W	1C22h	SES_PAR29[7:0]								00h
R/W	1D22h	SES_PAR30[7:0]								00h
R/W	1E22h	SES_PAR31[7:0]								00h
R/W	1F22h	SES_PAR32[7:0]								00h
R/W	2022h	SES_PAR33[7:0]								00h
R/W	2122h	SES_PAR34[7:0]								00h
R/W	2222h	SES_PAR35[7:0]								00h
R/W	2322h	SES_PAR36[7:0]								00h

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R/W	2422h	SES_PAR37[7:0]	00h
R/W	2522h	SES_PAR38[7:0]	00h
R/W	2622h	SES_PAR39[7:0]	00h
R/W	2722h	SES_PAR40[7:0]	00h
R/W	2822h	SES_PAR41[7:0]	00h
R/W	2922h	SES_PAR42[7:0]	00h
R/W	2A22h	SES_PAR43[7:0]	00h
R/W	2B22h	SES_PAR44[7:0]	00h
R/W	2D22h	SES_PAR45[7:0]	00h
R/W	2F22h	SES_PAR46[7:0]	00h
R/W	3022h	SES_PAR47[7:0]	00h
R/W	3122h	SES_PAR48[7:0]	00h
R/W	3222h	SES_PAR49[7:0]	00h
R/W	3322h	SES_PAR50[7:0]	00h
R/W	3422h	SES_PAR51[7:0]	00h
R/W	3522h	SES_PAR52[7:0]	00h
R/W	3622h	SES_PAR53[7:0]	00h
R/W	3722h	SES_PAR54[7:0]	00h
R/W	3822h	SES_PAR55[7:0]	00h
R/W	3922h	SES_PAR56[7:0]	0Fh
R/W	3A22h	SES_PAR57[7:0]	00h
R/W	3B22h	SES_PAR58[7:0]	00h
R/W	3D22h	SES_PAR59[7:0]	00h
R/W	3F22h	SES_PAR60[7:0]	00h
R/W	4022h	SES_PAR61[7:0]	00h
R/W	4122h	SES_PAR62[7:0]	00h
R/W	4222h	SES_PAR63[7:0]	00h
R/W	4322h	SES_PAR64[7:0]	00h
R/W	4422h	SES_PAR65[7:0]	00h
R/W	4522h	SES_PAR66[7:0]	00h
R/W	4622h	SES_PAR67[7:0]	00h
R/W	4722h	SES_PAR68[7:0]	00h
R/W	4822h	SES_PAR69[7:0]	00h
R/W	4922h	SES_PAR70[7:0]	00h
R/W	4A22h	SES_PAR71[7:0]	00h
R/W	4B22h	SES_PAR72[7:0]	00h
R/W	4C22h	SES_PAR73[7:0]	00h
R/W	4D22h	SES_PAR74[7:0]	00h

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R/W	4E22h	SES_PAR75[7:0]	00h
R/W	4F22h	SES_PAR76[7:0]	00h
R/W	5022h	SES_PAR77[7:0]	00h
R/W	5222h	SES_PAR78[7:0]	00h
R/W	5322h	SES_PAR79[7:0]	00h
R/W	5422h	SES_PAR80[7:0]	00h
R/W	5522h	SES_PAR81[7:0]	00h
R/W	5622h	SES_PAR82[7:0]	00h
R/W	5722h	SES_PAR83[7:0]	00h
R/W	5822h	SES_PAR84[7:0]	00h
R/W	5922h	SES_PAR85[7:0]	00h
R/W	5A22h	SES_PAR86[7:0]	00h
R/W	5B22h	SES_PAR87[7:0]	00h
R/W	5C22h	SES_PAR88[7:0]	00h
R/W	5D22h	SES_PAR89[7:0]	00h
R/W	5E22h	SES_PAR90[7:0]	00h
R/W	5F22h	SES_PAR91[7:0]	00h
R/W	6022h	SES_PAR92[7:0]	00h
R/W	6122h	SES_PAR93[7:0]	00h
R/W	6222h	SES_PAR94[7:0]	00h
R/W	6322h	SES_PAR95[7:0]	00h
R/W	6422h	SES_PAR96[7:0]	00h
R/W	6522h	SES_PAR97[7:0]	00h
R/W	6622h	SES_PAR98[7:0]	00h
R/W	6722h	SES_PAR99[7:0]	00h
R/W	6822h	SES_PAR100[7:0]	00h
R/W	6922h	SES_PAR101[7:0]	00h
R/W	6A22h	SES_PAR102[7:0]	00h
R/W	6B22h	SES_PAR103[7:0]	00h
R/W	6C22h	SES_PAR104[7:0]	00h
R/W	6D22h	SES_PAR105[7:0]	00h
R/W	6E22h	SES_PAR106[7:0]	00h
R/W	6F22h	SES_PAR107[7:0]	00h
R/W	7022h	SES_PAR108[7:0]	00h
R/W	7122h	SES_PAR109[7:0]	00h
R/W	7222h	SES_PAR110[7:0]	00h
R/W	7322h	SES_PAR111[7:0]	00h
R/W	7422h	SES_PAR112[7:0]	00h

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R/W	7522h	SES_PAR113[7:0]	00h
R/W	7622h	SES_PAR114[7:0]	00h
R/W	7722h	SES_PAR115[7:0]	00h
R/W	7822h	SES_PAR116[7:0]	00h
R/W	7922h	SES_PAR117[7:0]	00h
R/W	7A22h	SES_PAR118[7:0]	00h
R/W	7B22h	SES_PAR119[7:0]	00h
R/W	7C22h	SES_PAR120[7:0]	00h
R/W	7D22h	SES_PAR121[7:0]	00h
R/W	7E22h	SES_PAR122[7:0]	00h
R/W	7F22h	SES_PAR123[7:0]	00h
R/W	8022h	SES_PAR124[7:0]	00h
R/W	8122h	SES_PAR125[7:0]	00h
R/W	8222h	SES_PAR126[7:0]	00h
R/W	8322h	SES_PAR127[7:0]	00h
R/W	8422h	SES_PAR128[7:0]	00h
R/W	8522h	SES_PAR129[7:0]	00h
R/W	8622h	SES_PAR130[7:0]	00h
R/W	8722h	SES_PAR131[7:0]	00h
R/W	8822h	SES_PAR132[7:0]	00h
R/W	8922h	SES_PAR133[7:0]	00h
R/W	8A22h	SES_PAR134[7:0]	00h
R/W	8B22h	SES_PAR135[7:0]	00h
R/W	8C22h	SES_PAR136[7:0]	00h
R/W	8D22h	SES_PAR137[7:0]	00h
R/W	8E22h	SES_PAR138[7:0]	00h
R/W	8F22h	SES_PAR139[7:0]	00h
R/W	9022h	SES_PAR140[7:0]	00h
R/W	9122h	SES_PAR141[7:0]	00h
R/W	9222h	SES_PAR142[7:0]	00h
R/W	9322h	SES_PAR143[7:0]	00h
R/W	9422h	SES_PAR144[7:0]	00h
R/W	9522h	SES_PAR145[7:0]	00h
R/W	9622h	SES_PAR146[7:0]	00h

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Description	These commands are used to set Raydium SES algorithm parameter setting
Restriction	

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(FE22h): CMD Mode Switch

R/W	Addr	D7	D6	D5	D4	D3	D2	D1	D0	HEX
W	FE22h	CMD_Page[7:0]								00h

Description

This command is used to switch the Manufacture Command Pages and User Commands sets.

CMD_Page[7:0]	Description
00h (default)	User Command Set (UCS = CMD1)
10h	Manufacture Command Set Page Panel ID
12h	Manufacture Command Set Page SID
20h	Manufacture Command Set Page Panel
40h	Manufacture Command Set Page ABH Mode
82h	Manufacture Command Set Page Power
92h	Manufacture Command Set Page SD timing
50h	Manufacture Command Set Page Gamma1
60h	Manufacture Command Set Page Gamma2
30h	Manufacture Command Set Page Gamma3
52h	Manufacture Command Set Page Gamma4
70h	Manufacture Command Set Page GOA Timing 1
F0h	Manufacture Command Set Page GOA Timing 2
42h	Manufacture Command Set Page DBV
22h	Manufacture Command Set Page SES
80h	Manufacture Command Set Page APRC
90h	Manufacture Command Set Page ACL
62h	Manufacture Command Set Page CGM
C2h	Manufacture Command Set Page CGM LUT

Restriction

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(FF22h): Read CMD Status

R/W	Addr	D7	D6	D5	D4	D3	D2	D1	D0	HEX
R	FF22h	CMD_Status[7:0]								00h

Description	This command is used to read the status of Manufacture Command Pages. Please refer to FE00h
Restriction	-

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1.17MCS: CMD2 Page80, APRC Settings

Instruction	R/W	Addr	D7	D6	D5	D4	D3	D2	D1	D0	HEX
APRC	R/W	4B80h	APRC_PAR1[7:0]								00h
APRC	R/W	4C80h	APRC_PAR2[7:0]								00h
APRC	R/W	4D80h	APRC_PAR3[7:0]								00h
APRC	R/W	4E80h	APRC_PAR4[7:0]								00h
APRC	R/W	4F80h	APRC_PAR5[7:0]								00h
APRC	R/W	5080h	APRC_PAR6[7:0]								00h
APRC	R/W	5280h	APRC_PAR7[7:0]								00h
APRC	R/W	5380h	APRC_PAR8[7:0]								00h
APRC	R/W	5480h	APRC_PAR9[7:0]								00h
APRC	R/W	5580h	APRC_PAR10[7:0]								00h
APRC	R/W	5680h	APRC_PAR11[7:0]								00h
APRC	R/W	5780h	APRC_PAR12[7:0]								00h
APRC	R/W	5880h	APRC_PAR13[7:0]								00h
APRC	R/W	5980h	APRC_PAR14[7:0]								00h
APRC	R/W	5A80h	APRC_PAR15[7:0]								00h
APRC	R/W	5B80h	APRC_PAR16[7:0]								00h
APRC	R/W	5C80h	APRC_PAR17[7:0]								00h
APRC	R/W	5D80h	APRC_PAR18[7:0]								00h
APRC	R/W	5E80h	APRC_PAR19[7:0]								00h
APRC	R/W	5F80h	APRC_PAR20[7:0]								00h
APRC	R/W	6080h	APRC_PAR21[7:0]								00h
APRC	R/W	6180h	APRC_PAR22[7:0]								00h
APRC	R/W	6280h	APRC_PAR23[7:0]								00h
APRC	R/W	6380h	APRC_PAR24[7:0]								00h
APRC	R/W	6480h	APRC_PAR25[7:0]								00h
APRC	R/W	6580h	APRC_PAR26[7:0]								00h
APRC	R/W	6680h	APRC_PAR27[7:0]								00h
APRC	R/W	6780h	APRC_PAR28[7:0]								00h
APRC	R/W	6880h	APRC_PAR29[7:0]								00h
APRC	R/W	6980h	APRC_PAR30[7:0]								00h
APRC	R/W	6A80h	APRC_PAR31[7:0]								00h
APRC	R/W	6B80h	APRC_PAR32[7:0]								00h
APRC	R/W	6C80h	APRC_PAR33[7:0]								00h
APRC	R/W	6D80h	APRC_PAR34[7:0]								00h
APRC	R/W	6E80h	APRC_PAR35[7:0]								00h
APRC	R/W	6F80h	APRC_PAR36[7:0]								00h
APRC	R/W	7080h	APRC_PAR37[7:0]								00h
APRC	R/W	7180h	APRC_PAR38[7:0]								00h
APRC	R/W	7280h	APRC_PAR39[7:0]								00h
APRC	R/W	7380h	APRC_PAR40[7:0]								00h
APRC	R/W	7480h	APRC_PAR41[7:0]								00h
APRC	R/W	7580h	APRC_PAR42[7:0]								00h
APRC	R/W	7680h	APRC_PAR43[7:0]								00h
APRC	R/W	7780h	APRC_PAR44[7:0]								00h
APRC	R/W	7880h	APRC_PAR45[7:0]								00h
APRC	R/W	7980h	APRC_PAR46[7:0]								00h
APRC	R/W	7A80h	APRC_PAR47[7:0]								00h

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APRC	R/W	7B80h	APRC_PAR48[7:0]							00h
APRC	R/W	7C80h	APRC_PAR49[7:0]							00h
APRC	R/W	7D80h	APRC_PAR50[7:0]							00h
APRC	R/W	7E80h	APRC_PAR51[7:0]							00h
APRC	R/W	7F80h	APRC_PAR52[7:0]							00h
APRC	R/W	8080h	APRC_PAR53[7:0]							00h
APRC	R/W	8180h	APRC_PAR54[7:0]							00h
APRC	R/W	8280h	APRC_PAR55[7:0]							00h
APRC	R/W	8380h	APRC_PAR56[7:0]							00h
APRC	R/W	8480h	APRC_PAR57[7:0]							00h
APRC	R/W	8580h	APRC_PAR58[7:0]							00h
APRC	R/W	8680h	APRC_PAR59[7:0]							00h
APRC	R/W	8780h	APRC_PAR60[7:0]							00h
APRC	R/W	8880h	APRC_PAR61[7:0]							00h
APRC	R/W	8980h	APRC_PAR62[7:0]							00h
APRC	R/W	8A80h	APRC_PAR63[7:0]							00h
APRC	R/W	8B80h	APRC_PAR64[7:0]							00h
APRC	R/W	8C80h	APRC_PAR65[7:0]							00h
APRC	R/W	8D80h	APRC_PAR66[7:0]							00h
APRC	R/W	8E80h	APRC_PAR67[7:0]							00h
APRC	R/W	8F80h	APRC_PAR68[7:0]							00h
APRC	R/W	9080h	APRC_PAR69[7:0]							00h
APRC	R/W	9180h	APRC_PAR70[7:0]							00h
APRC	R/W	9280h	APRC_PAR71[7:0]							00h
APRC	R/W	9380h	APRC_PAR72[7:0]							00h
APRC	R/W	9480h	APRC_PAR73[7:0]							00h
APRC	R/W	9580h	APRC_PAR74[7:0]							00h
APRC	R/W	9680h	APRC_PAR75[7:0]							00h
APRC	R/W	9780h	APRC_PAR76[7:0]							00h
APRC	R/W	9880h	APRC_PAR77[7:0]							00h
APRC	R/W	9980h	APRC_PAR78[7:0]							00h
APRC	R/W	9A80h	APRC_PAR79[7:0]							00h
APRC	R/W	9B80h	APRC_PAR80[7:0]							00h
APRC	R/W	9C80h	APRC_PAR81[7:0]							00h
APRC	R/W	9D80h	APRC_PAR82[7:0]							00h
APRC	R/W	9E80h	APRC_PAR83[7:0]							00h
APRC	R/W	9F80h	APRC_PAR84[7:0]							00h
APRC	R/W	A080h	-	-	-	-	-	-	APRC_en[1:0]	00h
CMD Mode Switch	W	FE80h	CMD_Page[7:0]							00h
RD CMD Status	R	FF80h	CMD_Status[7:0]							00h

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(4B80h~9F80h) APRC Parameter

R/W	Addr	D7	D6	D5	D4	D3	D2	D1	D0	HEX
R/W	4B80h	APRC_PAR1[7:0]								00h
R/W	4C80h	APRC_PAR2[7:0]								00h
R/W	4D80h	APRC_PAR3[7:0]								00h
R/W	4E80h	APRC_PAR4[7:0]								00h
R/W	4F80h	APRC_PAR5[7:0]								00h
R/W	5080h	APRC_PAR6[7:0]								00h
R/W	5280h	APRC_PAR7[7:0]								00h
R/W	5380h	APRC_PAR8[7:0]								00h
R/W	5480h	APRC_PAR9[7:0]								00h
R/W	5580h	APRC_PAR10[7:0]								00h
R/W	5680h	APRC_PAR11[7:0]								00h
R/W	5780h	APRC_PAR12[7:0]								00h
R/W	5880h	APRC_PAR13[7:0]								00h
R/W	5980h	APRC_PAR14[7:0]								00h
R/W	5A80h	APRC_PAR15[7:0]								00h
R/W	5B80h	APRC_PAR16[7:0]								00h
R/W	5C80h	APRC_PAR17[7:0]								00h
R/W	5D80h	APRC_PAR18[7:0]								00h
R/W	5E80h	APRC_PAR19[7:0]								00h
R/W	5F80h	APRC_PAR20[7:0]								00h
R/W	6080h	APRC_PAR21[7:0]								00h
R/W	6180h	APRC_PAR22[7:0]								00h
R/W	6280h	APRC_PAR23[7:0]								00h
R/W	6380h	APRC_PAR24[7:0]								00h
R/W	6480h	APRC_PAR25[7:0]								00h
R/W	6580h	APRC_PAR26[7:0]								00h
R/W	6680h	APRC_PAR27[7:0]								00h
R/W	6780h	APRC_PAR28[7:0]								00h
R/W	6880h	APRC_PAR29[7:0]								00h
R/W	6980h	APRC_PAR30[7:0]								00h
R/W	6A80h	APRC_PAR31[7:0]								00h
R/W	6B80h	APRC_PAR32[7:0]								00h
R/W	6C80h	APRC_PAR33[7:0]								00h
R/W	6D80h	APRC_PAR34[7:0]								00h
R/W	6E80h	APRC_PAR35[7:0]								00h
R/W	6F80h	APRC_PAR36[7:0]								00h

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R/W	7080h	APRC_PAR37[7:0]	00h
R/W	7180h	APRC_PAR38[7:0]	00h
R/W	7280h	APRC_PAR39[7:0]	00h
R/W	7380h	APRC_PAR40[7:0]	00h
R/W	7480h	APRC_PAR41[7:0]	00h
R/W	7580h	APRC_PAR42[7:0]	00h
R/W	7680h	APRC_PAR43[7:0]	00h
R/W	7780h	APRC_PAR44[7:0]	00h
R/W	7880h	APRC_PAR45[7:0]	00h
R/W	7980h	APRC_PAR46[7:0]	00h
R/W	7A80h	APRC_PAR47[7:0]	00h
R/W	7B80h	APRC_PAR48[7:0]	00h
R/W	7C80h	APRC_PAR49[7:0]	00h
R/W	7D80h	APRC_PAR50[7:0]	00h
R/W	7E80h	APRC_PAR51[7:0]	00h
R/W	7F80h	APRC_PAR52[7:0]	00h
R/W	8080h	APRC_PAR53[7:0]	00h
R/W	8180h	APRC_PAR54[7:0]	00h
R/W	8280h	APRC_PAR55[7:0]	00h
R/W	8380h	APRC_PAR56[7:0]	00h
R/W	8480h	APRC_PAR57[7:0]	00h
R/W	8580h	APRC_PAR58[7:0]	00h
R/W	8680h	APRC_PAR59[7:0]	00h
R/W	8780h	APRC_PAR60[7:0]	00h
R/W	8880h	APRC_PAR61[7:0]	00h
R/W	8980h	APRC_PAR62[7:0]	00h
R/W	8A80h	APRC_PAR63[7:0]	00h
R/W	8B80h	APRC_PAR64[7:0]	00h
R/W	8C80h	APRC_PAR65[7:0]	00h
R/W	8D80h	APRC_PAR66[7:0]	00h
R/W	8E80h	APRC_PAR67[7:0]	00h
R/W	8F80h	APRC_PAR68[7:0]	00h
R/W	9080h	APRC_PAR69[7:0]	00h
R/W	9180h	APRC_PAR70[7:0]	00h
R/W	9280h	APRC_PAR71[7:0]	00h
R/W	9380h	APRC_PAR72[7:0]	00h
R/W	9480h	APRC_PAR73[7:0]	00h
R/W	9580h	APRC_PAR74[7:0]	00h

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R/W	9680h	APRC_PAR75[7:0]	00h
R/W	9780h	APRC_PAR76[7:0]	00h
R/W	9880h	APRC_PAR77[7:0]	00h
R/W	9980h	APRC_PAR78[7:0]	00h
R/W	9A80h	APRC_PAR79[7:0]	00h
R/W	9B80h	APRC_PAR80[7:0]	00h
R/W	9C80h	APRC_PAR81[7:0]	00h
R/W	9D80h	APRC_PAR82[7:0]	00h
R/W	9E80h	APRC_PAR83[7:0]	00h
R/W	9F80h	APRC_PAR84[7:0]	00h

Description	These commands are used to set Raydium APRC(Advanced Pixel Rendering Compensation) algorithm parameter setting
Restriction	

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(A080h) APRC Enable

R/W	Addr	D7	D6	D5	D4	D3	D2	D1	D0	HEX
R/W	A080h	-	-	-	-	-	-	APRC_en[1:0]		00h

Description	These commands are used to set the APRC enable Bit: APRC_en[1:0] Description: APRC enable Data: 0:disable 3:enable othres : Reserved
Restriction	

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(FE80h): CMD Mode Switch

R/W	Addr	D7	D6	D5	D4	D3	D2	D1	D0	HEX
W	FE80h	CMD_Page[7:0]								00h

Description

This command is used to switch the Manufacture Command Pages and User Commands sets.

CMD_Page[7:0]	Description
00h (default)	User Command Set (UCS = CMD1)
10h	Manufacture Command Set Page Panel ID
12h	Manufacture Command Set Page SID
20h	Manufacture Command Set Page Panel
40h	Manufacture Command Set Page ABH Mode
82h	Manufacture Command Set Page Power
92h	Manufacture Command Set Page SD timing
50h	Manufacture Command Set Page Gamma1
60h	Manufacture Command Set Page Gamma2
30h	Manufacture Command Set Page Gamma3
52h	Manufacture Command Set Page Gamma4
70h	Manufacture Command Set Page GOA Timing 1
F0h	Manufacture Command Set Page GOA Timing 2
42h	Manufacture Command Set Page DBV
22h	Manufacture Command Set Page SES
80h	Manufacture Command Set Page APRC
90h	Manufacture Command Set Page ACL
62h	Manufacture Command Set Page CGM
C2h	Manufacture Command Set Page CGM LUT

Restriction

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(FF80h): Read CMD Status

R/W	Addr	D7	D6	D5	D4	D3	D2	D1	D0	HEX
R	FF80h	CMD_Status[7:0]								00h

Description	This command is used to read the status of Manufacture Command Pages. Please refer to FE00h
Restriction	-

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1.18MCS: CMD2 Page90, ACL Settings

Instruction	R/W	Addr	D7	D6	D5	D4	D3	D2	D1	D0	HEX
ACL_YCOEF	R/W	9E90h	ACL_ycoef_r[7:0]								40h
ACL_YCOEF	R/W	9F90h	ACL_ycoef_g[7:0]								40h
ACL_YCOEF	R/W	A090h	ACL_ycoef_b[7:0]								80h
ACL_CLAMP	R/W	A390h	ACL_start_up_0[7:0]								99h
ACL_CLAMP	R/W	A490h	ACL_start_up_1[7:0]								99h
ACL_CLAMP	R/W	A590h	ACL_start_up_2[7:0]								99h
ACL_CLAMP	R/W	A690h	ACL_start_up_3[7:0]								99h
ACL_CLAMP	R/W	A790h	ACL_start_up_4[7:0]								99h
ACL_CLAMP	R/W	A990h	ACL_start_up_5[7:0]								99h
ACL_CLAMP	R/W	AA90h	ACL_start_up_6[7:0]								99h
ACL_CLAMP	R/W	AB90h	ACL_start_up_7[7:0]								99h
UD_psa	R/W	AC90h	-	-	-	-	-	-	UD_psa[1:0]		02h
ACL_DIM	R/W	AD90h	-	DIM_FT[2:0]			-	-	DIM_type[1:0]		02h
ACL_DIM	R/W	AE90h	-	DIM_FS[6:0]							01h
ACL_reserve	R/W	B090h	-	ACL_M_map[2:0]			-	ACL_H_map[2:0]			65h
ACL_reserve	R/W	B190h	-	-	-	-	-	ACL_L_map[2:0]			07h
ACL_reserve	R/W	B390h	ACL_slope_0[7:0]								0Fh
ACL_reserve	R/W	B490h	ACL_slope_1[7:0]								1Eh
ACL_reserve	R/W	B590h	ACL_slope_2[7:0]								2Dh
ACL_reserve	R/W	B690h	ACL_slope_3[7:0]								3Fh
ACL_reserve	R/W	B790h	ACL_slope_3[9:8]		ACL_slope_2[9:8]		ACL_slope_1[9:8]		ACL_slope_0[9:8]		00h
ACL_reserve	R/W	B890h	ACL_slope_4[7:0]								4Eh
ACL_reserve	R/W	B990h	ACL_slope_5[7:0]								5Fh
ACL_reserve	R/W	BA90h	ACL_slope_6[7:0]								71h
ACL_reserve	R/W	BB90h	ACL_slope_7[7:0]								85h
ACL_reserve	R/W	BC90h	ACL_slope_7[9:8]		ACL_slope_6[9:8]		ACL_slope_5[9:8]		ACL_slope_4[9:8]		00h
ACL_HBM	R/W	BD90h	HBM_ACL_by_UCS	-	-	-	ACL_hbm_en	ACL_hbm_level[2:0]			80h
CMD Mode Switch	W	FE90h	CMD_Page[7:0]								00h
CMD	R	FF90h	CMD_Status[7:0]								00h

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Status				

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(9E90h~A090h) ACL_YCOEF

R/W	Addr	D7	D6	D5	D4	D3	D2	D1	D0	HEX
R/W	9E90h	ACL_ycoef_r[7:0]								40h
R/W	9F90h	ACL_ycoef_g[7:0]								40h
R/W	A090h	ACL_ycoef_b[7:0]								80h

Description	These commands set the ratio for adjusting the RGB value. Parameter: ACL_ycoef_r[7:0], ACL_ycoef_g[7:0], ACL_ycoef_b[7:0] Description: Average Y value depends on weighted RGB value.
Restriction	

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(A390h~AB90h) ACL_CLAMP

R/W	Addr	D7	D6	D5	D4	D3	D2	D1	D0	HEX
R/W	A390h	ACL_start_up_0[7:0]								99h
R/W	A490h	ACL_start_up_1[7:0]								99h
R/W	A590h	ACL_start_up_2[7:0]								99h
R/W	A690h	ACL_start_up_3[7:0]								99h
R/W	A790h	ACL_start_up_4[7:0]								99h
R/W	A990h	ACL_start_up_5[7:0]								99h
R/W	AA90h	ACL_start_up_6[7:0]								99h
R/W	AB90h	ACL_start_up_7[7:0]								99h

Description

These commands set 8 different levels of start-up value for ACL_ curve setting.

Parameter	Description
ACL_ start_up _0[7:0]	This setting is valid when ACL_hbm_level or ACL_map=3’b000
ACL_ start_up _1[7:0]	This setting is valid when ACL_hbm_level or ACL_map=3’b001
ACL_ start_up _2[7:0]	This setting is valid when ACL_hbm_level or ACL_map=3’b010
ACL_ start_up _3[7:0]	This setting is valid when ACL_hbm_level or ACL_map=3’b011
ACL_ start_up _4[7:0]	This setting is valid when ACL_hbm_level or ACL_map=3’b100
ACL_ start_up _5[7:0]	This setting is valid when ACL_hbm_level or ACL_map=3’b101
ACL_ start_up _6[7:0]	This setting is valid when ACL_hbm_level or ACL_map=3’b110
ACL_ start_up _7[7:0]	This setting is valid when ACL_hbm_level or ACL_map=3’b111

Restriction

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(AC90h) ACL_PSA

R/W	Addr	D7	D6	D5	D4	D3	D2	D1	D0	HEX
R/W	AC90h	-	-	-	-	-	-	UD_psa [1:0]		02h

Description	This command sets the turning-point for the ACL function. Parameter: UD_PSA[1:0] Description: 2'b00 : From code 0 2'b01 : From code 64 2'b10 : From code 128 2'b11 : From code 192
Restriction	

(AD90h~AE90h) ACL_DIM

R/W	Addr	D7	D6	D5	D4	D3	D2	D1	D0	HEX
R/W	AD90h	-	DIM_FT[2:0]			-	-	DIM_type [1:0]		02h
R/W	AE90h	-	DIM_FS[6:0]							01h

Description	These commands define the dimming settings. Parameter: DIM_TYPE[1:0] Description: 2'b00 and 2'b11: No dimming 2'b01 : Fixed time dimming 2'b10 : Fixed slope dimming Parameter: DIM_FT[2:0] Description: The number of frames used for the dimming period Total period is 2^(DIM_FT[2:0]+1) frames. Parameter: DIM_FS[6:0] Description: The number of steps used for the dimming period
Restriction	

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(B090h~B190h) ACL_MAP

R/W	Addr	D7	D6	D5	D4	D3	D2	D1	D0	HEX
R/W	B090h	-	ACL_M_map[2:0]			-	ACL_H_map[2:0]			65h
R/W	B190h	-	-	-	-	-	ACL_L_map[2:0]			07h

Description	These commands set the levels of code reduction from old data to re-mapped ones. Parameter / Description ACL_L_MAP[2:0] — This setting is valid when ACL[1:0]=2'b01 ACL_M_MAP[2:0] — This setting is valid when ACL[1:0]=2'b10 ACL_H_MAP[2:0] — This setting is valid when ACL[1:0]=2'b11
Restriction	

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(B390h~BC90h) ACL_SLOPE

R/W	Addr	D7	D6	D5	D4	D3	D2	D1	D0	HEX
R/W	B390h	ACL_slope_0[7:0]								0Fh
R/W	B490h	ACL_slope_1[7:0]								1Eh
R/W	B590h	ACL_slope_2[7:0]								2Dh
R/W	B690h	ACL_slope_3[7:0]								3Fh
R/W	B790h	ACL_slope _3[9:8]		ACL_slope _2[9:8]		ACL_slope _1[9:8]		ACL_slope _0[9:8]		00h
R/W	B890h	ACL_slope_4[7:0]								4Eh
R/W	B990h	ACL_slope_5[7:0]								5Fh
R/W	BA90h	ACL_slope_6[7:0]								71h
R/W	BB90h	ACL_slope_7[7:0]								85h
R/W	BC90h	ACL_slope _7[9:8]		ACL_slope _6[9:8]		ACL_slope _5[9:8]		ACL_slope _4[9:8]		00h

Description

These commands set 8 different levels of slope for ACL_ curve setting.

Parameter	Description
ACL_slope_0[9:0]	This setting is valid when ACL_hbm_level or ACL_map=3’b000
ACL_slope_1[9:0]	This setting is valid when ACL_hbm_level or ACL_map=3’b001
ACL_slope_2[9:0]	This setting is valid when ACL_hbm_level or ACL_map=3’b010
ACL_slope_3[9:0]	This setting is valid when ACL_hbm_level or ACL_map=3’b011
ACL_slope_4[9:0]	This setting is valid when ACL_hbm_level or ACL_map=3’b100
ACL_slope_5[9:0]	This setting is valid when ACL_hbm_level or ACL_map=3’b101
ACL_slope_6[9:0]	This setting is valid when ACL_hbm_level or ACL_map=3’b110
ACL_slope_7[9:0]	This setting is valid when ACL_hbm_level or ACL_map=3’b111

Restriction

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(BD90h) ACL_HBM

R/W	Addr	D7	D6	D5	D4	D3	D2	D1	D0	HEX
R/W	BD90h	HBM_ACL_by_UCS	-	-	-	ACL_hbm_en	ACL_hbm_leve[2:0]			80h

Description	These commands set the ACL_ operational condition in HBM mode. Parameter / Description HBM_ACL_by_UCS: 1'b1 : ACL_ control by UCS(5500) in HBM mode; 1'b0 : ACL_ control by MCS(BD90[3]) in HBM mode ACL_hbm_en: ACL_ enable signal in HBM mode ACL_hbm_leve[2:0]: This setting is valid when HBM_ACL_by_UCS=1'b1 and ACL_hbm_en=1'b1
Restriction	

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(FE90h): CMD Mode Switch

R/W	Addr	D7	D6	D5	D4	D3	D2	D1	D0	HEX
W	FE90h	CMD_Page[7:0]								00h

Description

This command is used to switch the Manufacture Command Pages and User Commands sets.

CMD_Page[7:0]	Description
00h (default)	User Command Set (UCS = CMD1)
10h	Manufacture Command Set Page Panel ID
12h	Manufacture Command Set Page SID
20h	Manufacture Command Set Page Panel
40h	Manufacture Command Set Page ABH Mode
82h	Manufacture Command Set Page Power
92h	Manufacture Command Set Page SD timing
50h	Manufacture Command Set Page Gamma1
60h	Manufacture Command Set Page Gamma2
30h	Manufacture Command Set Page Gamma3
52h	Manufacture Command Set Page Gamma4
70h	Manufacture Command Set Page GOA Timing 1
F0h	Manufacture Command Set Page GOA Timing 2
42h	Manufacture Command Set Page DBV
22h	Manufacture Command Set Page SES
80h	Manufacture Command Set Page APRC
90h	Manufacture Command Set Page ACL
62h	Manufacture Command Set Page CGM
C2h	Manufacture Command Set Page CGM LUT

Restriction

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(FF90h): Read CMD Status

R/W	Addr	D7	D6	D5	D4	D3	D2	D1	D0	HEX
R	FF90h	CMD_Status[7:0]								00h

Description	This command is used to read the status of Manufacture Command Pages. Please refer to FE00h
Restriction	-

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1.19MCS: CMD2 Page62, CGM Settings

Instruction	R/W	Addr	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Color Temperature Setting Parameter	R/W	0062h	color_temp1_PAR1[7:0]								00h
	R/W	0162h	color_temp1_ PAR2[7:0]								00h
	R/W	0262h	color_temp1_PAR3[7:0]								00h
	R/W	0362h	color_temp2_PAR1[7:0]								00h
	R/W	0462h	color_temp2_PAR2[7:0]								00h
	R/W	0562h	color_temp2_PAR3[7:0]								00h
	R/W	0662h	color_temp3_PAR1[7:0]								00h
	R/W	0762h	color_temp3_PAR2[7:0]								00h
	R/W	0862h	color_temp3_PAR3[7:0]								00h
Color Gamut Mapping Parameter	R/W	0962h	cgm_PAR1[7:0]								00h
	R/W	0A62h	cgm_PAR2[7:0]								00h
	R/W	0B62h	cgm_PAR3[7:0]								00h
	R/W	0C62h	cgm_PAR4[7:0]								00h
	R/W	0D62h	cgm_PAR5[7:0]								00h
	R/W	0E62h	cgm_PAR6[7:0]								00h
	R/W	0F62h	cgm_PAR7[7:0]								00h
	R/W	1062h	cgm_PAR8[7:0]								00h
	R/W	1162h	cgm_PAR9[7:0]								00h
	R/W	1262h	cgm_PAR10[7:0]								00h
	R/W	1362h	cgm_PAR11[7:0]								00h
	R/W	1462h	cgm_PAR12[7:0]								00h
	R/W	1562h	cgm_PAR13[7:0]								00h
	R/W	1662h	cgm_PAR14[7:0]								00h
CGM Enable	R/W	3162h	-	-	-	-	-	cgm_en_HBM	cgm_en_B	cgm_en_A	00h
CMD Mode Switch	W	FE62h	CMD_Page[7:0]								00h
RD CMD Status	R	FF62h	CMD_Status[7:0]								00h

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(0062h~0862h) Color Temperature Parameter

R/W	Addr	D7	D6	D5	D4	D3	D2	D1	D0	HEX
R/W	0062h	color_temp1_PAR1[7:0]								00h
R/W	0162h	color_ temp1_PAR2[7:0]								00h
R/W	0262h	color_ temp1_PAR3[7:0]								00h
R/W	0362h	color_temp2_PAR1[7:0]								00h
R/W	0462h	color_ temp2_PAR2[7:0]								00h
R/W	0562h	color_ temp2_PAR3[7:0]								00h
R/W	0662h	color_temp3_PAR1[7:0]								00h
R/W	0762h	color_ temp3_PAR2[7:0]								00h
R/W	0862h	color_ temp3_PAR3[7:0]								00h

Description	These commands are used to set the color temperature transfer matrix. color_temp1_PAR1~PAR3: color temperature transfer matrix for 1st configuration color_temp2_PAR1~PAR3: color temperature transfer matrix for 2nd configuration color_temp3_PAR1~PAR3: color temperature transfer matrix for 3rd configuration
Restriction	

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(0962h~1662h) Color Gamut Mapping Parameter

R/W	Addr	D7	D6	D5	D4	D3	D2	D1	D0	HEX
R/W	0962h	cgm_PAR1[7:0]								00h
R/W	0A62h	cgm_PAR2[7:0]								00h
R/W	0B62h	cgm_PAR3[7:0]								00h
R/W	0C62h	cgm_PAR4[7:0]								00h
R/W	0D62h	cgm_PAR5[7:0]								00h
R/W	0E62h	cgm_PAR6[7:0]								00h
R/W	0F62h	cgm_PAR7[7:0]								00h
R/W	1062h	cgm_PAR8[7:0]								00h
R/W	1162h	cgm_PAR9[7:0]								00h
R/W	1262h	cgm_PAR10[7:0]								00h
R/W	1362h	cgm_PAR11[7:0]								00h
R/W	1462h	cgm_PAR12[7:0]								00h
R/W	1562h	cgm_PAR13[7:0]								00h
R/W	1662h	cgm_PAR14[7:0]								00h

Description	These commands are used to set the color gamut mapping parameter setting
Restriction	

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(3162h) CGM Enable

R/W	Addr	D7	D6	D5	D4	D3	D2	D1	D0	HEX
R/W	3162h	-	-	-	-	-	cgm_en_HBM	cgm_en_B	cgm_en_A	00h

Description	This command is used to select CGM enable: Bit: Description cgm_en_HBM: CGM enable for HBM mode cgm_en_B: CGM enable for IDLE mode cgm_en_A: CGM enable for normal mode
Restriction	

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(FE62h): CMD Mode Switch

R/W	Addr	D7	D6	D5	D4	D3	D2	D1	D0	HEX
W	FE62h	CMD_Page[7:0]								00h

Description

This command is used to switch the Manufacture Command Pages and User Commands sets.

CMD_Page[7:0]	Description
00h (default)	User Command Set (UCS = CMD1)
10h	Manufacture Command Set Page Panel ID
12h	Manufacture Command Set Page SID
20h	Manufacture Command Set Page Panel
40h	Manufacture Command Set Page ABH Mode
82h	Manufacture Command Set Page Power
92h	Manufacture Command Set Page SD timing
50h	Manufacture Command Set Page Gamma1
60h	Manufacture Command Set Page Gamma2
30h	Manufacture Command Set Page Gamma3
52h	Manufacture Command Set Page Gamma4
70h	Manufacture Command Set Page GOA Timing 1
F0h	Manufacture Command Set Page GOA Timing 2
42h	Manufacture Command Set Page DBV
22h	Manufacture Command Set Page SES
80h	Manufacture Command Set Page APRC
90h	Manufacture Command Set Page ACL
62h	Manufacture Command Set Page CGM
C2h	Manufacture Command Set Page CGM LUT

Restriction

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(FF62h): Read CMD Status

R/W	Addr	D7	D6	D5	D4	D3	D2	D1	D0	HEX
R	FF62h	CMD_Status[7:0]								00h

Description	This command is used to read the status of Manufacture Command Pages. Please refer to FE00h
Restriction	-

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1.20MCS: CMD2 Page C2, CGM LUT Settings

Instruction	R/W	Addr	D7	D6	D5	D4	D3	D2	D1	D0	HEX
CGM LUT Setting Parameters	R/W	00C2h	cgm_lut_PAR1[7:0]								00h
	R/W	01C2h	cgm_lut_PAR2[7:0]								00h
	R/W	02C2h	cgm_lut_PAR3[7:0]								00h
	R/W	03C2h	cgm_lut_PAR4[7:0]								00h
	R/W	04C2h	cgm_lut_PAR5[7:0]								00h
	R/W	05C2h	cgm_lut_PAR6[7:0]								00h
	R/W	06C2h	cgm_lut_PAR7[7:0]								00h
	R/W	07C2h	cgm_lut_PAR8[7:0]								00h
	R/W	08C2h	cgm_lut_PAR9[7:0]								00h
	R/W	09C2h	cgm_lut_PAR10[7:0]								00h
	R/W	0AC2h	cgm_lut_PAR11[7:0]								00h
	R/W	0BC2h	cgm_lut_PAR12[7:0]								00h
	R/W	0CC2h	cgm_lut_PAR13[7:0]								00h
	R/W	0DC2h	cgm_lut_PAR14[7:0]								00h
	R/W	0EC2h	cgm_lut_PAR15[7:0]								00h
	R/W	0FC2h	cgm_lut_PAR16[7:0]								00h
	R/W	10C2h	cgm_lut_PAR17[7:0]								00h
	R/W	11C2h	cgm_lut_PAR18[7:0]								00h
	R/W	12C2h	cgm_lut_PAR19[7:0]								00h
	R/W	13C2h	cgm_lut_PAR20[7:0]								00h
	R/W	14C2h	cgm_lut_PAR21[7:0]								00h
	R/W	15C2h	cgm_lut_PAR22[7:0]								00h
	R/W	16C2h	cgm_lut_PAR23[7:0]								00h
	R/W	17C2h	cgm_lut_PAR24[7:0]								00h
	R/W	18C2h	cgm_lut_PAR25[7:0]								00h
	R/W	19C2h	cgm_lut_PAR26[7:0]								00h
	R/W	1AC2h	cgm_lut_PAR27[7:0]								00h
	R/W	1BC2h	cgm_lut_PAR28[7:0]								00h
	R/W	1CC2h	cgm_lut_PAR29[7:0]								00h
	R/W	1DC2h	cgm_lut_PAR30[7:0]								00h
	R/W	1EC2h	cgm_lut_PAR31[7:0]								00h
	R/W	1FC2h	cgm_lut_PAR32[7:0]								00h
	R/W	20C2h	cgm_lut_PAR33[7:0]								00h
	R/W	21C2h	cgm_lut_PAR34[7:0]								00h
	R/W	22C2h	cgm_lut_PAR35[7:0]								00h
	R/W	23C2h	cgm_lut_PAR36[7:0]								00h
	R/W	24C2h	cgm_lut_PAR37[7:0]								00h
	R/W	25C2h	cgm_lut_PAR38[7:0]								00h
	R/W	26C2h	cgm_lut_PAR39[7:0]								00h
	R/W	27C2h	cgm_lut_PAR40[7:0]								00h
	R/W	28C2h	cgm_lut_PAR41[7:0]								00h
	R/W	29C2h	cgm_lut_PAR42[7:0]								00h
	R/W	2AC2h	cgm_lut_PAR43[7:0]								00h
	R/W	2BC2h	cgm_lut_PAR44[7:0]								00h
	R/W	2DC2h	cgm_lut_PAR45[7:0]								00h
	R/W	2FC2h	cgm_lut_PAR46[7:0]								00h
	R/W	30C2h	cgm_lut_PAR47[7:0]								00h

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CGM LUT Setting Parameters	R/W	31C2h	cgm_lut_PAR48[7:0]	00h
	R/W	32C2h	cgm_lut_PAR49[7:0]	00h
	R/W	33C2h	cgm_lut_PAR50[7:0]	00h
	R/W	34C2h	cgm_lut_PAR51[7:0]	00h
	R/W	35C2h	cgm_lut_PAR52[7:0]	00h
	R/W	36C2h	cgm_lut_PAR53[7:0]	00h
	R/W	37C2h	cgm_lut_PAR54[7:0]	00h
	R/W	38C2h	cgm_lut_PAR55[7:0]	00h
	R/W	39C2h	cgm_lut_PAR56[7:0]	00h
	R/W	3AC2h	cgm_lut_PAR57[7:0]	00h
	R/W	3BC2h	cgm_lut_PAR58[7:0]	00h
	R/W	3DC2h	cgm_lut_PAR59[7:0]	00h
	R/W	3FC2h	cgm_lut_PAR60[7:0]	00h
	R/W	40C2h	cgm_lut_PAR61[7:0]	00h
	R/W	41C2h	cgm_lut_PAR62[7:0]	00h
	R/W	42C2h	cgm_lut_PAR63[7:0]	00h
	R/W	43C2h	cgm_lut_PAR64[7:0]	00h
	R/W	44C2h	cgm_lut_PAR65[7:0]	00h
	R/W	45C2h	cgm_lut_PAR66[7:0]	00h
	R/W	46C2h	cgm_lut_PAR67[7:0]	00h
	R/W	47C2h	cgm_lut_PAR68[7:0]	00h
	R/W	48C2h	cgm_lut_PAR69[7:0]	00h
	R/W	49C2h	cgm_lut_PAR70[7:0]	00h
	R/W	4AC2h	cgm_lut_PAR71[7:0]	00h
	R/W	4BC2h	cgm_lut_PAR72[7:0]	00h
	R/W	4CC2h	cgm_lut_PAR73[7:0]	00h
	R/W	4DC2h	cgm_lut_PAR74[7:0]	00h
	R/W	4EC2h	cgm_lut_PAR75[7:0]	00h
	R/W	4FC2h	cgm_lut_PAR76[7:0]	00h
	R/W	50C2h	cgm_lut_PAR77[7:0]	00h
	R/W	52C2h	cgm_lut_PAR78[7:0]	00h
	R/W	53C2h	cgm_lut_PAR79[7:0]	00h
	R/W	54C2h	cgm_lut_PAR80[7:0]	00h
	R/W	55C2h	cgm_lut_PAR81[7:0]	00h
	R/W	56C2h	cgm_lut_PAR82[7:0]	00h
	R/W	57C2h	cgm_lut_PAR83[7:0]	00h
	R/W	58C2h	cgm_lut_PAR84[7:0]	00h
	R/W	59C2h	cgm_lut_PAR85[7:0]	00h
	R/W	5AC2h	cgm_lut_PAR86[7:0]	00h
	R/W	5BC2h	cgm_lut_PAR87[7:0]	00h
	R/W	5CC2h	cgm_lut_PAR88[7:0]	00h
	R/W	5DC2h	cgm_lut_PAR89[7:0]	00h
	R/W	5EC2h	cgm_lut_PAR90[7:0]	00h
	R/W	5FC2h	cgm_lut_PAR91[7:0]	00h
	R/W	60C2h	cgm_lut_PAR92[7:0]	00h
	R/W	61C2h	cgm_lut_PAR93[7:0]	00h
	R/W	62C2h	cgm_lut_PAR94[7:0]	00h
	R/W	63C2h	cgm_lut_PAR95[7:0]	00h
	R/W	64C2h	cgm_lut_PAR96[7:0]	00h
	R/W	65C2h	cgm_lut_PAR97[7:0]	00h
	R/W	66C2h	cgm_lut_PAR98[7:0]	00h

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CGM LUT Setting Parameters	R/W	67C2h	cgm_lut_PAR99[7:0]	00h
	R/W	68C2h	cgm_lut_PAR100[7:0]	00h
	R/W	69C2h	cgm_lut_PAR101[7:0]	00h
	R/W	6AC2h	cgm_lut_PAR102[7:0]	00h
	R/W	6BC2h	cgm_lut_PAR103[7:0]	00h
	R/W	6CC2h	cgm_lut_PAR104[7:0]	00h
	R/W	6DC2h	cgm_lut_PAR105[7:0]	00h
	R/W	6EC2h	cgm_lut_PAR106[7:0]	00h
	R/W	6FC2h	cgm_lut_PAR107[7:0]	00h
	R/W	70C2h	cgm_lut_PAR108[7:0]	00h
	R/W	71C2h	cgm_lut_PAR109[7:0]	00h
	R/W	72C2h	cgm_lut_PAR110[7:0]	00h
	R/W	73C2h	cgm_lut_PAR111[7:0]	00h
	R/W	74C2h	cgm_lut_PAR112[7:0]	00h
	R/W	75C2h	cgm_lut_PAR113[7:0]	00h
	R/W	76C2h	cgm_lut_PAR114[7:0]	00h
	R/W	77C2h	cgm_lut_PAR115[7:0]	00h
	R/W	78C2h	cgm_lut_PAR116[7:0]	00h
	R/W	79C2h	cgm_lut_PAR117[7:0]	00h
	R/W	7AC2h	cgm_lut_PAR118[7:0]	00h
	R/W	7BC2h	cgm_lut_PAR119[7:0]	00h
	R/W	7CC2h	cgm_lut_PAR120[7:0]	00h
	R/W	7DC2h	cgm_lut_PAR121[7:0]	00h
	R/W	7EC2h	cgm_lut_PAR122[7:0]	00h
	R/W	7FC2h	cgm_lut_PAR123[7:0]	00h
	R/W	80C2h	cgm_lut_PAR124[7:0]	00h
	R/W	81C2h	cgm_lut_PAR125[7:0]	00h
	R/W	82C2h	cgm_lut_PAR126[7:0]	00h
	R/W	83C2h	cgm_lut_PAR127[7:0]	00h
	R/W	84C2h	cgm_lut_PAR128[7:0]	00h
	R/W	85C2h	cgm_lut_PAR129[7:0]	00h
	R/W	86C2h	cgm_lut_PAR130[7:0]	00h
	R/W	87C2h	cgm_lut_PAR131[7:0]	00h
	R/W	88C2h	cgm_lut_PAR132[7:0]	00h
	R/W	89C2h	cgm_lut_PAR133[7:0]	00h
	R/W	8AC2h	cgm_lut_PAR134[7:0]	00h
	R/W	8BC2h	cgm_lut_PAR135[7:0]	00h
	R/W	8CC2h	cgm_lut_PAR136[7:0]	00h
	R/W	8DC2h	cgm_lut_PAR137[7:0]	00h
	R/W	8EC2h	cgm_lut_PAR138[7:0]	00h
	R/W	8FC2h	cgm_lut_PAR139[7:0]	00h
	R/W	90C2h	cgm_lut_PAR140[7:0]	00h
	R/W	91C2h	cgm_lut_PAR141[7:0]	00h
	R/W	92C2h	cgm_lut_PAR142[7:0]	00h
	R/W	93C2h	cgm_lut_PAR143[7:0]	00h
	R/W	94C2h	cgm_lut_PAR144[7:0]	00h
	R/W	95C2h	cgm_lut_PAR145[7:0]	00h
	R/W	96C2h	cgm_lut_PAR146[7:0]	00h
	R/W	97C2h	cgm_lut_PAR147[7:0]	00h
	R/W	98C2h	cgm_lut_PAR148[7:0]	00h
	R/W	99C2h	cgm_lut_PAR149[7:0]	00h

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CGM LUT Setting Parameters	R/W	9AC2h	cgm_lut_PAR150[7:0]	00h
	R/W	9BC2h	cgm_lut_PAR151[7:0]	00h
	R/W	9CC2h	cgm_lut_PAR152[7:0]	00h
	R/W	9DC2h	cgm_lut_PAR153[7:0]	00h
	R/W	9EC2h	cgm_lut_PAR154[7:0]	00h
	R/W	9FC2h	cgm_lut_PAR155[7:0]	00h
	R/W	A0C2h	cgm_lut_PAR156[7:0]	00h
	R/W	A2C2h	cgm_lut_PAR157[7:0]	00h
	R/W	A3C2h	cgm_lut_PAR158[7:0]	00h
	R/W	A4C2h	cgm_lut_PAR159[7:0]	00h
	R/W	A5C2h	cgm_lut_PAR160[7:0]	00h
	R/W	A6C2h	cgm_lut_PAR161[7:0]	00h
	R/W	A7C2h	cgm_lut_PAR162[7:0]	00h
	R/W	A9C2h	cgm_lut_PAR163[7:0]	00h
	R/W	AAC2h	cgm_lut_PAR164[7:0]	00h
	R/W	ABC2h	cgm_lut_PAR165[7:0]	00h
	R/W	ACC2h	cgm_lut_PAR166[7:0]	00h
	R/W	ADC2h	cgm_lut_PAR167[7:0]	00h
	R/W	AEC2h	cgm_lut_PAR168[7:0]	00h
	R/W	AFC2h	cgm_lut_PAR169[7:0]	00h
	R/W	B0C2h	cgm_lut_PAR170[7:0]	00h
	R/W	B1C2h	cgm_lut_PAR171[7:0]	00h
	R/W	B2C2h	cgm_lut_PAR172[7:0]	00h
	R/W	B3C2h	cgm_lut_PAR173[7:0]	00h
	R/W	B4C2h	cgm_lut_PAR174[7:0]	00h
	R/W	B5C2h	cgm_lut_PAR175[7:0]	00h
	R/W	B6C2h	cgm_lut_PAR176[7:0]	00h
	R/W	B7C2h	cgm_lut_PAR177[7:0]	00h
	R/W	B8C2h	cgm_lut_PAR178[7:0]	00h
	R/W	B9C2h	cgm_lut_PAR179[7:0]	00h
	R/W	BAC2h	cgm_lut_PAR180[7:0]	00h
	R/W	BBC2h	cgm_lut_PAR181[7:0]	00h
	R/W	BCC2h	cgm_lut_PAR182[7:0]	00h
	R/W	BDC2h	cgm_lut_PAR183[7:0]	00h
	R/W	BEC2h	cgm_lut_PAR184[7:0]	00h
	R/W	BFC2h	cgm_lut_PAR185[7:0]	00h
	R/W	C0C2h	cgm_lut_PAR186[7:0]	00h
	R/W	C1C2h	cgm_lut_PAR187[7:0]	00h
	R/W	C2C2h	cgm_lut_PAR188[7:0]	00h
	R/W	C3C2h	cgm_lut_PAR189[7:0]	00h
	R/W	C4C2h	cgm_lut_PAR190[7:0]	00h
	R/W	C5C2h	cgm_lut_PAR191[7:0]	00h
	R/W	C6C2h	cgm_lut_PAR192[7:0]	00h
	R/W	C7C2h	cgm_lut_PAR193[7:0]	00h
	R/W	C8C2h	cgm_lut_PAR194[7:0]	00h
	R/W	C9C2h	cgm_lut_PAR195[7:0]	00h
	R/W	CAC2h	cgm_lut_PAR196[7:0]	00h
	R/W	CBC2h	cgm_lut_PAR197[7:0]	00h
	R/W	CCC2h	cgm_lut_PAR198[7:0]	00h
	R/W	CDC2h	cgm_lut_PAR199[7:0]	00h
	R/W	CEC2h	cgm_lut_PAR200[7:0]	00h

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CGM LUT Setting Parameters	R/W	CFC2h	cgm_lut_PAR201[7:0]	00h
	R/W	D0C2h	cgm_lut_PAR202[7:0]	00h
	R/W	D1C2h	cgm_lut_PAR203[7:0]	00h
	R/W	D2C2h	cgm_lut_PAR204[7:0]	00h
	R/W	D3C2h	cgm_lut_PAR205[7:0]	00h
	R/W	D4C2h	cgm_lut_PAR206[7:0]	00h
	R/W	D5C2h	cgm_lut_PAR207[7:0]	00h
CMD Mode Switch	W	FEC2h	CMD_Page[7:0]	00h
RD CMD Status	R	FFC2h	CMD_Status[7:0]	00h

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(00C2h~D5C2h) CGM LUT Parameters

R/W	Addr	D7	D6	D5	D4	D3	D2	D1	D0	HEX
R/W	00C2h	cgm_lut_PAR1[7:0]								00h
R/W	01C2h	cgm_lut_PAR2[7:0]								00h
R/W	02C2h	cgm_lut_PAR3[7:0]								00h
R/W	03C2h	cgm_lut_PAR4[7:0]								00h
R/W	04C2h	cgm_lut_PAR5[7:0]								00h
R/W	05C2h	cgm_lut_PAR6[7:0]								00h
R/W	06C2h	cgm_lut_PAR7[7:0]								00h
R/W	07C2h	cgm_lut_PAR8[7:0]								00h
R/W	08C2h	cgm_lut_PAR9[7:0]								00h
R/W	09C2h	cgm_lut_PAR10[7:0]								00h
R/W	0AC2h	cgm_lut_PAR11[7:0]								00h
R/W	0BC2h	cgm_lut_PAR12[7:0]								00h
R/W	0CC2h	cgm_lut_PAR13[7:0]								00h
R/W	0DC2h	cgm_lut_PAR14[7:0]								00h
R/W	0EC2h	cgm_lut_PAR15[7:0]								00h
R/W	0FC2h	cgm_lut_PAR16[7:0]								00h
R/W	10C2h	cgm_lut_PAR17[7:0]								00h
R/W	11C2h	cgm_lut_PAR18[7:0]								00h
R/W	12C2h	cgm_lut_PAR19[7:0]								00h
R/W	13C2h	cgm_lut_PAR20[7:0]								00h
R/W	14C2h	cgm_lut_PAR21[7:0]								00h
R/W	15C2h	cgm_lut_PAR22[7:0]								00h
R/W	16C2h	cgm_lut_PAR23[7:0]								00h
R/W	17C2h	cgm_lut_PAR24[7:0]								00h
R/W	18C2h	cgm_lut_PAR25[7:0]								00h
R/W	19C2h	cgm_lut_PAR26[7:0]								00h
R/W	1AC2h	cgm_lut_PAR27[7:0]								00h
R/W	1BC2h	cgm_lut_PAR28[7:0]								00h
R/W	1CC2h	cgm_lut_PAR29[7:0]								00h

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R/W	1DC2h	cgm_lut_PAR30[7:0]	00h
R/W	1EC2h	cgm_lut_PAR31[7:0]	00h
R/W	1FC2h	cgm_lut_PAR32[7:0]	00h
R/W	20C2h	cgm_lut_PAR33[7:0]	00h
R/W	21C2h	cgm_lut_PAR34[7:0]	00h
R/W	22C2h	cgm_lut_PAR35[7:0]	00h
R/W	23C2h	cgm_lut_PAR36[7:0]	00h
R/W	24C2h	cgm_lut_PAR37[7:0]	00h
R/W	25C2h	cgm_lut_PAR38[7:0]	00h
R/W	26C2h	cgm_lut_PAR39[7:0]	00h
R/W	27C2h	cgm_lut_PAR40[7:0]	00h
R/W	28C2h	cgm_lut_PAR41[7:0]	00h
R/W	29C2h	cgm_lut_PAR42[7:0]	00h
R/W	2AC2h	cgm_lut_PAR43[7:0]	00h
R/W	2BC2h	cgm_lut_PAR44[7:0]	00h
R/W	2DC2h	cgm_lut_PAR45[7:0]	00h
R/W	2FC2h	cgm_lut_PAR46[7:0]	00h
R/W	30C2h	cgm_lut_PAR47[7:0]	00h
R/W	31C2h	cgm_lut_PAR48[7:0]	00h
R/W	32C2h	cgm_lut_PAR49[7:0]	00h
R/W	33C2h	cgm_lut_PAR50[7:0]	00h
R/W	34C2h	cgm_lut_PAR51[7:0]	00h
R/W	35C2h	cgm_lut_PAR52[7:0]	00h
R/W	36C2h	cgm_lut_PAR53[7:0]	00h
R/W	37C2h	cgm_lut_PAR54[7:0]	00h
R/W	38C2h	cgm_lut_PAR55[7:0]	00h
R/W	39C2h	cgm_lut_PAR56[7:0]	00h
R/W	3AC2h	cgm_lut_PAR57[7:0]	00h
R/W	3BC2h	cgm_lut_PAR58[7:0]	00h
R/W	3DC2h	cgm_lut_PAR59[7:0]	00h

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R/W	3FC2h	cgm_lut_PAR60[7:0]	00h
R/W	40C2h	cgm_lut_PAR61[7:0]	00h
R/W	41C2h	cgm_lut_PAR62[7:0]	00h
R/W	42C2h	cgm_lut_PAR63[7:0]	00h
R/W	43C2h	cgm_lut_PAR64[7:0]	00h
R/W	44C2h	cgm_lut_PAR65[7:0]	00h
R/W	45C2h	cgm_lut_PAR66[7:0]	00h
R/W	46C2h	cgm_lut_PAR67[7:0]	00h
R/W	47C2h	cgm_lut_PAR68[7:0]	00h
R/W	48C2h	cgm_lut_PAR69[7:0]	00h
R/W	49C2h	cgm_lut_PAR70[7:0]	00h
R/W	4AC2h	cgm_lut_PAR71[7:0]	00h
R/W	4BC2h	cgm_lut_PAR72[7:0]	00h
R/W	4CC2h	cgm_lut_PAR73[7:0]	00h
R/W	4DC2h	cgm_lut_PAR74[7:0]	00h
R/W	4EC2h	cgm_lut_PAR75[7:0]	00h
R/W	4FC2h	cgm_lut_PAR76[7:0]	00h
R/W	50C2h	cgm_lut_PAR77[7:0]	00h
R/W	52C2h	cgm_lut_PAR78[7:0]	00h
R/W	53C2h	cgm_lut_PAR79[7:0]	00h
R/W	54C2h	cgm_lut_PAR80[7:0]	00h
R/W	55C2h	cgm_lut_PAR81[7:0]	00h
R/W	56C2h	cgm_lut_PAR82[7:0]	00h
R/W	57C2h	cgm_lut_PAR83[7:0]	00h
R/W	58C2h	cgm_lut_PAR84[7:0]	00h
R/W	59C2h	cgm_lut_PAR85[7:0]	00h
R/W	5AC2h	cgm_lut_PAR86[7:0]	00h
R/W	5BC2h	cgm_lut_PAR87[7:0]	00h
R/W	5CC2h	cgm_lut_PAR88[7:0]	00h
R/W	5DC2h	cgm_lut_PAR89[7:0]	00h

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R/W	5EC2h	cgm_lut_PAR90[7:0]	00h
R/W	5FC2h	cgm_lut_PAR91[7:0]	00h
R/W	60C2h	cgm_lut_PAR92[7:0]	00h
R/W	61C2h	cgm_lut_PAR93[7:0]	00h
R/W	62C2h	cgm_lut_PAR94[7:0]	00h
R/W	63C2h	cgm_lut_PAR95[7:0]	00h
R/W	64C2h	cgm_lut_PAR96[7:0]	00h
R/W	65C2h	cgm_lut_PAR97[7:0]	00h
R/W	66C2h	cgm_lut_PAR98[7:0]	00h
R/W	67C2h	cgm_lut_PAR99[7:0]	00h
R/W	68C2h	cgm_lut_PAR100[7:0]	00h
R/W	69C2h	cgm_lut_PAR101[7:0]	00h
R/W	6AC2h	cgm_lut_PAR102[7:0]	00h
R/W	6BC2h	cgm_lut_PAR103[7:0]	00h
R/W	6CC2h	cgm_lut_PAR104[7:0]	00h
R/W	6DC2h	cgm_lut_PAR105[7:0]	00h
R/W	6EC2h	cgm_lut_PAR106[7:0]	00h
R/W	6FC2h	cgm_lut_PAR107[7:0]	00h
R/W	70C2h	cgm_lut_PAR108[7:0]	00h
R/W	71C2h	cgm_lut_PAR109[7:0]	00h
R/W	72C2h	cgm_lut_PAR110[7:0]	00h
R/W	73C2h	cgm_lut_PAR111[7:0]	00h
R/W	74C2h	cgm_lut_PAR112[7:0]	00h
R/W	75C2h	cgm_lut_PAR113[7:0]	00h
R/W	76C2h	cgm_lut_PAR114[7:0]	00h
R/W	77C2h	cgm_lut_PAR115[7:0]	00h
R/W	78C2h	cgm_lut_PAR116[7:0]	00h
R/W	79C2h	cgm_lut_PAR117[7:0]	00h
R/W	7AC2h	cgm_lut_PAR118[7:0]	00h
R/W	7BC2h	cgm_lut_PAR119[7:0]	00h

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R/W	7CC2h	cgm_lut_PAR120[7:0]	00h
R/W	7DC2h	cgm_lut_PAR121[7:0]	00h
R/W	7EC2h	cgm_lut_PAR122[7:0]	00h
R/W	7FC2h	cgm_lut_PAR123[7:0]	00h
R/W	80C2h	cgm_lut_PAR124[7:0]	00h
R/W	81C2h	cgm_lut_PAR125[7:0]	00h
R/W	82C2h	cgm_lut_PAR126[7:0]	00h
R/W	83C2h	cgm_lut_PAR127[7:0]	00h
R/W	84C2h	cgm_lut_PAR128[7:0]	00h
R/W	85C2h	cgm_lut_PAR129[7:0]	00h
R/W	86C2h	cgm_lut_PAR130[7:0]	00h
R/W	87C2h	cgm_lut_PAR131[7:0]	00h
R/W	88C2h	cgm_lut_PAR132[7:0]	00h
R/W	89C2h	cgm_lut_PAR133[7:0]	00h
R/W	8AC2h	cgm_lut_PAR134[7:0]	00h
R/W	8BC2h	cgm_lut_PAR135[7:0]	00h
R/W	8CC2h	cgm_lut_PAR136[7:0]	00h
R/W	8DC2h	cgm_lut_PAR137[7:0]	00h
R/W	8EC2h	cgm_lut_PAR138[7:0]	00h
R/W	8FC2h	cgm_lut_PAR139[7:0]	00h
R/W	90C2h	cgm_lut_PAR140[7:0]	00h
R/W	91C2h	cgm_lut_PAR141[7:0]	00h
R/W	92C2h	cgm_lut_PAR142[7:0]	00h
R/W	93C2h	cgm_lut_PAR143[7:0]	00h
R/W	94C2h	cgm_lut_PAR144[7:0]	00h
R/W	95C2h	cgm_lut_PAR145[7:0]	00h
R/W	96C2h	cgm_lut_PAR146[7:0]	00h
R/W	97C2h	cgm_lut_PAR147[7:0]	00h
R/W	98C2h	cgm_lut_PAR148[7:0]	00h
R/W	99C2h	cgm_lut_PAR149[7:0]	00h

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R/W	9AC2h	cgm_lut_PAR150[7:0]	00h
R/W	9BC2h	cgm_lut_PAR151[7:0]	00h
R/W	9CC2h	cgm_lut_PAR152[7:0]	00h
R/W	9DC2h	cgm_lut_PAR153[7:0]	00h
R/W	9EC2h	cgm_lut_PAR154[7:0]	00h
R/W	9FC2h	cgm_lut_PAR155[7:0]	00h
R/W	A0C2h	cgm_lut_PAR156[7:0]	00h
R/W	A2C2h	cgm_lut_PAR157[7:0]	00h
R/W	A3C2h	cgm_lut_PAR158[7:0]	00h
R/W	A4C2h	cgm_lut_PAR159[7:0]	00h
R/W	A5C2h	cgm_lut_PAR160[7:0]	00h
R/W	A6C2h	cgm_lut_PAR161[7:0]	00h
R/W	A7C2h	cgm_lut_PAR162[7:0]	00h
R/W	A9C2h	cgm_lut_PAR163[7:0]	00h
R/W	AAC2h	cgm_lut_PAR164[7:0]	00h
R/W	ABC2h	cgm_lut_PAR165[7:0]	00h
R/W	ACC2h	cgm_lut_PAR166[7:0]	00h
R/W	ADC2h	cgm_lut_PAR167[7:0]	00h
R/W	AEC2h	cgm_lut_PAR168[7:0]	00h
R/W	AFC2h	cgm_lut_PAR169[7:0]	00h
R/W	B0C2h	cgm_lut_PAR170[7:0]	00h
R/W	B1C2h	cgm_lut_PAR171[7:0]	00h
R/W	B2C2h	cgm_lut_PAR172[7:0]	00h
R/W	B3C2h	cgm_lut_PAR173[7:0]	00h
R/W	B4C2h	cgm_lut_PAR174[7:0]	00h
R/W	B5C2h	cgm_lut_PAR175[7:0]	00h
R/W	B6C2h	cgm_lut_PAR176[7:0]	00h
R/W	B7C2h	cgm_lut_PAR177[7:0]	00h
R/W	B8C2h	cgm_lut_PAR178[7:0]	00h
R/W	B9C2h	cgm_lut_PAR179[7:0]	00h

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R/W	BAC2h	cgm_lut_PAR180[7:0]	00h
R/W	BBC2h	cgm_lut_PAR181[7:0]	00h
R/W	BCC2h	cgm_lut_PAR182[7:0]	00h
R/W	BDC2h	cgm_lut_PAR183[7:0]	00h
R/W	BEC2h	cgm_lut_PAR184[7:0]	00h
R/W	BFC2h	cgm_lut_PAR185[7:0]	00h
R/W	C0C2h	cgm_lut_PAR186[7:0]	00h
R/W	C1C2h	cgm_lut_PAR187[7:0]	00h
R/W	C2C2h	cgm_lut_PAR188[7:0]	00h
R/W	C3C2h	cgm_lut_PAR189[7:0]	00h
R/W	C4C2h	cgm_lut_PAR190[7:0]	00h
R/W	C5C2h	cgm_lut_PAR191[7:0]	00h
R/W	C6C2h	cgm_lut_PAR192[7:0]	00h
R/W	C7C2h	cgm_lut_PAR193[7:0]	00h
R/W	C8C2h	cgm_lut_PAR194[7:0]	00h
R/W	C9C2h	cgm_lut_PAR195[7:0]	00h
R/W	CAC2h	cgm_lut_PAR196[7:0]	00h
R/W	CBC2h	cgm_lut_PAR197[7:0]	00h
R/W	CCC2h	cgm_lut_PAR198[7:0]	00h
R/W	CDC2h	cgm_lut_PAR199[7:0]	00h
R/W	CEC2h	cgm_lut_PAR200[7:0]	00h
R/W	CFC2h	cgm_lut_PAR201[7:0]	00h
R/W	D0C2h	cgm_lut_PAR202[7:0]	00h
R/W	D1C2h	cgm_lut_PAR203[7:0]	00h
R/W	D2C2h	cgm_lut_PAR204[7:0]	00h
R/W	D3C2h	cgm_lut_PAR205[7:0]	00h
R/W	D4C2h	cgm_lut_PAR206[7:0]	00h
R/W	D5C2h	cgm_lut_PAR207[7:0]	00h

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Description	These commands (cgm_lut_PAR1~ cgm_lut_PAR207) are used to set the CGM lookup table parameters.
Restriction	

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(FEC2h): CMD Mode Switch

R/W	Addr	D7	D6	D5	D4	D3	D2	D1	D0	HEX
W	FEC2h	CMD_Page[7:0]								00h

Description

This command is used to switch the Manufacture Command Pages and User Commands sets.

CMD_Page[7:0]	Description
00h (default)	User Command Set (UCS = CMD1)
10h	Manufacture Command Set Page Panel ID
12h	Manufacture Command Set Page SID
20h	Manufacture Command Set Page Panel
40h	Manufacture Command Set Page ABH Mode
82h	Manufacture Command Set Page Power
92h	Manufacture Command Set Page SD timing
50h	Manufacture Command Set Page Gamma1
60h	Manufacture Command Set Page Gamma2
30h	Manufacture Command Set Page Gamma3
52h	Manufacture Command Set Page Gamma4
70h	Manufacture Command Set Page GOA Timing 1
F0h	Manufacture Command Set Page GOA Timing 2
42h	Manufacture Command Set Page DBV
22h	Manufacture Command Set Page SES
80h	Manufacture Command Set Page APRC
90h	Manufacture Command Set Page ACL
62h	Manufacture Command Set Page CGM
C2h	Manufacture Command Set Page CGM LUT

Restriction

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(FFC2h): Read CMD Status

R/W	Addr	D7	D6	D5	D4	D3	D2	D1	D0	HEX
R	FFC2h	CMD_Status[7:0]								00h

Description	This command is used to read the status of Manufacture Command Pages. Please refer to FE00h
Restriction	-

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