Design Tools for RF Circuits with Microvias

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Abstract *– Advances in packaging technologies have enabled dramatic size reductions in portable and wireless products. While the package size for integrated circuits is decreasing, pin count is increasing. The resulting increase in pin and interconnect density, however, exceeds the limits of traditional printed circuit board (PCB) manufacturing technologies. The emergence of microvia PCB technology provides a bridge between high-density packaging and traditional PCB technologies. The more demanding requirements of microvia technology, however, introduce new challenges for many of today's PCB design tools. For portable and wireless product designers, these design challenges are compounded by the requirement to combine digital, analog, and RF (radio frequency) circuitry on a heterogeneous substrate. Without the right set of design tools, design iterations resulting from functional and manufacturing errors are likely to occur. This paper discusses the design and manufacturing issues that drive design tool requirements, and some of the solutions available today.*

Keywords: EDA, Microvia, RF Design, Wireless Design

Introduction

Today's wireless products require a mix of analog, digital, and RF circuitry on a single substrate. At the same time, size reduction is a primary goal particularly for mobile and handheld products. These conflicting requirements add complexity to the design task and demand new manufacturing technologies. For RF engineers and printed circuit board (PCB) designers, having access to the right set of design tools is critical to your success. Package and interconnect technology currently being used to achieve higher density for digital circuitry, must be factored into the design of the RF section when they share the same substrate. To take advantage of these new technologies, and still meet schedule constraints, RF designers must rely more and more on electronic design automation (EDA) tools. Microvia is one such technology that permits designers to realize significant increases in density. This paper examines the impact that this technology has on current EDA design tools and discusses the approach one EDA vendor has taken to create tools that allow RF designers to leverage this technology in a traditional design flow.

Microvia

Microvia technology allows PCB manufacturers to achieve much smaller dimensions with practical and cost effective modifications to their existing PCB manufacturing process. It has largely been driven by high density ball grid array (BGA) packaging that is now widely available in volume production. The course dimensions (Table 1) of typical PCB technology makes it difficult to route to BGA package pins. The

Table 1. Comparison of Typical Dimensions

	PCB	Microvia
Line width	.010 in / 250 µm	.004 in. / 100 µm
Space	.010 in / 250 µm	.004 in. / 100 µm
Via hole diameter	.020 in / 500 µm	.004 in. / 100 µm
Via pad diameter	.030 in / 750 µm	.012 in. / 300 µm

Table 2. Package Pin Count Comparison

	PGA	QFP	TSOP	BGA
Pin pitch	.100 in / 2.54 mm	.025 in / .65 mm	.012 in / .3 mm	.050 in / 1.27 mm
Pin count (32mm x 32mm)	100	184	392	600

introduction of microvia technology, however, does impact the materials and dimensions of the PCB and must be considered by the RF designer. Microvia layers are commonly applied on the top and/or bottom side of a traditional PCB core. Dielectric and conductive layers are sequentially added and patterned on top of a PCB core. Design tools must allow different rules for vias and routing that apply to the microvia layers and core PCB layers. The tools must capture the physical and electrical characteristics for simulation.

High Density Packages

Advances in integrated circuit package technology have enabled dramatic reductions in package size for high pin count packages. BGA packaging technology significantly reduces size, pin density and interconnect density. The fine pitch of BGA pins, however, complicates the task of routing interconnect. Table 2 shows the dramatic increase in pin density that BGA packages yield. While high pin counts can be realized in a smaller space, routing becomes more congested making it difficult to connect to all available pins. BGA pin pitch is smaller than that of through-hole packages and contains multiple rows of pins, which aren't available with QFPs. The challenge is for traces to escape or breakout from the inner rows of the array.

Re-distribution layer

Microvia technology provides one or more redistribution layers between the fine pitch high-density packages and the more coarse features of the traditional PCB. An additional advantage that microvia brings is the ability to place vias directly under the surface mount pins. Since most microvias are filled, solder wicking is not an issue. Traditional plated through-hole (PTH) vias require traces to be routed from the pin to the via. Eliminating the need to route a trace from the pin to the via preserves routing resources.

Microvia Design Requirements

In addition to smaller feature sizes, different via rules apply for microvia technology. The vias formed on the microvia layers are blind and/or buried vias. Depending on the manufacturer, there are constraints and extensions to via usage relative to core PCBs. The design tool must be able to control via coincidence or stacking. Stacking (figure 2) is the

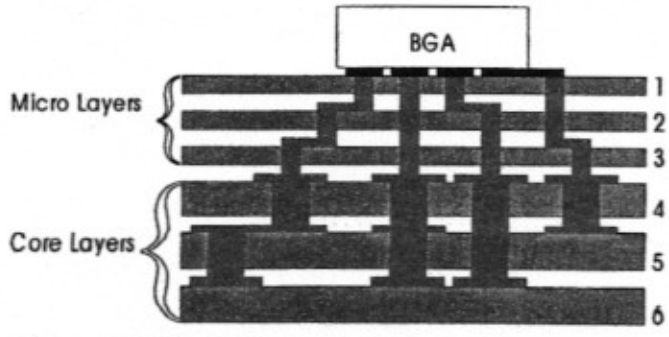

Figure 1. BGA & Microvia Cross Section

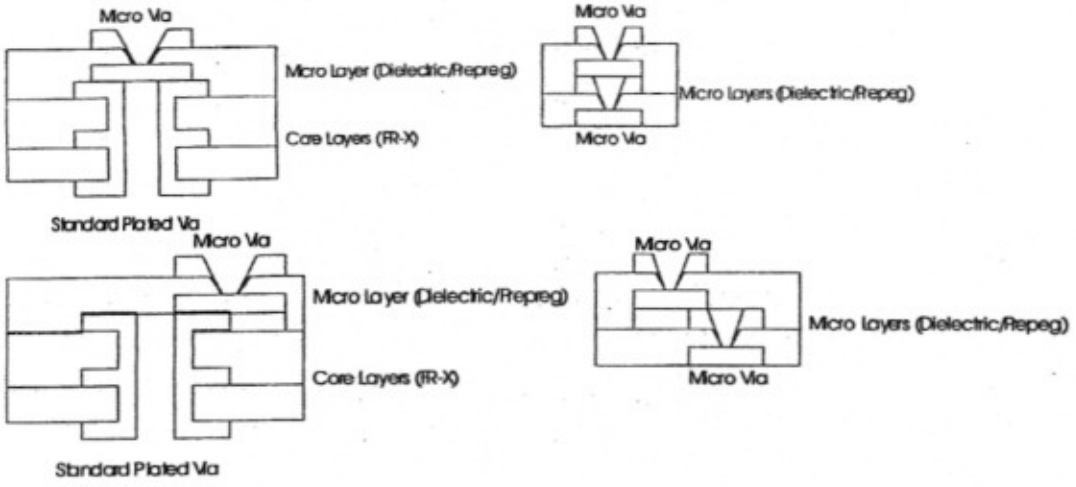

Figure 2. Stacked Microvias

ability to have two separate vias overlap. Vias may have overlapping centers, or they may be offset but share a pad on a given layer. Overlap may occur between two microvias or between a microvia and a core via. Core PTH vias are usually hollow which would inhibit the ability to manufacture a microvia coincident with a core via. Most microvia manufacturers, however, fill or cap the core vias permitting microvias to stack on top of core vias.

Mixed Technology Design Tools

Many RF designers still employ old design methodologies with design tools that don't easily fit into standard PCB design flows. Contrary to practices in the digital world, many RF designers still use mechanical drafting tools to accomplish the physical layout task. These drafting tools have no notion of the electrical characteristics of the drawn circuit. Regarding the electrical design process, many designers utilize a variety of specialized and often isolated tools for tasks ranging from linear circuit analysis, to harmonic balance simulators, to 3D electromagnetic (EM) simulation for parasitic extraction, S-parameter modeling, and analysis of coupling effects.

Having conceived the circuit using these tools, the designer must then merge the RF block(s) into his PCB containing digital and analog circuitry. This is sometimes achieved by re-entering data that was previously entered in a drafting tool. This is often a process in which the RF designer works closely (over the shoulder) with the PCB layout designer. The downside risks are: loss of data, increased probability of human-induced errors, and wasted time.

Layout-driven

It is common for RF designers to skip schematic entry and create sub-circuits strictly in layout. Many PCB design tools enforce a "correct by construction" design methodology in which changing connectivity during the layout process is not allowed. This approach is required in an enterprise design environment where team design processes are employed. For RF designers, the layout process is often the most critical step in the design process. The designer needs to be able to add, delete, and modify circuit elements and connectivity, then simulate to verify circuit behavior.

With the mix of circuitry on the same substrate, and confined to smaller area with each new generation, the RF designer must be able to layout the RF circuit in the context of the rest of circuitry and to take into account mechanical features in the PCB such as mounting holes, heat spreaders, cutouts, etc.

Parameter-Driven

Since distributed elements are etched on the conductive PCB layers, many layout tools will view them as continuous metal shorted together, or as opens in the case of planar capacitors, couplers, and similar elements. These elements tend to have complex shapes that can be tedious and time-consuming to create and edit. EDA tools need to recognize these RF elements and allow connecting components to abut. Since the dimensions of RF elements are critical, geometric parameters should be taken into account. By generating parameter-driven elements on-the-fly, the designer can quickly and accurately create complex RF elements by simply entering a set of parameters into a form. (Figure 3)

Predictive Analysis and Post-Layout Verification

With increased circuit density, it is essential to isolate adjacent components to avoid unwanted coupling effects. Coupling effects can be modeled and simulated several ways to verify compliance with specifications. The layout tool should have tight links to time and frequency domain simulation tools. In the ideal case, the design tool would bundle all layout and simulation capability into a single tool for digital, analog, and RF design. In practice, there is no single tool that is optimized for every type of design and every type of simulation. In the early stages of the design process, predictive tools are used to determine expected behavior. After layout is performed, verification is necessary to assess the affects of parasitics and unintended coupling, or the inevitable changes made during the layout process. The breadth of tools employed for predictive analysis and post-layout verification make interfaces to other tools a critical requirement. The intermediate file format (IFF) proposed by Agilent EEsof provides a means to transfer schematic and layout data between design tools.

Manufacturing Output

Finally, the resultant design must be manufactured. While the RF circuitry does not add any unique requirements to the manufacturing process, microvia technology does. Depending on the technology, vias may be formed by photo-imaging, laser drilling or

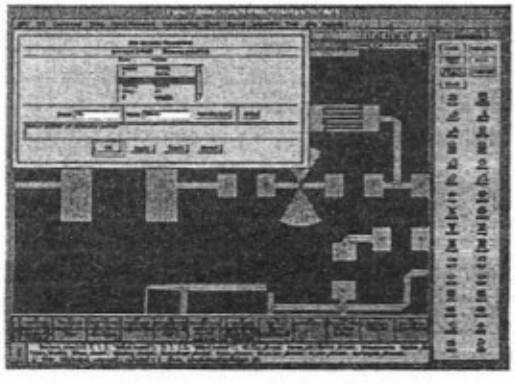

Figure 3. Parameter-driven RF distributed elements

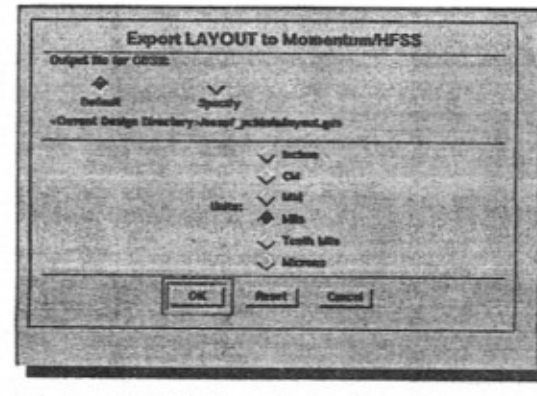

Figure 4. EM Simulation Interface

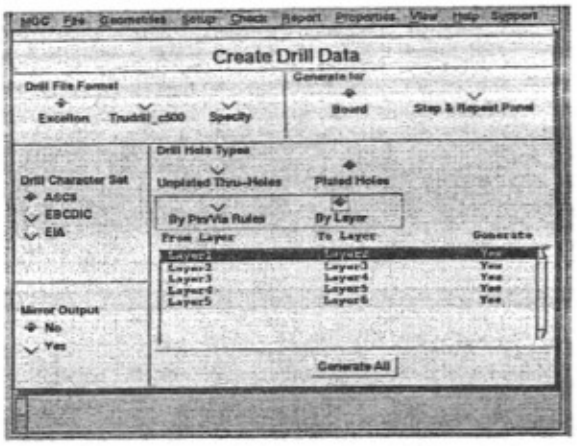

Figure 5. Output Microvia Drill Data

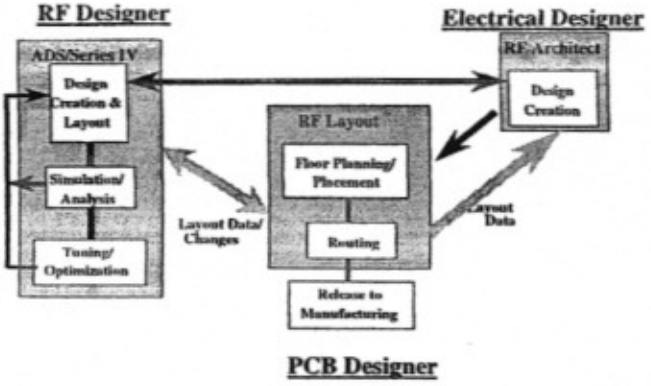

Figure 6. Complete Design Flow

plasma etching. Photo-imaging requires photomask artwork to be generated. Since traditional PCB technology assumes via holes will be formed with mechanical drills, photomasks for via formation is a new requirement. If traditional drill output is used to drive laser drill equipment, drill output files need to be properly organized by layer pair to drive the laser.

Conclusion

Microvia technology enables higher density than conventional PCBs for mixed RF designs. With RF Architect ™, RF Layout, Advanced Design System ™, and a standard design flow, RF designers can leverage that technology into their products without sacrificing development time or product performance.

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