Embedded Passive Components – A Challenge for RF Design Tools

John Cofield
Mentor Graphics Corporation
1001 Ridder Park Drive
San Jose, CA 95118
Phone: 408-451-5741, FAX: 408-451-5538
email: john_cofield@mentor.com

Abstract

The rapid growth in demand for wireless products is driving the need for design tools that allow designers to meet evermore challenging design constraints. Decreasing product life cycles and shrinking product size impose new challenges to RF product designers. Advances in packaging and substrate technologies that employ embedded passive components allow RF designers to achieve size targets and performance goals not previously achievable.

Key words: EDA, Embedded Passive, Integral Passive, PCB, RF Design, Wireless Design

Introduction

Wireless products are proliferating rapidly. Cell phones, wireless internet appliances, and personal digital assistants (PDA) are driving the rate at which new products are designed. By some estimates, wireless internet access is expected to grow to 30 million subscribers by 2003. Motorola estimates 100 million handsets that will ship in 2000 will feature web browsers. On the horizon are a new crop of Bluetooth enabled products that promise to bring wireless technology to a wide range of low cost consumer products.

For the coming generation of wireless products, most require a mix of analog, digital, and RF technologies on a single substrate. At the same time, consumers want smaller, "easier to carry" products. These trends add complexity to the design task. To compound the problem, many RF designers still employ disjointed design methodologies in which the RF circuits are designed using mechanical drafting tools or tools that are not well integrated, causing manual data re-entry, data loss, and iterations due to human-induced errors.

To meet these challenges, RF designers must rely more and more on electronic design automation (EDA) tools. New generations of "RF smart" tools are required to address the rapidly evolving requirements of today's designers. Embedded passive component technology is a new technology that promises size and performance benefits for wireless products. Embedded passives pose new challenges for EDA tools. This paper examines the impact that this technology has on current EDA design tools and highlights some of the challenges that EDA tool vendors must overcome.

While design requirements span several disciplines including electrical, physical layout, thermal, mechanical, and manufacturing, this paper will focus on the physical and electrical design process.

Embedded Passive Technology

Size is a critical factor for most handheld wireless devices. RF printed circuit boards (PCB) tend to make liberal use of discrete resistors, capacitors, and inductors. These components can account for as much as 90% of the components on the board and consume more than 90% of the area [1]. Some of these components are being integrated into the active semiconductor integrated circuits (IC) placed on the board, however, many will remain on the PCB. Integrating these components into the PCB and embedding them on inner layers yields significant area and volume savings. In addition to the space savings, the assembly process is simplified and the number of solder connections is reduced.

Table 1 Embedded passive overlap rules

Valid Overlap	Invalid Overlap
Top side discrete to top side embedded	Top side to top side discrete
Bottom side discrete to bottom side embedded	Bottom side to bottom side discrete
Top side discrete to top side embedded, unless copper interference occurs	Top side embedded to top side embedded
Bottom side discrete to bottom side embedded, unless copper interference occurs.	Bottom side embedded to bottom side embedded
Top or bottom side discrete to inner layer embedded.	Inner layer embedded on the same signal layers if copper interference occurs
Inner layer embedded on different signal layers	

When placed on inner layers, the component outlines can overlap the outlines discrete components or other distributed elements on the outer layers. From an electronic design automation (EDA) perspective, these overlapping components can be problematic for many PCB design tools in the physical layout and electrical domains.

With respect to traditional PCB layout design tools, overlapping components violate manufacturing rules. Most PCB layout tools assume that all components are added during the assembly process and that they are placed only on the top or bottom side of the PCB. In that case, the only component data required to create artwork is 1) pad information which is output for each corresponding conductive layers, and 2) silkscreen information to facilitate assembly. Board Station™, a PCB layout product from Mentor Graphics uses a special graphical attribute called a placement outline to determine component to component clearance. For embedded passives, however, the normal overlap rules do not apply. It is necessary to develop a set of exceptions to these rules (Table 1).

Embedded passives have characteristics similar to distributed elements such as transmission lines, couplers, stubs, etc. that are commonly used in RF designs. I'll refer to both classes as embedded RF elements. These elements may occupy one or more layers and may overlap RF elements or discrete components on other layers, thus the same set of rules apply. At the same time, components that occupy the same layers must not be allowed to overlap when clearance violations or shorts are possible. Note that elements on different layers may overlap from a top view, it is clear from the cross-section view in figure 1 that there is no physical interference.

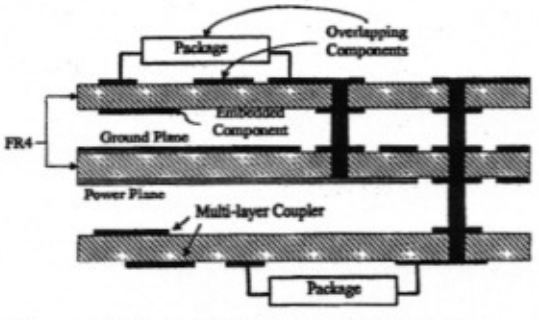

Figure 1. Embedded and multi-layer components

There are 2 requirements to implement embedded RF elements.

1. Pins must be defined on inner layers
2. Component outlines on inner layer (embedded) components, must be allowed to overlap without causing placement errors.

The first requirement can be satisfied with blind pins. The second requirement can be met by with modified placement design rules checking (DRC). While most EDA tools allow users to override or ignore phantom errors (i.e. intentional errors), it is possible to miss unintentional errors if the reported phantom errors are too numerous.

Precautions, such as 1) adequate spacing, 2) insertion of reference planes, and 3) shielding, must be taken to isolate adjacent components to avoid unwanted coupling effects. Coupling effects can be modeled and simulated several ways to verify compliance with specifications [2,3]. Ideally, DRC must focus on catching unintended clearance and overlap violations between conductors to avoid shorts and insure that parasitic coupling is kept below a minimum threshold. Design tools should warn the designer

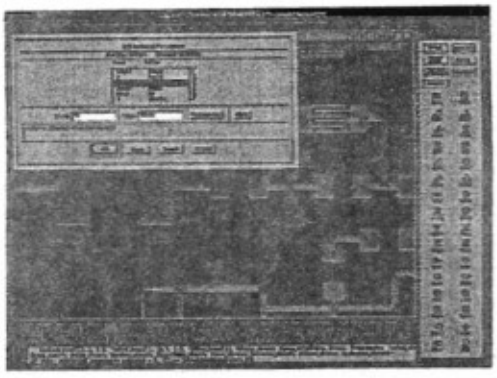

Figure 2 Parameter-driven RF distributed elements

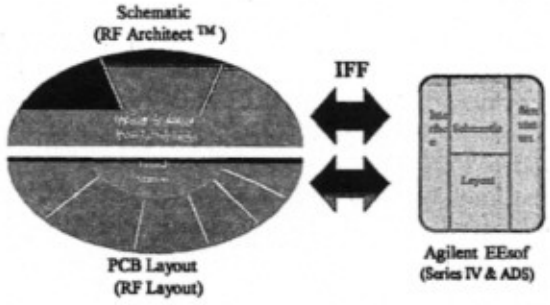

Figure 3 Schematic & layout interface

when physical and/or electrical rules are violated as the designer performs layout. In practice, however, this is an iterative process.

Change Design Methodology

Many RF designers still employ old design methodologies. Contrary to trends in the digital world, many RF designers still use mechanical drafting tools to accomplish the physical layout task. These drafting tools have no notion of the electrical characteristics of the drawn circuit. Regarding the electrical design process, many designers utilize a variety of specialized and often isolated tools for tasks ranging from linear circuit analysis, to harmonic balance simulators, to 3D electromagnetic (EM) simulation for parasitic extraction, S-parameter modeling, and analysis of coupling effects.

Having conceived the circuit using these tools, the designer then must merge the RF block(s) into his PCB containing digital and analog circuitry. This is sometimes achieved by re-entering data that was previously entered in a drafting tool. This is often a process in which the RF designer works closely (over the shoulder) with the PCB layout designer. The downside risks are: loss of data, increased probability of human-induced errors, and wasted time.

Since distributed elements are etched on the conductive PCB layers, many layout tools will view them as continuous metal shorted together, or as opens in the case of planar capacitors, couplers, and similar elements. These elements tend to have complex shapes that can be tedious and time-consuming to create and edit.

Smarter EDA Tools

The "over-the-wall" design methodology for mixed signal design is sub-optimal. When a RF block is designed outside of the mixed signal board context, the negative consequences can include:

1. Mechanical features such as mounting holes, connectors, and cutouts are not taken into account
2. Form factor of the RF block does not fit well within the space that was reserved
3. Complex shapes may not be drawn accurately
4. Schematic does not match layout
5. Designer may not be able to simulate layout

EDA tools need to recognize these RF elements and allow connecting components to abut. Since the dimensions of RF elements are critical, geometric parameters should be taken into account. By generating parameter-driven elements on-the-fly, the designer can quickly and accurately create complex RF elements by simply entering a set of parameters into a form. (See figure 2)

Layout-driven

It is common for RF designers to skip schematic entry and create sub-circuits strictly in layout. Many PCB design tools enforce a "correct by construction" design methodology in which changing connectivity during the layout process is not allowed. This approach is required in an enterprise design environment where team design processes are employed. For RF designers, the layout process is often the most critical step in the design process. The designer needs to be able to add, delete, and modify circuit elements and connectivity, then simulate to verify circuit behavior.

Predictive Analysis and Post-Layout Verification

The layout tool should have tight links to time and frequency domain simulation tools. In the ideal case, the design tool would bundle all layout and simulation capability into a single tool for digital, analog, and RF design. In practice, there is no single tool that is optimized for every type of design and every type of simulation. In the early stages of the design process, predictive tools are used to determine expected behavior. After layout is performed, verification is necessary to assess the affects of parasitics and unintended coupling, or the inevitable changes made during the layout process. The breadth of tools employed for predictive analysis and post-layout verification make interfaces to other tools a critical requirement. The intermediate file format (IFF) proposed by Agilent EEsof provides a means to transfer schematic and layout data between design tools. (See figure 3)

Manufacturability

Embedded passives and distributed elements must be treated as special case components in the traditional PCB manufacturing flow. Since these components are fabricated into the PCB, bill of materials (BOM) data and pick and place data do not apply. It may, however, be necessary to create additional artwork layers for embedded resistors or capacitors.

Conclusion

New technologies are addressing the need for smaller, cheaper, more feature-rich products. EDA tools are addressing some the needs in the areas of improved layout capability, predictive analysis, and interfaces. Still to be addressed are issues such as coupling effects and tighter tool integration.

RF designers also play a role in the evolution of these EDA tools. Designers need to embrace new methodologies and integrate their design process into standard PCB design flows.

References

1. R.C. Frye, P. Smith, Y. Low, "Inductive Crosstalk Between Integrated Passive Components in RF-Wireless Modules", Proceedings for the International Conference on Multichip Modules and High Density Packaging, April 15-17, 1998
2. Y. Seo, A. Triparthi, R. Lutz, R. Goyal, V. Triparthi, "Modeling Interconnect Coupling between Analog, Digital, and RF Layout Components for MCM Design", Proceedings for the International Conference on Multichip Modules and High Density Packaging, April 17-19, 1996
3. J. Parkerson, L. Shaper, T. Lenihan, "Design Considerations for Using Integrated Passive Components", Proceedings for the International Conference on Multichip Modules and High Density Packaging, April 2-4, 1997
4. R. Brown, "Embedded Passive Functions for RF and Mixed-Signal Circuits", Proceedings for the International Conference on Multichip Modules and High Density Packaging, April 2-4, 1997

Table of Contents

Assembled and Edited
by the
Technical Program Committee *and the* IMAPS Staff

Proceedings
2000 International Conference on High-Density Interconnect and Systems Packaging

IMAPS - International Microelectronics And Packaging Society
1850 Centennial Park Drive
Suite 105
Reston, VA 20191-1517 U.S.A.
Tel: 888-GO-IMAPS or 703-758-1060
Fax: 703-758-1066
E-mail: IMAPS@imaps.org
Home Page: http://www.imaps.org

ISBN 0-930815-60-2

The International Microelectronics And Packaging Society (IMAPS) is a nonprofit professional society dedicated to the advancement of nonmonolithic microelectronics. The Society's primary objective is to provide a forum for the dissemination of knowledge within the field of microelectronics and to serve as a common denominator for the diverse scientific and engineering disciplines upon which the microelectronics industry is based.

IMAPS encourages the exchange of information among the complementary technologies of materials (*ceramics, glasses, semiconductors, polymers, and metals*), thick and thin films, devices (*passive, semiconductor, sonic, microvacuum, optical, and optoelectronic*), sensors, monolithic integrated circuits, and multichip modules. These technologies require the symbiosis of metallurgy, packaging design (*mechanical, electric, and thermal*), processing techniques, computer-aided methods, equipment and instrumentation, fabrication, and application engineering.