USING MCM DESIGN KITS

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INTRODUCTION

A multichip module (MCM) design kit provides all the CAE tools necessary for a user to specify and verify the physical implementation of a MCM, based on the target manufacturing process. The tools necessary to implement a MCM include CAE software, technology libraries, vendor-specific software, and documentation. Designers must have the capability to design in all current MCM technologies including laminated, co-fired ceramic, and deposited substrate media.

Since each MCM vendor has a unique manufacturing processes, they must tailor their design tools to fit their process. Without a design kit, a designer wanting to use a particular vendor would need to know technical details about the materials that are used to manufacture the MCMs, the manufacturing equipment that the vendor might use, interfaces for exchanging customer data, and interfaces to vendor software that performs vendor-specific functions.

The design kit gives the customer that ability to implement his design to in accordance with the vendor's manufacturing requirements while allowing the systems designer to focus on the design without getting bogged down with manufacturing and interface details. This paper will discuss the elements of a MCM design kit and how it is used in the MCM design process. Some specific references will be made by way of example, to a design kit jointly developed by Mentor Graphics and MicroModule Systems (MMS).

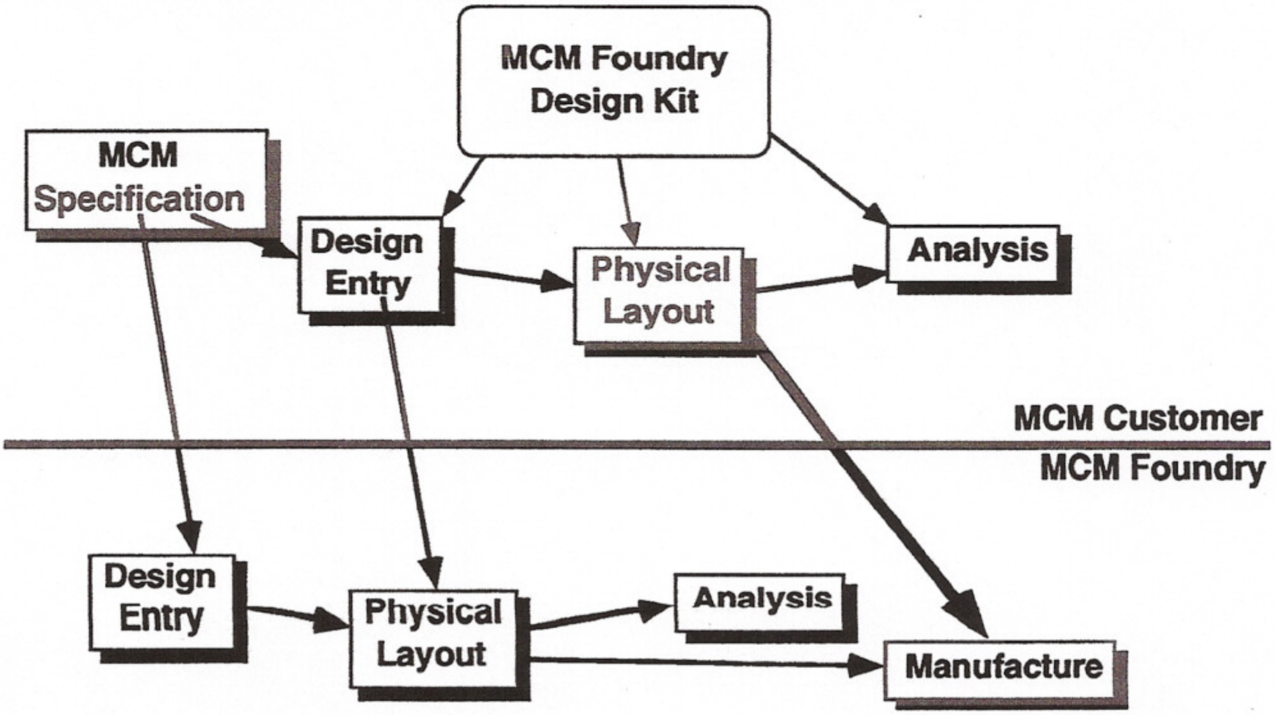


Figure 1.

ADVANTAGES TO MCM TECHNOLOGY

The reasons for designing MCMs are typically to achieve some combination of higher performance and higher density. While there is dispute as to whether an MCM is really a large ASIC, a hybrid circuit, or a small printed circuit board, we will refer to an MCM as a collection of unpackaged components, mounted on a substrate, and connected via substrate interconnect to form a complex circuit. The components are typically digital integrated circuits of LSI complexity or higher. In most cases, the substrate and components are packaged or encapsulated for subsequent mounting on a PC board.

By removing the component packages and packing components closer together, signal delays are reduced as a result of shorter interconnect distances. Lower parasitic loading results from the elimination of the packages and shorter interconnect. Signal propagation speed is also improved by the use of dielectric materials with a low dielectric constant. Some MCM technologies, provide significant reductions in noise and crosstalk as well, due to tighter impedance control.

STANDARDIZED DESIGN ENVIRONMENT AND DATA EXCHANGE

For systems designers to take advantage of this technology, however, CAD tools must allow designers to design MCMs in the same way that they currently design printed circuit boards. In much that same way that ASIC design kits were used when ASIC technology was emerging, MCM design kits isolate the designer from details of the manufacturing process, so that the designer does not have to become expert in the target technology in order to use it.

Each design kit is developed around a specific CAD software environment. MCM Station from Mentor Graphics, for instance, is designed specifically for MCM and hybrid design. With MCM Station and a design kit, the designer has a standard design environment, standard files, design rules, library elements, and simulation models to use during development. Vendor-specific utilities are provided for non-standard interfaces (e.g. test point locations). Upon design completion and verification, data can be transferred directly to the target foundry without converting from foreign formats.

There are different manufacturing techniques that are currently being used for most MCMs today. MCM-L where L stands for laminated, employs conventional PC board technology using fine pitch interconnect . MCM-C or co-fired ceramic, commonly used for hybrid circuits, is now being extended to MCMs. MCM-D or deposited uses integrated circuit fabrication techniques and equipment. There are cost, density, and performance trade-offs inherent with each of these technologies. Having selected a particular manufacturing technology that meets his design objectives, the designer must then implement the design in the target technology. Without a design kit, this requires some level of expertise in the target technology. By providing a library of physical, electrical, and thermal models, the designer can focus on implementing the design rather than meeting the manufacturer's requirements.

Substrate Insulators

Material	Dielectric Constant	Thermal Conductivity W/cm-K	Technology
Alumina (ceramic)	9.5	0.3	MCM-C, MCM-D
Beryllia (ceramic)	6.7	2.0	MCM-C, MCM-D
Epoxy glass (PC Board)	5.0	0.003	MCM-L
Polyimide	3.5	0.004	MCM-D, MCM-L
Silicon dioxide	3.9	0.01	MCM-D

Table 1.

MCM DESIGN PROCESS

A typical MCM design process using CAD tools starts with design entry in the form of schematic data and ends with manufacturing output in the form of documentation and photomask data (see figure 2). As a design progresses, there are iteration points where physical design data is fed back to simulation tools to reflect the impact of actual layout on the original engineering "best guess" at electrical and thermal characteristics. Since the library models for schematic entry and logic simulation are well defined, the design kit focuses on the physical layout, thermal analysis, and electrical characteristics of the interconnect, none of which has well defined models as they are dependent upon the layout implementation and characteristics of the materials that go into the module.

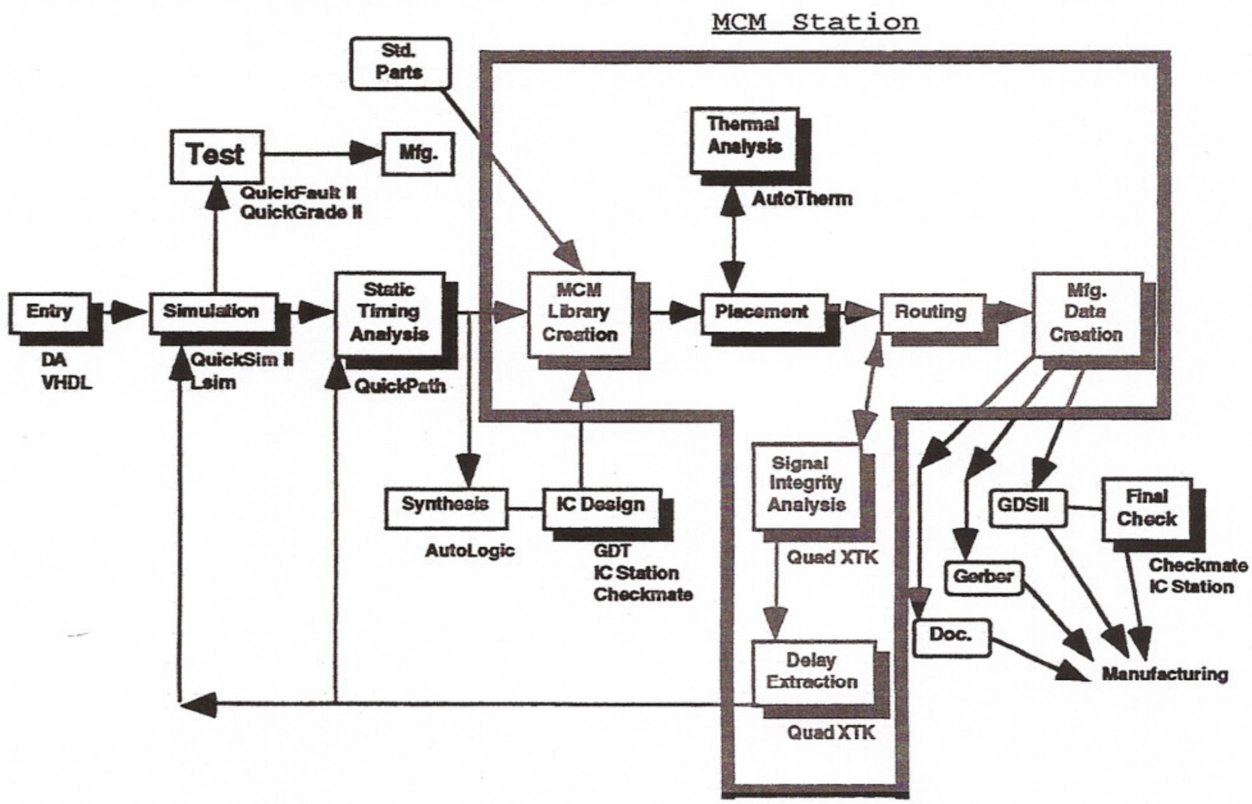


Figure 2.

PHYSICAL DESIGN

Physical models include: geometries representing substrates, components, vias, test structures, and other geometric design data required by the manufacturer. Some manufacturers offer standard packages, substrate sizes, and heatsinks, reducing non-recurring engineering (NRE) costs associated with custom tooling. Since MCMs tend to be high pin count devices, PGA packages and fine pitch quad flat packs (QFP) are common. Board technology may determine whether a through-hole or surface mount package is selected. Overall system requirements such as hermeticity can determine whether a ceramic package or substrate is needed vs epoxy (plastic package and FR4 PC board) material.

The MMS design kit stores technology information such as physical design rules, layer materials, electrical characteristics, routing constraints, and other technology information in a technology file. Some MCM foundries offer multiple rules sets and multiple technologies such as MCM-L, MCM-C, and/or MCM-D. In this case, technology files for each technology and rules set is required.

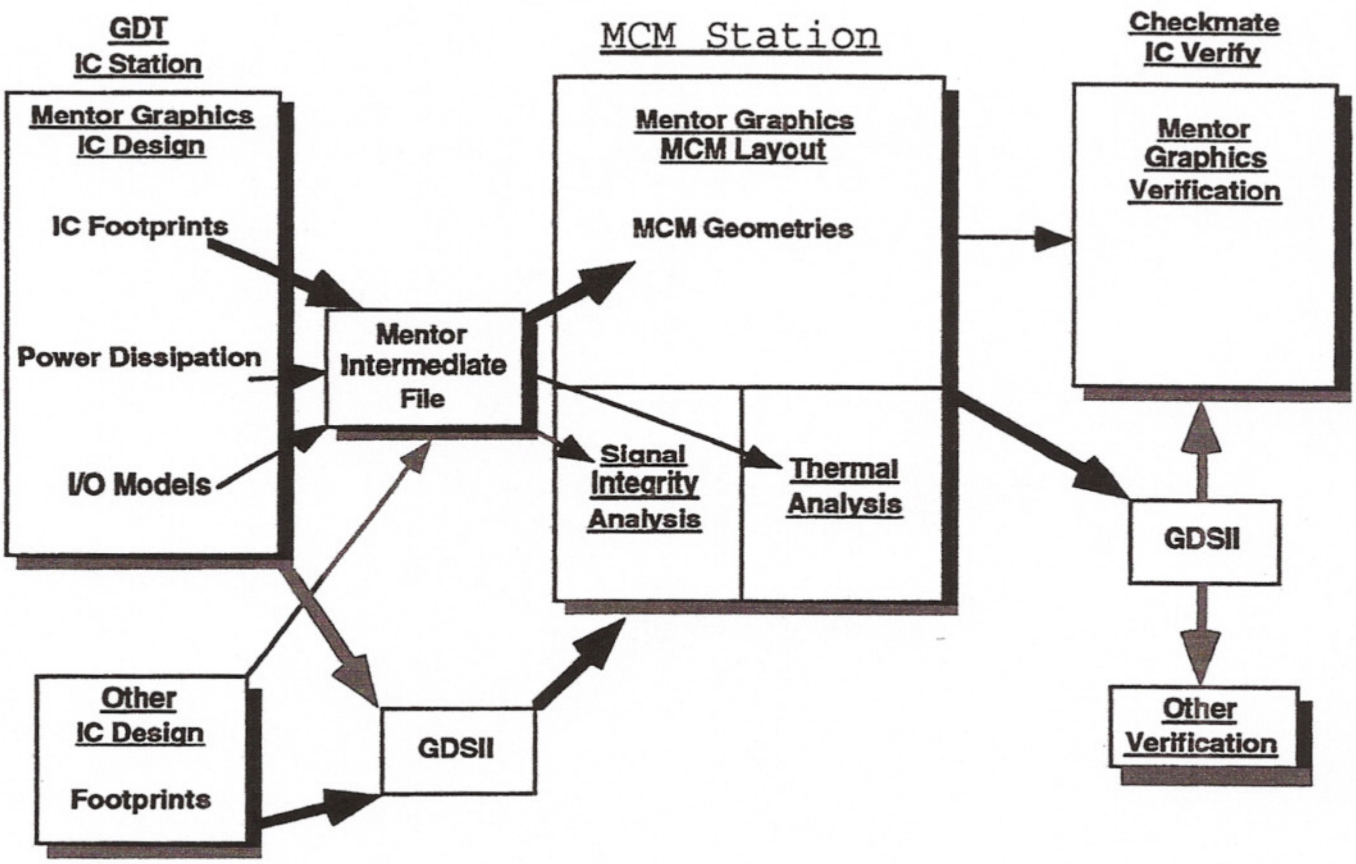


Figure 3.

Component geometry libraries in MCM design kits are not yet robust for a number of reasons. The effort required to create and update libraries of unpackaged components is much more complex than for packaged components because of their uniqueness. A 28 pin dip package, for example, is standard for many components in a variety of technologies and functions. On the other hand, components in their unpackaged silicon form, tend to change frequently as IC manufacturers make process and design improvements. With packaged components, these changes are transparent to the system designer, therefore the geometry that he uses does not change. It is therefore likely that the designer using a design kit will still need to create many of the necessary components. To facilitate the component creation process, CAD vendors are working together with MCM vendors to automate this process with interfaces that extract component data from standard GDSII data bases, directly from the CAD vendor's proprietary data base, or from ASCII files that specify die size, pad location and size, and pin type, as well as other information that may be specific to the target MCM technology or the component characteristics. The components must be created to accommodate a variety of connection technologies as well, including wire bond, TAB, and flip-chip.

Other geometries are more standard and are provided in the design kit geometry library and are building blocks for components and substrates. These primitive geometries include: vias, pads (bond sites), test structures, alignment targets, and other structures that aid the manufacturer in monitoring the fabrication process.

Design rules in the technology file determine minimum width and spacing for traces, vias, and pins, exceptions for critical nets, and other physical rules associated with the manufacturer's process. Routing constraints are specified in this file. If, for example, it is necessary to control characteristic impedance, trace widths may be specified from layer to layer. The technology file or set of files therefore provide the rules that allow the designer to design in full compliance with the MCM manufacturer's design rules.

ELECTRICAL ANALYSIS

Prior to layout, any electrical analysis is done based on a best guess of interconnect delays. Actual delays and signal quality will vary depending upon the number of layers used, the conductor material used, the dielectric constant of the insulating material between traces, and trace widths, spacing, and thickness. Until layout is completed, it is difficult to know how routing will affect signal quality. With high speed designs, transmission line effects are no longer negligible. Impedance mismatch and cross-talk can adversely affect signal quality. It is therefore necessary to perform signal integrity analysis on high speed or noise sensitive designs in order to catch, correct , and re-simulate the design before modules are manufactured.

(1)

unit propagation delay

t_{pd} = square root (e_r) x t_o (distance/sec)

where:

e_r is the effective dielectric constant of the substrate material

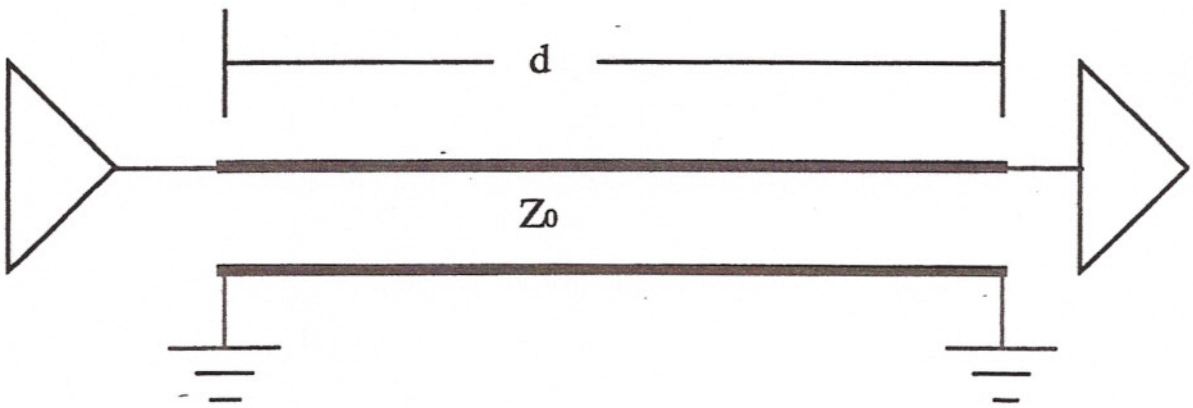
t_o is the speed of light in a vacuum

As a rule of thumb, interconnect must be treated as a transmission line if the driver rise or fall time is shorter than the signal delay to the receiver and back. Equation 2.

(2)

$$t_r < t_{pd} \times 2d$$

where:
tr is the driver rise time
d is the distance to the receiver



$$Z_0 = \sqrt{\frac{L}{C}}$$

where:
L = inductance per unit length
C = capacitance per unit length

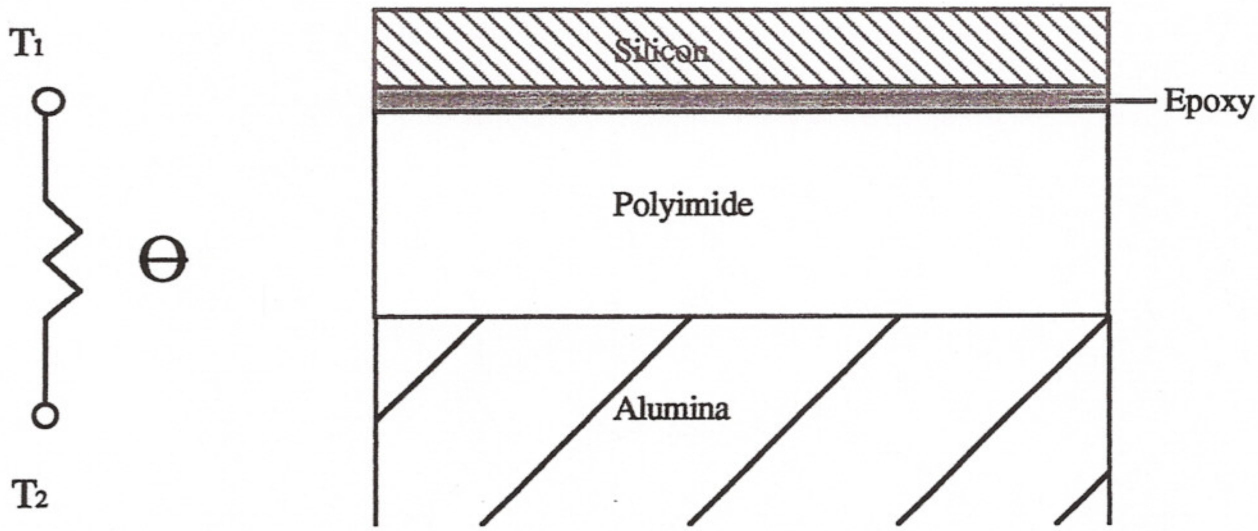
Figure 4. Transmission Line

Interconnect characteristics can be extracted from the layout data base by tools that perform 2 dimensional or 3 dimensional field analysis in order to accurately model the transmission line and mutual coupling effects. Libraries of driver and receiver models allow the designer to observe the effects of the interconnect and receiver load(s) on the waveform generated by the driver.

While first order effects can be approximated using empirical formulas, high speed designs require more accurate analysis that accounts for skin effect, high frequency harmonics, and lossy effects in the conductor and dielectric materials. In addition, cross-coupling to quiet lines can be significant when the quiet line is surrounded by active lines both on the same layer and on adjacent layers.

THERMAL ANALYSIS

The increases in packing density derived from MCMs, gives rise to a corresponding increase in power density. As a result, thermal analysis becomes more critical. Thermal analysis is in many ways analogous to electrical analysis where heat (power) is analogous to electrical current, temperature is analogous to voltage, and thermal resistance is of course analogous to electrical resistance. A simplified model of the thermal path from a component to the substrate is illustrated in figure 5.



Θ = effective thermal resistance of thermal path

Figure 5.

The design kit provides the material properties necessary to model from the junction of each component to the ambient environment. The model includes thermal resistance, power consumption, maximum junction temperature, and other properties necessary for thermal analysis. Thermal analysis is linked to layout since placement changes made during thermal analysis for example, must be reflected in layout.

MANUFACTURING INTERFACES

After the design has been implemented and analyzed, manufacturing output must be generated. Post layout processing may be performed to insure manufacturability. Assembly drawings are created to guide die attach and bond equipment operators. Die attach equipment may be manually operated or automated. MCM-L and MCM-C typically require Gerber format photo mask data and drill data. MCM-D typically requires GDSII format photo mask data for higher resolution photolithography.

TEST

Testing is performed at multiple levels. First, the substrate is tested to verify the interconnect without components. MMS has developed a bare die test technique that allows bare dies to be completely tested and burned in without any special processing as would be required with TAB. The design kit specifies a test file format for die and substrate testing prior to assembly. After the module is fully assembled, it can be tested as an integrated circuit or as a subsystem. Electrical, mechanical, and environmental tests can be performed.

SUMMARY

MCM design kits, in conjunction with CAD tools, provide a means for systems to overcome the barriers to entry into MCM technology. There are many infrastructure issues that are being addressed because of the growing demand for MCM technology. These include such enabling technologies as bare die test, CAD tools, specialized equipment, package standards, and test standards. As they develop, more systems designers will be able to take advantage of the benefits of MCM technology.

REFERENCES

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*No paper available at time of publication; contact speaker for further information.

†Paper published separately; contact speaker for further information.

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