A New Standard for PCB/MCM Data Exchange

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Abstract

Today's PCB and MCM designers often work in a heterogeneous environment in which software from multiple Electronic Design Automation (EDA) software vendors is used to create design and manufacturing data. In this environment, data must be shared or transferred between groups, transferred to manufacturers, or archived for later retrieval or ECO. A smooth seamless interface between the designer and manufacturer helps designers meet their goals for minimum time to market of their products and lower product cost. Standards allow designers to develop products in multi-vendor environments without requiring tight integration of tools. This paper discusses the value of EDIF 4 0 0 for transferring design and manufacturing data for PCBs and MCMs.

Keywords: ASEM CAD, CAM, Data Exchange, EDA, EDAC, EDIF

Design to Manufacturing Data Transfer

The manufacture, assembly, and test of printed circuit boards (PCB) and multichip modules (MCM) requires a variety of files in numerous formats. Artwork, drill, and milling data drive photo mask and drill machines. Component type and location drive assembly equipment. Test points, probe type, and test strategies drive test equipment. Each piece of equipment has its own format. Data for these target machines are typically generated from the design data base as a sea of separate dissociated files.

PCB manufactures recognize that manufacturing data alone is not sufficient to insure optimum manufacturability and assembly. Contract manufacturers may add value by checking the artwork for yield enhancement. Recommendations for edits must be communicated back to the designer, artwork and drill data must be regenerated, and transmitted back to the manufacturer. Time and cost savings can be realized if yield

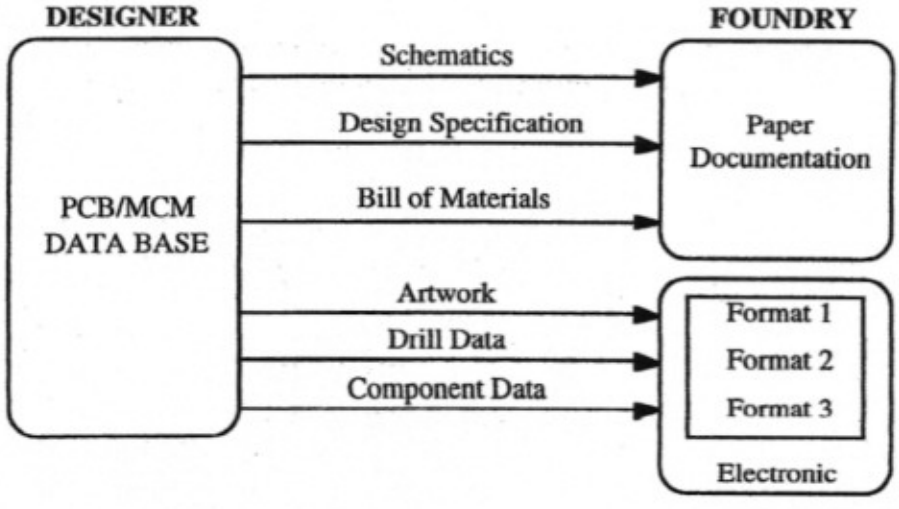

Figure 1. Current Foundry Interface

enhancement modifications are made by the manufacturer. The risk associated with the current process, however, is that the original design intent is not contained in the artwork. Modifications to artwork data may violate electrical, thermal, or mechanical design requirements that are not obvious by inspection.

MCM foundries have recognized the need to easily transfer complete design data between incompatible EDA systems. Many of these foundries have internal design tools with manufacturing interfaces optimized for their factory. Asserting that design time and costs of multichip modules are significantly increased because of the lack of design information, foundries and EDA vendors came together in 1993 to form the ASEM (Application-Specific Electronic Modules) CAx Interface Alliance, an ARPA funded consortium. With a mission to define specifications for bi-directional exchange of ASEM information and data, the Alliance selected EDIF (Electronic Design Interchange Format) as the preferred format because of its robustness and ability to satisfy most of the requirements of the ASEM information model.

The Need for Standards

In the absence of industry standards, the transfer of design data between incompatible EDA systems can be problematic. While point to point translators translate directly from one EDA vendor's format to another, it is difficult to faithfully translate the original design intent as represented by technology rules, electrical properties, thermal properties, manufacturing data, assembly data, and test requirements.

A PCB or MCM data base can consist of schematic sheets, schematic symbol libraries, a physical layout data base, component libraries, technology data, driver/receiver models, artwork files, aperture files, drill files, and documentation. Loss of critical design information can lead to schedule delays, additional development costs, and errors. While Gerber's RS-274 for example, an EIA standard for PCB artwork data exchange, is sometimes used as a means of transferring electronic design data. Regrettably, it is woefully inadequate as a data base from which to reconstruct a complete design, or extract any data other than artwork. RS-274 was originally intended to drive photoplotters and lacks any logical connectivity information. EDA tools exist that will reconstruct logical connectivity, but the process is time consuming and error-prone. In addition, aperture table and drill information may not be available, preventing accurate reproduction of the original design. Computer-aided manufacturing (CAM) equipment, compounds the problem. A single EDA vendor's design tools must map to multiple formats to drive manufacturing equipment.

EDIF 4 0 0 provides for transfer and archival of design and manufacturing data for PCBs and multichip modules (MCMs). It builds upon a clear and unambiguous information model, eliminating problems inherent in previous revisions of EDIF. Industry support for

	Type of Data								
	Connectivity	Artwork	Rules	Placement	Drawing	Test	3D Mechanical	Material Properties	MCM Features
DXF	No	Yes	No	No	Yes	No	Yes	No	No
EDIF 4 0 0	Yes	Yes	Yes	Yes	Yes	No	Limited	Yes	Yes
GDSII	No	Yes	No	No	No	No	No	No	No
Gerber	No	Yes	No	No	No	No	No	No	No
HPGL	No	Yes	No	No	No	No	No	No	No
IGES	No	No	No	No	Yes	No	Yes	No	No
IPC-D-35x	352	350	352	352	351	356	350	No	No
STEP AP 210	Yes	Yes	No	Yes	Yes	No	Yes	No	No

Table 1. Some Existing Design-to-Manufacturing Data Exchange Formats

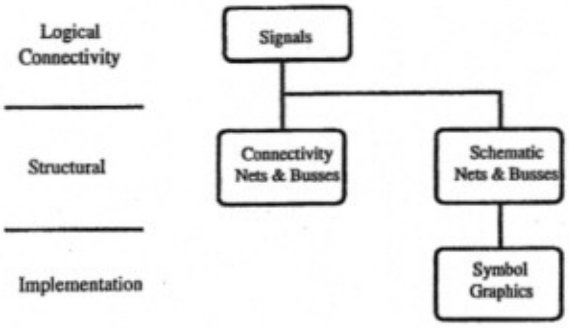

Figure 2. EDIF 3 0 0 Architectural View
Source: EDIF TSC

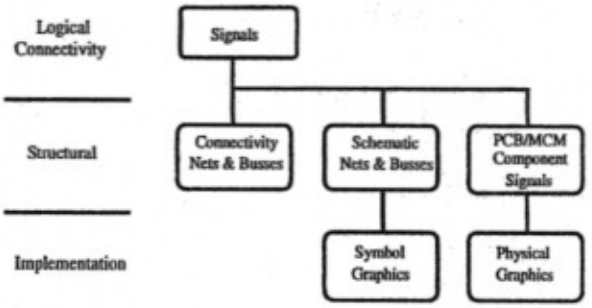

Figure 3. EDIF 4 0 0 Architectural View

EDIF 4 0 0 is mounting. It is the goal of the Product Marketing Counsel of the Electronic Design Automation Companies (EDAC PMC) to "Ensure a robust yet complementary minimum set of PCB standards, such that end users and vendors can maximize their productivity. This includes all standards that facilitate data exchange for design, development, and manufacturing of PCBs and MCMs." To this end, the EDAC PMC has endorsed EDIF 4 0 0.

EDIF Improvements

Released in 1987, EDIF 2 0 0 was widely used for schematic and netlist transfer and accepted as an ANSI standard, but was prone to ambiguities. PCB layout received little support from EDA vendors. EDIF 3 0 0 released in 1993, sought to resolve these problems by specifying an information model using an information modeling language called EXPRESS G. It allows for definition of objects, attributes, relationships, and constraints. Information modeling helps clarify requirements and eliminate ambiguities by explicitly defining objects, attributes, and their relationships.

The architecture of EDIF 3 0 0 defined three views: logical connectivity, structural connectivity, and implementation (Figures 2 & 3). While its scope was limited to schematic and netlist, it provided stubs for other extensions, including PCB layout. EDIF 4 0 0 is extended to include PCB and MCM models. It covers parts, packages, components, materials, bare boards, assembled boards, design rules, and manufacturing drawings.

ASEM Information Model

Definition of an information model was the key to capturing the requirements of the ASEM Alliance foundry interface. This information model includes bare dies, wire bond, flip chip, TAB, MCM-C, -D, -L, chips-first, thick/thin film, and embedded components.

The ASEM interface model identifies customer to foundry interaction at multiple entry points ranging from system definition through physical layout. With an initial focus on physical layout, the Alliance determined that extensions to the EDIF 3 0 0 information model mapped well with the ASEM Alliance interface model.

Customer to foundry interface requirements include transfer of the following data.

- schematic
- netlist
- component, mechanical, & package geometries
- drawings
- routing
- manufacturing data - holes, coupons, test structures
- assembly rules
- technology rules
- layer stackup

The initial PCB extension, implemented in EDIF 3 5 0, included information models and syntax for schematic, netlist, parts, packages, components, bare boards, and assembled boards. EDIF 4 0 0 was extended to include design rules, material properties, manufacturing drawings, and MCM requirements such as bare dies and wire bonds. In an effort to leverage existing industry standards, EDIF 4 0 0 references IBIS, VHDL, and DIE formats. While EDIF 4 0 0 can readily be extended in the future, the information model does not currently include test requirements, high speed timing, or crosstalk requirements. The EDIF Technical Subcommittee (TSC) is currently working with other standards organizations such as the CAD Framework Initiative (CFI), the Standard for the Exchange of Product Model Data (STEP) organization, and the Electronics Industry Association of Japan (EIAJ). The EDIF Technical Subcommittee (TSC) is working with CFI and STEP (Standard for the Exchange of Product Model Data) to agree on a common information models and minimize overlap in standards.

Archival

Archival is another step in the product development process that derives benefit from a common design data format such as EDIF. Archived data must, in the case of mil-aerospace companies for example, be retained for long periods of time. If the data needs to be restored to an EDA system incompatible with the original system, or the data base format has changed, it may be difficult, if not impossible, to faithfully retrieve the original design data.

Archival is critical to the mil-aerospace industry in which data archival for long periods of time is necessary for potential engineering modifications (ECO) late in a product's life cycle. Design software and data base formats can change from the time the design was originally archived to the time it is retrieved.

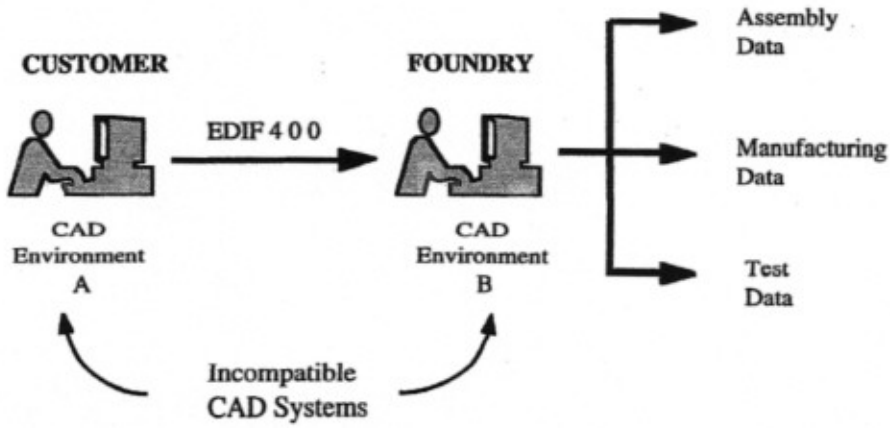

Figure 4. ASEM Foundry Interface Model

Summary

The history of standards has often been a mixed blessing. Standards that are not robust and not well defined are subject to poor translator implementations. Design data exchange standards must permit designers faithful reproduce the original intent of the design. Retaining the design intent can enhance yield and minimize costs in the manufacturing, assembly, and test phases of the design process. EDIF 4 0 0 has received support from industry standards organizations because of its focus on design data, a well conceived approach to applying information modeling to capture requirements, and goal of leveraging existing standards wherever possible. The final test, of course, is that EDA, CAD, and CAM vendors implement tools to read and write the formats, and their customers use them in their product development process.

Information on the Internet

For more information on EDIF, visit the EDIF web site at

http://www.edif.org
http://www.EDAC.org

or send email to

edif-support@cs.man.ac.uk

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032	**Signal Integrity Tools For High Speed Design** Dale Parker	155
033	**Board Fabrication 101** Glenn Heath Tom Molamphy	**
041	**EDA Face To Face** Nick Lester	*
051	**A Design Methodology and Design Automation Environment for DFM** Tony Mazullo	163
052	**SEX at the CAM Station- The Strategic Exchange of Extracted Data** Richard Nedball	173
061	**Introduction to Electromagnetic Interference** Stephen Lum	181
062	**EDIF - A New Standard For Data Exchange** John Cofield	193
071	**EMC - Test, Measurement, and Simulation** Dr. Al Wexler and Ernie Gant	201
072	**A Walk Through the Board Shop** Gary Ferrari	**
073	**Layout and Routing Techniques for Dense Surface-Mount PCBs** Genny Filtranti	217

** Panel discussion - No paper available* *** Paper not available at time of publication*

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