Topological Structure and Physical Layout Codesign for Wavelength-Routed Optical Networks-on-Chip

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***Abstract*—The wavelength-routed optical network-on-chip (WRONoC) is a promising solution for signal transmission in modern system-on-chip (SoC) designs. Previous works do not handle three main issues for WRONoC's: correlations between the topological structure and physical layout, trade-offs between the maximum insertion loss and wavelength power, and a fully automated flow to generate predictable designs. As a result, the insertion loss estimation is inaccurate, and thus only suboptimal results are obtained. To remedy these disadvantages, we present a fully automated topological structure and physical layout codesign flow to minimize the maximum insertion loss and the wavelength power simultaneously with a significant speedup. Experimental results show that our codesign flow significantly outperforms state-of-the-art works in the maximum insertion loss, wavelength power, and runtimes.**

I. Introduction

With the ever-increasing requirements of high-speed low-power transmission for large System-on-Chip (SoC) integration designs, the optical network-on-chip (ONoC) emerges as a promising solution. ONoC is regarded as a next-generation signal transmission standard for large SoC designs thanks to its ability to deliver power-efficient on-chip communication with high bandwidth and low latency. Due to these technical advantages, academia, industry and government have shown high interest in ONoC designs [1], [2], [3], [4], [5].

In ONoCs, electrical signals are converted to optical ones, transmitted through optical waveguides, and then converted back to electrical signals when received, as shown in Figure 1. Lasers are used for optical transmission in the optical waveguides. To maintain the signal integrity, the operating power reached at all receiving ports should be larger than a threshold value. The maximum insertion loss in ONoCs determines the minimum required laser power, Therefore, maximum insertion loss minimization is critical in ONoC designs.

Among many recent advanced techniques for ONoC designs, the wavelength-routed ONoC (WRONoC) shows a great potential of providing higher-bandwidth on-chip communication with reasonable power overheads with the aid of the Wavelength Division Multiplexing (WDM) technique [6]. With proper signal routing and multiple wavelengths usage, dedicated signal paths for each communication are reserved at the design time, and thus all signals in WRONoCs can be transmitted concurrently without data collisions. The number of used wavelengths is the same as the number of required laser sources, which is proportional to the wavelength power required by the WRONoCs.

However, poor signal routing may incur extra insertion loss, and multiple wavelengths usage needs additional wavelength power. Both costs would reduce the power efficiency provided by WRONoCs, if not handled properly. As a result, how to properly assign the routing resource, such as waveguides, microring resonators (MRRs), and wavelengths, to minimize maximum insertion loss and wavelength power becomes the main objective in WRONoC design. Figure 2 shows some functions of MRRs and waveguides.

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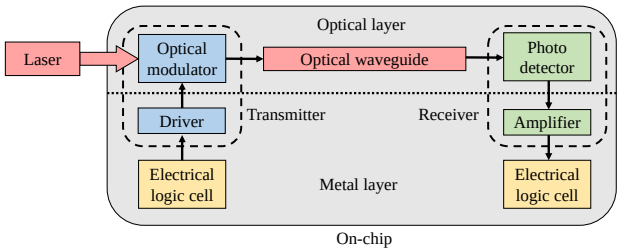


Fig. 1. An overview of an ONoC design. A signal from an electrical logic cell is converted into an optical signal, transmitted on an optical layer, and then converted back to an electrical signal when received.

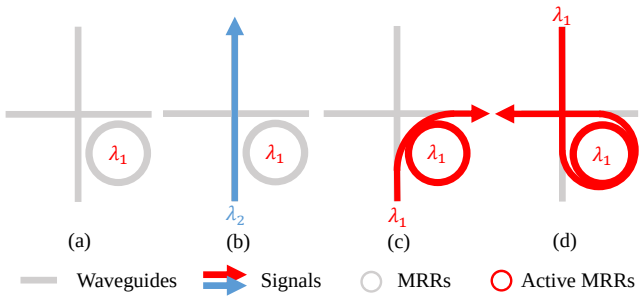


Fig. 2. (a) The microring resonator (MRR) and waveguide representation. (b) If the characteristic wavelength of the MRR λ_1 is different from the wavelength of the signal λ_2, the signal will pass the MRR. (c)(d) Otherwise, the signal will be bent and thus be transmitted to the adjacent waveguide.

To handle the WRONoC design, researchers have proposed to partition the original design into two stages: *topological structure* and *physical layout* [7]. Given placed devices and their communication requirements, the topological structure includes the netlist of all devices and MRRs, the wavelength assignment of all signals, and the usage of all MRRs. The physical layout, on the other hands, includes information such as the orientation of all devices, the placement of all devices and MRRs, and the location of all waveguides. Previous works addressing topological structure and/or physical layout design problems will be detailed in Section I-A.

However, as the design complexity of WRONoCs continues to increase, two disadvantages arise. First, the estimation error induced by separate stages is no longer negligible. For example, the maximum insertion loss and wavelength power minimization during topolog-

ical structure generation is inaccurate, due mainly to the lack of physical layout information, and the quality of maximum insertion loss minimization during physical layout generation is suboptimal because the topological structure is fixed. Second, the existing design flows are not fully automated, thus reducing the predictability of generated designs. To the best of our knowledge, no previous works can eliminate the estimation error induced by separate stages in a fully automated way. In this work, we propose a fully automated topological structure and physical layout codesign flow that can generate a predictable WRONoC design to minimize the maximum insertion loss and wavelength power.

A. Previous Works

WRONoC design problems addressing challenges of topological structure and/or physical layout were extensively studied over the past decade. For topological structure design automation, Li *et al.* proposed an ILP-based topological structure generation method for application-specific WRONoCs [8]. For physical layout design automation, Boos *et al.* proposed a placement-and-routing engine for fast performance evaluation [9], and Chuang *et al.* proposed a graph-based concurrent placement and routing scheme for planar circuits to minimize the number of signal crosses [10]. For topological structure and physical layout codesign, Truppel *et al.* proposed an ILP-based topological structure and physical layout generation method based on manual design templates [7].

For the aforementioned previous works with various considerations, there are three main drawbacks with them:

- The correlations of topological structure and physical layout are insufficient.
- The trade-offs between the maximum insertion loss and wavelength power are neglected.
- The design flows are not fully automated, and thus the generated results are unpredictable.

This paper intends to remedy these drawbacks.

B. Our Contributions

We summarize the main contributions of this paper as follows:

- We propose a topological structure and physical layout codesign flow for WRONoCs to minimize the maximum insertion loss and the wavelength power effectively and efficiently. To the best of our knowledge, this is the *first* fully automated flow that can generate a WRONoC design with its topological structure and physical layout simultaneously.
- We propose a cost estimation function that trades off between the maximum insertion loss and wavelength power during topological structure and physical layout codesign.
- The proposed design flow is fully automated, no manual design templates are needed, which substantially increases the predictability of generated designs.
- Experimental results based on a real WRONoC benchmark show that our codesign flow significantly outperforms published works in the maximum insertion loss, wavelength power, and runtimes.

The remainder of this paper is organized as follows. Section II introduces the sources of insertion loss, and then formulates the topological structure and physical layout codesign problem for WRONoCs. Section III presents our codesign flow. Section IV reports and analyzes the experimental results. Finally, Section V concludes this paper.

II. Preliminaries

In this section, we first introduce various sources of insertion loss in WRONoCs addressed in this work, and then give our formulation of the topological structure and physical layout codesign problem for WRONoCs.

A. Insertion Loss

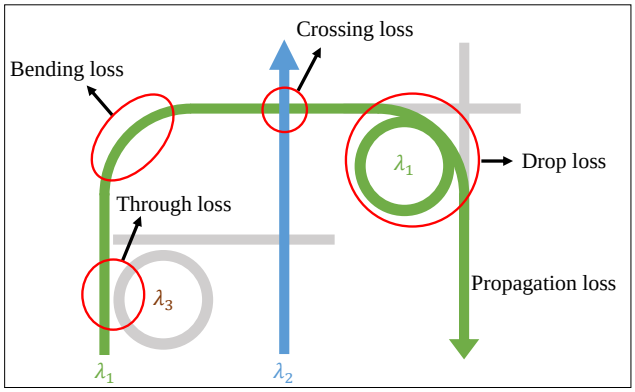


Fig. 3. Five major sources of insertion loss in WRONoCs.

For WRONoC design, one objective is to minimize the maximum insertion loss of all signals. Here we introduce five major sources of insertion loss in WRONoCs: *crossing loss*, *through loss*, *drop loss*, *bending loss*, and *path loss* as shown in Figure 3.

- *Crossing Loss* (L_{crs}): The crossing loss is induced when two signals intersect with each other.
- *Through Loss* (L_{thr}): The through loss is induced when a signal passes an MRR without activating it.
- *Drop Loss* (L_{drp}): The drop loss is induced when a signal is switched from one waveguide to others by activating an MRR.
- *Bending Loss* (L_{bnd}): The bending loss occurs when a signal is transmitted through a bent waveguide.
- *Path Loss* (L_{pth}): The path loss is induced when a signal is transmitted through waveguides.

In this work, the insertion loss L is calculated as follows:

$$L = L_{crs} + L_{thr} + L_{drp} + L_{bnd} + L_{pth}. \quad (1)$$

B. Problem Formulation

The topological structure and physical layout codesign problem for WRONoCs addressed in this paper can be formulated as follows:

*Problem 1 (**Topological Structure and Physical Layout Codesign**):* Given placed devices, communication requirements, and wavelength power consumption, generate a WRONoC design with its topological structure and physical layout that minimizes the maximum insertion loss and the wavelength power.

III. Proposed Algorithms

In this section, we first give an overview of our topological structure and physical layout codesign flow, and then introduce how we trade off between the maximum insertion loss and wavelength power in the proposed flow. Figure 4 shows our topological structure and physical layout codesign flow which consists of the following three stages: (1) *Preprocessing*, (2) *Structure-Layout Codesign*, and (3) *Refinement*. In Preprocessing, we create routing grids according to the positions of placed devices. Structure-Layout Codesign then iteratively generates the topological structure and physical layout simultaneously to minimize both the maximum insertion loss and the wavelength power. Finally, Refinement smooths the sharp bendings to further reduce bending loss. These three stages will be detailed in Sections III-A, III-B and III-C.

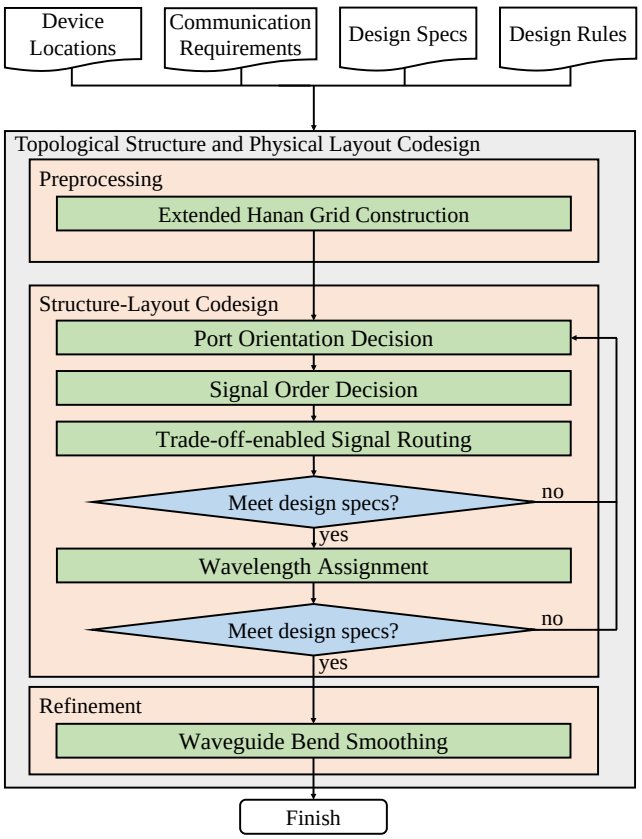


Fig. 4. The topological structure and physical layout codesign flow

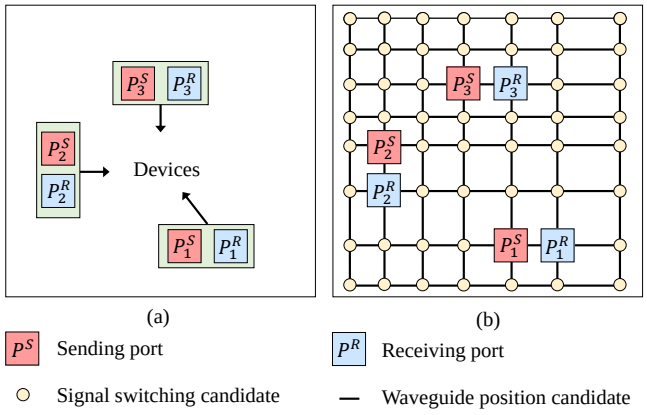


Fig. 5. During preprocessing, (a) given devices and their sending/receiving port positions, (b) we generate an extended Hanan grid as waveguide position and signal switching candidates.

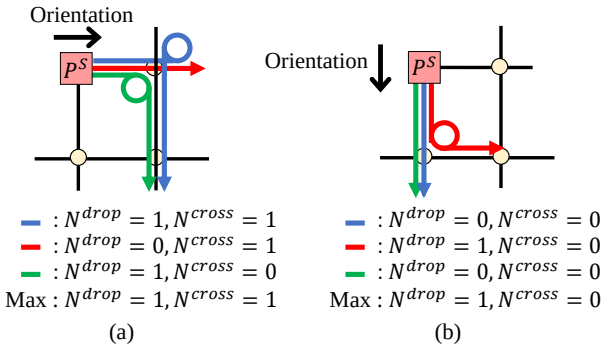


Fig. 6. During port orientation decision, (a) knowing the codesign results of the previous iteration, (b) we adjust the port orientations to reduce the maximum insertion loss. Here N^{drop} represents the number of signal droppings, and N^{cross} the number of signal crossings.

A. Preprocessing

In WRONoC design, topological structure and physical layout focus on different design aspects. For the topological structure, the netlist of all devices and MRRs, the wavelength assignment of all signals, and the usage of all MRRs are considered. The physical layout, on the other hand, records the orientations of all devices, the placement of all devices and MRRs, and the locations of all waveguides. To achieve a codesign paradigm, a representation which supports both aspects is required. Here we propose an extended Hanan grid to facilitate considerations of topological structure and physical layout in the subsequent stages. The extended Hanan grid is generated based on the vertical and horizontal positions of all devices. Both topological structure and physical layout can be embedded into the extended Hanan grid. Each line gives a waveguide position candidate for signal transmission, and each intersection of lines makes a signal switching candidate for signal bending, crossing, and dropping. Figure 5 shows an example of an extended Hanan grid.

Given the positions of all devices and their sending/receiving ports, we first construct a Hanan grid based on the original work [11]. Then we insert extra lines to form an extended Hanan grid according to g_{min} and g_{max}, respective parameters for the minimum and maximum bending radius constraint handling. The relationship between the bending radius r, the wire width w, the wire spacing s, and the extended Hanan grid width g is $g = \max(w + s, 2r)$. Given the maximum and minimum bending radii, therefore, we can get the respective maximum and minimum grid widths, g_{max} and g_{min}, by the above formula. By setting the grid width between g_{max} and g_{min}, all the bending radii are within the permitted range, and thus the minimum and the maximum bending radius constraints are satisfied.

The extra lines are inserted between and outside the original Hanan grid. These additional lines increase the number of waveguide and MRR position candidates for possible crossing and wavelength power reduction.

B. Structure-Layout Codesign

In this stage, we iteratively generate both the topological structure and the physical layout of WRONoCs that minimize the maximum insertion loss and wavelength power.

1) Port Orientation Decision: The objective of this step is to decide the orientations of the sending/receiving ports on all devices to minimize the maximum insertion loss. Different port orientations might lead to different amounts of insertion loss. Take Figure 6 as an example. Suppose that the red signal has much lower insertion loss, as shown in Figure 6 (a), rotating the port will increase the insertion loss of the red signal but reduce the insertion loss of both green and blue signals, hence reducing the maximum insertion loss, as shown in Figure 6 (b).

In the first iteration, the port orientation is decided only by the port position. The orientation of a port is determined by the average angle formed with all connected ports. Knowing the previous codesign results, we adjust in the subsequent iterations the orientation such that the maximum insertion loss is minimized.

2) Signal Order Decision: Signal Order Decision is a critical step for WRONoCs to decide the signal order for Trade-off-enabled

Signal Routing in the next step. A poor signal order for WRONoCs increases not only the path loss, but also the crossing loss and wavelength power. To minimize the maximum insertion loss and the wavelength power, the signal order is determined by the non-increasing order of the signal criticality. Signal criticality is initially defined by the half-perimeter wirelength (HPWL) between the signal sending and receiving ports, and is defined by the signal insertion loss in the following iterations. Since longer signals are more likely to incur larger bending and crossing loss and share waveguides with other signals, they are potentially more critical for the maximum insertion loss and wavelength power minimization; on the other hand, shorter signals are unlikely to cross or bend during transmission and seldom share waveguides with other signals, thus potentially uncritical for the maximum insertion loss and wavelength power minimization.

3) Trade-off-enabled Signal Routing: After Port Orientation and Signal Order Decision, we perform an A* search-based Trade-off-enabled Signal Routing on the extended Hanan grid to generate both topological structures and physical layouts simultaneously. To guide the searching algorithm to find a better design, we use the following equation to predict the routing cost:

$$c_i = \alpha * \Delta L_{max} + \beta * L_i + \gamma * N_i^{drop}, \tag{2}$$

where c_i is the cost of routing the signal s_i, ΔL_{max} is the variation of the maximum insertion loss of all routed signals when the signal s_i is routed, L_i denotes the insertion loss of the signal s_i, N_i^{drop} denotes the number of drops of the signal s_i, and α, β, and γ are user-defined coefficients to trade off between the maximum insertion loss and wavelength power.

The first term of Equation (2) is to reduce the maximum insertion loss. Figure 7 illustrates the importance of considering the maximum insertion loss. The orange signal is routed after the green and blue signals. If the cost function considers only the insertion loss of the orange signal, the maximum insertion loss of all signals might be larger, as shown in Figure 7 (a). However, if we consider the maximum insertion loss during signal routing, the maximum insertion loss of all signals could be further minimized, as shown in Figure 7 (b).

The second term of Equation (2) speeds up the A* searching. Since the maximum insertion loss increases only when additional signal droppings or crossings occur on the most critical signal, considering only the maximum insertion loss leads to inefficient cost searching during A* search. Therefore, the insertion loss of the current routed signal is a good tie breaker for speedups.

The last term of Equation (2) penalizes the number of droppings for the signal i. When a signal drops into a waveguide, the wavelength of this signal must be different from the others to avoid data collisions. By setting a penalty to reduce the number of unnecessary signal droppings, the number of wavelengths could be reduced, and thus the wavelength power can be minimized.

Using this cost estimation function on the extended Hanan grid, we route each signal to generate both topological structures and physical layouts simultaneously. As shown in Figure 8, given a signal routing result, MRRs are placed where the signals drop, and waveguides are placed on the edges in the extended Hanan grid where the signals pass. Therefore, the netlist of all ports and MRRs, the placement of all MRRs, and the locations of all waveguides are all generated.

4) Wavelength Assignment: After signal routing, the netlist of all devices and MRRs, the placement of all MRRs, and the locations of all waveguides are determined. In this step, we assign a wavelength to each signal to complete the topological structure design.

To prevent data collisions, all signals in a waveguide must be transmitted in different wavelengths. The assignment of the wavelength,

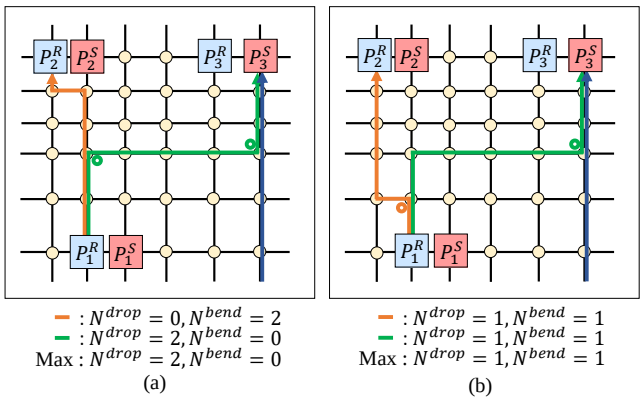


Fig. 7. Comparison of different cost estimation functions for signal routing. (a) Cost estimation function considering only the insertion loss of the current routed signal might increase the maximum insertion loss. (b) Our cost estimation function considers both the insertion loss of the current routed signal and the maximum insertion loss of all signals, and thus a better routing solution with smaller maximum insertion loss can be obtained. Here N^{bend} represents the number of signal bendings.

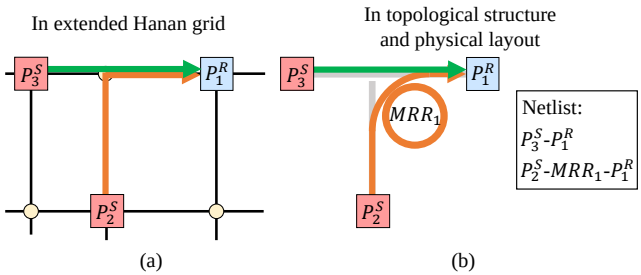
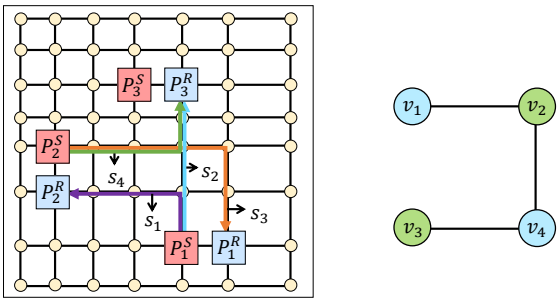


Fig. 8. An example of the topological structure and physical layout codesign by the extended Hanan grid. (a) Given a signal routing result on the extended Hanan grid, (b) MRRs are placed where the signals are dropped, waveguides are placed along the signal paths, and the netlist of all devices and MRRs is updated, and thus both topological structure and physical layout are generated simultaneously.

called *the wavelength assignment problem*, is equivalent to the graph vertex coloring problem, which is a well-known NP-complete problem. Given the signal routing result S for a wavelength assignment problem, we can generate the corresponding graph $G = (V, E)$ for the graph vertex coloring problem as follows: For each signal s_i in S, a vertex v_i is created in V. An edge e_{ij} is formed between the vertices v_i and v_j if the signals s_i and s_j are transmitted using the same waveguide. A solution to the graph vertex coloring problem on G is then equivalent to that to the wavelength assignment problem on S. An example with four signals and two wavelengths as an optimal solution of a wavelength assignment problem and its corresponding graph is shown in Figure 9.

To minimize the number of wavelengths, therefore, we need to find an optimal solution to the graph vertex coloring problem. We solve this problem by the ILP formulation proposed by [12]. Vertices with the same color imply that the corresponding signals will use the same wavelength.

After Wavelength Assignment, topological structure and physical layout are both determined. We then check if the number of wavelengths and the maximum insertion loss meet the design specifications. If the specifications are not met, we proceed with a



(a) (b)

Fig. 9. An example of Wavelength Assignment. (a) Given a signal routing result, (b) we create a corresponding graph and solve the graph vertex coloring problem.

new iteration based on the result of this iteration to further optimize the design. These steps continue until all design specifications are satisfied or the execution time limit is exceeded.

C. Refinement

The previous stages generate topological structures and physical layouts for WRONoCs automatically and simultaneously. However, since the bending loss of the optical waveguides is inversely proportional to the bending radius [13], we replace all right-angle waveguide bendings with smooth arcs to prevent large bending loss.

IV. Experimental Results

We implemented our topological structure and physical layout codesign flow in the C++ programming language. All experiments were performed on an Intel Xeon 3.5GHz workstation with 72GB memory. The Gurobi [14] solver was used to solve the wavelength assignment problem. We performed the experiments based on the benchmark in PSION [7], which is an optical networks-on-chip design with eight devices and 44 communications. *Since all related works used only this benchmark for their comparative studies, we shall focus on it for fair comparison.* The insertion loss settings were the same as those in PSION: 0.5dB per drop, 0.15dB per cross, 0.005dB per bend, 0dB per through, and 1.5×10^{-5}dB per centimeter. And the wavelength power was evaluated by the number of wavelengths.

To show the effectiveness, efficiency, and completeness of our codesign flow, we performed two experiments. First, we evaluated the results of our codesign flow and compared with the state-of-the-art works PSION [7], PlanarONoC [10], and PROTON [9]. Then, we compared our flow without the wavelength power minimization to examine the quality of our trade-off strategy in the signal routing algorithm.

In the first experiment, we compared the maximum insertion loss and the wavelength power of our codesign flow with the previous works PSION, PlanarONoC, and PROTON. The statistics and results of the previous works are based on the report in PSION [7]. As shown in Tables I and II, our proposed topological structure and physical layout codesign flow achieved an 8% maximum insertion loss reduction compared with PSION, a 43.5% maximum insertion loss reduction compared with PlanarONoC, and a 55.4% maximum insertion loss reduction compared with PROTON. Our flow also achieved the minimum number of wavelengths for this benchmark. Since all output signals of a device are transmitted by the same sending port, all output signals of a device must be transmitted in distinct wavelengths to avoid data collisions. Therefore, the maximum number of output signals among all devices is a lower bound of the minimum number of wavelengths for a WRONoC. Since the maximum number of output signals among all devices is seven for this benchmark, and the number of wavelengths used in our results is also seven, our flow indeed achieved the minimum number of wavelengths for this benchmark. For the runtime comparisons, only our codesign flow is complete and fully automated, while PSION requires manual physical layout design templates, and both PlanarONoC and PROTON only generate physical layouts based on topological structures designed manually. So our codesign flow is very efficient. Figure 10 shows the resulting layout, and Table IV lists the resulting wavelength assignment.

In the second experiment, we compared our codesign flow without the wavelength power minimization. That is, the coefficient γ in Equation (2) was set to zero. As shown in Table III, our codesign flow achieved a 3.1X speedup with a 3.7% maximum insertion loss overhead using only seven wavelengths, compared with the codesign flow without the wavelength power minimization that needs eight wavelengths.

The reasons why our proposed codesign flow can achieve significant reductions in the maximum insertion loss and wavelength power with reasonable runtimes are analyzed as follows:

- Our codesign flow generates topological structures and physical layouts simultaneously considering both the maximum insertion loss and the wavelength power. This flow avoids quality degradation induced by separate stages and thus ensures solution quality. In contrast, previous works suffer from non-automatic design flow and/or fixed topological structures. For example, the solution quality of PSION is limited by the quality of manual design templates, and that of PlanarONoC and PROTON is limited by the fixed input topological structures.
- We propose the extended Hanan grid to guide the topological structure and physical layout codesign flow. The additional lines provide a larger solution space, and therefore better solutions with lower maximum insertion loss could be obtained. In the PSION design flow, in contrast, the manual design templates often contain insufficient routing resource, thus limiting the solution quality.
- We propose an A* search cost estimation function for signal routing considering both the maximum insertion loss and the wavelength power minimization. The user-defined coefficients enable designers to trade off between these optimization objectives.
- We utilize the A*-search algorithm, instead of an ILP, to efficiently generate topological structures and physical layouts. Therefore, a significant runtime reduction can be achieved compared with PSION.

V. Conclusions

We have proposed a fully automated topological structure and physical layout codesign flow. With a novel A* search cost estimation function for signal routing, we can generate a WRONoC design that minimizes the maximum insertion loss and the wavelength power simultaneously and efficiently. Experimental results have shown that our codesign flow is superior to the existing WRONoC design flows in the maximum insertion loss, wavelength power, and runtimes.

References

[1] Bringing photonic signaling to digital microelectronics. Accessed: 2019-08-10. [Online]. Available: https://www.darpa.mil/news-events/2018-11-01

[2] Made in IBM Labs: IBM lights up silicon chips to tackle big data. Accessed: 2019-11-16. [Online]. Available: https://www-03.ibm.com/press/us/en/pressrelease/39641.wss

[3] IBM Research—zurich: Silicon photonics. Accessed: 2019-11-16. [Online]. Available: https://www.zurich.ibm.com/st/photonics/devices.html

TABLE I
COMPARISONS OF THE NUMBER OF WAVELENGTHS (#WL), THE MAXIMUM INSERTION LOSS (MAX IL), THE NUMBER OF MRRS (#MRRS), AND CPU TIMES (SEC) FOR PSION [7], PLANARONOC [10], PROTON [9], AND OUR WORK FOR THE RESULTS WITH THE BEST MAXIMUM INSERTION LOSS.

Best Max IL	#WLs	Max IL	#MRRs	Time (sec)	Max IL Comparisons
PSION	8	3.18dB	52	271	1.08
PlanarONoC	8	5.20dB	56	<1	1.77
PROTON	8	6.60dB	56	134	2.24
Ours	8	2.94dB	65	12	1.00

TABLE II
COMPARISONS OF THE NUMBER OF WAVELENGTHS (#WLS), THE MAXIMUM INSERTION LOSS (MAX IL), THE NUMBER OF MRRS (#MRRS) AND CPU TIMES (SEC) FOR PSION [7], PLANARONOC [10], PROTON [9], AND OUR WORK FOR THE RESULTS WITH THE BEST NUMBER OF WAVELENGTHS.

Best #WLs	#WLs	Max IL	#MRRs	Time (sec)	Max IL Comparisons
PSION	7	4.08dB	40	6	1.34
PlanarONoC	7	6.40dB	48	<1	2.10
PROTON	7	8.10dB	48	79	2.65
Ours	7	3.05dB	64	4	1.00

TABLE III
COMPARISONS OF THE NUMBER OF WAVELENGTHS (#WLS), THE MAXIMUM INSERTION LOSS (MAX IL), THE NUMBER OF MRRS (#MRRS), AND CPU TIMES (SEC) FOR OUR CODESIGN FLOW WITH AND WITHOUT THE WAVELENGTH POWER MINIMIZATION.

	#WLs	Max IL	#MRRs	Time (sec)	Max IL Comparisons	Time Comparisons
Our w/o Wavelength Power Minimization	8	2.94dB	65	12.42	0.96	3.09
Our w Wavelength Power Minimization	7	3.05dB	64	4.02	1.00	1.00

TABLE IV
THE RESULTING WAVELENGTH ASSIGNMENT OF THE BENCHMARK WITH BOTH THE MAXIMUM INSERTION LOSS AND THE WAVELENGTH POWER MINIMIZATION.

	P_1^R	P_2^R	P_3^R	P_4^R	P_5^R	P_6^R	P_7^R	P_8^R
P_1^S	–	λ_6	λ_1	λ_3	λ_5	λ_7	λ_2	λ_4
P_2^S	λ_5	–	λ_4	λ_1	λ_6	λ_2	λ_3	λ_7
P_3^S	λ_7	λ_5	–	–	–	–	λ_6	λ_1
P_4^S	λ_3	λ_1	–	–	–	–	λ_5	λ_2
P_5^S	λ_1	λ_3	–	–	–	–	λ_4	λ_6
P_6^S	λ_4	λ_2	–	–	–	–	λ_7	λ_3
P_7^S	λ_2	λ_7	λ_3	λ_4	λ_1	λ_6	–	λ_5
P_8^S	λ_6	λ_4	λ_7	λ_2	λ_3	λ_5	λ_1	–

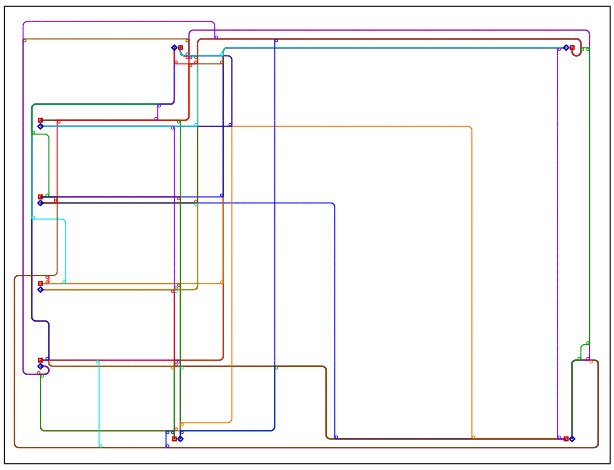


Fig. 10. The resulting layout of the benchmark with both the maximum insertion loss and the wavelength power being minimized.

[4] C. Sun, M. T. Wade, Y. Lee, J. S. Orcutt, L. Alloatti, M. S. Georgas, A. S. Waterman, J. M. Shainline, R. R. Avizienis, S. Lin *et al.*, "Single-chip microprocessor that communicates directly using light," *Nature*, vol. 528, no. 7583, p. 534, 2015.

[5] 25-56 Gbps silicon photonics on 28nm cmos. Accessed: 2019-11-16. [Online]. Available: https://www.tsmc.com/support/oip/2017/techpapers/2_01.htm

[6] T.-M. Tseng, A. Truppel, M. Li, M. Nikdast, and U. Schlichtmann, "Wavelength-routed optical NoCs: design and EDA — state of the art and future directions," in *Proc. of DAC*, 2019.

[7] A. Truppel, T.-M. Tseng, D. Bertozzi, J. C. Alves, and U. Schlichtmann, "PSION: combining logical topology and physical layout optimization for wavelength-routed ONoCs," in *Proc. of ISPD*, 2019, pp. 49–56.

[8] M. Li, T.-M. Tseng, D. Bertozzi, M. Tala, and U. Schlichtmann, "CustomTopo: a topology generation method for application-specific wavelength-routed optical NoCs," in *Proc. of ICCAD*, 2018, p. 100.

[9] A. Boos, L. Ramini, U. Schlichtmann, and D. Bertozzi, "PROTON: an automatic place-and-route tool for optical networks-on-chip," in *Proc. of ICCAD*, 2013, pp. 138–145.

[10] Y.-K. Chuang, K.-J. Chen, K.-L. Lin, S.-Y. Fang, B. Li, and U. Schlichtmann, "PlanarONoC: concurrent placement and routing considering crossing minimization for optical networks-on-chip," in *Proc. of DAC*, 2018, p. 151.

[11] M. Hanan, "On steiner's problem with rectilinear distance," *SIAM Journal on Applied Mathematics*, vol. 14, no. 2, pp. 255–265, 1966.

[12] A. M. de Lima and R. Carmo, "Exact algorithms for the graph coloring problem," *Revista de Informática Teórica e Aplicada*, vol. 25, no. 4, pp. 57–73, 2018.

[13] D. Ding, Y. Zhang, H. Huang, R. T. Chen, and D. Z. Pan, "O-Router: an optical routing framework for low power on-chip silicon nano-photonic integration," in *Proc. of DAC*, 2009, pp. 264–269.

[14] *Gurobi optimizer reference manual*, Gurobi Optimization, Inc., 2018. [Online]. Available: http://www.gurobi.com