EUV and E-Beam Manufacturability: Challenges and Solutions*

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ABSTRACT

As process nodes continue to shrink, the semiconductor industry faces severe manufacturing challenges. Two most expected technologies may push the limits of next-generation lithography: extreme ultraviolet lithography (EUVL) and electron beam lithography (EBL). EUVL works by emitting intense beams of ultraviolet light that are reflected from a reflective mask into a resist for nanofabrication, while EBL scans focused beams of electrons to directly draw high-resolution feature patterns on a resist without employing any mask. Each of the two technologies encounters unique design challenges and requires solutions for a breakthrough. In this paper, we focus on the design-for-manufacturability issues for EUVL and EBL. We investigate the most critical design challenges of the two technologies, flare and shadowing effects for EUVL, and heating, stitching, fogging, and proximity effects for EBL. Preliminary solutions for these effects are explored, which can contribute to the continuing scaling of the CMOS technology. Finally, we provide future research directions for these key effects.

Categories and Subject Descriptors

B.7.2 [**Integrated Circuits**]: Design Aids

General Terms

Algorithms, Design, Performance

Keywords

Extreme ultraviolet lithography, electron beam lithography, physical design, design for manufacturability, flare effect, shadowing effect, heating effect, stitching effect, proximity effect, fogging effect

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1. INTRODUCTION

As reported by the ITRS roadmap that semiconductor process will soon reach sub-10nm technology nodes [2], dramatically increasing design complexity and severe process variation would cause enormous manufacturing challenges. Conventional 193nm immersion lithography is reaching its limit and will not be applicable soon with the rapid shrinking of feature sizes. Multiple patterning lithography is the major technique for current sub-20nm volume production, which uses multiple masks for the exposure process of each device/metal layer. However, more and more masks will be required for finer process nodes, resulting in prohibitively expensive manufacturing cost.

Many next-generation lithography (NGL) technologies have been proposed and are expected to have lower cost and higher resolution to replace conventional optical lithography. Among them, extreme ultraviolet lithography (EUVL) and electron beam lithography (EBL) are the two most expected candidates. EUVL works by emitting intense beams of ultraviolet light to print mask patterns on a silicon wafer (see Figure 1(a) for an illustration). With the wavelength of only 13.5nm, EUVL greatly improves the problem of pattern distortions caused by light diffraction. However, the light is absorbed by most materials, and thus only reflective optics (mirrors) and masks can be used; further, the scanning processing must be performed in a vacuum environment. See Figure 1(b) for the system layout of an ASML NXE:3100 EUVL platform [1]. For the process using clear-field masks, layout patterns on the masks are made by light absorbers, forming the dark regions on a wafer. In contrast, regions not covered by patterns are bright. As a result, the *flare effect* due to the surface roughness of the reflective optical components could reduce the contrast between bright regions and dark ones. In particular, flare is inversely proportional to squared wavelength; the employed small wavelength makes EUVL suffer from high flare level. In addition, the thickness of absorbers and the incident angle of light cause the *shadowing effect*. Both process effects could result in significant critical dimension (CD) distortions or shape variations.

EBL uses focused beams of electrons to directly draw layout patterns on wafers, whose extremely small wavelength and maskless exposure process (thus no more diffraction limitation of light) contribute to its high resolution. See Figure 2 for two different EBL writing strategies. Figure 2(a) shows E-beam direct writing (EBDW) by using a Gaussian-shaped beam to write one pixel at a time, and Figure 2(b) illustrates cell projection (CP) that defines cell patterns on a stencil, and a cell pattern is completely covered by the square beam deflected from the first aperture and thus can be written within an exposure shot. EBL has some critical challenges that need to be resolved before it is ready for high-volume production. For example, high-voltage (say, 100 KeV) beams used for mask fabrication could cause pattern distortions due to the *heating effect*, which

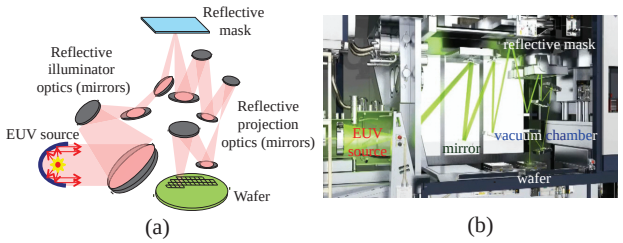

Figure 1: EUVL scanning strategy. (a) Illustration of EUVL technology, with reflective optics (mirrors) and masks. (b) System layout of an ASML NXE:3100 EUVL platform in a vacuum chamber [1].

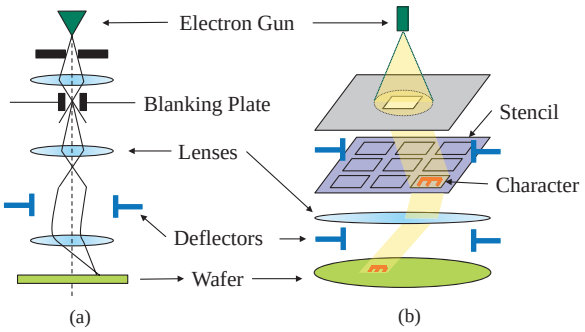

Figure 2: Two different EBL writing strategies. (a) E-beam direct writing (EBDW) uses a Gaussian-shaped beam to write one pixel at a time. (b) Cell projection (CP) defines many cell patterns on a stencil, and a cell pattern is completely covered by the square beam deflected from the first aperture and thus can be written within an exposure shot.

would further deteriorate its unfavorable low throughput. For high-volume manufacturing, a pattern may be written by more than one beam because of the *stitching effect*, suffering from the overlay error among different beams. Furthermore, the scattering and re-scattering of electrons in resist and substrate respectively could cause undesired influence in the regions close to those exposed by the electron beams, respectively called the *proximity effect* and the *fogging effect*, and both make the control of CD uniformity harder.

The rest of this paper is organized as follows: Section 2 and Section 3 respectively explain the process effects and the process-induced design challenges of the two lithography technologies, and existing design techniques for these challenges are introduced. Section 4 gives some future research directions in design for manufacturability related to these two technologies. Finally, Section 5 concludes this paper.

2. EUVL DESIGN CHALLENGES AND SOLUTIONS

EUVL is the most invested NGL technology. In addition to process difficulties such as light source and resist selection, some process effects also pose challenges in the design stage. We explain the flare effect and the shadowing effect in the following subsections, together with the design strategies addressing these effects.

2.1 Flare Effect

Flare is the undesired scatter light due to the surface roughness of the reflective optical components and masks used in

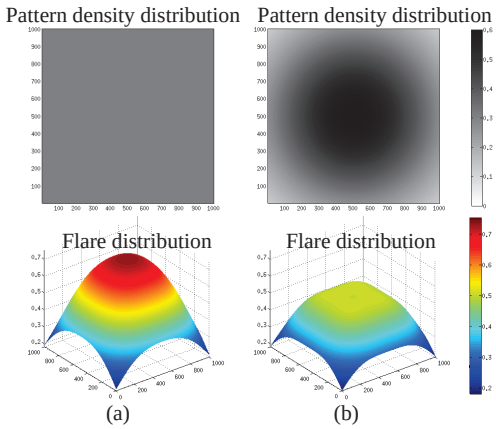

Figure 3: Flare distribution of layouts with different density distributions [10]. (a) A layout with uniform density distribution has large flare variation due to the flare periphery effect. (b) A layout with the density distribution conforming to the global flare distribution has smaller flare variation.

EUVL. Because flare is inversely proportional to squared wavelength and the wavelength of the light used in EUVL is only 13.5 nm, EUVL suffers from rather high flare level. In addition, the non-uniformity of pattern distribution and the flare periphery effect (the central region of a chip receives much more flare than the peripheral region) result in large flare variation across a chip. Both the high flare and variation can damage the control of CD uniformity [10].

Dummification (dummy fill) is one of flare mitigation strategies that has the ability to simultaneously reduce flare level and variation, which could greatly simplify the global CD resizing process [19, 30]. Existing dummification algorithms designed for Chemical Mechanical Polishing (CMP), whose objective is to achieve maximum pattern density uniformity, are not suitable for EUV flare mitigation [6, 7, 8, 9, 39]. As illustrated in Figure 3(a) from [10], a uniform pattern density distribution still incurs large flare variation. In contrast, a layout with density distribution conforming to the global flare distribution has smaller flare variation, as shown in Figure 3(b).

Fang and Chang proposed the first dummification flow for flare mitigation [10]. They used a quasi-inverse lithography technique to generate a dummy demand map indicating the amount of dummies required by each sub-region for flare compensation. Then, the dummy demand map guides a top-down dummy value assignment process using linear programming formulations. However, dummification only considering flare could seriously deteriorate metal thickness uniformity after the CMP process.

Liu et al. [20] then proposed dummification algorithms simultaneously considering flare variation minimization and CMP control. They first approximated the optimal density distribution that minimizes flare level and variation under specified density constraints. The sigmoid function is used to generate density demand maps, whose parameters are adjusted according to chip areas and the flare point spread function. With the generated demand map as an initial solution, a gradient search method is then applied to further minimize density variation and density gradient while keeping flare deterioration small.

To consider metal density distribution at the design stage, Liu and Chang [21] proposed the first work of simultaneous EUV flare- and CMP-aware placement. An expected metal density map is first constructed by considering flare mitigation and density uniformity. A metal-aware pin model is also

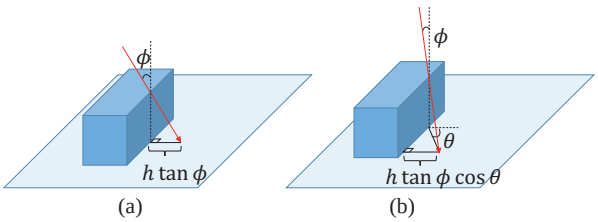

Figure 4: The shadowing effect due to the oblique incident ray. (a) and (b) respectively illustrate that the angles formed by the projection of the incident ray and the normal of a pattern edge are zero and non-zero.

developed to obtain a better trade-off between efficiency and accuracy of metal density estimation. Then the expected metal density map and the density estimation model are incorporated into a non-linear analytical global placer to simultaneously optimize wirelength, flare distribution, and density uniformity. After that, flare- and CMP-aware legalization and detailed placement algorithms are applied to further optimize these objectives.

2.2 Shadowing Effect

The incident light in EUVL has an angle (usually 6°) relative to the axis perpendicular to the mask plane. Consequently, the oblique illumination and absorber thickness result in shadows around patterns represented by the absorber shapes, making patterns wider during an exposure process [33]. As illustrated in Figure 4, as the incident ray is perpendicular to the pattern edge, the shadow width is computed by $h \tan \phi$, where ϕ is the incident angle with respect to the z-axis, as shown in Figure 4(a). As the angle formed by the projection of the incident chief ray and the normal of a pattern edge θ is non-zero, the shadow width becomes $h \tan \phi \cos \theta$, as shown in Figure 4(b). Pattern distortion due to the shadowing effect depends on not only pattern shapes but also pattern locations.

To compensate the shadowing effect, rule-based optical proximity correction (OPC) techniques were first proposed. Yoo et al. proposed to use a sloped-wall absorber stack to fix the shadowing effect; however, the oblique incident light still generates shadows [40]. Schmoeller et al. and Kang et al. found that the amount of pattern shift is almost linearly proportional to the amount of mask defocus, which implies that introducing mask defocus can reduce the pattern shift due to the shadowing effect [14, 31]. In addition, Lorusso et al. and Myers et al. adopted correction CD biases for shadowing compensation [23, 25]. Because a pattern could have varying shadows with the angle θ, as illustrated in Figure 4(b), CD biases are computed and applied according to pattern positions.

Although the rule-based OPC approaches are efficient, shadow widths cannot be simply estimated by the absorber height and pattern positions for nanofabrication. The complex interaction among incident electric fields, three-dimensional absorbers, and multi-layer topography makes the required corrections depend not only on pattern positions but also on pattern sizes, pitches, and types. Figure 5 shows the image contrast loss due to mask-side non-telecentricity [32]. It can be observed that horizontal 1-D equal L/S patterns of 30 nm pitch (P30H) suffer from rather high contrast loss compared to P60H. To compensate the shadowing effect in advanced process nodes, therefore, recent studies mainly focus on developing model-based OPC techniques [26, 28, 33]. Different shadowing models and lithography simulators adopted in these model-based OPC flows present a trade-off between runtime efficiency and correction effectiveness.

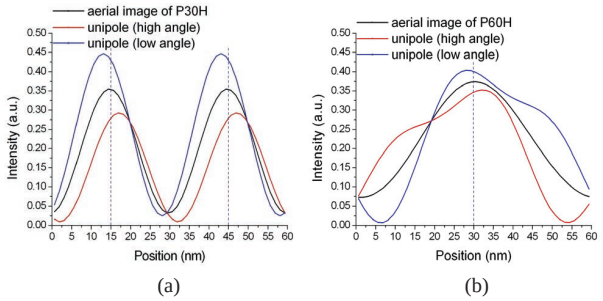

Figure 5: Image contrast loss due to non-telecentricity at the mask side is more serious in dense patterns (from the presentation slides of [32]).

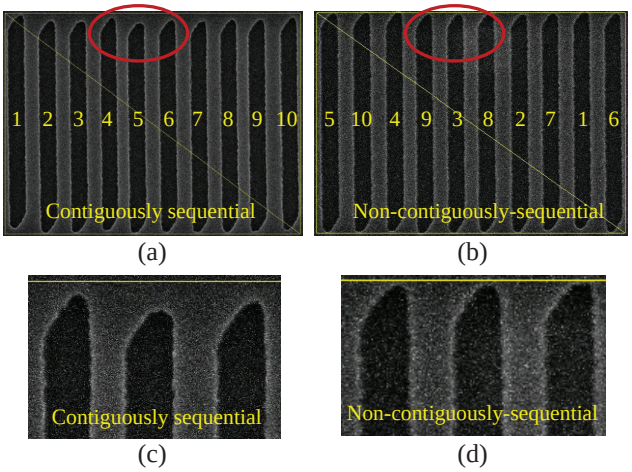

Figure 6: SEM images of 1-D lines with different writing orders [11]. (a)(c) The SEM images with the contiguously sequential writing process. (b)(d) The SEM images with the non-contiguously-sequential writing process. The line-end roughness is much improved.

3. EBL DESIGN CHALLENGES AND SOLUTIONS

EBL is another very promising NGL technology. Since the wavelength of an electron is much smaller than that of a photon, the resolution of EBL is not limited by diffraction. However, many process effects could deteriorate the manufacturability of EBL, such as heating, stitching, fogging, and proximity effects. In the following subsections, we briefly explain each process effect and give existing solutions from the design perspective.

3.1 Heating Effect

Both the dramatic decrease in feature sizes of semiconductor devices and the high-resolution requirement make high-voltage single e-beam lithography systems popular in photomask fabrication. An input layout is first split into subfields and the patterns are written by beam deflection and stage movement. Conventionally, the high-voltage beams write subfields in a contiguously sequential manner, causing considerable amount of heat deposited in a small area and resulting in CD distortion. Figure 6 shows the SEM images of a set of 1-D lines written in the contiguously and non-contiguously sequential orders [11]. Figures 6(c) and (d) reveal that writing layout patterns in a non-contiguously sequential order could mitigate the heating effect and improve line-end roughness.

To solve the heating problem, Babin et al. proposed the concept of subfield scheduling that reorders the writing sequence of subfields to avoid successive writing on close subfields [4]. Consequently, the subfield scheduling problem finds a labeling of subfields, where the minimum distance between two subfields with consecutive labels is maximized. Babin et al. first adopted a well-spaced labeling algorithm proposed by Lagarias [16] to schedule the subfield writing process. The labeling algorithms guarantees that the minimum Manhattan distance between two subfields with consecutive labels is at most one less than the optimal solution. However, since heat is diffused and distributed radiatively, distances among subfields should be measured and optimized using the Euclidean metric. Later, the authors proposed a greedy subfield scheduling algorithm that iteratively improves a randomly generated initial solution by greedily swapping the orders of pairs of subfields [5]. However, the algorithm requires $O(|S|^3)$ time for each swap operation, where $|S|$ is the number of subfileds, and thus the solution quality cannot be much improved within reasonable runtime as the problem size increases.

To tackle these deficiencies, Fang et al. transformed the subfield scheduling problem into a constrained maximum scatter traveling salesman problem (constrained MSTSP) and proposed a graph-based algorithm flow to efficiently find good scheduling solutions [11]. In addition, the authors also considered the problem of blocked subfields; that is, a subfield should not be written if its temperature is higher than a threshold value. In addition, in the case that the moving time of an e-beam writer cannot be ignored compared to the pattern writing time, the total traveling distance should also be minimized. Fang et al. also proposed strategies to achieve a good trade-off between thermal mitigation and throughput maximization [16].

3.2 Stitching Effect

Although single e-beam lithography provides very high resolution and thus suitable for mask fabrication, it cannot be applied to high-volume manufacturing due to its extremely low throughput. Thus, the concept of multiple e-beam lithography (MEBL) was proposed, which simultaneously uses thousands or even millions of beams to greatly improve the throughput. Several MEBL systems have been under development and shown their great promise for practical applications [15, 24, 36].

Due to the parallel writing strategy adopted in MEBL, a layout being exposed should be first split into stripes, as shown in Figure 7(a), and the boundary between two stripes is defined as a stitching line. Therefore, a layout pattern cut by a stitching line will be written by two neighboring beams and thus suffer from the overlay error of the two beams. This overlay error could cause varying degrees of pattern distortion on different patterns. As illustrated in Figure 7(b), a horizontal line cut by the stitching line has acceptable shape variation and thus fine electrical performance. In contrast, vias and vertical lines cut by stitching lines could suffer from severe pattern distortion, incurring large electrical variation or significant yield loss.

Short polygons are another type of stitching line-induced bad patterns due to the data processing flow in EBL, each of which is composed of a short wire segment cut by a stitching line and a landing via. To expose patterns using e-beams, a layout needs to be transformed into a pixel-based black/white bit map. As shown in Figure 8, a gray-level bit map is first constructed according to the pattern coverage in each pixel, and then the gray-level bit map is further transformed into a black/white bit map. The transformation error of a pixel in this dithering process is not neglected but diffused to its neighboring and unprocessed bits. Therefore, irregular pixels could occur at the corner of a short polygon, causing a severe defect with a landing via.

Liu et al. proposed the first work of stitch-aware routing for MEBL [12, 22]. Considering the impacts of the three stitching line-induced bad patterns on manufacturability, the router strictly forbids wires and vias to route and land on stitching lines. To minimize the number of short polygons, stitch-aware routing algorithms are proposed for each routing stage, including global routing, layer and track assignment, and detailed routing.

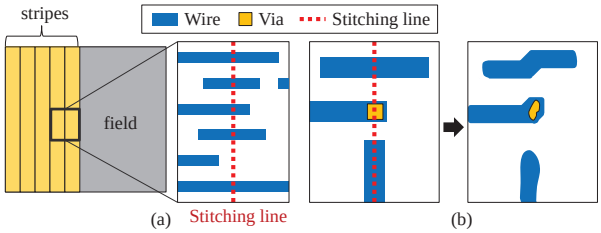

Figure 7: Layout division and overlay error in MEBL [12, 22]. (a) A layout is split into stripes and the stripe boundaries are defined as the stitching lines. (b) Features cut by stitching lines suffer from different degrees of pattern distortion.

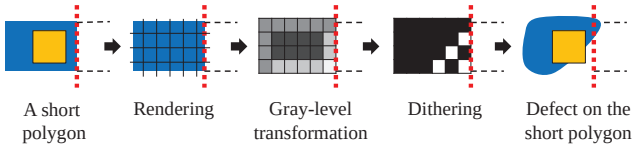

Figure 8: A short polygon occurs due to dithering with error diffusion in the EBL data processing flow [12, 22].

3.3 Proximity and Fogging Effects

The proximity effect is induced from the scattered electrons in the resist and substrate, as illustrated in 9. The scattered electrons expose onto the resist to cause deviations from the nominal pattern size, degrading the CD control and uniformity for fine patterns. The deposited energy distribution can be modeled by the point spread function (PSF) as a double Gaussian expression below [29]:

$$PSF(r) = \frac{1}{\pi(1+\eta)}\left(\frac{1}{\beta_f^2}\exp\left(-\frac{r^2}{\beta_f^2}\right) + \frac{\eta}{\beta_b^2}\exp\left(-\frac{r^2}{\beta_b^2}\right)\right), \quad (1)$$

where r is the distance from the incident point, β_f and β_b the respective forward- and backward-scattering ranges, and η is the ratio of the backward-scattering energy to the forward one. The first term is forward scattering in the resist, and the second the backward one from the substrate. The proximity effect occurs mainly from back scattered electrons and then forward scattered ones. For correctable minimum sizes, β_f is from 0.02 μm to 0.06 μm, β_b is 30 μm, and η is 0.6 for 100 kV electrons in silicon substrate and thin resist film [27].

Fogging refers to the backscattering of secondary electrons (electrons generated as the incident beam electrons collide with the resist or the substrate) that produce undesired exposure over a range of millimeters on the resist, which is typically a long-range effect compared to the short-range proximity effect with only up to tens of micrometers [27]. Both the proximity and fogging effects are affected by pattern dosage and the density and dimensions of layout patterns. For example, with a uniform pattern density, the central region of a chip would suffer from higher proximity and fogging effects, due to the more severe electron scattering in that region.

The proximity and fogging effects can be corrected by using dose correction, shape modification, equalization of background dose, and so on [29]. For correction with layout tech-

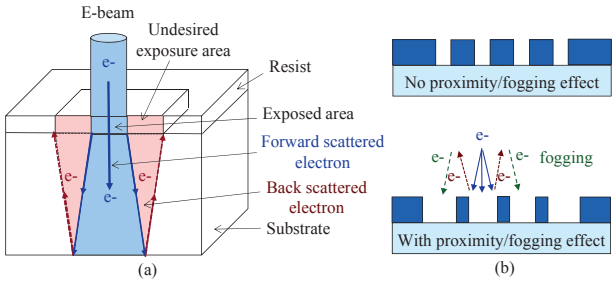

Figure 9: Proximity and fogging effects [29]. (a) Proximity effects with forward and back scattered electrons. (b) Layout distortions with proximity and fogging effects.

niques, Osawa et. al. presented a proximity effect correction algorithm using pattern shape modification and the area density map method [27], and Sundberg et. al. applied patterning techniques to characterize long-range proximity effects (such as fogging) and explored the influence of pattern density on these effects in EBL [34].

4. FUTURE RESEARCH DIRECTIONS

In this section, we provide some research directions of design for manufacturability related to EUVL and EBL.

1. **Flare- and CMP-aware Full-Chip Routing**: Compared to a flare- and CMP-aware placer that estimates the metal densities of sub-regions from a placement result, flare and pattern density distributions are precisely determined in the routing stage. Due to the flare periphery effect, the wire density of the central region should be highest to reduce its flare, which would cause congestion and thus poor routability. Therefore, it is desirable to develop a flare- and CMP-aware router that can better distribute wires density for both flare mitigation and routability enhancement.

2. **Simultaneous Shadowing and Flare Compensation with OPC**: Optical proximity correction (OPC) is one of the most popular compensation techniques both for the flare effect or for the shadowing effect. For the flare effect, OPC corrects the CD of a layout pattern according to the flare value the pattern receives [35, 41]. For the shadowing effect, OPC modifies each layout pattern according to the pattern shape and the pattern location [26, 33]. However, these two effects should be simultaneously considered since they might conflict with each other, reducing OPC efforts. Thus, it is desirable to develop a novel OPC technique that simultaneously considers the flare effect and the shadowing effect.

3. **Subfield Scheduling Considering m-Neighbors**: Fang et al. tackled the subfield scheduling problem by solving MSTSP [11], which maximizes the shortest distance between any pair of successively written subfields. Nevertheless, a good solution to MSTSP could cause very short distance between a pair of m-neighbors. An m-neighbor of a subfield s_i on a writing schedule is a subfield that is at most m subfields away from s_i on this schedule. As illustrated in Figure 10(a), the first and the third subfields are very close 2-neighbors of each other in an MSTSP solution. The writing processes of the two close subfields may significantly raise the temperature of their neighboring regions. Therefore, it is necessary to simultaneously maximize the distances between a subfield and its m-neighbors during subfield scheduling, as an example shown in Figure 10(b).

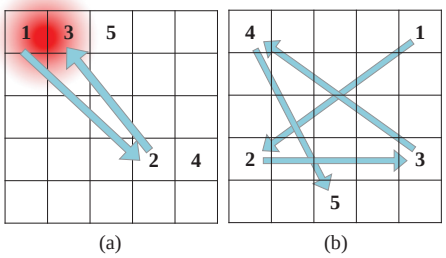

Figure 10: (a) A scheduling solution derived by solving MSTSP. (b) Subfield scheduling considering m-neighbors.

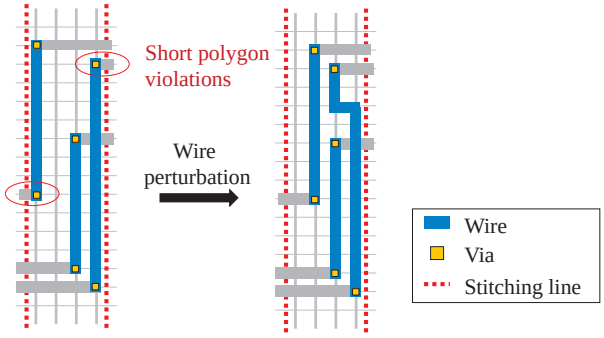

Figure 11: Short polygon violations elimination with wire perturbation.

4. **Stitch-aware Wire Perturbation**: Even if stitch-aware routing introduced in Section 3.2 is applied, violations still occur due to high design complexity and the lack of global optimization in each routing stage. Thus, layout modification is required to eliminate all short polygon violations. In addition, considering these stitching line-induced issues in the routing stage may degrade the quality of original routing objectives such as wirelength and routability, which can be avoided if stitching line-induced bad patterns can be eliminated with global layout modification. Figure 11 shows an example of short polygon elimination with wire perturbation, in which the wires are perturbed between two stitching lines. To improve perturbation flexibility, wires should be able to move across stitching lines to further reduce short polygon violations.

5. **Hybrid Electron Proximity Correction**: To compensate the proximity effect, electron proximity correction (EPC) methods are applied. Two popular correction techniques are dose modification (e.g., pattern-area-density technique) and pattern shape modification. The former adjusts the required dose for each pixel of a layout pattern, and the later modifies the shapes of layout patterns to directly compensate the proximity effect [3, 13, 17, 18, 27, 38]. Both the two techniques increase either data complexity or pattern complexity, degrading the data compression rate or pattern writing efficiency. A hybrid EPC algorithm concurrently adopting the two techniques and maximizing throughput is desirable.

6. **Proximity, Fogging, and CMP Co-optimization**: Layout density uniformity (both density gradient and variation) significantly affects the optimization of the proximity, fogging, and CMP effects. The proximity effect is a short-range (local) effect for up to tens of micrometers, while fogging a long-range (global) one for even millime-

ters, respectively similar to (local) density gradient and (global) density variation on layout uniformity. Consequently, applying layout techniques such as sizing, shaping, perturbation, and dummification, these global effects and local effects can be optimized separately, based on their influential scales. Alternatively, the proximity and fogging effects can also be simultaneously optimized by modeling them as summations of related Gaussian distribution functions.

7. **Data Compression Rate-Aware Routing**: Huge data volume also poses a serious challenge in MEBL. To achieve a throughput of only ten wafers per hour, writing 3.5-nm pixels at two levels (black-white bit maps) even requires a data stream bandwidth of up to 45 Tbit/s [36]. Thus, layout data must be first compressed before being transferred to an MEBL systems. In addition, some critical patterns having high complexity after EPC could deteriorate the data compression rate. Developing a data compression rate-aware router that minimizes the number of those complex patterns could improve the efficiency of the data delivery process.

5. CONCLUSIONS

In this paper, we have introduced some critical process effects and their induced design challenges of EUVL and EBL. Many existing studies have shown their effectiveness in manufacturability enhancement. However, there are still many challenges before the two lithography technologies are ready for mass production, providing much more future research directions in design for manufacturability. In addition to EUVL and EBL, some other NGL technologies such as directed self-assembly (DSA) and the nanoimprint lithography have shown their potentials for sub-10 nm process nodes. Their process effects and manufacturability problems will also open up great research opportunities for future design for manufacturability.

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