- 1. Recall that speedup is defined as T1/T2 where T1 is the execution time before some modification is made and T2 is the execution time after the modification. A certain program contains multiply instructions as well as other types of instructions. The CPI for each instruction in the program is 4. An improvement is made to the multiply instruction such that after the improvement the CPI for the multiply instruction is reduced to 3. The multiply instruction accounts for 22% of the total instructions in the program.
- a) (10) What would be the speedup factor provided for the program by the improvement in the multiply instruction? Express your answer to two decimal places.
- b) (10) If the multiply instruction had a CPI greater than 4 before the improvement, what must have been the CPI for the multiply instruction if a speedup of 1.76 results from reducing the CPI of the multiply instruction to 3? Express your answer to the nearest integer.
- 2. Twenty million instructions from a certain program are executed on a processor with a clock cycle time of 50 pico-seconds. The divide instruction on this machine requires 12 clock cycles and accounts for 10% of the total number of instructions executed in the program. The other 90% of the instructions in the program require an average of 4 clock cycles per instruction.
- a) Complete the following statements:
 - (10) The clock rate for this machine is GHz.
 - (10) The total number of clock cycles consumed by the entire program is . .
- b) (10) Suppose that an improvement is made such that each divide instruction only takes two clock cycles. What speedup factor would this improvement provide for the program? Express your answer in the form dd.dd (i.e. to two decimal places).
- c) (5) What is the minimum number of clock cycles required to execute a single individual instruction on the processor?
- c) (5) What is the maximum speedup that can be obtained for this program by improving only the divide instructions? Express your answer to two decimal places.
- 3. Assume that each of the following instruction types requires the indicated number of clock cycles when executed on a MIPS processor with a 4 GHz clock rate:

		Instruction	Clock cycles required	Consider the following program:		
		addi	4			
		sub	5	prog1:	addi	\$6,\$0,100
		lw	8		addi	\$4,\$0,4000
		SW	6		addi	\$5,\$4,5000
a)	(10) The average CPI rating for this instruction sequence is				lw	\$3,0(\$4)
b)	(10) The native MIPS rating for this instruction sequence is				lw	\$2,0(\$5)
c)	(10) The peak MIPS rating for this machine, assuming these are the only available types of instructions, is				sub	\$3,\$3,\$2
-)					sw	\$3,0(\$5)
					addi	\$5,\$5,4
d)	(10) The total number of clock cycle consumed by the sequence is				SW	\$0,4(\$5)