Computer Science 605.411

Problem Set 9 Name_____

1. A certain system includes 4 Gigabytes ($4*2^{30}$ bytes) of central memory and also employs a 768 Kbyte ($768*2^{10}$ byte) instruction cache each of whose lines can hold 128 instructions.

a) (10) To fetch a single instruction, what is the maximum number of tags that would have to be examined to detect a hit or miss in this instruction cache if it is organized as a fully associative cache?

b) (10) How many bits would be required for the set number if this instruction cache is organized as a 4-way set associative cache?

2. A sequenceof instructions resides in memory beginning at address 0x0244 and is executed on our non-pipelined multi-cycle data-path system that employs an instruction cache (I-cache) that contains 4 lines. Each cache line can hold two instructions. The I-cache is initially empty and employs LRU replacement if needed. The following 19 instruction addresses are referenced in the exact order given while executing the code: 0x244, 0x248, 0x24C, 0x250, 0x254, 0x258, 0x25C,0x260,0x264, 0x268, 0x26C,0x250, 0x254, 0x258, 0x25C,0x260, 0x264, 0x268, 0x26C

a) (10) Assume that the I-cache is direct mapped. For each of the 19 references indicate:
- the block number for the memory block that is referenced
- the cache line that is used or referenced
- whether the reference generates a hit or a miss

b)(10) Assume that the I-cache is 2-way set associative. For each of the 19 references indicate:
- the block number for the memory block that is referenced
- the set to which the reference maps
- the way that is used or accessed within the set
- whether the reference generates a hit or a miss

Lines are loaded into each set sequentially until the set is full (i.e. way0, way1, etc.)

c) (10) Assume that the I-cache is fully associative. For each of the 19 references indicate:
- the block number for the memory block that is referenced
- the cache line used or accessed for the reference
- whether the reference generates a hit or a miss

Lines are sequentially loadedin to the fully associative cache until it is full (i.e. line 0, line1, etc.).

(over)

3. A small four-way set associative data cache(D-cache) employs a line size of 128 bytes and our 3-bit pseudo LRU replacement policy. The cache can hold 4096 bytes of data (not counting the tags, valid, modify, and pseudo LRU bits).

a)(5) How many sets does the cache contain?

b) (20) If the sequence of 32-bit **DECIMAL** memory addresses: 293824, 2948, 41728, 3072, 1920, 5016, 6536, 293764, 4088 and 3184 is referenced in the order listed, fill in the table below to show the corresponding information. The LRU bits are the 3-bit pseudo LRU patterns. Recall that as lines are brought into a set, they are loaded into the next available way within the set. All LRU bits are initially 0.

address	TAG	SET	Way	LRU Bits	Hit/Miss
293824					
2948					
41728					
3072					
1920					
5016					
6536					
293764					
4088					
3184					

c) (5) How many replacements were required?
d) (5) For each replacement, which way was selected by the pseudo LRU bits?
e) (5) Which way was the actual least recently used way for each replacement?

4. A system has a unified cache with a 10ns access time, and a memory with a 120 ns access time.
a) (5) With the cache operating in look-through mode, the effective (i.e. average) access time for reads is 22ns. What would be the corresponding hit ratio for reads?
b) (5) If the cache operates in look-aside mode and has a read hit ratio of 85% and a hit ratio for writes of 78%, what is the corresponding effective (i.e. average) access time for reads?