Computer Science 605.411

Problem Set 7 Name_____

Note: The default behavior of our MIPS 5-stage pipeline is to write registers in the first half of the clock cycle and to read registers in the second half of the clock cycle. In addition, delayed branching is employed and, when necessary, flushing of instructions other than the one in the branch delay slot to cope with control hazards. These conditions apply to ALL problems on this problem set.

1. The two instruction sequences shown below and meant to accomplish the same result. However, the sequence on the left uses conditional move instructions while the one on the right does not:

```
        ori  $14,$0,14
        ori  $12,$0,12
        addi $8,$0,-16
        lui $4,0x8000
        xor $9,$8,$4
        movz $12,$5,$9
        movn $14,$5,$9
```

```
        ori  $14,$0,14
        ori  $12,$0,12
        addi $8,$0,-16
        bltz  $8,minus
        move   $14,$9
        b     done
        nop
minus:
        move   $12,$5
done:
        nop
```

(10) a) How many cycles would be required to execute the instruction sequence on the left on our 5-stage MIPS pipeline using data forwarding, a hazard detection unit, but no branch prediction?

(10) b) How many cycles would be required to execute the instruction sequence on the right on our 5-stage MIPS pipeline using data forwarding, a hazard detection unit, but no branch prediction?

(10) c) What would be the final values left in registers $14 and $12 by the sequence on the left?

(10) d) What would be the final values left in registers $14 and $12 by the sequence on the right?

(over)

2. Assume that a degree-2 superscalar version of our 5-stage pipelined system includes a hazard detection unit but no forwarding unit. "Degree-2" means that each pipeline stage can handle up to 2 instructions at a time. Consider the following instruction sequence:

```
sw      $5,0($8)
lw      $7,0($8)
lw      $8,44($5)
beq     $5,$0,exit
sll     $0,$0,0
```

(10) Identify all potential data hazards within the above instruction sequence on this superscalar system as well as the type for each (i.e. indicate whether it is RAW, WAR or WAW).

3. Twenty independent instructions are to be executed on each of the systems listed below, all of which employ one or more 5-stage pipelines with the same clock period. There are no dependencies and no branches or jumps among the 20 instructions. What **INTEGRAL** (i.e. whole) number of clock cycles would be required to execute the entire sequence of instructions on:

a) (10) a scalar pipeline
b) (10) a superscalar system of degree 3
c) (10) a superpipelined system of degree 3 (i.e. with three clock phases per stage)
d) (10) a superscalar-superpipelined system of degree 3 (i.e. a system with three pipelines each of which is a degree-3 superpipeline)

(over)

4. (10) Suppose that the following instruction sequence executes on our original scalar 5-stage MIPS pipeline system to which the conditions stated in the note at the top of this problem set apply and that employs data forwarding and a hazard detection unit that causes stalls when necessary. "Scalar" means that each pipeline stage can contain at most one instruction at a time.

```
                lui   $8,0x200
                ori   $4,$0,1
                sw    $4,16($8)
loop:           lw    $9,16($8)
                sll   $9,$9,1
                bne   $4,$0,loop
                addi  $4,$4,-1
                nop
                sw    $9,16($8)
                xor   $9,$9,$9
```

Taking into account any looping that might be performed, use the table below to show the contents of each pipeline stage until the xor instruction reaches the write-back stage, or for the first 25 clock cycles, which ever comes first.

Cycle	Fetch	Decode	Execute	Memory	Write-back
1					
2					
3					
4					
5					
6					
7					
8					
9					
10					
11					
12					
13					
14					
15					
16					
17					
18					
19					
20					
21					
22					
23					
24					
25					

(over)