Computer Science 605.411

Problem Set 5 Name_____

1. One of the actions taken to cope with data dependencies within our 5-stage MIPS pipelined machine is to perform register writes within the first half of a clock cycle and to perform register reads in the second half of the clock cycle. Other possible actions include:

- creating pipeline bubbles by stalling dependent instructions
- inserting nop instructions to delay dependent instructions until the result is available
- rearranging instructions to remove the data hazards
- data forwarding operations

Suppose that the instruction sequence shown below is to be executed on our MIPS 5-stage pipelined machine.

```
prog1:   ori   $4,$4,64
         lui   $4,0x00EB
         and   $5,$4,$5
         addi  $5,$0,8
         sw    $5,0($4)
         sll   $5,$5,3
         lw    $6,0($4)
         slt   $7,$6,$5
         sw    $8,4($5)
```

a) (25) Assuming for this problem that the only action taken to cope with data dependencies is to write registers in the first half of the clock cycle and read registers in the second half of the clock cycle. Construct a table, like the one below, to show the instruction in each pipeline stage and the contents of registers $4 through $8 for each clock cycle. Include as many additional rows as needed. The initial contents of $4 through $8 are shown in the table.

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Cycle	Fetch	Decode	Execute	Memory	Writeback	$4	$5	$6	$7	$8
1						4	0x14	0x26	7	0x28
2										

b) (25) What would be the final contents of $4, $5, $6, $7 and $8 if the instruction sequence had been executed on the non-pipelined multi-cycle datapath?

2. The following instruction sequence is to be executed on our 5-stage MIPS pipelined system for which register writes occur in the first half of the clock cycle and register reads occur in the second half of the clock cycle:

```
ori     $12,$0,0xC280
addiu   $12,$12,8
lw      $4,40($12)
slt     $5,$4,$0
sll     $5,$5,2
nop
sw      $5,44($12)
add     $4,$4,$5
lw      $6,44($12)
```

a) (25) How many clock cycles would be required to execute this instruction sequence on our MIPS 5-stage pipelined system if the only other action taken to cope with data dependencies is to stall dependent instructions until they are assured of reading the updated result.

b) (25) If register writes occur in the first half of each cycle and reads occur in the second half, and the only other techniques used are data forwarding and stalls when needed, how many clock cycles would be required?