## Computer Science 605.411

Problem Set 6	
Name	

- 1. a) (10 On our 5-stage MIPS pipeline system, in which stage of the pipeline will a conditional branch instruction reside when the PC is set to the branch target address, if the branch is taken?
- b) (10) In which stage of the pipeline would an unconditional branch or jump reside when the PC is set to the branch or jump target address?
- 2. Suppose that the following instruction sequence executes on our 5-stage MIPS pipeline system that employs data forwarding and a hazard detection unit that causes stalls when necessary. However, on this system, no action is taken for branch or control hazards (i.e. no flushing of the pipeline is performed).

- a) (10) Does the code sequence contain an infinite loop?
- b) (30) If the code does contain an infinite loop, show the contents of each pipeline stage until the bne instruction completes the write-back stage for the second time. Otherwise show the contents of each pipeline stage until all of the instructions have exited the pipeline.
- 3. (20) A "data dependency" is said to exist when an instruction uses as input the contents of a register written by another instruction ahead of it in the pipeline. Iidentify all data dependencies in the instruction sequence listed in problem 2 above. A "dependent instruction" is one that uses as input a register value written by another instruction ahead of it in the pipeline.
- 4. (20) A "data hazard" is said to exist when the result or effect produced by a dependent instruction would be incorrect unless the dependency is resolved. The result or effect is considered incorrect if it would differ from that obtained on the non-pipelined sequential system. Identify all data hazards in the instruction sequence listed in problem 2 above.