Computer Science 605.411

Problem Set 8 Name_____

1. The null terminated character string “Spring 2014” is stored in memory beginning at address 0x100C0004. The first character in the string is “S”, the second is “p”, etc. The null character at the end contains eight 0 bits.

a) (16) Assuming that big endian memory storage order is used, show the hex contents of each of the following locations in this byte addressable memory:

Address	Contents
0x100C004	
0x100C005	
0x100C006	
0x100C00B	

b) (16) Assuming that little endian memory storage order is used, show the hex contents of each of the following locations in this byte addressable memory:

Address	Contents
0x100C004	
0x100C005	
0x100C006	
0x100C00B	

2. (24) The contents of the memory bytes at locations 0x80000 through 0x80003 are as follows:

Address	Contents
0x80000	0xA9
0x80001	0x87
0x80002	0xD5
0x80003	0x43

Show, in hex, the contents of register $t0 produced by each of the instructions listed below assuming first that the byte addressable system employs big endian storage order and then that it employs little endian storage. Register $t1 contains the value 0x80000, **lw** is load word, **lh** is load half word, **lhu** is load half word unsigned, **lb** is load byte, and **lbu** is load byte unsigned.

	Big endian	Little endian
lw $t0,0($t1)		
lhu $t0,2($t1)		
lb $t0,3($t1)		
lbu $t0,0($t1)		
lb $t0,1($t1)		
lh $t0,2($t1)		

(over)

3. A computer system includes an instruction memory whose total size is 128 megabytes (one megabyte = 2^{20} bytes). The memory is organized as a group modules (i.e. chips) each of which has a storage capacity of 134217728 bits. Address registers and the PC (program counter) on this system are 32 bits wide.

The width of a module is defined as the number of data bits that are transferred to or from the module for a single read or write operation. Each module can be thought of as a D×W array of cells. W is the width of each cell and D is the number of cells within the array. Each access (read or write) transfers the contents of one cell. The modules are numbered sequentially starting from 0. The first cell within module 0 would correspond to address 0.

a) (5) How many separate memory modules would be required for this system if W=8 bits (that is, each cell is an 8-bit byte)?

b) (5) What would be the corresponding value for D if W=8?

c) (5) If the system employs high order interleaving, what is the appropriate address format? Show the position and width of each field in this address format.

d) (5) If the system employs low order interleaving, what is the appropriate address format? Show the position and width of each field in this address format.

e) (5) What is the minimum number of lines (i.e. minimum width) required for the address bus on this system if only word-aligned 4-byte accesses are allowed?

f) (5) Would allowing unaligned accesses have any effect of the minimum required address bus width? If so, what would be the effect?

g) (5) What is the module number to which the address 0x00040084 maps, if low order interleaving is used? That is, which module contains the cell with address 0x00040084?

h) (5) What is the module number to which the address 0x00040084 maps, if high order interleaving is used instead of low order interleaving? That is, which module contains the cell with address 0x00040084?

i) (4) If the computer that contains this memory system shares it between two processor cores (i.e. 2 independent processors each of which has the required hardware to issue a memory access at the same time), which would be a better choice for the memory organization: high order interleaving or low order interleaving? Explain your answer.

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