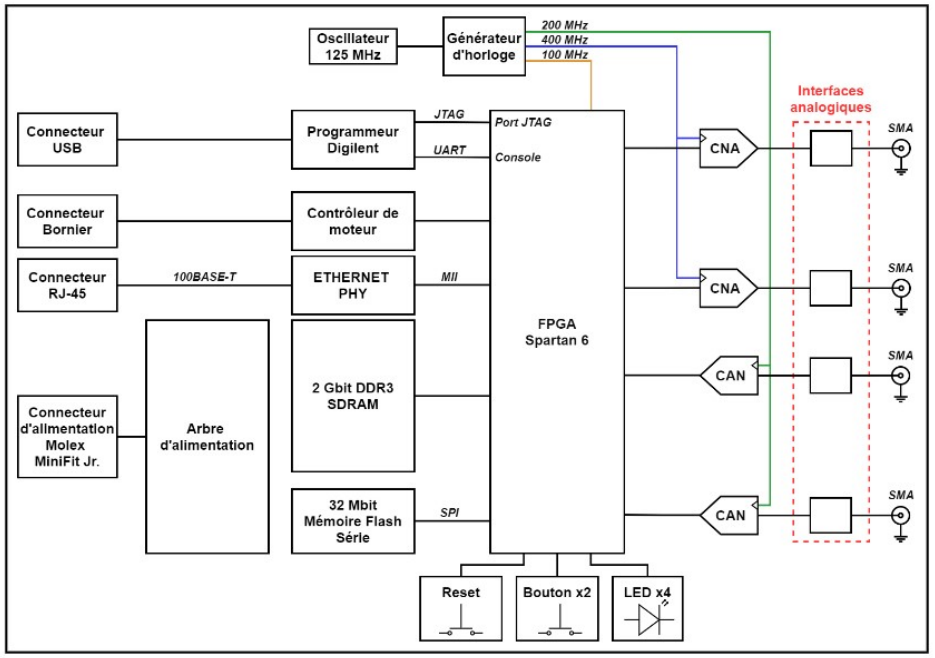
Carte Mère Pléiades

APP1

P07

Revision 1.00

Date : 2025-02-11



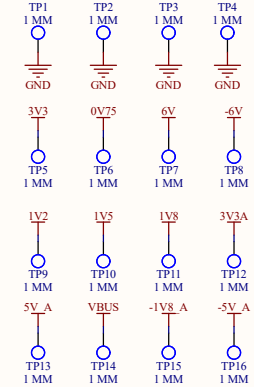
Revision history	
0.00	SCHÉMA DÉPART
1.00	SCHÉMA FINAL 2025-01-10

Package size conversion	
Metric	*Imperial*
1005	0402
1608	0603
2012	0805
3216	1206
3225	1210
6432	2512

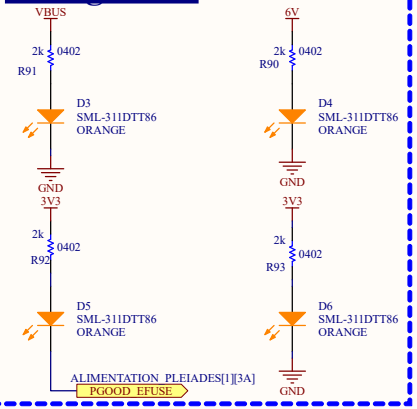
Fiducials

Mounting holes M3

Test points



Debug LEDs



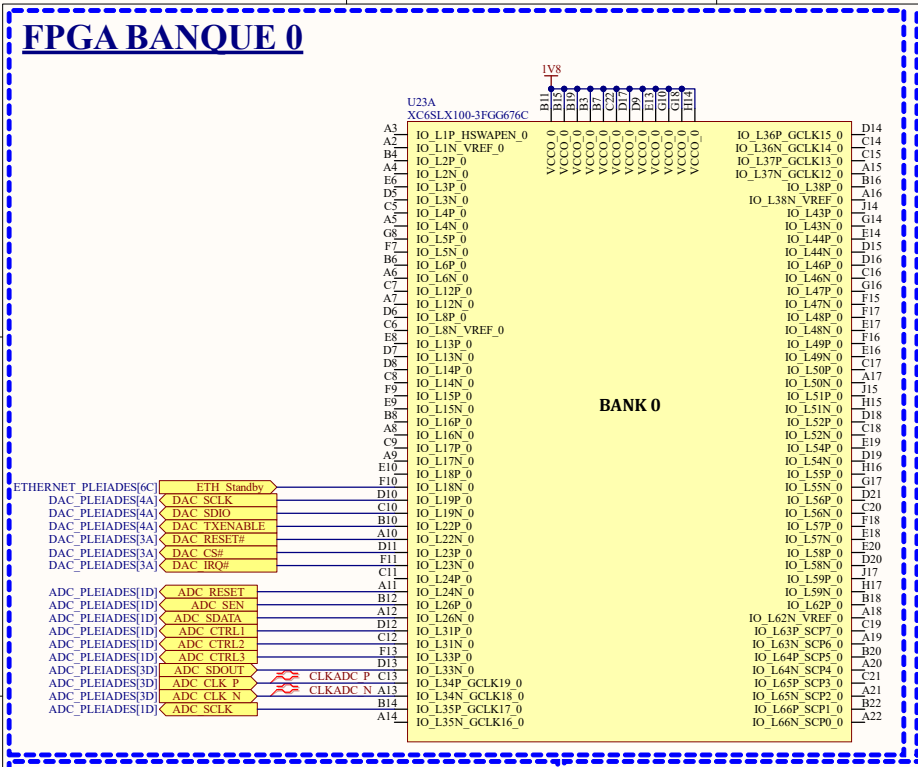
Heat sink

maxiFLOW/superGRIP-Low-Profile
BGA Heat Sink - High Performance

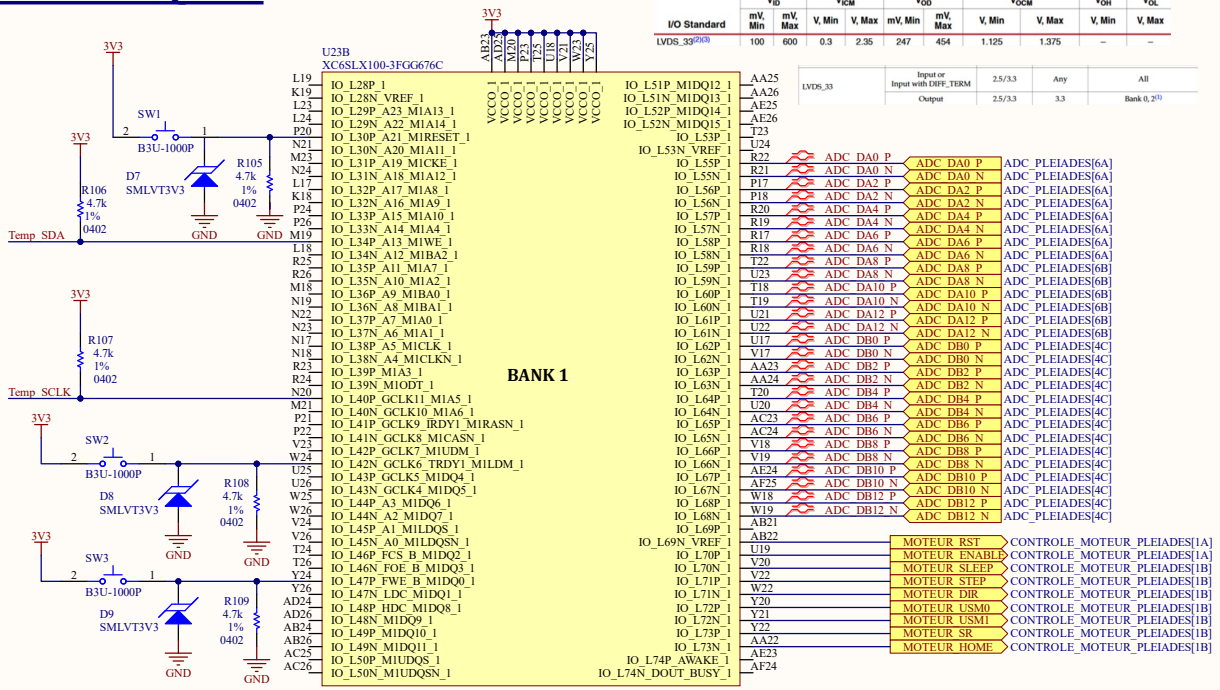
PN: ATS-X51270K-C1-R0
Aucun trou de montage nécessaire

Project Title: **Carte Mère Pléiades**		
Global Project: ***APP1***		
Size: 11x17	Group: P07	Revision: 1.00
Date: 2025-02-11		Sheet: 1 of 12
Filename: PAGE-TITRE_PLEIADES.SchDoc		Designers: François Major, Alexis Juteau, -, -

FPGA BANQUE 0



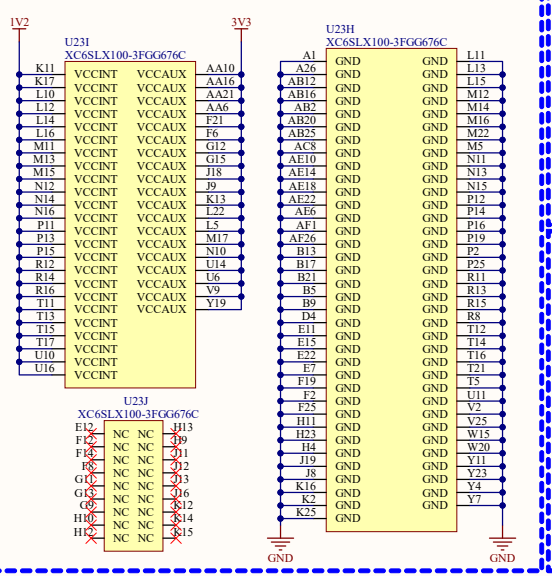
FPGA BANQUE 1



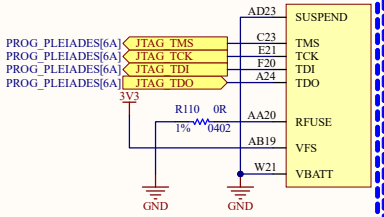
I/O Standard	V_{ID} mV, Min	V_{ID} mV, Max	V_{ICM} V, Min	V_{ICM} V, Max	V_{OD} mV, Min	V_{OD} mV, Max	V_{OCM} V, Min	V_{OCM} V, Max	V_{OH} V, Min	V_{OL} V, Max
LVDS_33[2][3]	100	600	0.3	2.35	247	454	1.125	1.375	–	–

LVDS_33	Input or Input with DIFF_TERM	2.5/3.3	Any	All
	Output	2.5/3.3	3.3	Bank 0, 2[1]

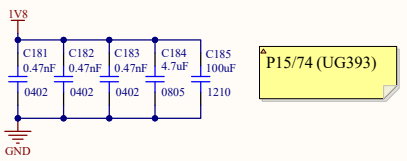
ALIMENTATION FPGA



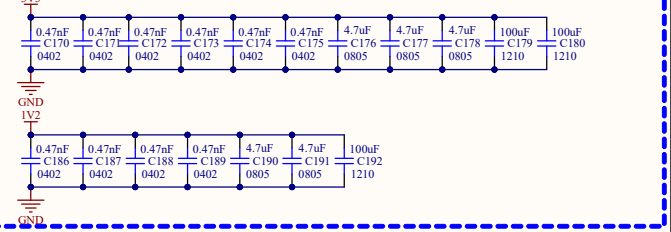
JTAG



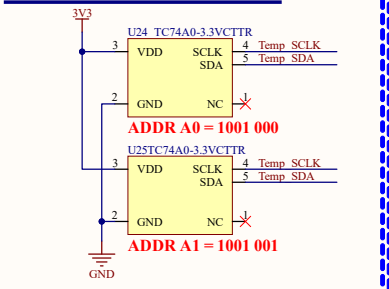
DÉCOUPLAGE BANQUE 0



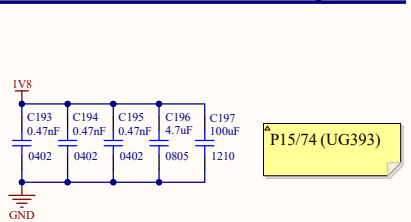
DÉCOUPLAGE ALIMENTATION FPGA



TEMP. SENSORS

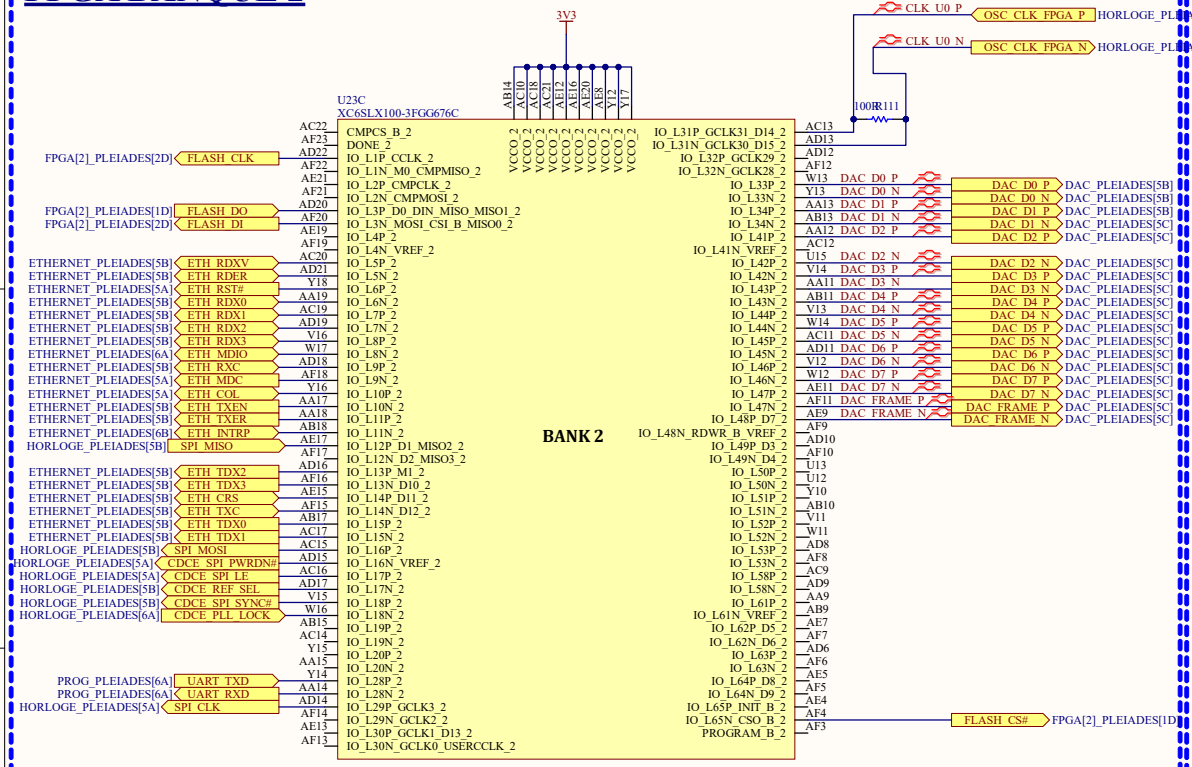


DÉCOUPLAGE BANQUE 1

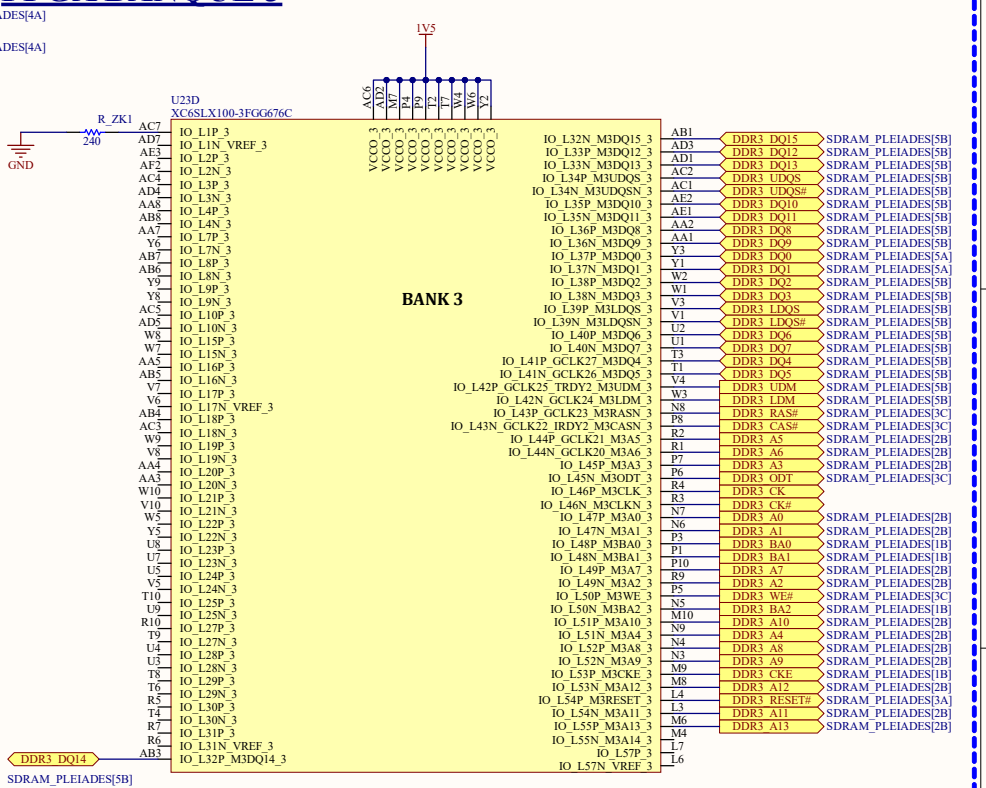


Sheet Name	FPGA[1]_PLEIADES
Project Title	Carte Mère Pléiades
Global Project	*APP1*
Size	11x17
Group	P07
Revision	1.00
Date	2025-02-11
Sheet	2 of 12
Filename	FPGA[1]_PLEIADES.SchDoc
Designers	François Major Alexis Juteau

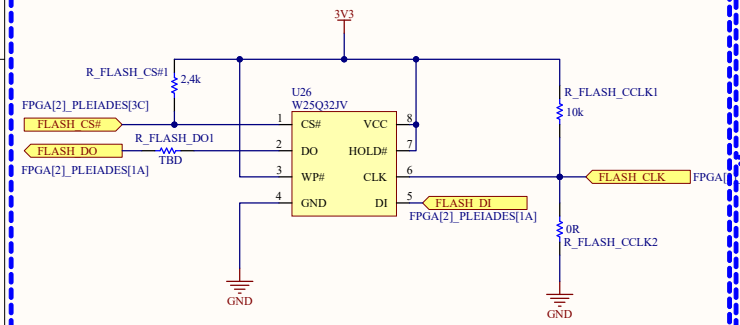
FPGA BANQUE 2



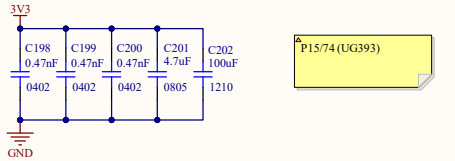
FPGA BANQUE 3



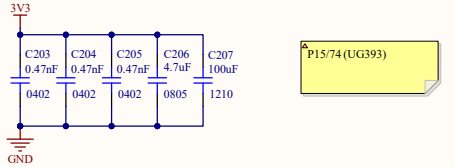
FLASH



DÉCOUPLAGE BANQUE 2

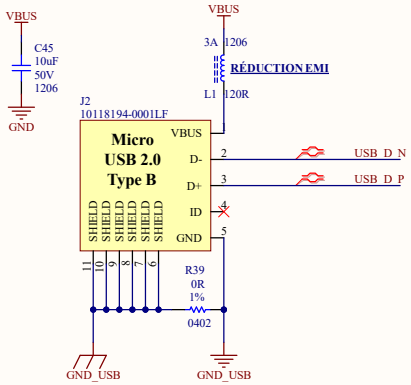


DÉCOUPLAGE BANQUE 3

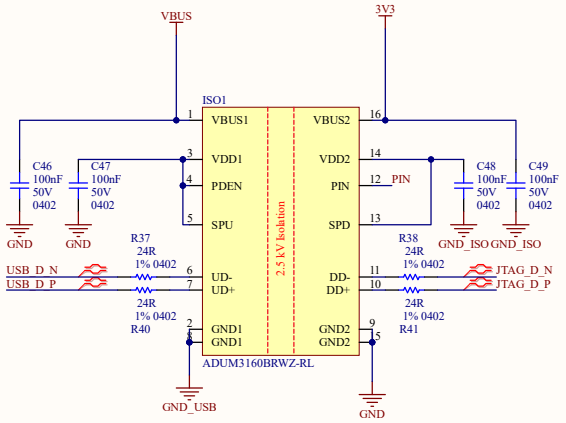


Sheet Name	FPGA[2]_PLEIADES	
Project Title	Carte Mère Pléiades	
Global Project	*APP1*	
Size: 11x17	Group: P07	Revision: 1.00
Date: 2025-02-11	Sheet: 3 of 12	
Filename: FPGA[2]_PLEIADES.SchDoc	Designers: François Major, Alexis Juteau	

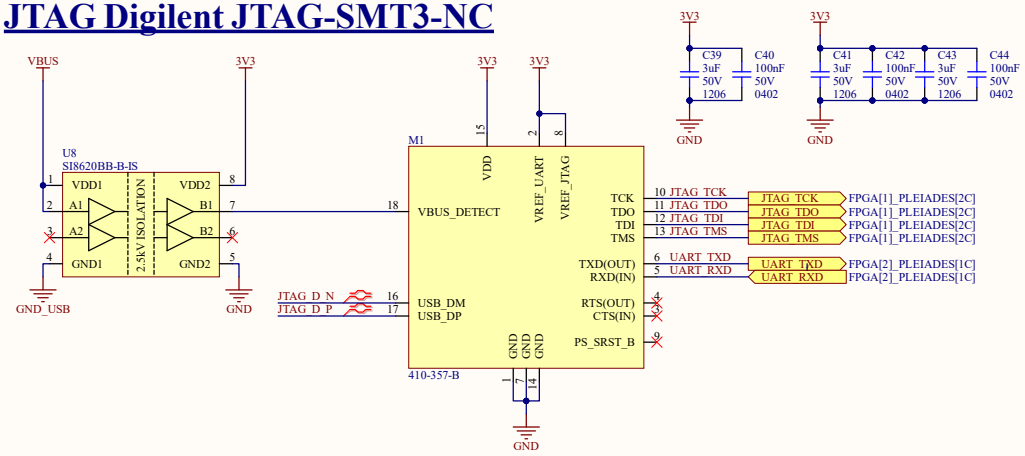
USB



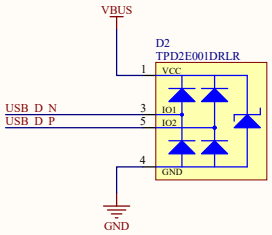
Isolation USB



JTAG Digilent JTAG-SMT3-NC

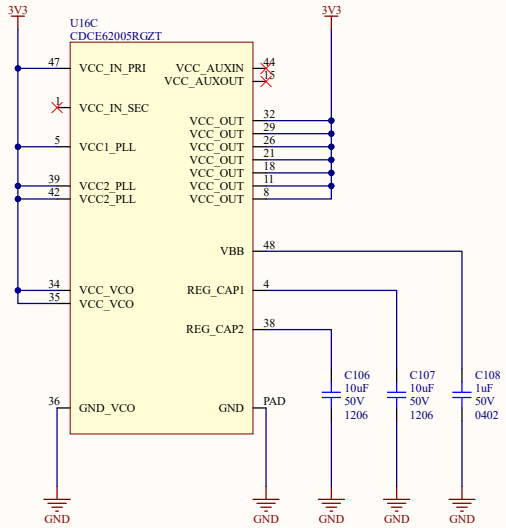


Dual 1.5-pF, 5.5-V, ±8-kV ESD protection diode

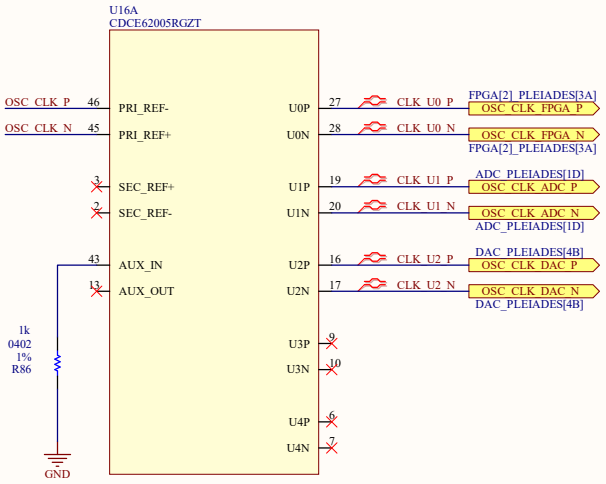


Sheet Name	PROG_PLEIADES	
Project Title	Carte Mère Pléiades	
Global Project	*APP1*	
Size: 11x17	Group: P07	Revision: 1.00
Date: 2025-02-11	Sheet: 4 of 12	
Filename: PROG_PLEIADES.SchDoc	Designers: François Major, Alexis Juteau	

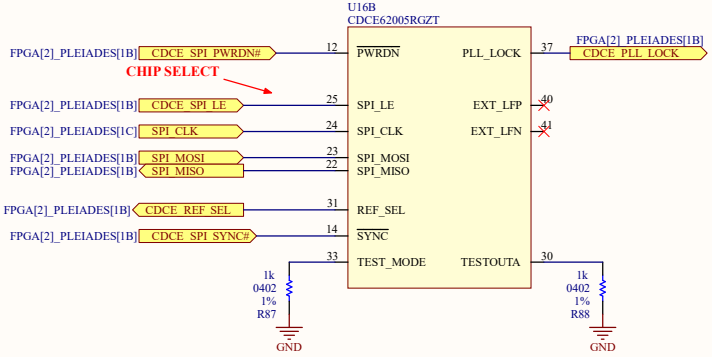
CDCE62005 ALIMENTATION



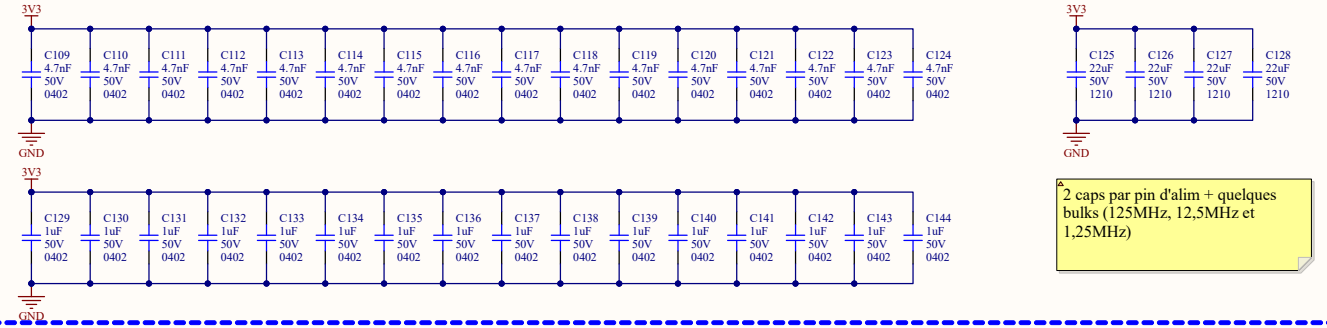
CDCE62005 HORLOGES



CDCE62005 CONTRÔLE

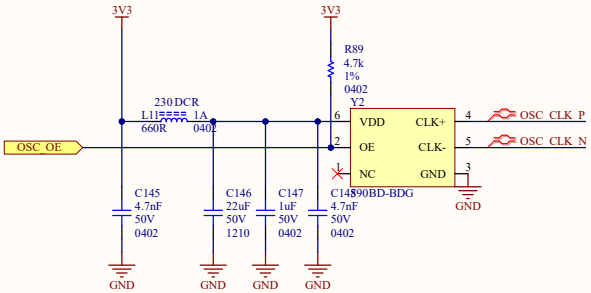


DÉCOUPLAGE PLL



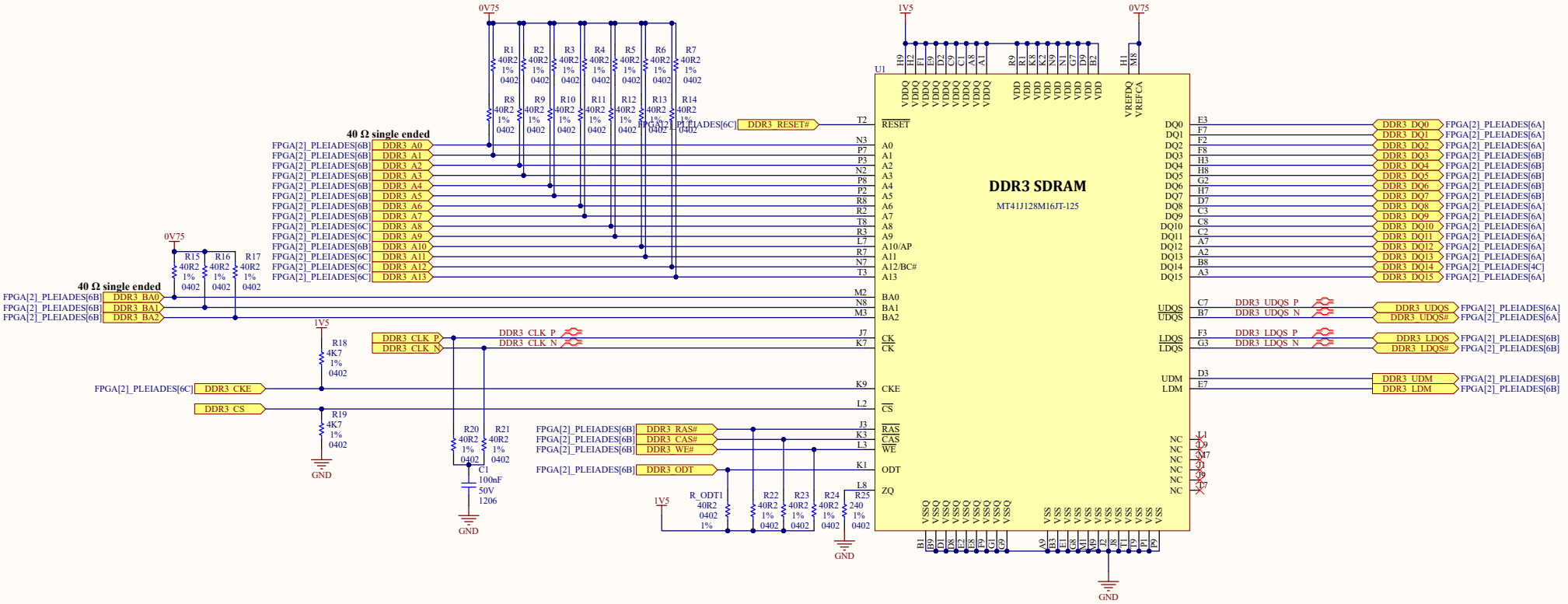
2 caps par pin d'alim + quelques bulks (125MHz, 12,5MHz et 1,25MHz)

OSCILLATEUR 125MHZ

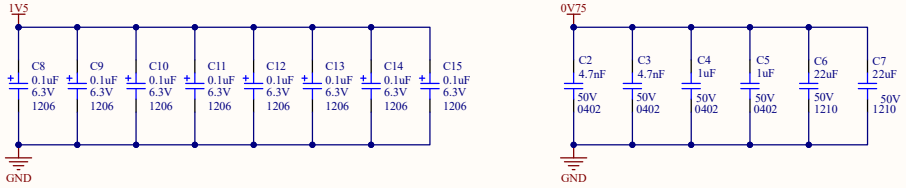


Sheet Name: **HORLOGE_PLEIADES**		
Project Title: **Carte Mère Pléiades**		
Global Project: ***APP1***		
Size: 11x17	Group: P07	Revision: 1.00
Date: 2025-02-11	Sheet: 5 of 12	
Filename: HORLOGE_PLEIADES.SchDoc	Designers: François Major, Alexis Juteau	

DDR3 – 16 Meg x 16 x 8 Banks



DÉCOUPLAGE ALIMENTATION DDR3

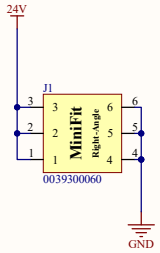


ON DÉCOUPLE À 200MHz, 20MHz ET 2MHz

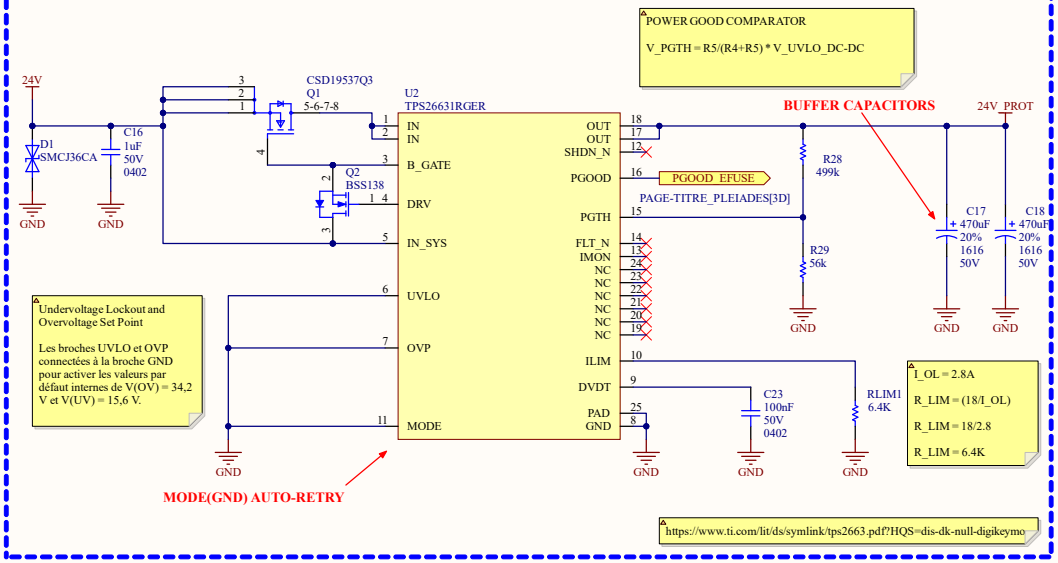
APPLICATION NOTE P(9/27) ET P(14/16)

Sheet Name	SDRAM_PLEIADES
Project Title	Carte Mère Pléiades
Global Project	*APP1*
Size	11x17
Group	P07
Revision	1.00
Date	2025-02-11
Sheet	6 of 12
Filename	SDRAM_PLEIADES.SchDoc
Designers	François Major Alexis Juteau

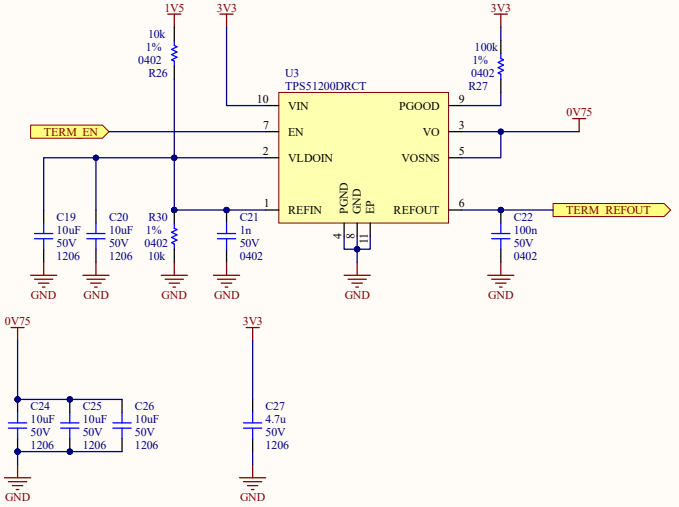
ENTRÉE ALIM



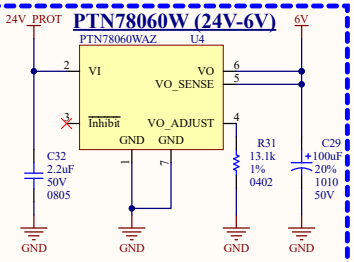
TPS26631RGER - Electronic Fuse Regulator 6A



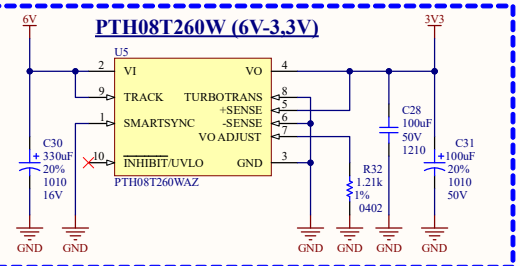
Alimentation terminaison



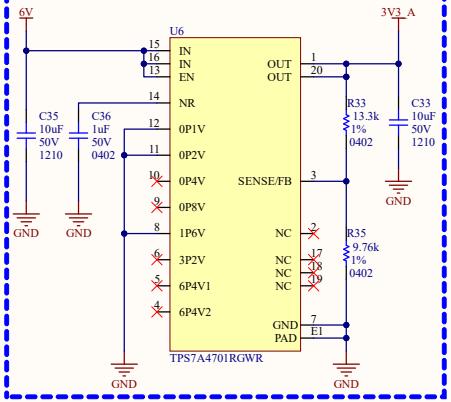
PTN78060W (24V-6V)



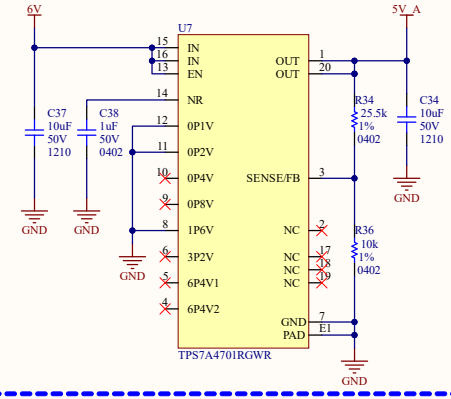
PTH08T260W (6V-3,3V)



TPS7A47 (6V-3,3V LDO)

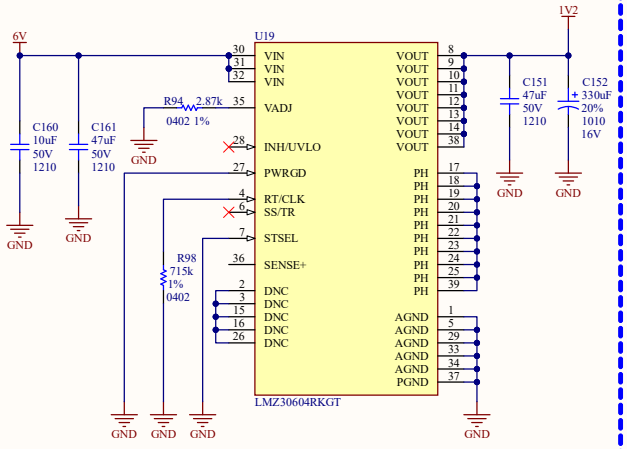


TPS7A47 (6V-5V LDO)

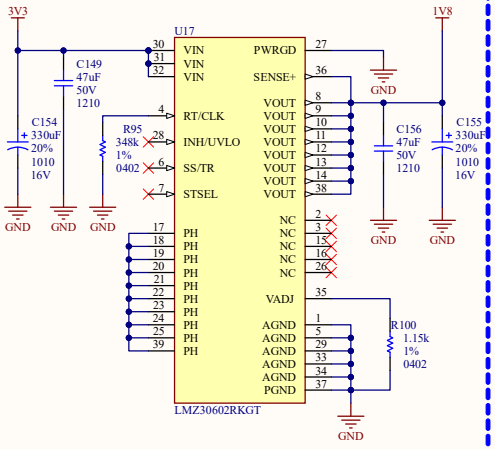


Sheet Name: **Alimentation[1]_PLEIADES**		
Project Title: **Carte Mère Pléiades**		
Global Project: ***APP1***		
Size: 11x17	Group: P07	Revision: 1.00
Date: 2025-02-11	Sheet: 7 of 12	
Filename: ALIMENTATION_PLEIADES[1].SchDoc	Designers: François Major, Alexis Juteau	

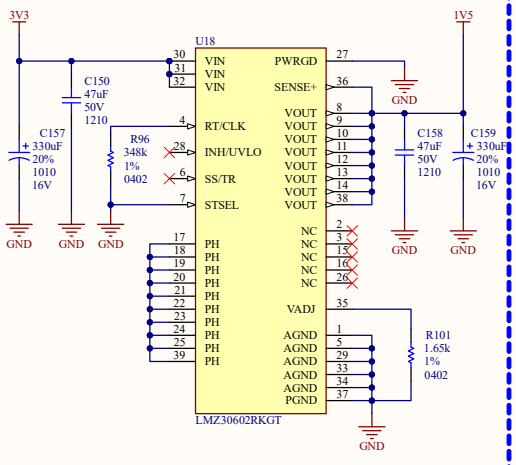
LMZ30604 (3,3V-1,2)



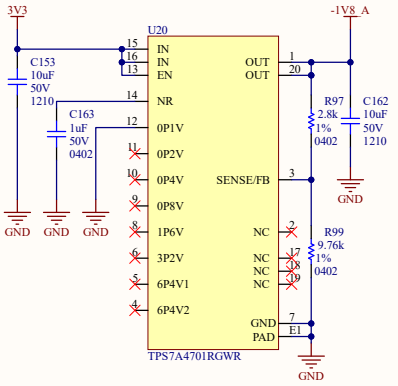
LMZ30602 (3,3V-1,8)



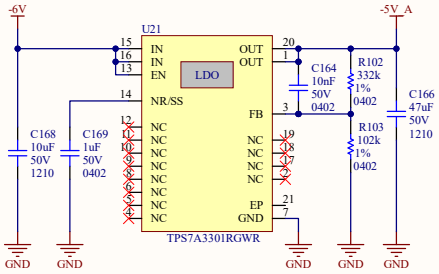
LMZ30602 (3,3V-1,5)



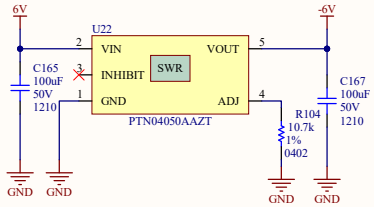
TPS7A47 (3,3V-1,8 LDO)



TPS7A33 (-6V--5V LDO)

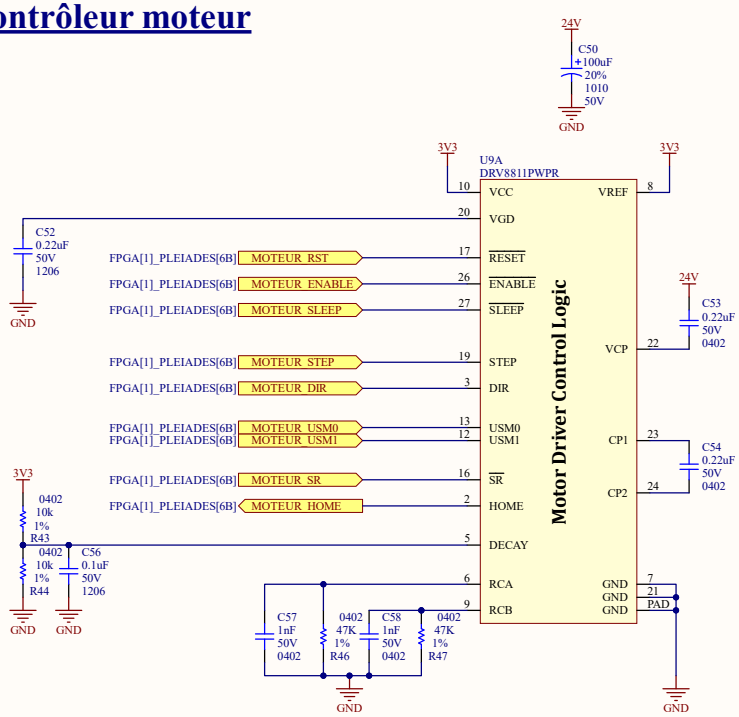


PTN04050A (6V--6V)

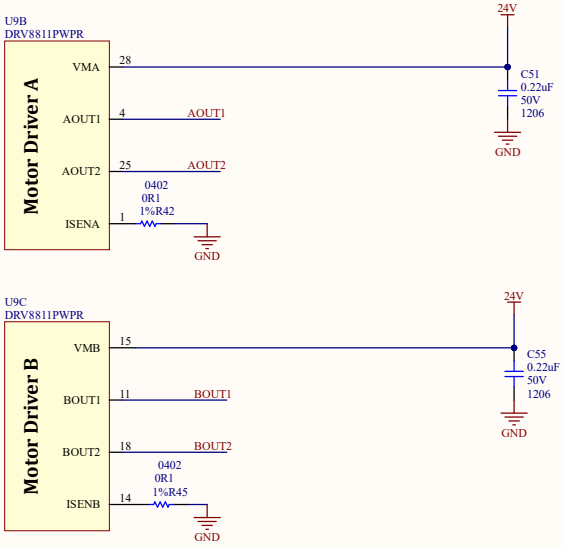


Sheet Name	**Alimentation[2]_PLEIADES**	
Project Title	**Carte Mère Pléiades**	
Global Project	***APP1***	
Size: 11x17	Group: P07	Revision: 1.00
Date: 2025-02-11	Sheet: 8 of 12	
Filename: ALIMENTATION[2]_PLEIADES.SchDoc	Designers: François Major, Alexis Juteau	

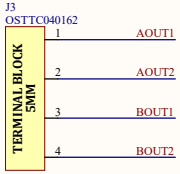
Contrôleur moteur



DRIVES SORTIES

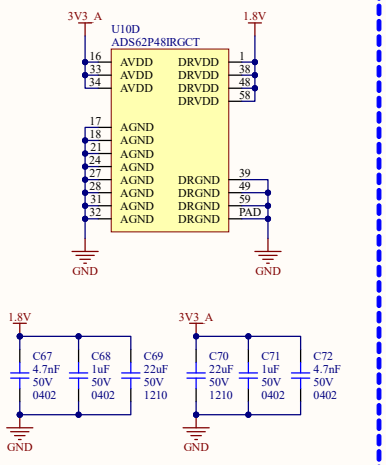


TERMINAL MOTEUR

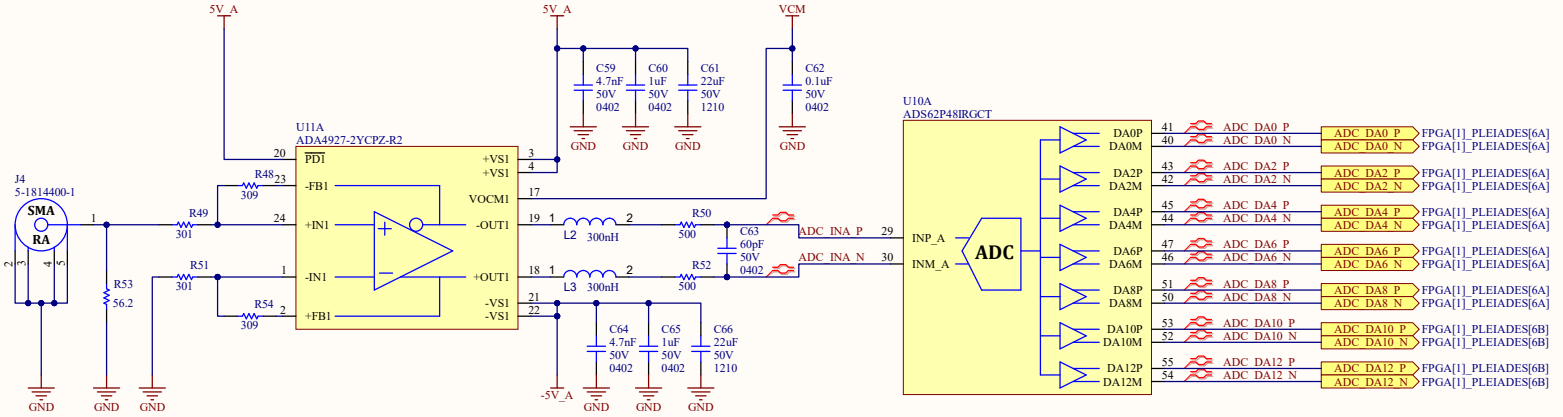


Sheet Name: **CONTROLE_MOTEUR_PLEIADES**		
Project Title: **Carte Mère Pléiades**		
Global Project: ***APP1***		
Size: 11x17	Group: P07	Revision: 1.00
Date: 2025-02-11	Sheet: 9 of 12	
Filename: CONTROLE_MOTEUR_PLEIADES.SchDoc	Designers: François Major, Alexis Juteau	

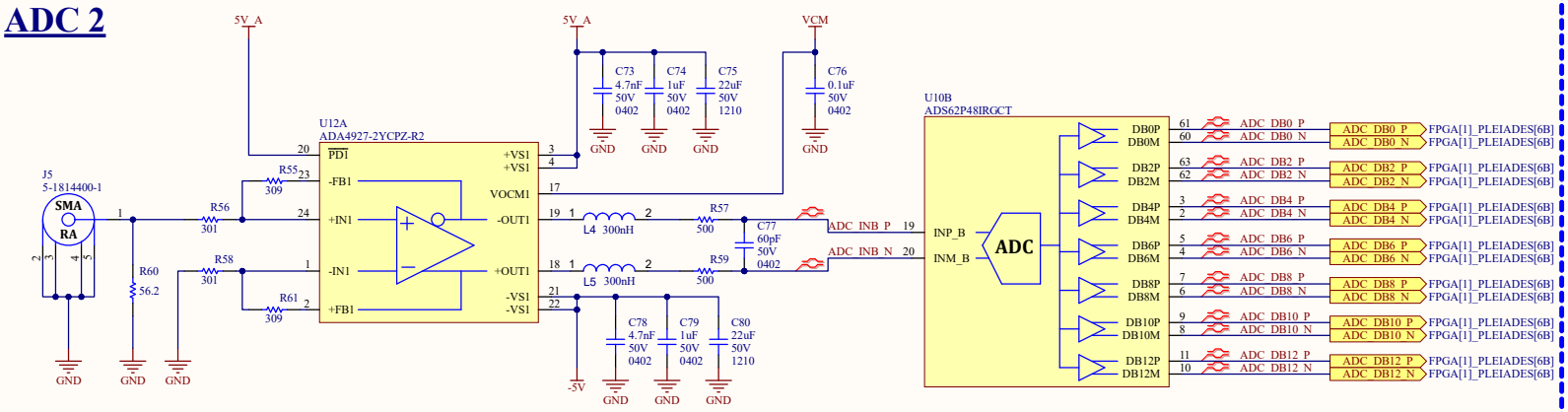
ALIMENTATION ADC



ADC 1



ADC 2



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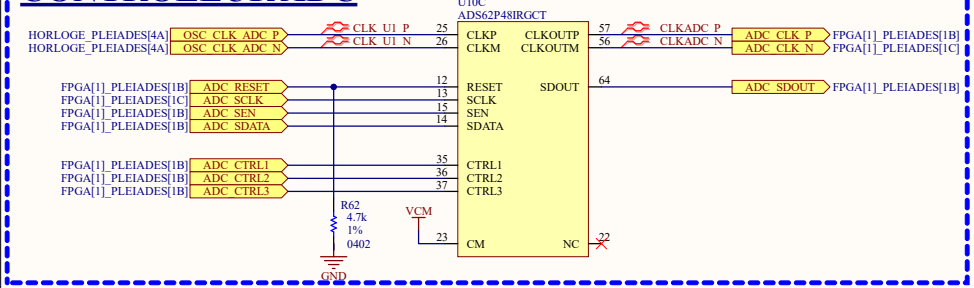

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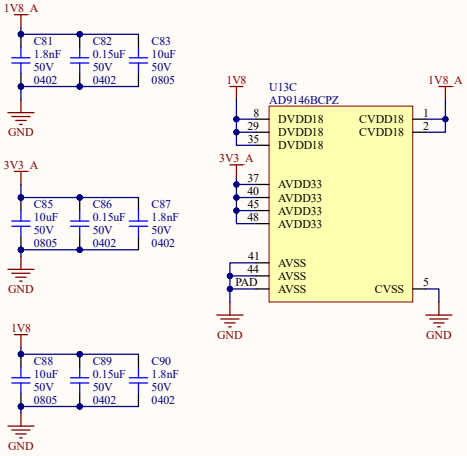
ALIMENTATION DAC



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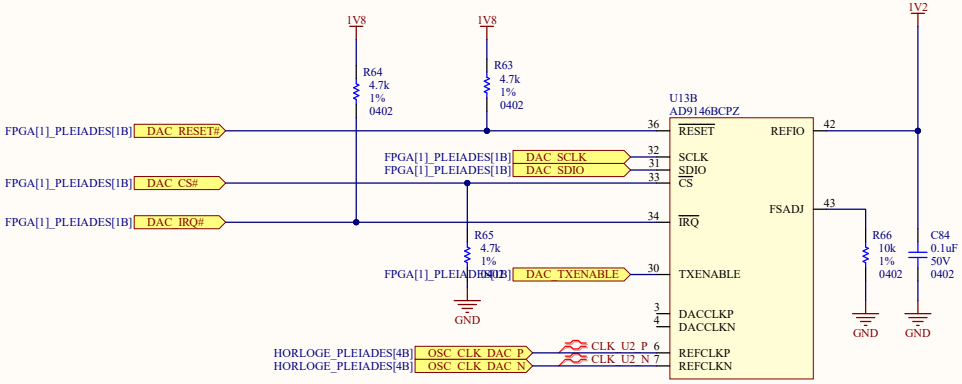

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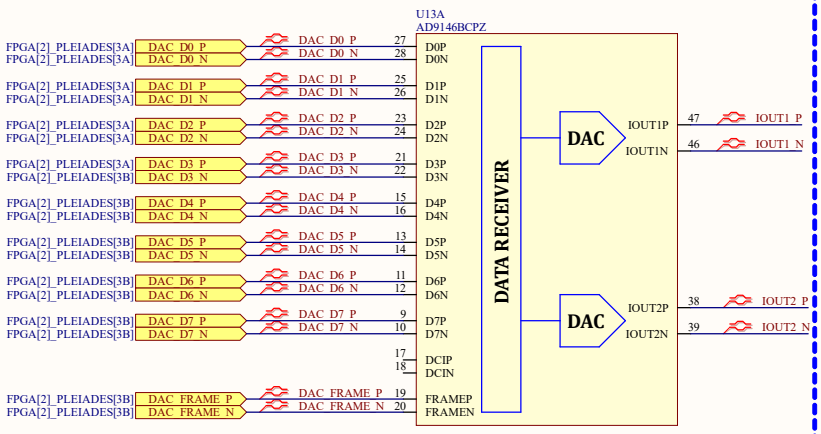

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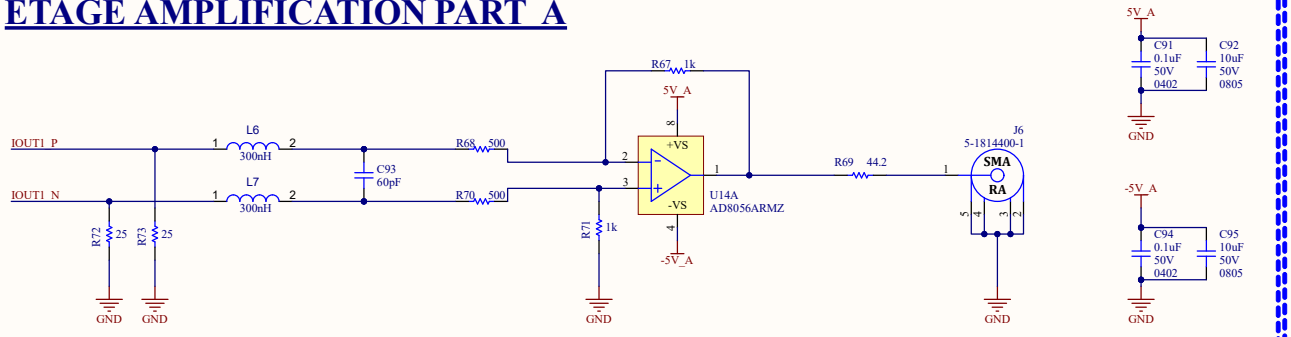

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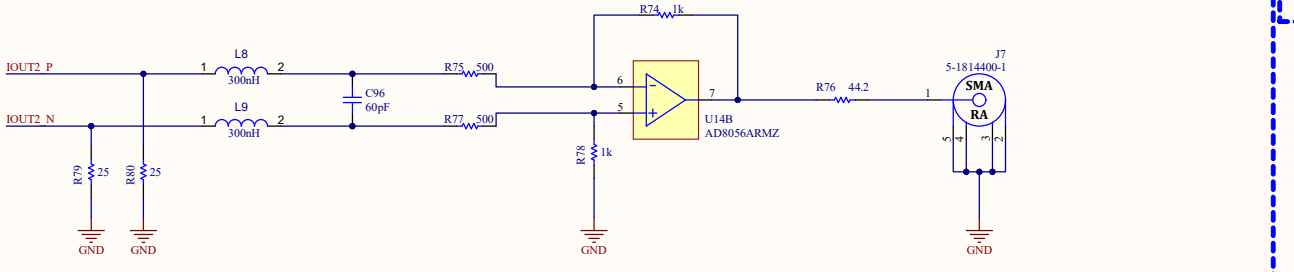

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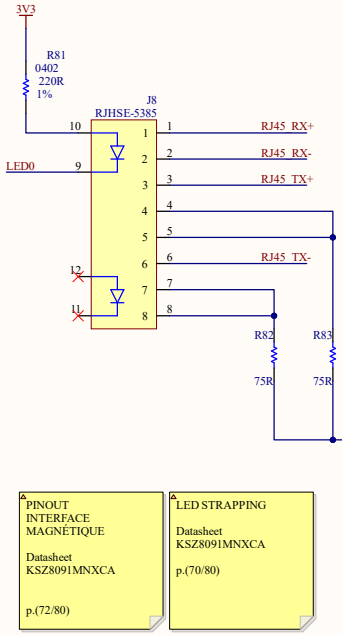
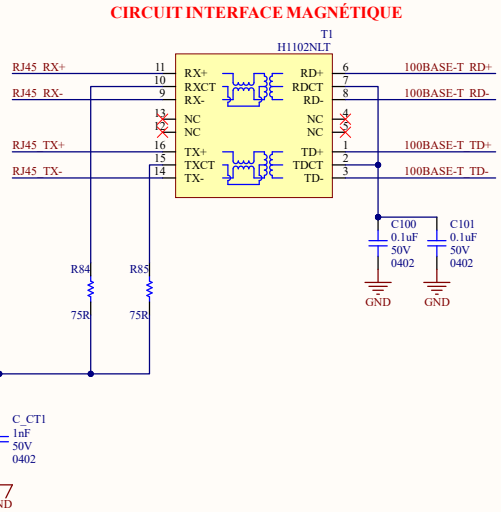
CONNECTEUR RJ-45



ETHERNET TRANSFORMATEURS



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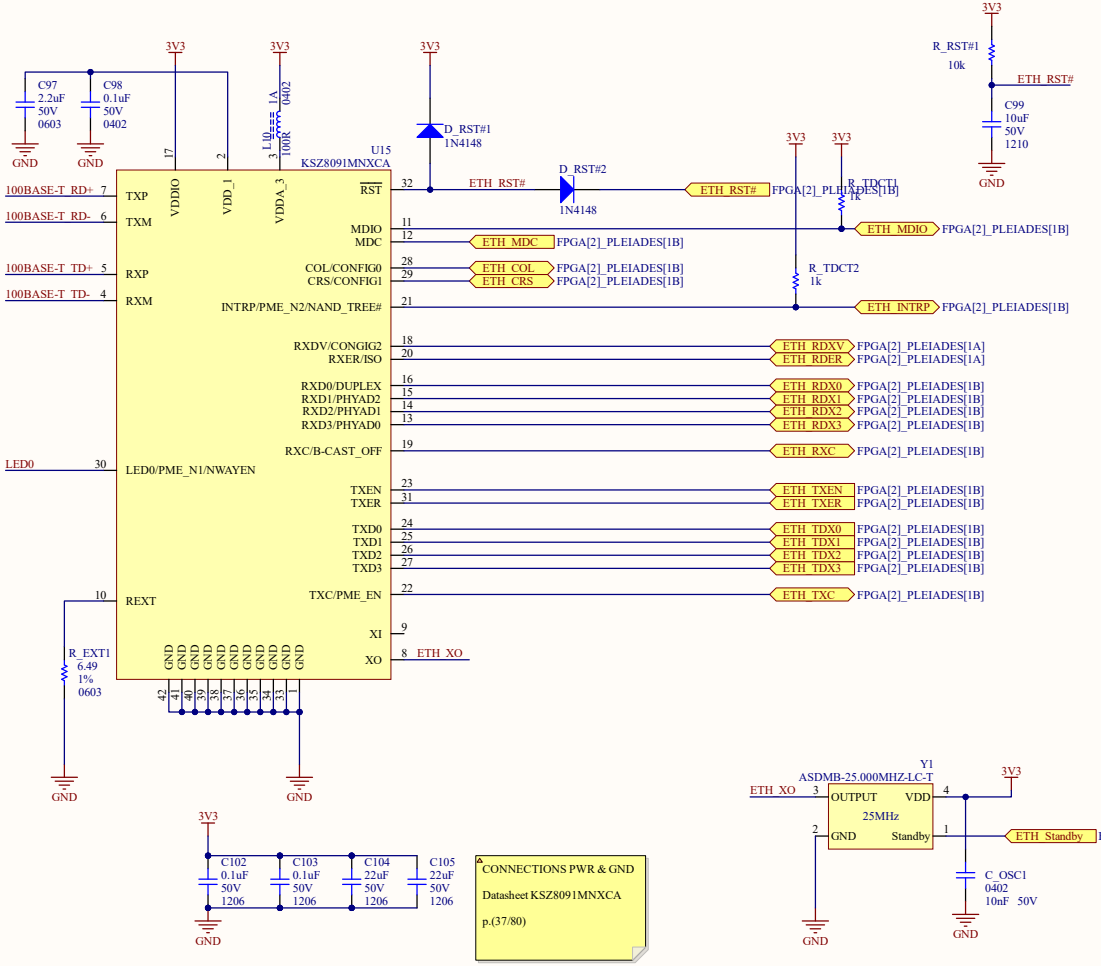

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