Sumanth Umesh

B.Tech in Electrical Engineering
Indian Institute of Technology Jodhpur
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Education

Program/Exam	Year	Institute	GPA/Percentage
B. Tech, Electrical Engineering	2016-2020	Indian Institute of Technology, Jodhpur	9.57/10.0
Senior Secondary (DPUEK)	2014-2016	VVS GJ PU College, Mysuru	96.3%
Secondary (CBSE)	2013-2014	Atomic Energy Central School, Mysuru	10.0/10.0

Work Experience

ASIC Engineer
NVIDIA, Bangalore **[Aug 2021 - Present]**

- Working on microarchitecture and RTL design for datalink layer of PCIe - Gen 6 controller
- Handling synthesis and timing for PCIe - Gen 5 IP

Design Engineer
Silicon Labs, Hyderabad **[Aug 2020 - Aug 2021]**

- Worked on microarchitecture and RTL design of security accelerators (SHA3, Poly1305 and ChaCha20) for low-power wireless SoC
- Handled design quality, synthesis and timing checks for security sub-module
- Wrote firmware for ThreadArch multi-threaded network processor

Internships

Posit Arithmetic
Bosch Corporate Research, Bangalore **[May 2019 - Jul 2019]**

- Designed parameterized and scalable arithmetic modules (adder, subtractor and multiplier) for posit numbers as an alternative to floating point
- Optimized the design to deliver performance comparable to floating point with lower resource utilization on an FPGA

Spintronics and Processing in Memory
Dr Sparsh Mittal | IIT Hyderabad **[May 2018 - Jul 2018]**

- Conducted a comparative study of spintronic-memory based Processing in Memory (PIM) architectures and classified them on the basis of memory device, design and switching mechanisms
- Analyzed STT-RAM, SOT-RAM and Domain Wall Memory based neuromorphic computing architectures and compiled their advantages and disadvantages compared to their SRAM, DRAM and ReRAM counterparts

Publications

Google Scholar

A Survey of Techniques for Intermittent Computing
Umesh S. and Mittal S., *Journal of Systems Architecture* (2020): 101859 {Impact Factor: 3.77}

A Survey on Hardware Accelerators and Optimization Techniques for RNNs
Mittal S. and **Umesh S.**, *Journal of Systems Architecture* (2020): 101839

A Survey of Spintronic Architectures for Processing in Memory and Neural Networks
Umesh S. and Mittal S., *Journal of Systems Architecture* (2019): 349-372

Research and Technical Skills

Research experience:

- Processing-in-memory, intermittent computing, neuromorphic computing
- Device technologies: Spintronic devices
- Computer arithmetic: Posit arithmetic, approximate computing

Programming and tools:

Programming Languages	:	C • C++ • Python • Matlab • C#
HDL	:	Verilog • Systemverilog
Software	:	Synopsys EDA tools (VCS, DC, Spyglass) • Xilinx Vivado

Projects

FPGA Implementation of SHA3 Hash Functions
[Jan 2020 - May 2020]

Dr. Shree Prakash Tiwari | IIT Jodhpur

- Designed area optimized modules for SHA3 hash functions including SHAKE128/SHAKE256 extendable output functions
- Implemented "context saving" to process large size inputs as sequence of smaller blocks with support to pause and resume operations

IEEE-754 Compliant Approximate Multiplier with Tunable Accuracy
[Aug 2019 - Dec 2019]

Dr. Shree Prakash Tiwari | IIT Jodhpur

- Designed fixed point approximate multiplier with tunable accuracy based on rounding and truncation
- Integrated into IEEE-754 float multiplier for floating point support
- Tested resource utilization and accuracy against IEEE float multiplier with Otsu image binarization and Fourier transform as benchmarks

FPGA Implementation of Reed Solomon ECC
[Jan 2019 - May 2019]

Dr. Shree Prakash Tiwari | IIT Jodhpur

- Designed Reed-Solomon encoder and decoder in Verilog and synthesized for Xilinx Virtex FPGA
- Implemented small area inverse cyclotomic Fourier transform for syndrome calculation
- Designed scalable Galois Field arithmetic modules to support differernt primitive polynomial

NETRA - Indoor Navigator for Visually Impaired
[Nov 2018 - Mar 2019]

India Innovation Challenge Design Contest 2018

- Developed a user-friendly and cost effective system to assist the visually impaired in indoor navigation without GPS or internet connectivity
- Demonstrated offline navigation using 9-axis IMU (accelerometer, gyroscope and magnetometer) on Beaglebone Black using dead reckoning

Academic Achievements

- **Awarded institute gold medal for the best all-round performance in the class of 2020, IIT Jodhpur**
- **Awarded institute silver medal for best academic performance in Electrical Engineering, IIT Jodhpur**
- **Team leader of project 'Automated Farm Security System' and reached semi-finals of IICDC 2017 organized by Texas Instruments**
- **Technical head for the project 'NETRA' which reached the semi-finals of IICDC 2018 organized by Texas Instruments**
- **Placed among top 0.6 percentage of 1.2 million candidates in Joint Entrance Examination 2016**
- **Recipient of National Talent Search Examination Scholarship (2014), awarded to only 1000 meritorious high school students in the country**

Coursework (UG)

- Digital and System-on-Chip Design
- Digital VLSI and Design
- Microprocessors and Microcontrollers
- Analog and Interfacing Circuits
- IC Technology
- Computer Programming
- Contemporary Communication Systems
- Digital Signal Processing
- Probability, Statistics and Random Processes
- Complex Analysis and Differential Equations
- Linear Algebra and Calculus