2022 Digital IC Design Homework 2

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Functional Simulation Result					
Stage 1	Pass/Fail	Stage 2	Pass/Fail	Stage 3	Pass/Fail

Stage 1

```
add wave -r sim:/testfixture/*
VSIM 9> run -all
# ----------------------
# -- Simulation Start --
# ----------------------
# --stage1 simulation--
#
# Setting1: PASS
#
# Setting2: PASS
#
# Setting3: PASS
#
# Setting4: PASS
#
# Setting5: PASS
#
# Setting6: PASS
#
# Setting7: PASS
#
# Setting8: PASS
#
# Setting9: PASS
#
# Setting10: PASS
#
```

Stage 2

```
#
# --stage2 simulation--
#
# Setting11: PASS
#
# Setting12: PASS
#
# Setting13: PASS
#
# Setting14: PASS
#
# Setting15: PASS
#
# Setting16: PASS
#
# Setting17: PASS
#
# Setting18: PASS
#
# Setting19: PASS
#
# Setting20: PASS
#
```

Stage 3

```
# --stage3 simulation--
#
# Setting21: PASS
#
# Setting22: PASS
#
# Setting23: PASS
#
# Setting24: PASS
#
# Setting25: PASS
#
# Setting26: PASS
#
# Setting27: PASS
#
# Setting28: PASS
#
# Setting29: PASS
#
# Setting30: PASS
#
# ------------------------------------------------
# --    Simulation finish,  ALL PASS            --
# ------------------------------------------------
# ** Note: $finish    : D:/Downloads/graduate school/Course/first_grade_down/IC/Labs/Lab2/HW2/file/TLS_tb.sv(205)
#    Time: 97650 ns  Iteration: 1  Instance: /testfixture
# 1
```

Description of your design

根據老師上課教的 Controller 起手式 2C1S 來設計其中的 Controller。
Controller 的部分就是根據他的輸入輸出分成 State Reg、Next state logic、Output Logic, 顧名思義第一部分就是用來儲存已經運算好的值，等到 Clk 來的時候再把他傳給 Output Logic 然後再根據訊號傳給 Datapath 運算完之後，再傳給 Next state Logic 如此往復。

Controller:

State Reg: 判斷該情況是要 reset,set,stop,還是 jump,並且給 currentstate 賦值。

Next state Logic: 根據 Datapath 所運算出要不要轉燈號的值來決定 Nextstate 要是什麼情況。

Output Logic: 根據 currentstate 的值來決定 module 的輸出要是甚麼。

Datapath:

Compare: 用來比較有沒有到達轉跳的次數，如果有就把需要轉跳的情形傳給 Counter。

Counter: 判斷該情況是要 reset,set,stop,還是 jump,並且決定當前燈號已經亮了幾次了，是要+1 還是要歸零。

大概就是這兩 Part 只要完成第一部分後面兩部分就一直加一下條件就可以了。