2022 Digital IC Design
Homework 4: Edge-Based Line Average interpolation

NAME	陳柏維
Student ID	P76101283

Simulation Result

Functional simulation	Pass or Fail	Gate-level simulation	Pass or Fail	Clock width	20	Gate-level simulation time	41589329

```
    START!!! Simulation Start .....
----------------------------------------------------------------


------------------------S U M M A R Y--------------------------

    Congratulations!

    Result image data are generated successfully!

    The result is PASS!!!

----------------------------------------------------------------

** Note: $finish    : D:/Downloads/graduate school/Course/first_gra
   Time: 51975 ns  Iteration: 0  Instance: /TB_ELA
```

```
# ----------------------------------------------------------------
#
#
#
# ------------------------S U M M A R Y--------------------------
#
#     Congratulations!
#
#     Result image data are generated successfully!
#
#     The result is PASS!!!
#
# ----------------------------------------------------------------
#
# ** Note: $finish    : D:/Downloads/graduate school/Course/first_grade_
#    Time: 41589329 ps  Iteration: 0  Instance: /TB_ELA
# 1
# Break in Module TB_ELA at D:/Downloads/graduate school/Course/first_gr
```

Synthesis Result

Total logic elements	2423
Total memory bit	0
Embedded multiplier 9-bit element	0

Flow Summary

Flow Status	Successful - Fri May 13 21:32:05 2022
Quartus II 64-Bit Version	13.0.1 Build 232 06/12/2013 SP 1 SJ Web Edition
Revision Name	ELA
Top-level Entity Name	ELA
Family	Cyclone II
Device	EP2C70F896C8
Timing Models	Final
Total logic elements	2,423 / 68,416 (4 %)
Total combinational functions	2,143 / 68,416 (3 %)
Dedicated logic registers	821 / 68,416 (1 %)
Total registers	821
Total pins	39 / 622 (6 %)
Total virtual pins	0
Total memory bits	0 / 1,152,000 (0 %)
Embedded Multiplier 9-bit elements	0 / 300 (0 %)
Total PLLs	0 / 4 (0 %)

Description of your design

就找出它的規律並且分成四個階段

1. Read : 除了第一次的 Row1 要進行特殊處理之外，其他基本上就是把 data_in 的資料儲存起來而已。為了節省空間這邊只用一個 512 大小的暫存器，並且前半後半輪流寫入。
2. Write : 就是把第一步讀取的東西寫入到記憶體中，沒有特別好註解的
3. Calculate : 就是根據第一階段中的兩 Row 值根據題目規則做計算並且存入

一個 256 大小的暫存器中。

4. Write : 把第三階段算出來的東西，直接存入到記憶體中，跟第二階段其實是同個東西 只是做了一點條件判斷。

*Scoring = (Total logic elements + total memory bit + 9*embedded multiplier 9-bit element) × (longest gate-level simulation time in ns)*