2022 Digital IC Design Homework 3

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| **Simulation Result** | | | | | | | |
| Functional simulation | Pass/ Fail (encoder) | | Pass/ Fail (decoder) | Gate-level simulation | Pass/ Fail (encoder) | | Pass/ Fail (decoder) |
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| **Synthesis Result** | | | | **encoder** | | **decoder** | |
| Total logic elements | | | | 475 | | 80 | |
| Total memory bit | | | | 16384 | | 0 | |
| Embedded multiplier 9-bit element | | | | 0 | | 0 | |
| Simulation time img0 | | | | 538590 | | 61590 | |
| Simulation time img1 | | | | 524070 | | 61620 | |
| Simulation time img2 | | | | 399210 | | 61590 | |
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| **Description of your design** | | | | | | | |
| Encoder:  就等到資料讀取完成之後，才開始做計算。主要Stage大概分成4個部分  1.Reading 2.Calculate 3.Output 4.Finish 。  Reading : 又分成一開始的資料讀取跟look-ahead buffer 未滿之前的讀取。  Calculate: 原先是寫一個function但是後來不能合成就把它改成一個clk依 據sliding windows 的方式來偵測有沒有對到。  Output: 就把剛剛算出來的答案做輸出而已。  Finish: 就結束而已。  Decoder:  我認為沒有甚麼stages可言，所以直接用一個sequential block 來輸出每一 個clk所產生的output。並且把提前半個clk來的code\_pos,code\_len,用一個wire存起來，並在clk來的時候，針對剛剛所存的做判斷如果index == code\_len 則輸出 chardata[3:0] 否則 輸出之前的search\_buffer[code\_pos] 並且index ++。 | | | | | | | |

*Scoring = (Total logic elements + total memory bit + 9\*embedded multiplier 9-bit element)*