Hsin-Tang Cheng

Taipei, Taiwan | kevincheng60303@gmail.com | +886 905 256 628 | yourwebsite.com
linkedin.com/in/hsintangcheng | github.com/dodochicha

Education

National Taiwan University (NTU) Taipei, Taiwan
B.S. in Electrical Engineering Sep. 2021 – Jun. 2025

National Taiwan University (NTU) Taipei, Taiwan
M.S. in Integrated Circuit Design and Automation, EDA Group Sep. 2025 – Present
- Advisor: Prof. Hui-Ru Jiang

Coursework

Digital System Design, DSP in VLSI, Computer-Aided VLSI System Design, Digital Communication Integrated Circuits Design,Physical Design for Nanometer ICs, Logic Synthesis and Verification, Parallel Programming, Machine Learning

Experience

Analog CAD Engineer Intern, Silicon Motion – Taipei, Taiwan Jul. 2025 – Aug. 2025

- Developed an API-based automation tool by integrating **Synopsys Custom Compiler** and **ParagonX**, achieving 60× faster P2P resistance queries with shortest-path visualization.
- Leveraged **Python** and **TCL** to automate and streamline workflows across industry-standard **EDA tools**, greatly enhancing analog CAD productivity.

ICCAD 2024 Contest Problem B – Domestic Distinguished, NTU Jul. 2024 – Sep. 2024

- Developed C++ algorithms to optimize component placement using MBFF banking and debanking strategies.
- Balanced timing, power, and area (PPA) with improved placement efficiency.

Projects

QR Solver - Linear Equation Solver, NTU Spring 2025

- Implemented a hardware-based QR decomposition solver using systolic array architecture and CORDIC algorithm for 4×4 linear equation systems.
- Developed bit-true Python model with self-verification capabilities for parameter optimization and precision analysis.
- Achieved RMSE $<$ 1e-3 accuracy through systematic bit-true modeling experiments and quantization analysis.
- Designed modular Verilog architecture with configurable bit-width parameters (26-bit input, 16-bit output) and 14-clock-cycle total latency.

Camera Filter Based on FPGA, NTU Spring 2024

- Built an FPGA-based system integrating YOLO v8 for facial blemish detection and image processing.
- Implemented VGA display to visualize processed results.

Pipeline RISC-V, NTU Spring 2024

- Designed and implemented a pipelined RISC-V processor with branch prediction, compressed instruction support, and hardware-accelerated multiplication.

Technologies

Languages: C++, Python, TCL, Verilog