Shu-Yu Lin

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Education

National Taiwan University — Sept. 2018 - present
Bachelor of Science in Electrical Engineering — GPA: 3.64/4.3

National Taiwan University — Sept. 2019 - present
Bachelor of Arts in Political Science (Double major) — GPA: 4.3/4.3

Work Experience

Technical Intern — Sept. 2022 - present
MIH Consortium — Taipei, Taiwan

- Construct a car model with **3D Scenes of Azure Digital Twins**.
- Develop an embedded system based on **AUTOSAR4.4** on **NXP's S32K144-Q100 General-Purpose Evaluation Board**.

Hardware Platform Application Engineer Intern — July 2021 - June 2022
Intel Corporation — Taipei, Taiwan

- Contributor of **Highly Efficient Automatic PCIe Validation Tool Kit**, responsible for **Linux** test environment setup by **Shell Script** and **Python**, providing OS image by **Clonezilla** for teams worldwide. Using **Python** to parse error log of **100,000**+ lines within seconds for further usage. Enacting code release and validation flow for the project.
- Publish documents including Tool Kit testing environment setup and instructions, OS image creation and restoration.

Field Application Engineer Intern — July 2020 - Sept. 2020
Arrow Electronics — Taipei, Taiwan

- Conduct **RF circuit debug** on 5G/2.4G printed circuit board(PCB) by impedance adjustment, utilizing network analyzer for observation.
- Analyze waveform and debug by **Verilog** on **Altera FPGA**.

Research

Federated Learning on Person Re-Identification — Sept. 2021 - present
Media IC and System Lab (Advisor: Professor Shao-Yi Chien) — Taipei, Taiwan

- Study Federated Learning and ReID techniques. Conducting experiments based on **Selective Knowledge Aggregation** and develop **robust tool kit** for Federated Learning on ReID.
- Link: **Project Website**

Low Complexity Deep Neural Network Training Algorithm — Sept. 2020 - Feb. 2021
MicroSystem Research Laboratory (Advisor: Professor Tzi-Dar Chiueh) — Taipei, Taiwan

- Study **Quantization** of Convolutional Neural Network in **Pytorch**.
- Design pipelined multi-input format Convolution Multiply Accumulate circuit by **Verilog**, compatible with **INT4, INT8, FloatSD4** input format.

Projects

Bikesla — Fall 2021
Embedded System Labs final project — GitHub Link

- Develop IoT application based on **STM32L4 Discovery kit IoT node** and **iPadOS App** to control the device via Bluetooth.
- Functionality includes **speeding detection**, **anti-theft**, **lock/unlock**, and **bicycle finding**.

SWE Explore — Fall 2021
Database Management final project — GitHub Link

- Full stack project for software engineer job seekers to check salaries, locations, and other features worldwide.
- Front-end: **React.js**, back-end: **Django REST framework**, database: **PostgreSQL**.

Pipelined RISC-V CPU Design — Spring 2021
Digital System Design final project — GitHub Link

- Design a **5-stage pipelined RISC-V processor** with instruction cache and data cache.
- Implement **branch prediction** mechanism, **L2 cache** and **compressed instructions**.

Achievements

Presidential Award — This award is given each semester to students ranking within **the top 5% of their class**. 2019

Technical Skills

Programming languages: C++, Python, Go, MATLAB, Verilog
ML/AI: Pytorch, Numpy, Pandas, Matplotlib
Web Technologies: Node.js, React.js, Django, GraphQL
Miscellaneous: MySQL, PostgreSQL, Git, Shell, LaTeX

Relevant Coursework

Electrical Engineering: Integrated Circuit Design, Computer Architecture, Digital System Design, Solid State Electronics, Embedded System Lab, Biomedical Engineering Lab, Electronic Design Automation, DSP in VLSI Design
Computer Science: Algorithms, Data Structure, Machine Learning, Operating Systems, Multimedia Security, Database Management, Computer Networks, Information Security, Web Programming
Mathematics: Linear Algebra, Differential Equation, Discrete Mathematics, Probability and Statistics, Signals and Systems