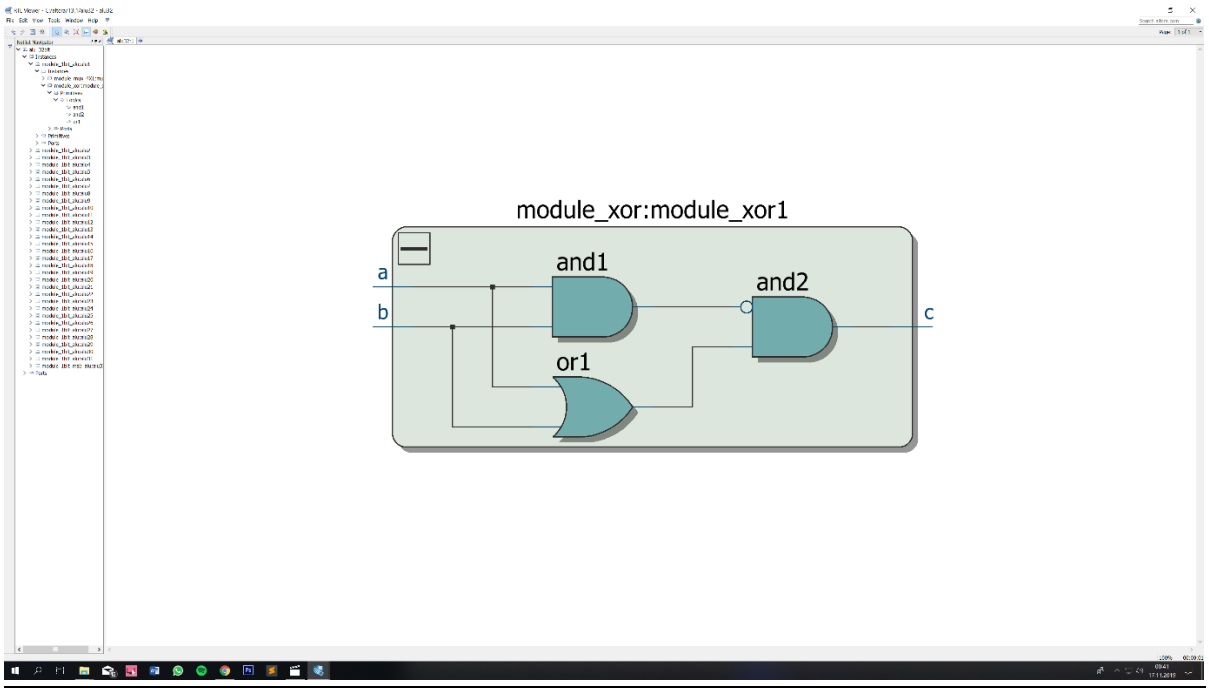
COMPUTER ORGANIZATION ASSIGNMENT-2 REPORT

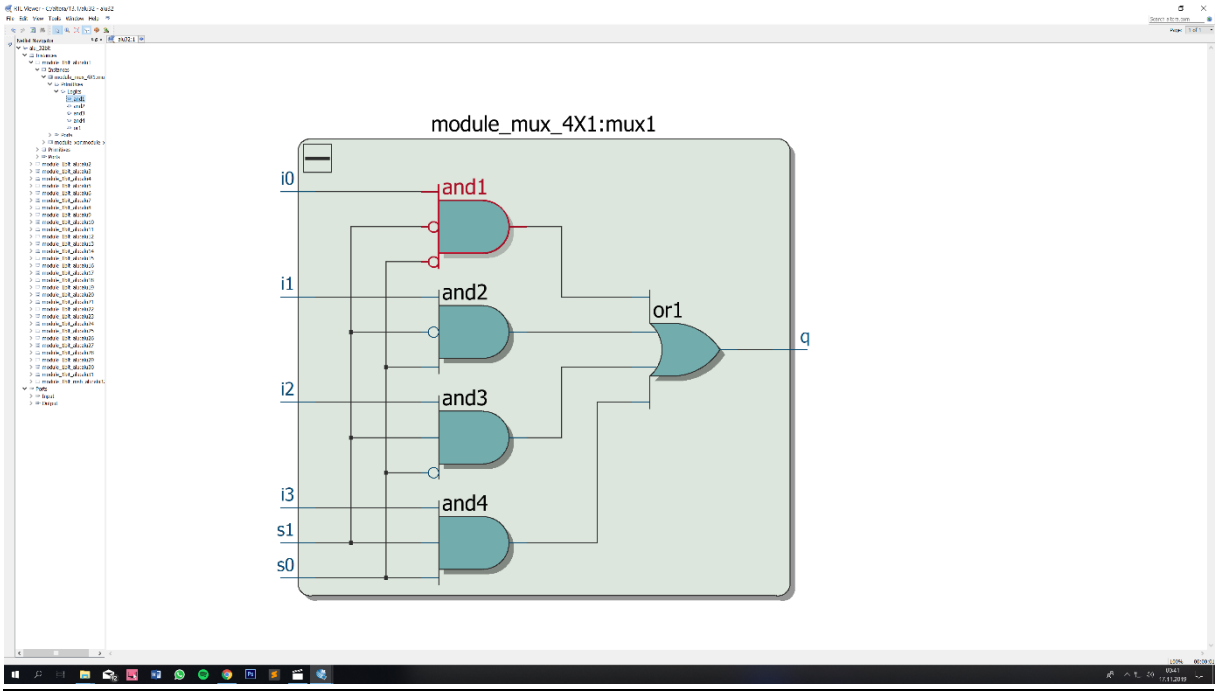
151044061

DOGU CEM DOGAN

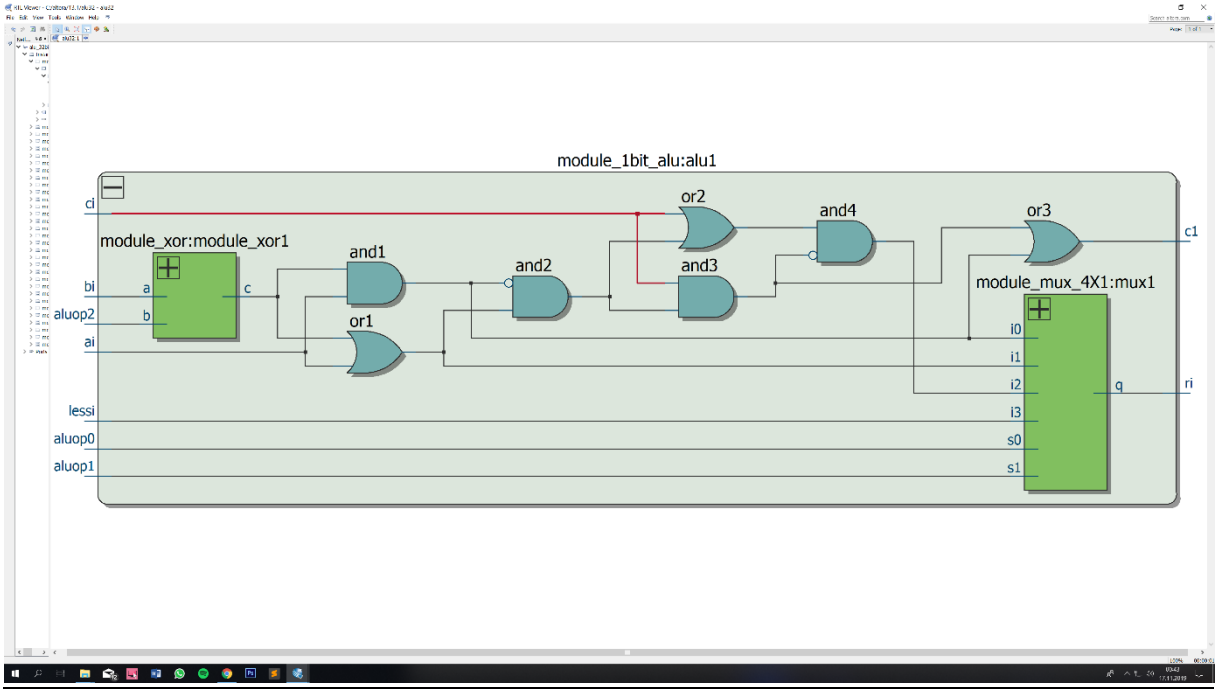
Implementation of XOR:



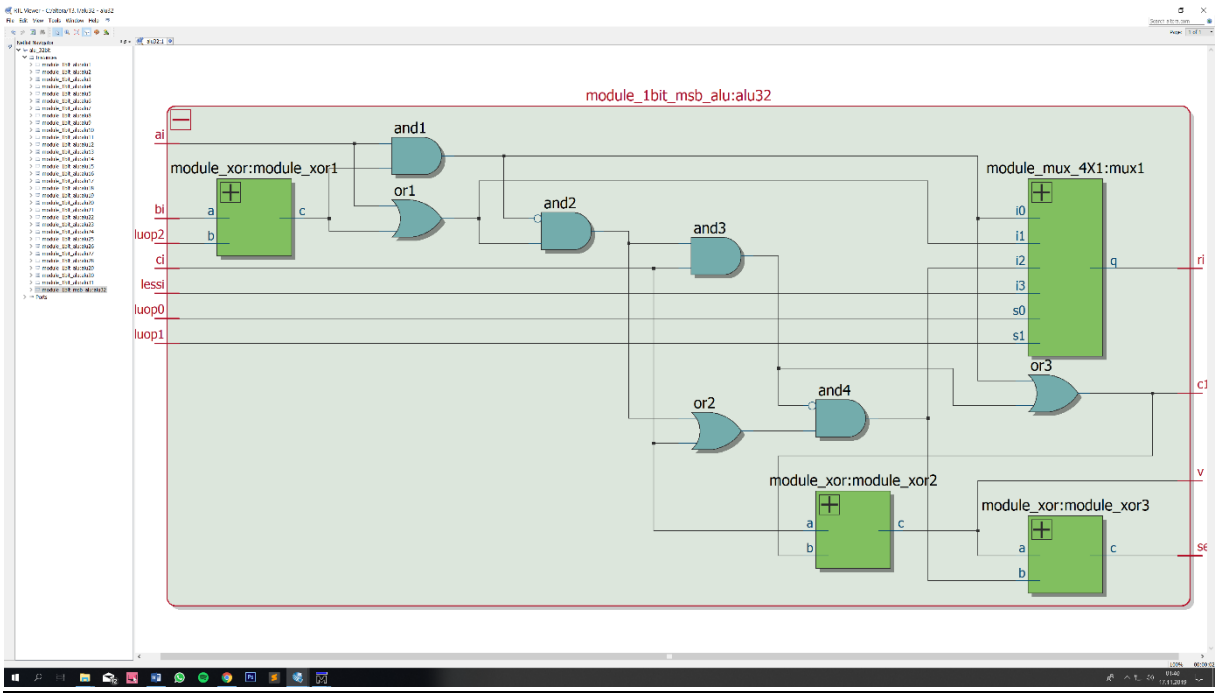
Implementation of MUX 4x1:



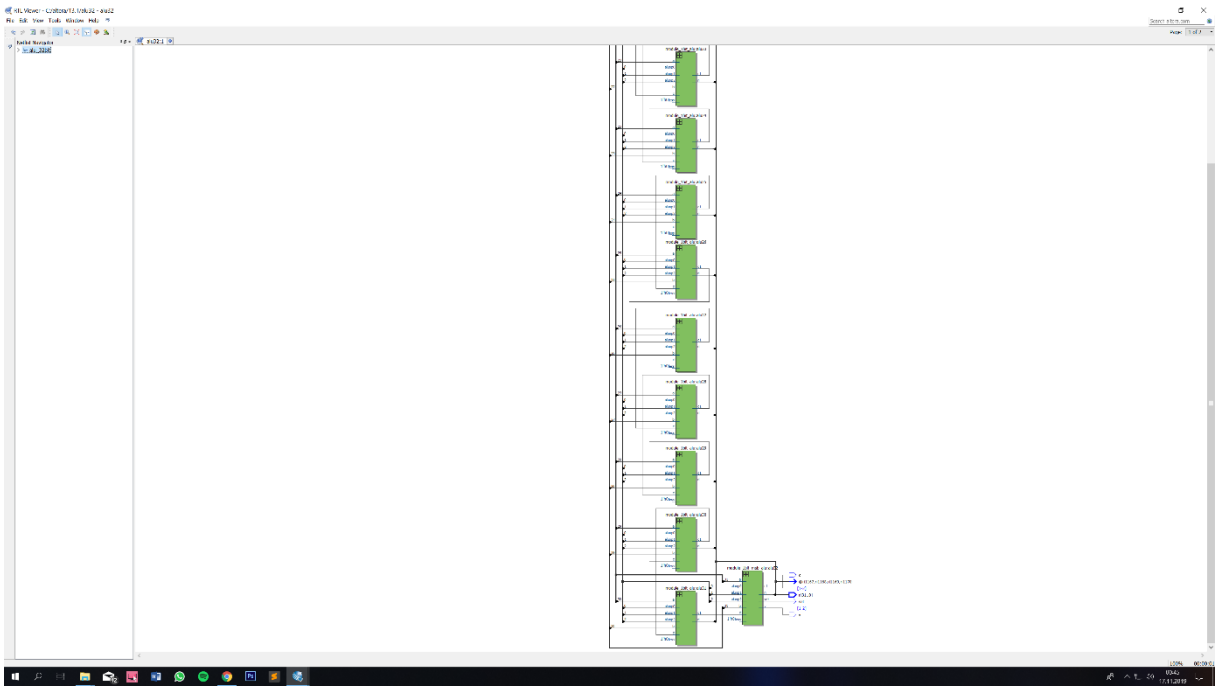
Implementation of 1bit ALU:



Implementation of 1bit MSB ALU:



Implementation of 32bit ALU (concatenated 31 ALU and 1 bit MSB ALU):



32 bit ALU testbench result:

Transcript

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Transcript

```
# -- Compiling module module_mux_4X1
#
# Top level modules:
#       module_mux_4X1
# vlog -vlog01compat -work work +incdir+C:/Users/DCD/Desktop/hw2_restored {C:/Users/DCD/Desktop/hw2_restored/module_1bit_alu.v}
# Model Technology ModelSim ALTERA vlog 10.1d Compiler 2012.11 Nov  2 2012
# -- Compiling module module_1bit_alu
#
# Top level modules:
#       module_1bit_alu
# vlog -vlog01compat -work work +incdir+C:/Users/DCD/Desktop/hw2_restored {C:/Users/DCD/Desktop/hw2_restored/module_1bit_msb_alu.v}
# Model Technology ModelSim ALTERA vlog 10.1d Compiler 2012.11 Nov  2 2012
# -- Compiling module module_1bit_msb_alu
#
# Top level modules:
#       module_1bit_msb_alu
# vlog -vlog01compat -work work +incdir+C:/Users/DCD/Desktop/hw2_restored {C:/Users/DCD/Desktop/hw2_restored/alu_32bit.v}
# Model Technology ModelSim ALTERA vlog 10.1d Compiler 2012.11 Nov  2 2012
# -- Compiling module alu_32bit
#
# Top level modules:
#       alu_32bit
#
vlog -reportprogress 300 -work work C:/Users/DCD/Desktop/hw2_restored/alu_32bit_testbench.v
# Model Technology ModelSim ALTERA vlog 10.1d Compiler 2012.11 Nov  2 2012
# -- Compiling module alu_32bit_testbench
#
# Top level modules:
#       alu_32bit_testbench
ModelSim> vsim work.alu_32bit_testbench
# vsim work.alu_32bit_testbench
# Loading work.alu_32bit_testbench
# Loading work.alu_32bit
# Loading work.module_1bit_alu
# Loading work.module_xor
# Loading work.module_mux_4X1
# Loading work.module_1bit_msb_alu
add wave -position insertpoint  \
sim:/alu_32bit_testbench/a \
sim:/alu_32bit_testbench/aluop \
sim:/alu_32bit_testbench/b \
sim:/alu_32bit_testbench/c \
sim:/alu_32bit_testbench/r \
sim:/alu_32bit_testbench/v
VSIM 5> step -current
# time =  0, a =00000000000000000000000000001011, b=00000000000000000000000000000110, ri=00000000000000000000000000000010 , ALUop=000
# time = 20, a =00000000000000000000000000001011, b=00000000000000000000000000000110, ri=00000000000000000000000000001111 , ALUop=001
# time = 40, a =00000000000000000000000000001011, b=00000000000000000000000000000110, ri=00000000000000000000000000010001 , ALUop=010
# time = 60, a =00000000000000000000000000001011, b=00000000000000000000000000000110, ri=00000000000000000000000000000101 , ALUop=110
# time = 80, a =00000000000000000000000000001011, b=00000000000000000000000000000110, ri=00000000000000000000000000000000 , ALUop=111

VSIM 6>
```

All modules RTL views shows above.

All modules have own testbenchs codes and these modules were concratenated after the test seperately. Final 32bit modul tested by alu_32bit_testbench.v.

A(32bit binary input) B(32bit binary input) Ri(32bit binary result output)

ALUop: 000 and

ALUop: 001 or

ALUop:010 add

ALUop: 110 substruct

ALUop: 111 set on less than (if a>b ri is 0,otherwise 1)