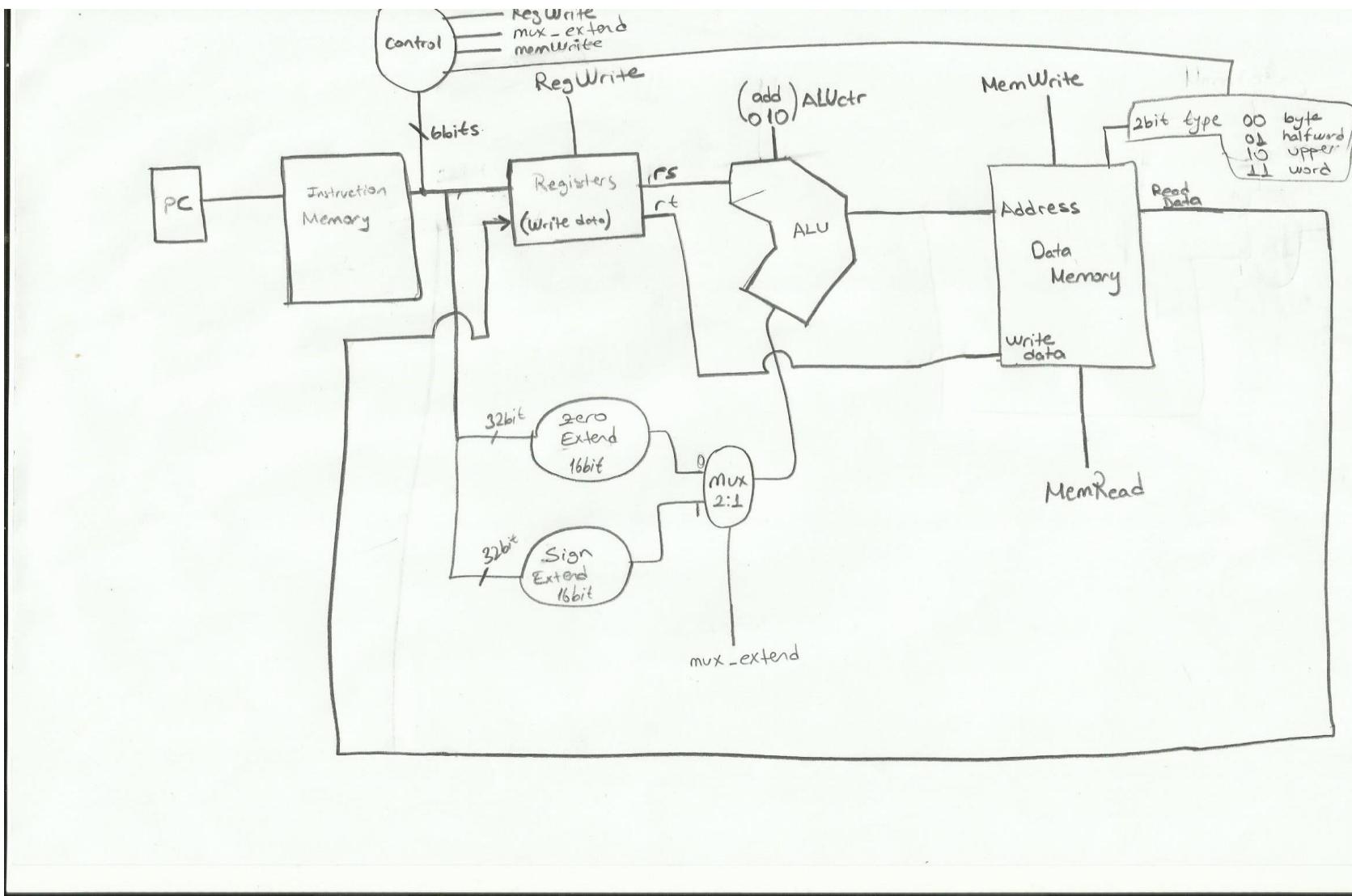
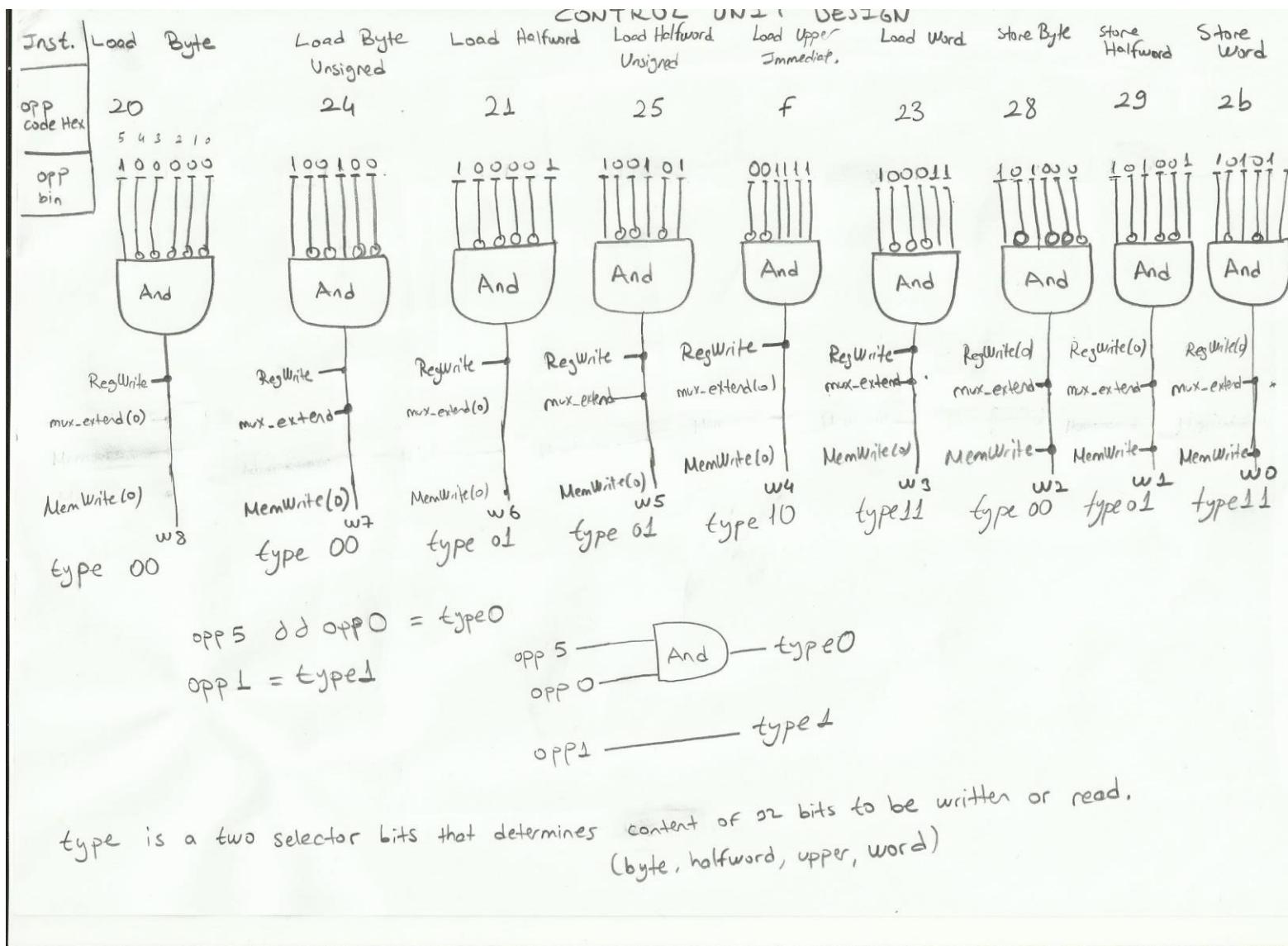


COMPUTER ORGANIZATION ASSIGNMENT-3 REPORT
151044061
DOGU CEM DOGAN

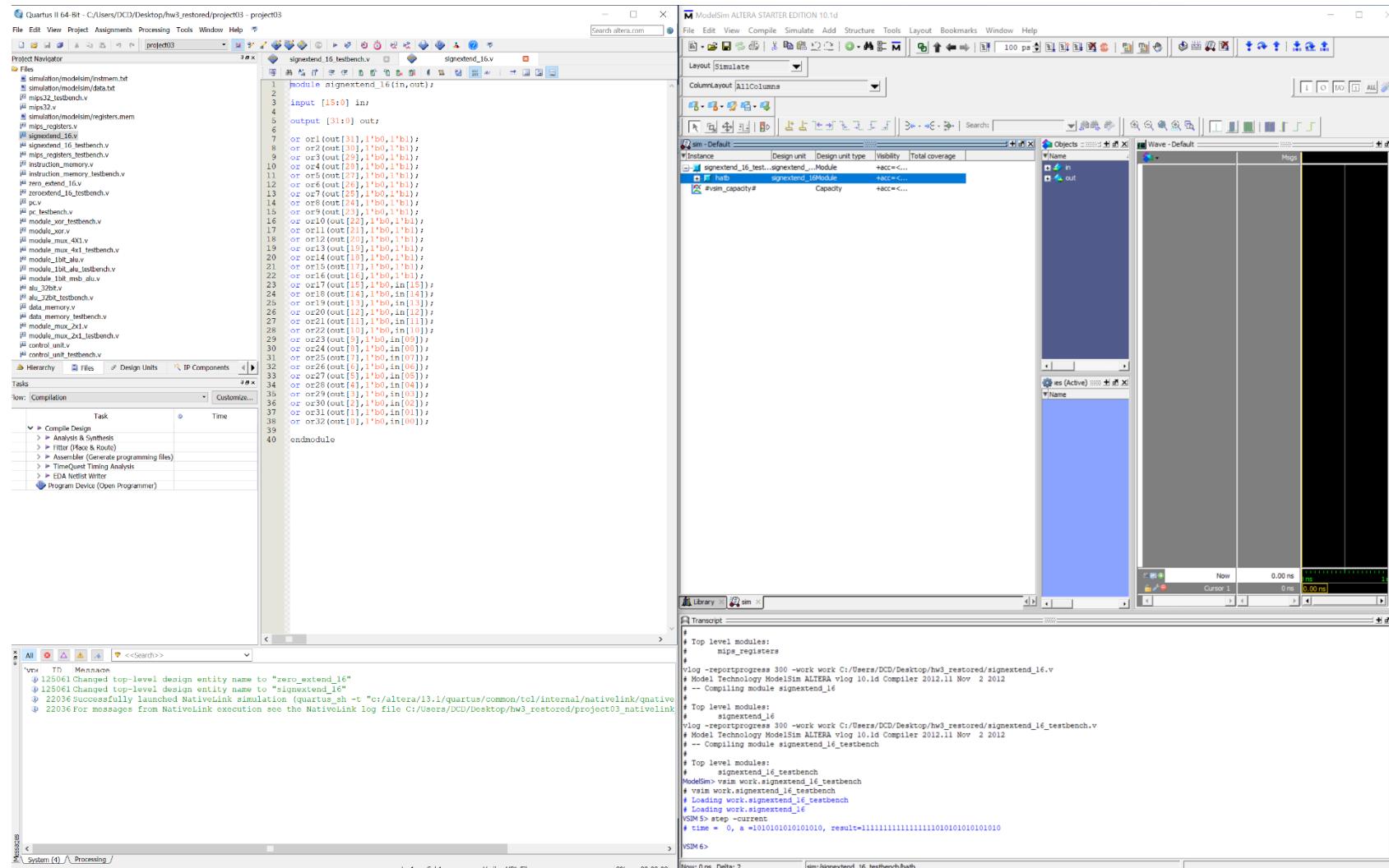
DATAPATH DESIGN



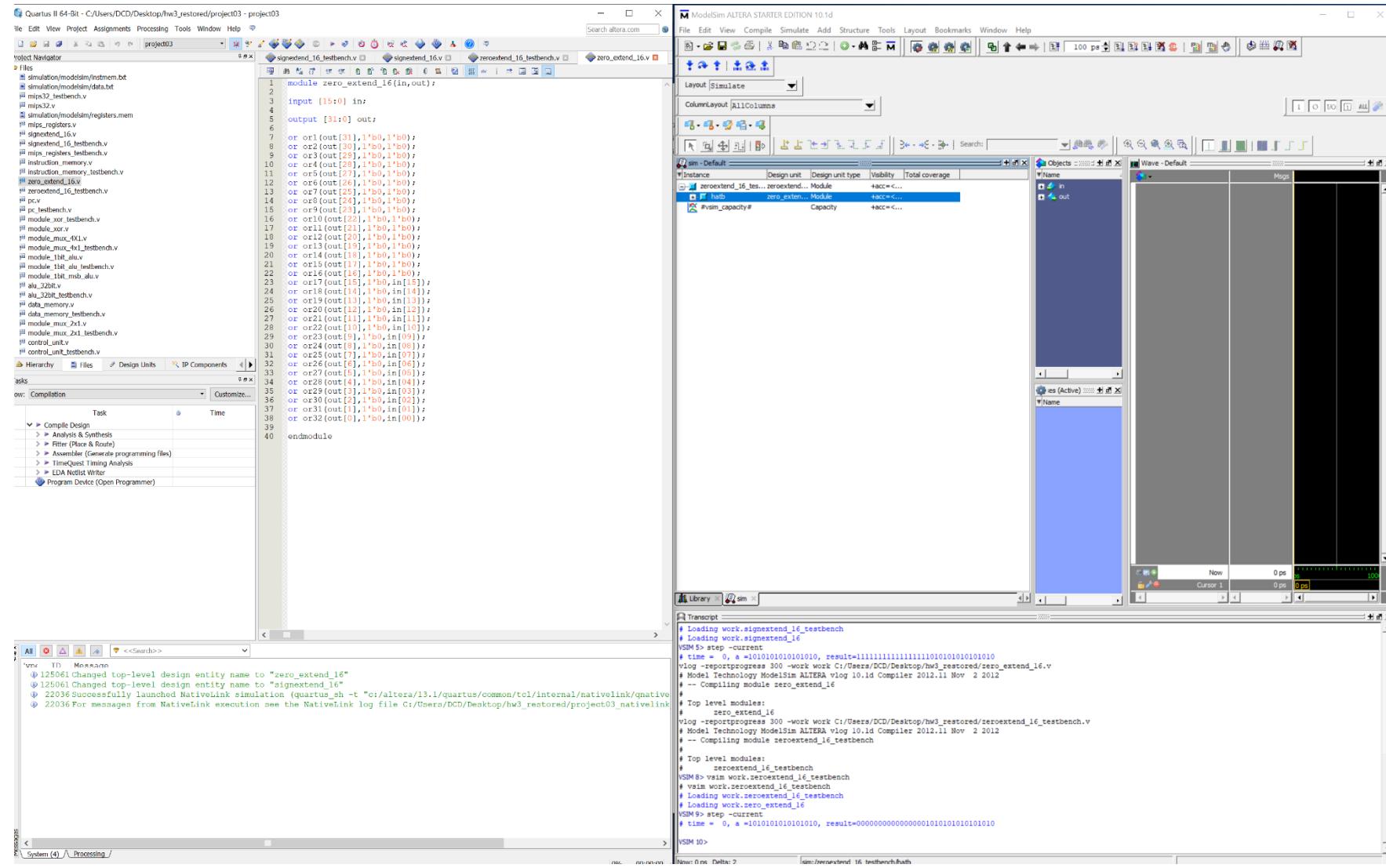
CONTROL UNIT DESIGN



MODULE: SIGN EXTEND TEST



MODULE: ZERO EXTEND TEST



MODULE: PROGRAM COUNTER TEST

Quartus II 64-Bit - C:/Users/DCD/Desktop/hw3_restored/project03 - project03

File Edit View Project Assignments Processing Tools Window Help

Project Navigator

- Files
 - signed_bench.v
 - sl.v
 - zeroet..bench.v
 - zer..6.v
 - pc.v
 - pc..v

```

1 module pc(clock,out);
2 input clock;
3 output [31:0] out;
4 reg [31:0] next;
5
6 initial next = 32'b0;
7 always @(posedge clock)
8 begin
9     next = next + 1'b1;
10    end
11
12 assign out = next;
13 endmodule

```

Hierarchy Files Design Units IP Components

Tasks

| Task | Time |
|--|------|
| Compile Design | |
| Analysis & Synthesis | |
| Timing (Power & Route) | |
| Assembler (Generate programming files) | |
| TIMEQuest Timing Analysis | |
| EDA Netlist Writer | |
| Program Device (Open Programmer) | |

Messages

All TD Messages

- ③ 125061 Changed top-level design entity name to "zero extend 16"
- ③ 125061 Changed top-level design entity name to "signextend 16"
- ③ 22036 Successfully launched NativeLink simulation (quartus sh -t "c:/altera/13.1/quartus/common/tcl/internal/nativelink/qnative
- ③ 22036 For messages from NativeLink execution see the NativeLink log file C:/Users/DCD/Desktop/hw3_restored/project03_nativelink

ModelSim ALTERA STARTER EDITION 10.1d

File Edit View Compile Simulate Add Source Tools Layout Bookmarks Window Help

Layout: Simulate ColumnLayout: AllColumns

sim - Default Objects

| Instance | Design unit | Design unit type | Visibility | Total coverage |
|-----------------|--------------|------------------|------------|----------------|
| pc_testbench | pc_testbench | Module | +acc=<.. | |
| pc | pc | Module | +acc=<.. | |
| #ALWAYS#12 | pc_testbench | Process | +acc=<.. | |
| avsim_capacity# | | Capacity | +acc=<.. | |

ln# Name

```

1 module pc_testbench();
2
3 reg clock;
4 wire [31:0]out;
5
6 pc pc1(clock,out);
7
8
9 initial clock = 0;
10
11 always
12 begin
13     #10 clock=~clock;
14
15 if(out==32'b00000000000000000000000000000000)
16 begin
17     $finish;
18 end
19
20
21
22
23
24 initial
25 begin
26     $monitor("time = %2d, clock=%b, out=%32b",
27 end
28
29
30
31
32 endmodule

```

Library sim

Wave pc_testbench.v

VSM 13> step -current

```

# time = 0, clock=0, out=00000000000000000000000000000000
# time = 10, clock=1, out=00000000000000000000000000000001
# time = 20, clock=0, out=00000000000000000000000000000000
# time = 30, clock=1, out=00000000000000000000000000000001
# time = 40, clock=0, out=00000000000000000000000000000000
# time = 50, clock=1, out=00000000000000000000000000000001
# time = 60, clock=0, out=00000000000000000000000000000000
# time = 70, clock=1, out=00000000000000000000000000000001
# time = 80, clock=0, out=00000000000000000000000000000000
# time = 90, clock=1, out=00000000000000000000000000000001
# time = 100, clock=0, out=00000000000000000000000000000000
# time = 110, clock=1, out=00000000000000000000000000000001
# time = 120, clock=0, out=00000000000000000000000000000000
# time = 130, clock=1, out=00000000000000000000000000000001
# time = 140, clock=0, out=00000000000000000000000000000000
# time = 150, clock=1, out=00000000000000000000000000000000
# time = 160, clock=0, out=00000000000000000000000000000000
** Note: $finish : C:/Users/DCD/Desktop/hw3_restored/pc_testbench.v(18)
# Time: 160 ps Iteration: 0 Instance: /pc_testbench
# Break in Module pc_testbench at C:/Users/DCD/Desktop/hw3_restored/pc_testbench.v line 18
# 18 Col: 0 READ

```

VSM 14>

System (4) / Processing /

0% 00:00:00 Now: 160 ps Delta: 0 sim:pc_testbench#ALWAYS#12

In: 18 Col: 0 READ

MODULE: INSTRUCTION MEMORY TEST

MODULE: CONTROL UNIT TEST

Quartus II 64 Bit - C:/Users/DCD/Desktop/hw3_restored/project03 - project03

File Edit View Project Assignments Processing Tools Window Help

Search altera.com

Project Navigator

- simulation/modelsim/data.txt
- mp32.v
- simulation/mips32_tb.v
- mips32_tb.bench
- mips_registers.v
- sigextend16.v
- sigextend16_tb.bench.v
- mips_registers_tb.bench.v
- instruction_memory.v
- instruction_memory_tb.bench.v
- zero_extend_16.v
- zero_extend_16_tb.bench.v
- pc.v
- pc_tb.bench.v
- module_xor_tb.bench.v
- module_xor.v
- module_mux_4x1.v
- module_mux_4x1_tb.bench.v
- module_mux_2x1.v
- module_mux_2x1_tb.bench.v
- control_unit.v
- control_unit_tb.bench.v

control_unit.v

```

1 module control_unit(opp5,opp4,opp3,opp2,opp1,opp0,RegWrite,Mux_extend,MemWrite,Type);
2
3 input opp5,opp4,opp3,opp2,opp1,opp0;
4 output RegWrite,Mux_extend,MemWrite;
5
6 output [1:0] Type;
7
8 wire not_opp5,not_opp4,not_opp3,not_opp2,not_opp1,not_opp0;
9
10 wire w0,w7,w6,w5,w4,w3,w2,w1,w0;
11
12 not not5(not_opp5,opp5);
13 not not4(not_opp4,opp4);
14 not not3(not_opp3,opp3);
15 not not2(not_opp2,opp2);
16 not not1(not_opp1,opp1);
17 not not0(not_opp0,opp0);
18
19 and Load_Byt (W0,opp5,not_opp4,not_opp3,not_opp2,not_opp1,not_opp0);
20 and Load_Byt_Usigned(w7,opp5,not_opp4,not_opp3,opp2,not_opp1,not_opp0);
21 and Load_Halfword_Usigned(w5,opp5,not_opp4,not_opp3,opp2,not_opp1,opp0);
22 and Load_Upper_Imm(w4,opp5,not_opp5,not_opp4,opp3,opp2,opp1,opp0);
23 and Load_Word(W3,opp5,not_opp4,opp3,not_opp2,not_opp1,not_opp0);
24 and Store_Byt (W2,opp5,not_opp4,opp3,not_opp2,not_opp1,opp0);
25 and Store_Halfword(W1,opp5,not_opp4,opp3,not_opp2,opp1,opp0);
26 and Store_Word(W0,opp5,not_opp4,opp3,not_opp2,opp1,opp0);
27
28 or or_RegWrite(RegWrite,1'b0,w8,w7,w6,w5,w4,w3);
29 or or_Mux_Extend(Mux_Extend,1'b0,w7,w6,w5,w3,w2,w1,w0);
30 or or_MemWrite(MemWrite,1'b0,w2,w1,w0);
31
32 // type bits to determine content of 32bits to be written or read, (byte,halfword,upper,word).
33 and_and_type0(Type[0],opp5,opp0);
34 or_or_type1(Type[1],1'b0,opp1);
35
36 endmodule

```

Text Editor - C:/Users/DCD/Desktop/hw3_restored/project03 - project03 - [control_unit_tb.bench.v]

```

1 module control_unit_tb.bench();
2
3 req opp5,opp4,opp3,opp2,opp1,opp0;
4
5 wire RegWrite,Mux_Extend,MemWrite;
6 wire [1:0]Type;
7
8 control_unit unit(opp5,opp4,opp3,opp2,opp1,opp0,RegWrite,Mux_Extend,MemWrite,Type);
9
10 initial begin
11 opp5 = 1'b1; opp4 = 1'b0; opp3 = 1'b0; opp2 = 1'b0; opp1 = 1'b0; opp0 = 1'b0; // Load Byte OPCODE 100000
12 #20
13 opp5 = 1'b1; opp4 = 1'b0; opp3 = 1'b0; opp2 = 1'b1; opp1 = 1'b0; opp0 = 1'b0; // Load Byte Unsigned OPCODE 100100
14 #20
15 opp5 = 1'b1; opp4 = 1'b0; opp3 = 1'b0; opp2 = 1'b0; opp1 = 1'b0; opp0 = 1'b1; // Load Halfword OPCODE 100001
16 #20
17 opp5 = 1'b1; opp4 = 1'b0; opp3 = 1'b0; opp2 = 1'b1; opp1 = 1'b0; opp0 = 1'b1; // Load Halfword Unsigned OPCODE 100101
18 #20
19 opp5 = 1'b0; opp4 = 1'b0; opp3 = 1'b1; opp2 = 1'b1; opp1 = 1'b0; opp0 = 1'b1; // Load Upper Immediate OPCODE 001111
20 #20
21 opp5 = 1'b1; opp4 = 1'b0; opp3 = 1'b0; opp2 = 1'b0; opp1 = 1'b1; opp0 = 1'b1; // Load Word OPCODE 100011
22 #20
23 opp5 = 1'b1; opp4 = 1'b0; opp3 = 1'b1; opp2 = 1'b0; opp1 = 1'b0; opp0 = 1'b0; // Store Byte OPCODE 101000
24 #20
25 opp5 = 1'b1; opp4 = 1'b0; opp3 = 1'b1; opp2 = 1'b0; opp1 = 1'b0; opp0 = 1'b1; // Store Halfword OPCODE 101011
26 #20
27 opp5 = 1'b1; opp4 = 1'b0; opp3 = 1'b1; opp2 = 1'b0; opp1 = 1'b1; opp0 = 1'b1; // Store Word OPCODE 101011
28
29 end
30
31 initial
32 $monitor("time = %d, opp5=%b,opp4=%b,opp3=%b,opp2=%b,opp1=%b,opp0=%b,RegWrite=%b,Mux_Extend=%b,MemWrite=%b,Type=%b ", $time, opp5,
33 opp4,opp3,opp2,opp1,opp0,RegWrite,Mux_Extend,MemWrite,Type);
34 end
35
36 endmodule

```

Transcript

```

All <> ID Memname <> Search>
```

```

* Top level modules:
*   control_unit
* Log - Error: parse error 300 -work work C:/Users/DCD/Desktop/hw3_restored/control_unit_tb.bench.v
Model Technology ModelSim ALTERA vlog 10.1d Compiler 2012.11 Nov 2 2012
-- Compiling module control_unit_tb.bench
# Top level modules:
control_unit_tb.bench
#SM:20: warning: work.control_unit_tb.bench
# VIM work.control_unit_tb.bench
# Loading work.control_unit_tb.bench
# Loading work.control_unit
VSM:21: step -current
# time = 0, opp5=1,opp4=0,opp3=0,opp2=0,opp1=0,opp0=0,RegWrite=1,Mux_Extend=0,MemWrite=0,Type=00
# time = 20, opp5=1,opp4=0,opp3=0,opp2=1,opp1=0,opp0=0,RegWrite=1,Mux_Extend=1,MemWrite=0,Type=00
# time = 40, opp5=1,opp4=0,opp3=0,opp2=0,opp1=0,opp0=1,RegWrite=1,Mux_Extend=0,MemWrite=0,Type=01
# time = 60, opp5=1,opp4=0,opp3=0,opp2=1,opp1=0,opp0=0,RegWrite=1,Mux_Extend=1,MemWrite=0,Type=01
# time = 80, opp5=0,opp4=0,opp3=1,opp2=1,opp1=1,opp0=1,RegWrite=1,Mux_Extend=0,MemWrite=0,Type=10
# time = 100, opp5=1,opp4=0,opp3=1,opp2=0,opp1=1,opp0=1,RegWrite=1,Mux_Extend=1,MemWrite=0,Type=11
# time = 120, opp5=1,opp4=0,opp3=1,opp2=0,opp1=0,opp0=0,RegWrite=0,Mux_Extend=1,MemWrite=1,Type=00
# time = 140, opp5=1,opp4=0,opp3=1,opp2=0,opp1=1,opp0=1,RegWrite=0,Mux_Extend=1,MemWrite=1,Type=01
# time = 160, opp5=1,opp4=0,opp3=1,opp2=0,opp1=1,opp0=1,RegWrite=0,Mux_Extend=1,MemWrite=1,Type=11

```

Messages

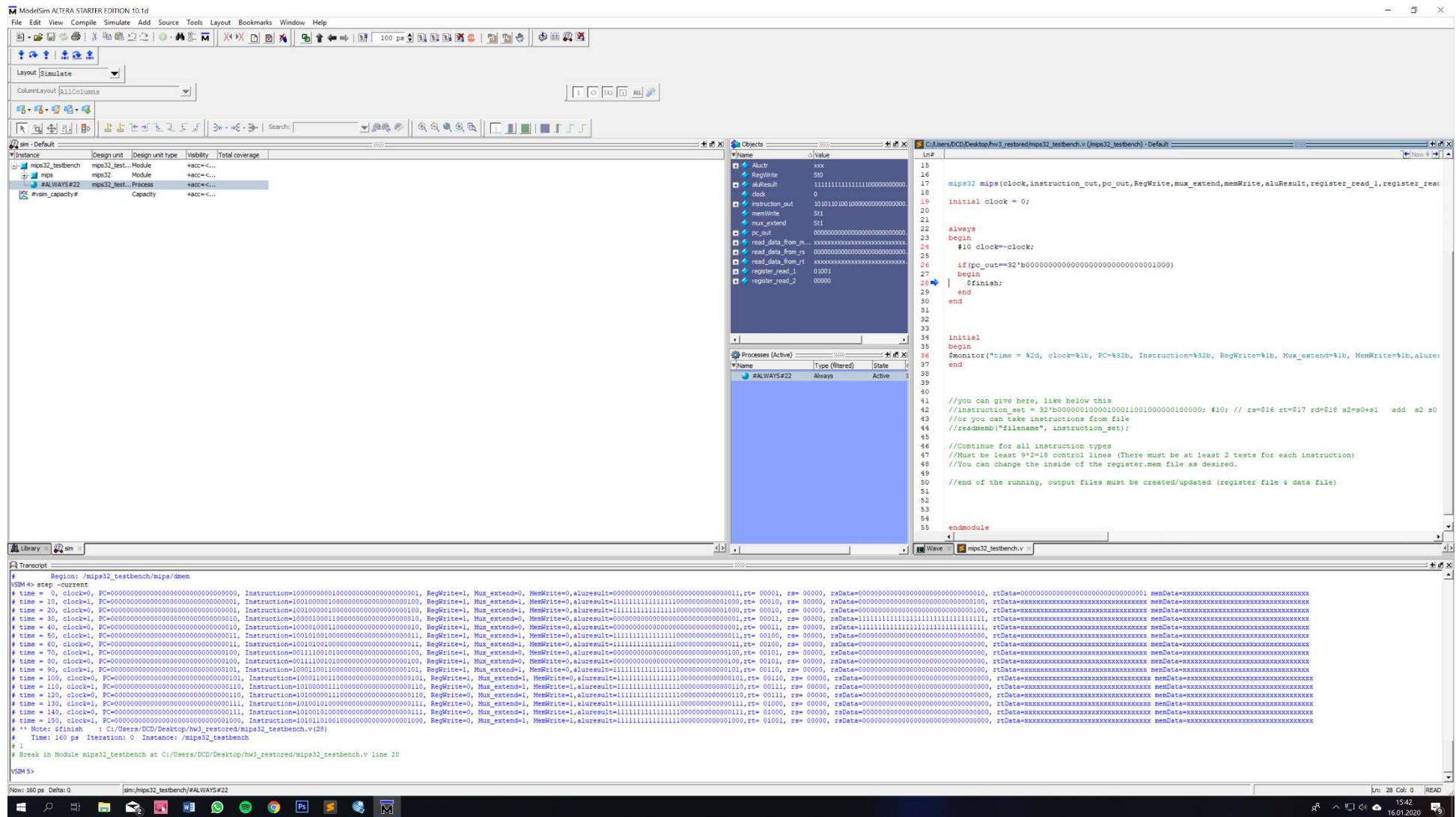
System (4) / Processing /

MODULE: DATA MEMORY TEST

The screenshot displays two main windows from the Quartus II and ModelSim software environments. The left window, titled 'Quartus II 64-Bit - C:/Users/DCD/Desktop/hw3_restored/project03 - project03', shows the project navigator with files like 'data_memory.v', 'data_memory_tb.v', and 'simulation/memtest.mem'. It also shows the hierarchy of the design, including modules such as 'alu_32bit.v', 'alu_32bit_tb.v', 'data_memory.v', and 'data_memory_tb.v'. The right window, titled 'ModelSim ALTERA STARTER EDITION 10.1d - C:/Users/DCD/Desktop/hw3_restored/project03 - [simulation/modelsim/data...]', shows the 'File' and 'Edit' menus. Below these are tabs for 'Layout', 'Simulate', and 'ColumnLayout'. A tree view under 'Design' shows 'Instance' and 'IP Core'. The 'Sim' tab is selected, displaying a waveform viewer with multiple waveforms. The bottom right of the window shows a transcript of simulation logs, including memory data files and specific testbench code. The status bar at the bottom indicates 'Now: 85 ps Delta: 0'.

MODULE: REGISTERS TEST

MODULE: MIPS32 TEST(ALL MODULE CONNECTED)



CONCLUSION

All module works very well seperately but when they are connected each other,they do not work properly.
There is a few problems.