✓ **Correct** 3/3 Points

1. Individual blocks or records have a unique address based on physical location with _____.

- (●) direct access ✓
- ( ) physical access
- ( ) associative access
- ( ) sequential access

✓ **Correct** 3/3 Points

2. A common example of system interconnection is by means of a _____

- ( ) data transport
- ( ) register
- ( ) control device
- (●) system bus ✓

✓ **Correct** 3/3 Points

3. _____ attributes include hardware details transparent to the programmer.

- Interface
- Organizational ✓
- Memory
- Architectural

✓ **Correct** 2/2 Points

4. Interfaces between the computer and peripherals is an example of an organizational attribute.

- True ✓
- False

✓ **Correct** 3/3 Points

5. A(n) _____ is generated by a failure such as power failure or memory parity error.

- (●) hardware failure interrupt ✓
- ( ) timer interrupt
- ( ) I/O interrupt
- ( ) program interrupt

✓ **Correct** 3/3 Points

6. It is a(n) _____ design issue whether a computer will have a multiply instruction.

- (●) architectural ✓
- ( ) elementary
- ( ) organizational
- ( ) memory

✓ **Correct** 3/3 Points

9. _____ enables the processor to keep its execution engines as busy as possible by executing instructions that are likely to be needed.

speculative execution

✓ **Correct** 3/3 Points

10. In a _____, binary values are stored using traditional flip-flop logic-gate configurations.

- ROM
- RAM
- SRAM ✓
- DRAM

✓ **Correct** 3/3 Points

7. The interface between processor and _____ is the most crucial pathway in the entire computer because it is responsible for carrying a constant flow of program instructions and data between memory chips and the processor.

- ○ clock speed
- ◉ main memory ✓
- ○ pipeline
- ○ control unit

✓ **Correct** 2/2 Points

8. DRAM is much costlier than SRAM

- ○ True
- ◉ False ✓

✓ **Correct** 3/3 Points

9. _____ enables the processor to keep its execution engines as busy as possible by executing instructions that are likely to be needed.

speculative execution

✓ **Correct** 3/3 Points

10. In a _____, binary values are stored using traditional flip-flop logic-gate configurations.

- ROM
- RAM
- SRAM ✓
- DRAM

✕ **Incorrect** 0/2 Points

11. A cache line includes a _____ that identifies which particular block is currently being stored.

- ○ cache
- ◉ hit
- ○ tag ✓
- ○ miss
- ○ locality
- ○ parity bit

✕ **Incorrect** 0/3 Points

12. The major structural components of the CPU are: control unit, register, CPU interconnection, and _____.

CPU

Correct answers: ALU | Arithmetic Logic Unit

✓ **Correct** 3/3 Points

13. The QPI _____ layer is used to determine the course that a packet will traverse across the available system interconnects.

- ○ protocol
- ○ application
- ○ link
- ◉ routing ✓
- ○ phsical

✓ **Correct** 3/3 Points

14. _____ enables a processor to work simultaneously on multiple instructions by performing a different phase for each of the multiple instructions at the same time.

pipelining

✓ **Correct** 2/2 Points

15. The width of a track is double that of the head.

- ○ True
- ◉ False ✓

✗ **Incorrect** 8/28 Points

16. Consider a direct-mapped cache with 8 lines, each holding 16 bytes of data. The cache is byte-addressable and the main memory consists of 64 KB, which is also byte-addressable. Assume that a program reads 16KB of memory sequentially. Answer the following questions:

    a) How many bits are required for the tag, index, and offset fields of a cache address?
    b) What is the cache size in bytes?
    c) What is the block size in bytes?
    d) What is the total number of blocks in main memory?
    e) How many cache hits and misses will occur for the program, assuming that the cache is initially empty?
    f) What is the hit ratio?
    g) Give an example virtual address (in BINARY) that will be placed in cache line 5.
    (Non-anonymous question)

✓ **Correct** 2/2 Points

17. It is not possible to connect I/O controllers directly onto the system bus.

- ○ True
- ◉ False ✓

✓ **Correct** 5/5 Points

18. Draw a RAID 1+0 model by doing a RAID 1 first on the disks and then RAID 0 on the top. If you have ABCD how individual bytes stored in a 4 disk RAID1+0 system.
    (Non-anonymous question)

✓ **Correct** 3/3 Points

19. Computer _____ refers to those attributes that have a direct impact on the logical execution of a program.

- organization
- specifications
- design
- architecture ✓

✓ **Correct** 3/3 Points

20. Each data path consists of a pair of wires (referred to as a _____) that transmits data one bit at a time.

- line
- chip
- lane ✓
- port

✗ **Incorrect** 0/2 Points

21. With *write back* updates are made only in the cache.

- (●) True
- ( ) False ✓

✓ **Correct** 2/2 Points

22. _____ law deals with the potential speedup of a program using multiple processors compared to a single processor.

- ( ) Little's
- ( ) Moore's
- ( ) Murphy's
- (●) Amdahl's ✓

✓ **Correct** 2/2 Points

23. For set-associative mapping the cache control logic interprets a memory address as three fields: Set, Word, and _____.

- (●) Tag ✓
- ( ) block
- ( ) line index
- ( ) map index

✗ **Incorrect** 0/2 Points

24. A straight comparison of clock speeds on different processors tells the whole story about performance.

- (●) True
- ( ) False ✓

✓ Correct 2/2 Points

25. When using the _____ technique all write operations made to main memory are made to the cache as well.

- write back
- LRU
- LFU
- write through ✓

✓ Correct 2/2 Points

26. Virtually all contemporary computer designs are based on concepts developed by _____ at the Institute for Advanced Studies, Princeton.

- John Andersen
- John Eckert
- John von Neumann ✓
- Herman Hollerith

✓ **Correct** 2/2 Points

27. NOR memory is better suited for external memory such as USB flash drives and memory cards.

- ○ True
- ◉ False ✓

✓ **Correct** 2/2 Points

28. When data are moved over longer distances, to or from a remote device, the process is known as _____.

- ○ data transport
- ○ structuring
- ◉ data communications ✓
- ○ registering

✗ **Incorrect** 0/2 Points

29. The number of bits used to represent various data types is an example of an architectural attribute

- ○ True ✓
- ◉ False