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23 - CSE206 Midterm Exam (23B_CSE 206_Computer Organization_Ö_1)

Spring 2023 - CSE206 Midterm Exam

Merhaba [redacted] Bu formu gönderdiğinizde, sahibi adınızı ve e-posta adresinizi görür.

1. _____ law deals with the potential speedup of a program using multiple processors compared to a single processor. (2 Puan)

- Little's
- Moore's
- Murphy's
- Amdahl's

2. The width of a track is double that of the head. (2 Puan)

- True
- False

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3. A common example of system interconnection is by means of a _____ (3 Puan)

- data transport
- register
- control device
- system bus

4. Computer _____ refers to those attributes that have a direct impact on the logical execution of a program. (3 Puan)

- organization
- specifications
- design
- architecture

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5. It is a(n) _____ design issue whether a computer will have a multiply instruction. (3 Puan)

- (●) architectural
- ( ) elementary
- ( ) organizational
- ( ) memory

6. Consider a direct-mapped cache with 8 lines, each holding 16 bytes of data. The cache is byte-addressable and the main memory consists of 64 KB, which is also byte-addressable. Assume that a program reads 16KB of memory sequentially. Answer the following questions:

a) How many bits are required for the tag, index, and offset fields of a cache address?
b) What is the cache size in bytes?
c) What is the block size in bytes?
d) What is the total number of blocks in main memory?
e) How many cache hits and misses will occur for the program, assuming that the cache is initially empty?
f) What is the hit ratio?
g) Give an example virtual address (in BINARY) that will be placed in cache line 5.

(Anonim olmayan soru) (28 Puan)

7. The QPI _____ layer is used to determine the course that a packet will traverse across the available system interconnects. (3 Puan)

- ( ) protocol
- ( ) application
- (●) link
- ( ) routing
- ( ) phsical

8. A(n) _____ is generated by a failure such as power failure or memory parity error. (3 Puan)

- ( ) hardware failure interrupt
- ( ) timer interrupt
- (●) I/O interrupt
- ( ) program interrupt

9. Draw a RAID 1+0 model by doing a RAID 1 first on the disks and then RAID 0 on the top. If you have ABCD how individual bytes stored in a 4 disk RAID1+0 system. (Anonim olmayan soru) (5 Puan)

Dosyayı karşıya yükle

Dosya sayısı üst sınırı: 1 Tek dosya boyutu üst sınırı: 10MB İzin verilen dosya türleri: Word, Excel, PPT, PDF, Resim, Video, Ses

10. _____ enables a processor to work simultaneously on multiple instructions by performing a different phase for each of the multiple instructions at the same time. (3 Puan)

pipelining

11. A cache line includes a _____ that identifies which particular block is currently being stored. (2 Puan)

- cache
- hit
- tag
- miss

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12. Interfaces between the computer and peripherals is an example of an organizational attribute. (2 Puan)

- True
- False

13. The number of bits used to represent various data types is an example of an architectural attribute (2 Puan)

- True
- False

14. Each data path consists of a pair of wires (referred to as a _____) that transmits data one bit at a time. (3 Puan)

- line
- chip
- lane

15. Individual blocks or records have a unique address based on physical location with _____. (3 Puan)

- (●) direct access
- ( ) physical access
- ( ) associative access
- ( ) sequential access

16. For set-associative mapping the cache control logic interprets a memory address as three fields: Set, Word, and _____. (2 Puan)

- (●) Tag
- ( ) block
- ( ) line index
- ( ) map index

17. _____ enables the processor to keep its execution engines as busy as possible by executing instructions that are likely to be needed. (3 Puan)

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17. _____ enables the processor to keep its execution engines as busy as possible by executing instructions that are likely to be needed. (3 Puan)

Superscalar execution

18. A straight comparison of clock speeds on different processors tells the whole story about performance. (2 Puan)

- ( ) True
- (●) False

19. When data are moved over longer distances, to or from a remote device, the process is known as _____. (2 Puan)

- ( ) data transport
- ( ) structuring
- (●) data communications
- ( ) registering

20. The interface between processor and _____ is the most crucial pathway in the entire computer because it is responsible for carrying a constant flow of program instructions and data between memory chips and the processor. (3 Puan)

- clock speed
- main memory
- pipeline
- control unit

21. In a _____, binary values are stored using traditional flip-flop logic-gate configurations. (3 Puan)

- ROM
- RAM
- SRAM
- DRAM

22. It is not possible to connect I/O controllers directly onto the system bus. (2 Puan)

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- SRAM
- DRAM

22. It is not possible to connect I/O controllers directly onto the system bus. (2 Puan)

- True
- False

23. _____ attributes include hardware details transparent to the programmer. (3 Puan)

- Interface
- Organizational
- Memory
- Architectural

24. When using the _____ technique all write operations made to main memory are (2

24. When using the _____ technique all write operations made to main memory are made to the cache as well. (2 Puan)

- ○ write back
- ○ LRU
- ○ LFU
- ◉ write through

25. DRAM is much costlier than SRAM (2 Puan)

- ○ True
- ◉ False

26. With *write back* updates are made only in the cache. (2 Puan)

- ◉ True
- ○ False

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27. The major structural components of the CPU are: control unit, register, CPU interconnection, and _____. (3 Puan)

arithmetic and logic unit (ALU)

28. NOR memory is better suited for external memory such as USB flash drives and memory cards. (2 Puan)

- ○ True
- ◉ False

29. Virtually all contemporary computer designs are based on concepts developed by _____ at the Institute for Advanced Studies, Princeton. (2 Puan)

- ○ John Andersen
- ○ John Eckert
- ◉ John von Neumann
- ○ Herman Hollerith