Name Surname : .....

Student Id : ..... Signature:.....

19/04/2022 09:00
Duration: 75 min

Akdeniz University, Engineering Faculty
Computer Engineering Department
CSE206 Computer Organization Midterm Exam

Q 1. *(5pts) Explain the **difference** between Computer organization and Computer Architecture.*

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Q 2. *(17pts) Write the full name of the abbreviated terms considering the context of computer organization.*

a) MBR : .....
b) MAR : .....
c) IBR : .....
d) PC : .....
e) AC : .....
f) ARM : .....
g) QPI : .....
h) MMU : .....
i) RAID : .....
j) RAS : .....
k) ALU : .....
l) GPU : .....
m) USB : .....
n) ISA : .....
o) RISC : .....
p) CISC : .....
q) DMA : .....

Q 3. *(5pts) If 80% of an application is performed serially, **what is the maximum speedup**? Write the **formula and solution**.*

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Q 4. *(10pts) A 4-way set-associative cache memory unit with a capacity of 16 KB is built using a block size of **8 words (be careful!)**. The **word length is 32 bits**. The size of the physical address space is 4 GB. What is the number of bits for the TAG field?*

Q 5. *(4pts) How many check bits are needed if the Hamming error correction code is used to detect single bit errors in a 1024-bit data word?*

Q 6. *(4pts) Which RAID level provides the highest capacity for the same number of disks?*

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Q 7. *(10pts) The following code word 010101100010 has a problem. Perform your computations in the following empty area assuming that the code word was created using an* ***even parity*** *Hamming Code.*

a) Which bit is incorrect (indicate the position)

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b) Write the correct code word.

c) Indicate what the original (correct) data was (8 bit data)

Q 8. *(10pts) Consider a memory system that uses a 32-bit address to address at the byte level, plus a cache that uses a 64-byte line size. Assume a direct mapped cache with a tag field in the address of 20 bits. Show the address format and determine the following parameters:*

number of addressable units :……

number of blocks in main memory :……

number of lines in cache : ……

total cache memory capacity : ……

size of tag : ……

Q 9. *(5pts) What is speculative execution?*

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Q 10. *(10pts) Given the* ***memory contents*** *of the IAS computer shown below:*

Address	Contents
08A	010FA210FB
08B	010FA0F08D
08C	020FA210FB
08D	

Explain (semantically) what this program does? You can find IAS instruction format and IAS Instruction set in ***Figure 1*** *and* ***Table 2****.*

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Q 11. *(20pts) Write an IAS program to compute the factorial f(n)=n! using instructions from the Table 2 where the value of n is stored at the memory location **0FA**. After the execution of your program the output value f(n) must be stored at location **0FB**. For example, if the content of 0FA is 4 then a value of 24 (4!) must be present in memory location 0FB. **A snapshot of the memory is given as a table on the right.** Write your code below:*
***Hint:** I added a new instruction (MOV) in Table 2 to assign a scalar value to* AC. *At first, think about the pseudocode.*

0FA	*4*
0FB	*0*
0FC	*0*
0FD	*0*

Address	Symbolic Name	Contents
08AL		
08AR		
08BL		
08BR		
08CL		
08CR		
08DL		
08DR		
08EL		
08ER		
08FL		
08FR		
090L		
090R		
091L		
091R		
092L		

Address	Symbolic Name	Contents
092R		
093L		
093R		
094L		
094R		
095L		
095R		
096L		
096R		
097L		
097R		
0A8L		
0A8R		
0A9L		
0A9R		
0AAL		
0AAR		

Your pseudocode:

Table 2 The IAS Instruction Set

Instruction Type	Opcode	Symbolic Representation	Description
Data transfer	00001010	LOAD MQ	Transfer contents of register MQ to the accumulator AC
	00001001	LOAD MQ,M(X)	Transfer contents of memory location X to MQ
	00100001	STOR M(X)	Transfer contents of accumulator to memory location X
	00000001	LOAD M(X)	Transfer M(X) to the accumulator
	00000010	LOAD – M(X)	Transfer –M(X) to the accumulator
	00000011	LOAD |M(X)|	Transfer absolute value of M(X) to the accumulator
	00000100	LOAD – |M(X)|	Transfer –|M(X)| to the accumulator
Unconditional branch	00001101	JUMP M(X,0:19)	Take next instruction from left half of M(X)
	00001110	JUMP M(X,20:39)	Take next instruction from right half of M(X)
Conditional branch	00001111	JUMP + M(X,0:19)	If number in the accumulator is nonnegative, take next instruction from left half of M(X)
	00010000	JUMP + M(X,20:39)	If number in the accumulator is nonnegative, take next instruction from right half of M(X)
Arithmetic	00000101	ADD M(X)	Add M(X) to AC; put the result in AC
	00000111	ADD |M(X)|	Add |M(X)| to AC; put the result in AC
	00000110	SUB M(X)	Subtract M(X) from AC; put the result in AC
	00001000	SUB |M(X)|	Subtract |M(X)| from AC; put the remainder in AC
	00001011	MUL M(X)	Multiply M(X) by MQ; put most significant bits of result in AC, put least significant bits in MQ
	00001100	DIV M(X)	Divide AC by M(X); put the quotient in MQ and the remainder in AC
	00010100	LSH	Multiply accumulator by 2; that is, shift left one bit position
	00010101	RSH	Divide accumulator by 2; that is, shift right one position,
	00010011	MOV	Move the scalar value presented in the address field in AC
Address modify	00010010	STOR M(X,8:19)	Replace left address field at M(X) by 12 rightmost bits of AC
	00010011	STOR M(X,28:39)	Replace right address field at M(X) by 12 rightmost bits of AC

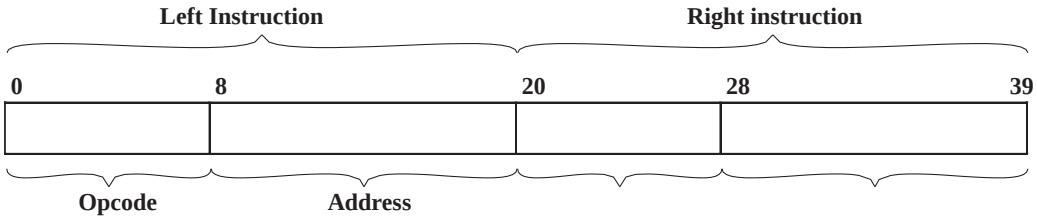

Figure 1. IAS Instruction format