# Science / Computer Science

#### **Question**



Consider a machine with a byte addressable main memory of  $2^{16}$  bytes and block size of 8 bytes. Assume that a direct mapped cache consisting of 32 lines is used with this machine.

a. How is a 16-bit memory address divided into tag, line number, and byte number? b. Into what line would bytes with each of the following addresses be stored? 0001 0001 0001 1011

1100 0011 0011 0100

1101 0000 0001 1101

1010 1010 1010 1010

- c. Suppose the byte with address 0001 1010 0001 1010 is stored in the cache. What are the addresses of the other bytes stored along with it?
- d. How many total bytes of memory can be stored in the cache?
- e. Why is the tag also stored in the cache?

# Solution Verified Answered 2 years ago

**Step 1** 1 of 6

Consider the parameters given:

- \* direct-mapped cache
- \* \$2^{16}\$B main memory size \$\rightarrow\$ \$16\$-bit address size
- \* \$8\$B = \$2^3\$B block size
- \* \$32 = 2^5\$ lines

**Step 2** 2 of 6

a) From the values given, construct the address format:

Word field: 3 bits Line field: 5 bits

Tag field: 16 - 3 - 5 = 8 bits

Tag	Line	Word
8 bits	5 bits	3 bits

**Step 3** 3 of 6

**b)** To get the line of each address, we must look into its **line field** and translate it into a decimal number.

 $0001\ 0001\ 0001\ 1011 \rightarrow \text{line } 3$ 

 $1100\ 0011\ 0011\ 0100 \rightarrow \text{line } 6$ 

 $1101\ 0000\ 0001\ 1101 \rightarrow line\ 3$ 

 $1010\ 1010\ {\color{red}1010}\ {\color{red}1010}\ {\color{red}1010}\ {\color{red}} \rightarrow {\color{red}line}\ {\color{red}21}$ 

**Step 4** 4 of 6

 ${f c}$ ) Here we're actually looking for addresses with the same tag and line identifiers, only differing in words: (0001 1010 0001 1010).

In other words, the addresses will range from one whose word bits are the smallest number represented with  $\bf 3$  bits, to the one where it's the largest:

0001 1010 0001 1000 to 0001 1010 0001 1111

**Step 5** 5 of 6

 ${f d}$  ) The cache consists of  $2^5$  lines of  $2^3$  words, so its capacity is:

$$2^5 \times 2^3 = 2^8 B$$
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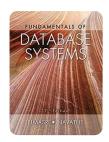
**Step 6** 6 of 6

**e)** The tag bits are needed to specify exactly which memory location the data comes from, since a place in the cache can store data from more than one location.

# Rate this solution



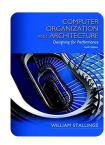
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