e _____

1) Instruction Queue is placed in _____ of Intel 8086.

A) Control and Timing Unit
B) Execution Unit
C) Register File
D) Bus Interface Unit
E) Arithmetic Logic Unit

2) _____ is the act of synchronizing two systems that op

A) Serial communication
B) Handshaking
C) Transmission
D) Parallel communication
E) Peripheral interface

3) Which of the followings are interrupt pins found on Intel micr

I. INTA
II. INTC
III. INTQ
IV. INTR

A) I and IV B) I, III, IV C) Only III

4) Which of the following communication architectures are serial?

I. USB
II. PCI
III. PCI Express
IV. ISA

A) I, II, IV B) I, II, III C) I and III D) Only I

5) Which flag is tested by a conditional interrupt instruction?

A) Interrupt B) Carry C) Parity D) Overflow

6) Regarding SRAM and DRAM, which of the following statements are true?

I. DRAM is faster than SRAM. −
II. SRAM is more expensive than DRAM. +
III. DRAM requires periodical refresh. +
IV. SRAM consumes more power than DRAM. −

A) II and III B) I, II, IV C) Only I D) I and IV

7) What is the IEEE 754 single precision floating point representation of decimal +10.0?

A) 41200000h B) C1A00000h C) 41A00000h D) C1200000h

8) Which of the following statements is not true when an interrupt occurs?

I. Flags register contents are pushed on the stack. +
II. Interrupt flag is set.
III. Contents of CS and IP are pushed onto the stack. +
IV. Related ISR is executed.

A) Only II B) I and III C) III and IV D) II and II

9) Using little endian format, 4321h is to be stored in an 8-bit memory starting at 200 memory address 201h after storing?

A) 34h B) 43h C) 12h D) Empty

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Using the error checking method provided below, detect position of the er

C1 = XOR of bits (1, 3, 5, 7, 9, 11)
C2 = XOR of bits (2, 3, 6, 7, 10, 11)
C4 = XOR of bits (4, 5, 6, 7, 12)
C8 = XOR of bits (8, 9, 10, 11, 12)

A) Bit-2 B) Bit-4 C) Bit-6 D)

11) What is the corresponding value of -76.5 in nearest even rounding mode

A) -77 B) -75 C) -78 D

12) The code below computes the sum of numbers from 1 to N using the for instruction should be inserted into the missing line within the code?

$$\sum_{x=1}^{N} x = N.(N+1)/2$$

```
ORG 100h
CALL sum
RET

sum PROC
MOV AL, N
MOV BL, N
INC BL
MUL BL
missing instruction?
RET
sum ENDP

N DB 8
```

A) DEC AL B) SHR AL, 1 C) SUB AL, 2

DIV AL, 2

13) What is the decimal equivalent of IEEE 754 single precision floating

A) -20.25 B) -40.125 C) -10.50

14) What is the size of Personal Computer I/O map?

64 KB

16) In 8086, 32-bit addition can performed by adding low 16-bits of the operand high 16-bits of the operands using _____ instruction.

A) ADC - SBB
B) ADD - ADC
C) ADC - ADC
D) ADD - ADD
E) ADC - ADD

17) What is the IEEE 754 floating point equivalent of - ∞ ?

A) 10000000011111111111111111111111b
B) 10000000000000000000000000000000b
C) 00000000000000000000000000000000b
D) 11111111100000000000000000000000b
E) 11111111111111111111111111111111b

18) It is given that the following code computes factorial of var_N. Then, wha code?

```
MOV AX, 1
MOV BX, var_N
MOV CX, var_N
label:
MUL BX
missing instruction?
LOOP label
RET
var_N DW 6
```

A) INC AX B) DEC CX C) INC BX

19) Which field of an instruction specifies the addressing mode to be used

A) REG B) R/M C) Direction

20) Assume that CS=1000H, DS=2000H, SS=3000H, and IP=2000H. Then next instruction executed by the microprocessor?

A) 12000H B) 22000H C) 1000H

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21) Which of the following instructions converts any BCD value available in AX register into A
Hint. ASCII equivalent of a BCD code can be obtained by appending $(011)_2$ to left of the BC

A) AND AX, 07h
B) OR AX, 0Fh
C) AND AX, 0Fh
D) XOR AX, 0Fh
E) OR AX, 30h

22) Assume that SP=0100H. What is the value of SP after execution of POP AX instruction?

A) 00FFH B) 0101H C) 0102H D) 00FEH

23) Which of the following communication architectures are parallel?

I. USB
II. PCI
III. PCI Express
IV. ISA

A) I and II B) I, II, III C) I and III D) II and IV

2 G

24) How many (128Mx16) memory device is needed to store 1 G bytes of data?

A) 1 B) 16 C) 2 D) 8

25) Which of the following connections are common to all memory devices?

I. Address
II. Read Control
III. Write Control
IV. Data

A) I, II, IV B) I, II, III, IV C) Only IV D) I, II

E) I and IV