Name Surname : .....

Student Id : ..... Signature:.....

10/04/2017 10:30
Duration: 60 min

Akdeniz University, Engineering Faculty
Computer Engineering Department
CSE206 Computer Organization Midterm Exam

Q 1. *(5pts) Explain the* ***difference*** *between Computer organization and Computer Architecture.*

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Q 2. *(5pts) Define the terms* ***word*** *and* ***wafer****?*

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Q 3. *(10pts) Write the full name of the abbreviated terms considering the context of computer organization.*

a) MBR : .....
b) MAR : .....
c) IBR : .....
d) PC : .....
e) AC : .....
f) ARM : .....
g) QPI : .....
h) MMU : .....
i) RAID : .....
j) SIMD : .....

Q 4. *(10pts) If 20% of an application is performed serially,* ***what is the maximum speedup****? Write the formula and solution.*

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Q 5. *(10pts) Test if the code word* ***011101100011*** *is correct, assuming that it was created using an even parity Hamming Code.*

a) If it is incorrect, indicate what the correct code word should have been.

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b) Indicate what the original data was.

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Q 6. *(20pts) Given the* ***memory contents*** *of the IAS computer shown below:*

Figure 1.

Address	Contents
08A	010FA210FB
08B	010FA0F08D
08C	020FA210FB
08D	

a) *Show the* ***symbolic representation*** *of the program, starting at address* ***08A****. You can find IAS instruction format and IAS Instruction set in* ***Figure 1*** *and* ***Table 2****.*

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b) *Explain what this program does?*

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Q 7. *(15pts) Consider a machine with a byte addressable main memory of* 2^{16} *bytes and block size of 8 bytes. Assume that a direct mapped cache consisting of 32 lines is used with this machine.*

a) *How is a 16-bit memory address divided into tag, line number, and byte number?*

b) *Into what line would bytes with each of the following addresses be stored?*

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0001 0001 0001 1011      ->
1100 0011 0011 0100      ->
1101 0000 0001 1101      ->
1010 1010 1010 1010      ->
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c) *Suppose the byte with address 0001 1010 0001 1010 is stored in the cache. What are the* ***addresses*** *of the other bytes stored along with it?*

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d) *How many total bytes of memory can be stored in the cache?*

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Q 8. *(10pts) Consider a memory system that uses a 32-bit address to address at the byte level, plus a cache that uses a 64-byte line size. Assume a direct mapped cache with a tag field in the address of 20 bits. Show the address format and determine the following parameters: number of addressable units, number of blocks in main memory, number of lines in cache, size of tag.*

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Q 9. *(15pts) Write a program for one-address machine for performing the following operations in sequence. You allowed to use* ***only*** *the list of instructions from Table 1.*

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X = (A + B) * (C - D);
Y = X / (A * D);
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Table 1 One-address instructions

1 Address Instructions
LOAD M
STORE M
ADD M
SUB M
MUL M
DIV M

Table 2 The IAS Instruction Set

Instruction Type	Opcode	Symbolic Representation	Description
Data transfer	00001010	LOAD MQ	Transfer contents of register MQ to the accumulator AC
	00001001	LOAD MQ,M(X)	Transfer contents of memory location X to MQ
	00100001	STOR M(X)	Transfer contents of accumulator to memory location X
	00000001	LOAD M(X)	Transfer M(X) to the accumulator
	00000010	LOAD – M(X)	Transfer –M(X) to the accumulator
	00000011	LOAD |M(X)|	Transfer absolute value of M(X) to the accumulator
	00000100	LOAD – |M(X)|	Transfer –|M(X)| to the accumulator
Unconditional branch	00001101	JUMP M(X,0:19)	Take next instruction from left half of M(X)
	00001110	JUMP M(X,20:39)	Take next instruction from right half of M(X)
Conditional branch	00001111	JUMP + M(X,0:19)	If number in the accumulator is nonnegative, take next instruction from left half of M(X)
	00010000	JUMP + M(X,20:39)	If number in the accumulator is nonnegative, take next instruction from right half of M(X)
Arithmetic	00000101	ADD M(X)	Add M(X) to AC; put the result in AC
	00000111	ADD |M(X)|	Add |M(X)| to AC; put the result in AC
	00000110	SUB M(X)	Subtract M(X) from AC; put the result in AC
	00001000	SUB |M(X)|	Subtract |M(X)| from AC; put the remainder in AC
	00001011	MUL M(X)	Multiply M(X) by MQ; put most significant bits of result in AC, put least significant bits in MQ
	00001100	DIV M(X)	Divide AC by M(X); put the quotient in MQ and the remainder in AC
	00010100	LSH	Multiply accumulator by 2; that is, shift left one bit position
	00010101	RSH	Divide accumulator by 2; that is, shift right one position
Address modify	00010010	STOR M(X,8:19)	Replace left address field at M(X) by 12 rightmost bits of AC
	00010011	STOR M(X,28:39)	Replace right address field at M(X) by 12 rightmost bits of AC

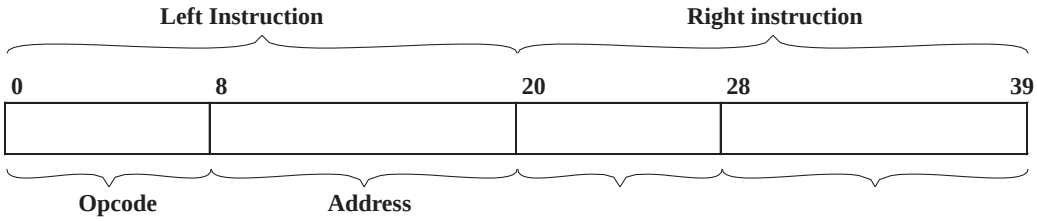

Figure 1. IAS Instruction format