Emulation FAQ

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Emulation FAQ

Hardware

How should the connection to the TRST signal be terminated?

There is some confusion about the termination of the JTAG TRST signal. This signal is also called the nTRST signal, referring to the fact that the logic is inverted. When TRST is high, the emulation logic is out of reset. When TRST is low, the emulation logic is in reset.

The databooks on TI devices report that *the DSP includes an internal pulldown (IPD) on the TRST pin to ensure that TRST will always be asserted on power up, and the DSP's internal emulation logic will always be properly initialized when this pin is not routed out. JTAG Controllers from Texas Instruments actively drive TRST high. However some third-party JTAG controllers may not drive TRST high, but expect the user of an external pullup resitor on TRST. When using this type of JTAG controller, assert TRST to initialize the DSP after powerup and externally drive TRST high before attempting any emulation or boundary scan operations"*

There has been confusion as to whether this means that a external pullup should be used or not used. **An external pullup resistor should NOT be used.** This simply means that for third-party JTAG controllers to work, logic must be added to the board which drives TRST high to initialize the emulation logic.

I am using OMAPL1xx, where can I look?

- A: OMAP-L1x JTAG

Any information about TMS320C671x?

- A: TMS320C671x Emulation boot

Software

Q: Is there some way to step two processors simultaneously/parallel?

- A: Yes, please check Multi-Core Debug with CCS or by using the parallel debug manager in CCS 3.3.

Q: Is there a way to load a COFF (OUT) file without using or installing CCStudio?

- A: Yes, Blackhawk has a stand alone program load utility, **BHLoader**, available here (http://www.blackhawk-dsp.com/products/emusoftware.aspx).

Q: Where can I learn about Connect / Disconnect?

- A: Emulation Connect/Disconnect

Q: My CPU is hung, what can I do?

- A:
- See Emulation Connect/Disconnect
- See Emulation FAQ
- See Debugging JTAG Connectivity Problems
- See Emulation Force Ready

References: Other places to look for information

There is a page on Debugging JTAG Connectivity Problems.

What are the advantages to programming AET with Aetlib over programming it with the CCStudio Plugin?

- Dynamic programming and reuse of AET resources
  - AET resources can be reclaimed and reprogrammed at run time. Programming AET from Code Composer Studio requires load-time configuration and no reuse. With CCS, all addresses must be known at load time, which makes it impossible to trigger on execution of a dynamically allocated thread or task.
- Context based AET use
  - AET can be enabled/disabled based on a particular context (i.e. single thread, etc)

Where can I find Documentation and Examples for using Aetlib?

All of the necessary documentation and examples are included in the release package. See the Help documents under the doc folder and a number of examples under the examples folder.

Can Aetlib be used to allow AET to trigger interrupts?

AETLIB can be used to generate an interrupt based on an AET event. There's an example included with AETLIB that accomplishes this. It's called slice_watchpoint_in_range, and uses the slice applicaiton to generate an interrupt when a specified data range is written to.

A few things to keep in mind....`

- The only interrupt that can be generated by AET is the RTOS interrupt. Many people ask if they can generate an NMI or some other interrupt with AET, but that's not possible.
- Due to a design flaw in the 64x (Kelvin) devices, you must use an emulator/debugger. With the 64x+ (Joule/Full-Gem) devices, it can be used entirely without an emulator attached.

Which ISAs does AETLIB support?

At present AETLIB supports the c64x and c64xPlus Instruction Set Architectures.

Can all of the system events be used as the trigger event when using TRACE ON EVENT?

Yes, any of the system events can be used as the trigger event when using TRACE ON EVENT. Keep in mind that during a single session you can only use events from the same family. There are 3 families, Memory Events, Stall Events, and Miscellaneous/System Events

For the AETLib, some functions are invalid on C64x DSPs. Do we have a list to clarify which functions are invalid on C64x DSPs

Any functions which are not supported by the AET hardware on a 64x DSP are obviously not supported on the 64x device. These include triggering on events and anything that uses the watermark counter.

If a data breakpoint is set with datasize as BYTE|HALFWORD, and an access occurs with access size WORD, will it trigger the breakpoint?

No, it will not trigger the breakpoint. If you want "ANY" write to trigger the breakpoint, then you must logically OR all of the write sizes together in the datasize value.(NOTE: This FAQ applies to AET, but not AETLIB specifically. In AETLIB, there is no ability to specify the write size. AETLIB always uses "ANY" as the write size. This is a limitation that was consciously chosen in order to align with the majority of use cases, and to reduce the complexity and memory footprint of AETLIB)

When an AET Job is configured with an RTOS trigger, is it re-armed by AET logic or does it have to be re-armed explicitly by application? If so, what is the procedure to re-arm?

Yes, once the "RTOS" interrupt is triggered, it should be cleared in the Interrupt Service Routine that services it. There is an API provided in aet.h to enable this. The API is AET_CLEAR_RTOS_INT();

Once an AET_releaseJob() is issued, are those resources available to be reused by the application or is it also necessary to issue an AET_release() command before those resources can be reassigned?

The AET_releaseJob() API reclaims all resources used in the job being released so that they can be used again in future jobs. The AET_release() API releases ownership of the AET unit So, the answer to this specific question is yes, as soon as AET_releaseJob() is called, the resources from the job being released are immediately available to be reassigned. = XDS560 TraceFAQ =

When using TraceDisplay, what's the meaning of the up/down arrow in the beginning of each line?

These are indicators of a PC Discontinuity in the Trace Output. They are implemented with reverence to an address page that would have 0x0 at the top, and 0xFFFFFFFF at the bottom. An up arrow indicates a discontinuity to a lower address. A down arrow indicates a discontinuity to a higher address.

Where can I learn more about XDS560 Trace?

- http://focus.ti.com/docs/toolsw/folders/print/xds560trace.html
- http://www.blackhawk-dsp.com/Usb560t.aspx

Can I use XDS560 Trace with just a standard XDS560?

- Yes, with the embedded trace buffer (ETB) please check this page about the Embedded Trace Buffer

What do I need to do to design in the XDS560 Trace Header?

- Yes, please check this presentation. Trace_Header_Design-ext.pdf

How much memory is available on the XDS560 Trace Buffer?

- Initially, the XDS560 Trace Buffer supported only 224Kb of memory. Now, extended buffer memory is available through a software update. The new Extended Buffer Memory (EBM) is user configurable between 256K abd 64Mb (in increments of 256k)

I've been using the standard Trace with 224Kb memory capacity. What needs to be done to get access to the 64mB Extended Buffer Memory?

- Nothing needs to be done to the Trace Pod, all trace Pods have the Full 64Mb of memory. However, a software update is needed, and it's contained in CCS 3.3 SR8 (or later)

How do I configure the size of the XDS560 Trace Extended Buffer Memory?

- This setting can be found in the dialog obtained by selecting Tools->XDS560 Trace->Control. There is a drop-down box which enables the selection.

What is the XDS560 Emulator?

- Please see this link for more information XDS560.

Where can I learn more about how to turn the trace system on and off?

- Please see the Advanced Event Triggering or Unified Breakpoint Manager for details.

I am having trouble with my JTAG connection. Where can I learn how to find and fix the problem?

- For debugging issues with JTAG, you may want to check the topic Debugging JTAG Connectivity Problems

Does the XDS560 Trace unit support HSRTDX?

- No, the XDS560 Trace pod does not support HSRTDX.

How can I turn on Logging for Trace for TI support?

- Set the environment variable TI_TRACE_LOGGING to be equal to 6.
- To turn on trace logging in Windows:

1. Quit CCS.
2. Right click on the “MyComputer” icon on your desktop.
3. Select “Properties”.
4. In the System Properties dialog, click on the “Advanced” tab.
5. In the Advanced tab, click on the “Environment Variables” button.
6. In the “Environment Variables” dialog, under the “User variables” group, verify that the “TI_TRACE_LOGGING” environment variable exists and has a value of 6. Create it if it is not there.
7. Click “OK” in all dialogs.

8. Restart CCS.
9. Reproduce the problem, noting what steps were performed in what order.
10. If the problem is in the trace data:
    1. Send the C:\Users\UserName\.TI-trace\ti_trace_log_MMDDYY_PID.txt file.
    2. Zip file of Trace Analyzer/Display TDF file
    3. Application .OUT file (optional)

Can I get Trace if I use the simulator?

- Please see PDATS Trace

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