Design and implementation of a simple Multi-Cycle Processor.

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1 Problem statement

Design and Implement an 8-bit Processor on Digilent BASYS3 FPGA Board. Target device is Xilinx Artix-7 XC7A35T- ICPG236C (Family Artix-7, Part XC7A35T, Package CPG236, Speed Grade -1). The Processor is 8-bit RISC with 8-bit Address space. Processor is Multi-cycle processor, which does fetch, decode, execution, and write stages sequentially.

It should support minimal arithmetic, logic and branch instructions with program counter and stack pointer. It need not have external interrupts or exception handling. Most Instructions can be of length 1 byte supporting 4 Registers. Branch instruction is a 2-byte instruction supporting 1 byte for op-code and another for address. Test the processor with a multiplication algorithm doing shift and add in a loop.

Design the Datapath block schematic and FSM state diagram first. Then do the HDL coding. Give the IO Constraints and Timing Constraints to achieve maximum delay performance. Do the Timing Analysis and Timing simulation with proper testbench. Refer to the User manual of BASYS3 Board for resources available, external circuit, and pin numbers where external resources are connected. Use LVCMOS33 IO standard on pins. You can do the pin assignment and give timing constraints using GUI or manually creating xdc file in proper format and adding it to the project. Explain the context of the experiment here. Why is condensed matter physics interesting or important? Optional things you could talk about (but don't have to – this is up to you): transistors, computers, Quantum computers, fundamental knowledge (e.g. the resistance quantum).

2 Basic Block Diagram

2.1 Data path and control path

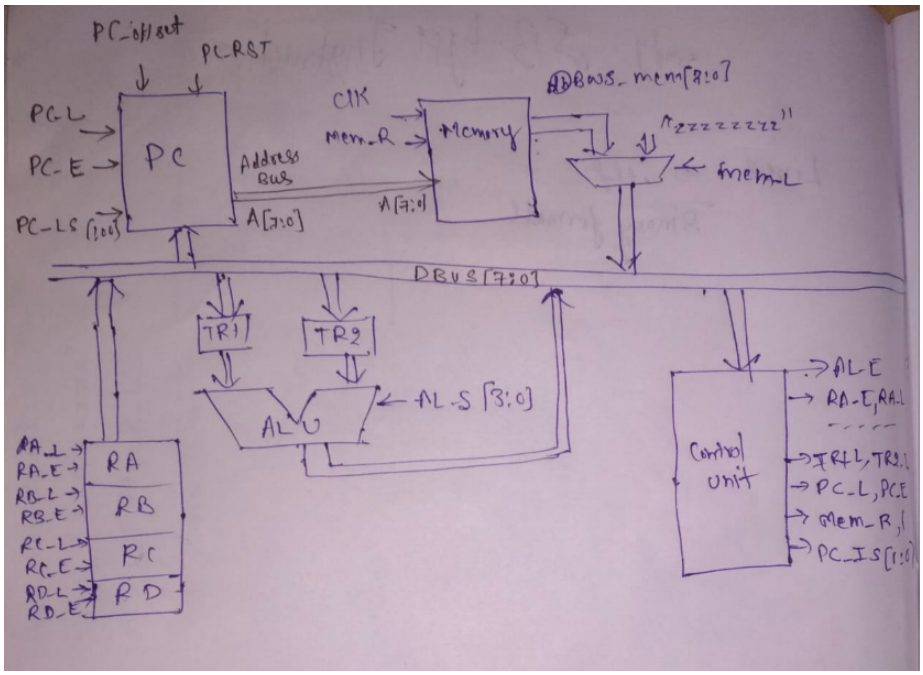

Figure 1: Data path and control path.

2.2 Program Counter

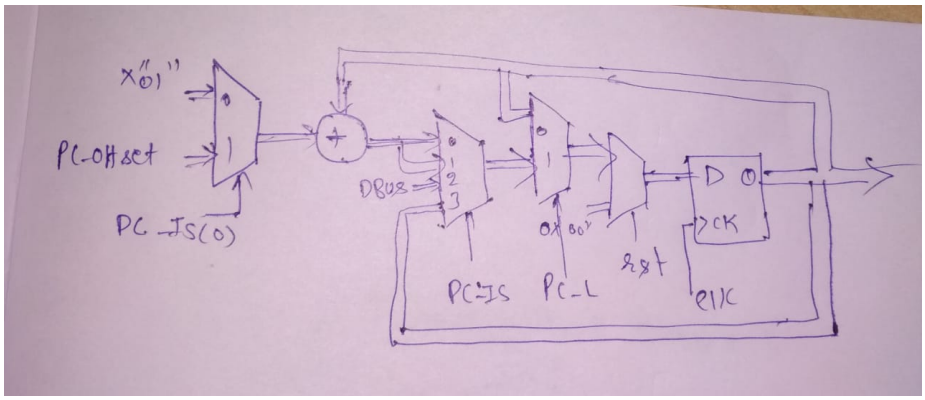

Figure 2: Program Counter.

2.3 Register

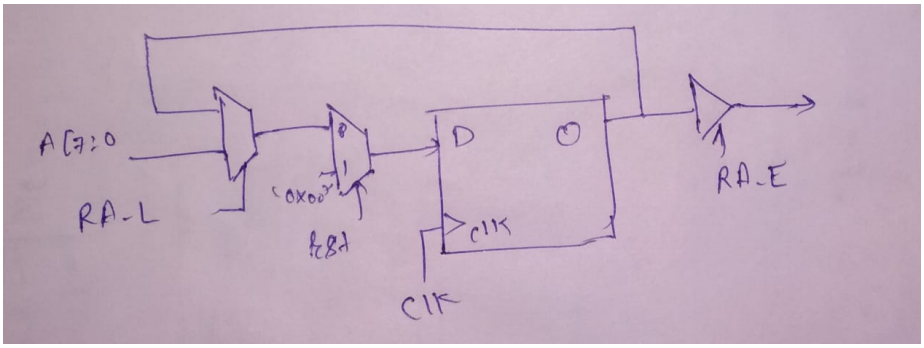

Figure 3: Registers.

2.4 Controller design

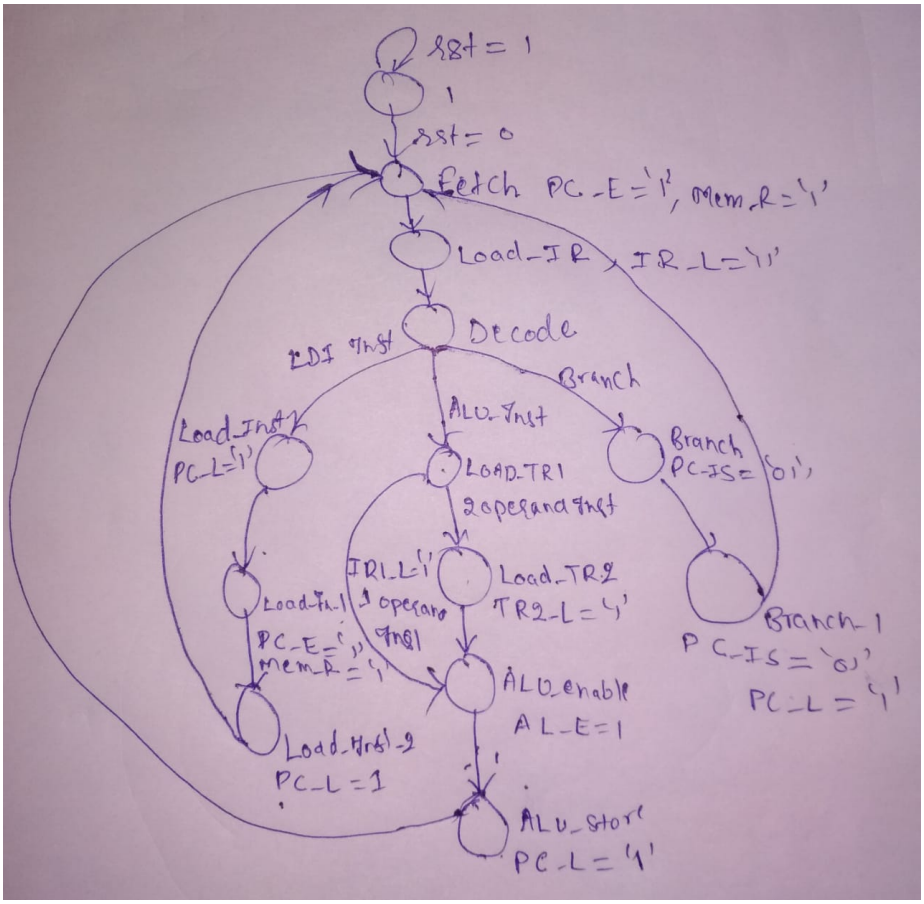

Figure 4: FSM state diagram.

3 CPU Specifications:

CPU specifications are:

- 8 Bit Address Space
- 8 Bit Separate Data Bus
- 8 Bit Program Counter
- Four 8 Bit Registers

3.1 Instruction Set

Instruction	Opcode
AND	0
OR	1
XOR	2
XNOR	3
ADD	4
SUB	5
SRA	6
SLA	7
SRL	8
INC	9
DEC	A
BIZ	B
BNZ	C
NOP	D
NOP	E
LDI	F

Table 1: Instruction Set.

3.2 Instruction format for R type instructions

Opcode[7:4]	Operand1[3:2]	Operand2[1:0]

3.3 Instruction format for J type instructions

Opcode[7:4]	XX	Offset[3:0]

3.4 Single Operant Instruction

Opcode[7:4]	Operand1[3:2]	XX

4 Testing by Multiplication of two numbers

Assembly code	Instruction in hex
LDI RA, #04	F0, 04
LDI RB, #06	F4, 06
LDI RC, #00	F8, 00
LOOP: ADD RC,RB	46
DEC RA	A0
BNZ LOOP	CE
NOP	D0

Table 2: Instruction Set.

5 Results

8 bit multi-cycle processor was designed , synthesized and implemented successfully. Its functionality was tested successfully by using multiplication.

5.1 Timing Report

Timing constraints was given as a clock period of 10ns and the worst negative slack was found to be 3.01 ns.There were no other timing violations. So the maximum frequency the circuit can operate is 143Mhz.

Design Timing Summary

Setup		Hold		Pulse Width	
Worst Negative Slack (WNS):	3.026 ns	Worst Hold Slack (WHS):	0.237 ns	Worst Pulse Width Slack (WPWS):	4.500 ns
Total Negative Slack (TNS):	0.000 ns	Total Hold Slack (THS):	0.000 ns	Total Pulse Width Negative Slack (TPWS):	0.000 ns
Number of Failing Endpoints:	0	Number of Failing Endpoints:	0	Number of Failing Endpoints:	0
Total Number of Endpoints:	102	Total Number of Endpoints:	102	Total Number of Endpoints:	82

All user specified timing constraints are met.

Figure 5: Timing Summary

5.2 Utilization Report

Name	Slice LUTs (20800)	Slice Registers (41600)	F7 Muxes (16300)	Slice (8150)	LUT as Logic (20800)	LUT Flip Flop Pairs (20800)	Block RAM Tile (50)	Bonded IOB (106)	BUFGCTRL (32)
TOP_MODULE	125	94	8	45	125	32	0.5	10	1
alu1 (ALU)	43	24	0	26	43	8	0	0	0
block_ram (blk_me...	0	0	0	0	0	0	0.5	0	0
cnt1 (controller)	77	28	8	38	77	11	0	0	0
pc1 (Program_coun...	5	8	0	5	5	1	0	0	0
RA (Reg_A)	0	8	0	2	0	0	0	0	0
RB (Reg_A_0)	0	8	0	2	0	0	0	0	0
RC (Reg_A_1)	0	8	0	2	0	0	0	0	0
RD (Reg_A_2)	0	8	0	2	0	0	0	0	0

Figure 6: Utilization Summary

Summary

Resource	Utilization	Available	Utilization %
LUT	125	20800	0.60
FF	94	41600	0.23
BRAM	0.50	50	1.00
IO	10	106	9.43

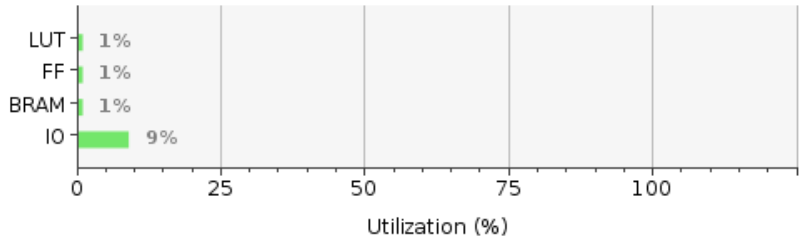

Figure 7: Utilization Summary

6 Simulation

6.1 Behavioral simulation

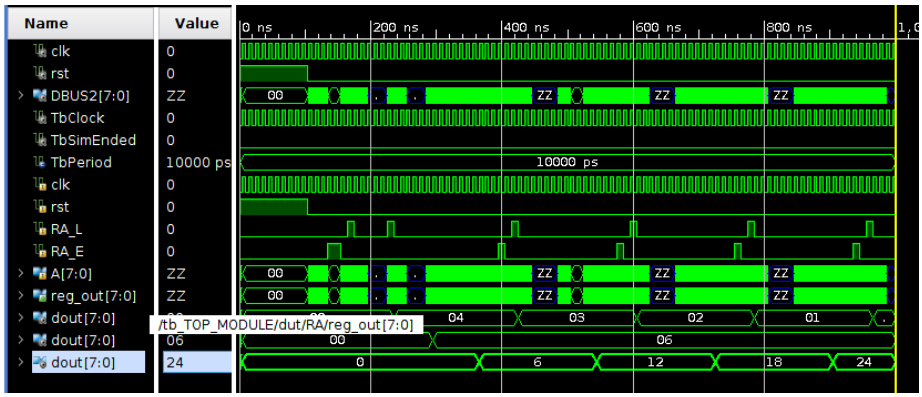

Figure 8: Behavioral simulation

6.2 Post implementation timing simulation

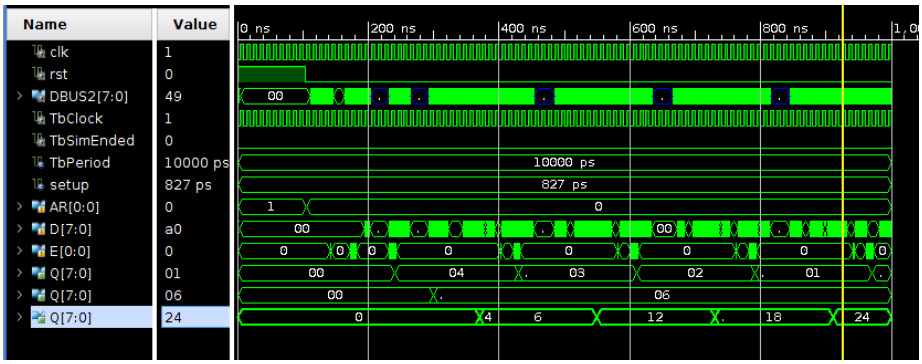

Figure 9: Post implementation timing simulation