Design and Implementation of a Pipelined 32-bit RISC-V Processor.

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1 Problem statement

Implement the pipelined RISC-V processor. Board. Processor should support basic arithmetic-logic instructions, branch instructions and load-store instructions. You need to implement only the user mode of RISC-V. Test the processor with a suitable algorithm. Target Device is Xilinx Artix-7 XC7A35T-ICPG236C (Family Artix-7, Part XC7A35T, Package CPG236, Speed Grade -1). The Processor is 32-bit RISC-V Processor. Design the Datapath block schematic first and then pipelined processor.

2 Basic Block Diagram

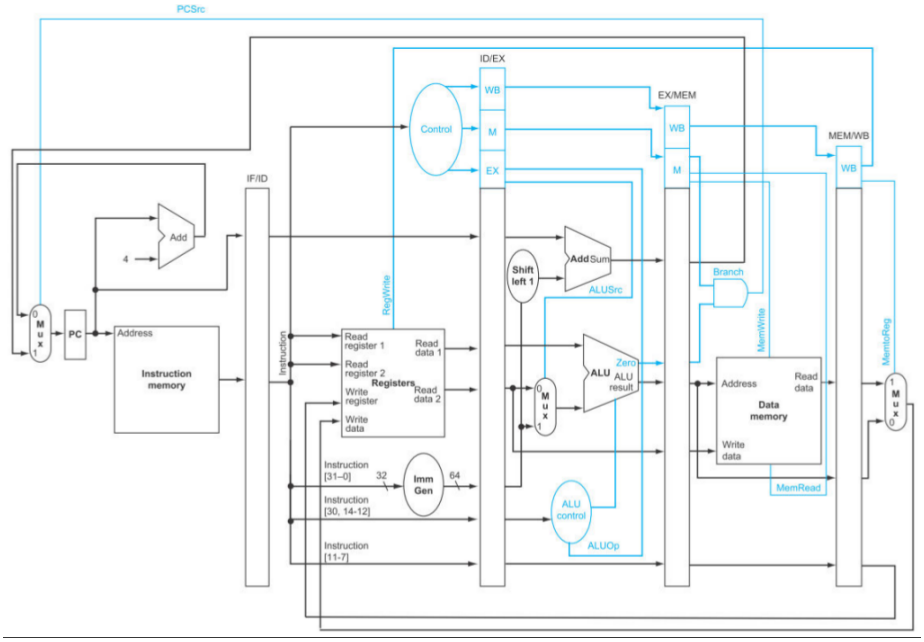

Figure 1: Data path and Control Signals.

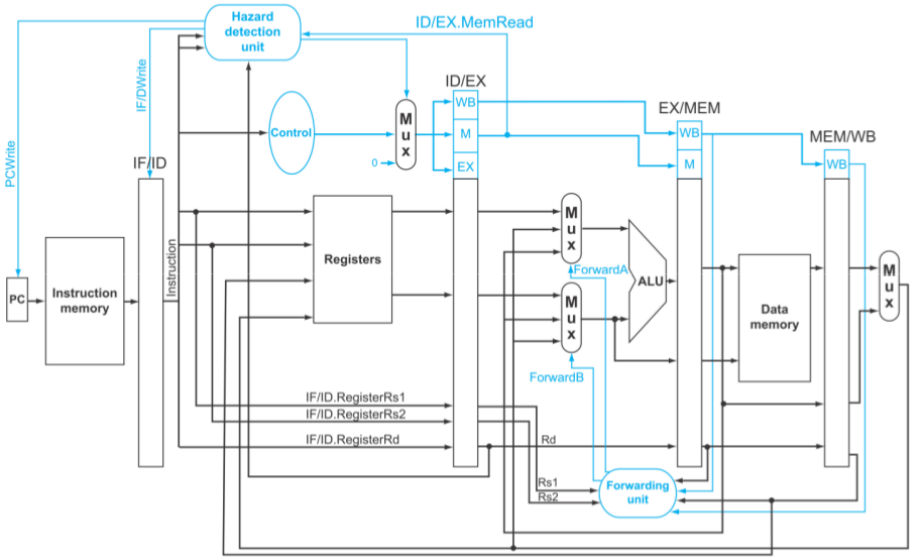

Figure 2: Forwarding and Hazard Detection.

3 CPU Specifications:

CPU specifications are:

- 5 Stages of pileline
- 32-Bit Address Space
- 32-Bit Separate Data Bus
- 32-Bit Program Counter
- 32 32-Bit Registers

4 Testing by Multiplication of two numbers

Assembly code	Instruction in hex
ld x1, 0(x2)	00013083H
ld x2, 1(x0)	00103103H
ld x3, 3(x0)	00303183H
LOOP: subx1, x1, x3	40308033H
add x4, x4, x2	00220233H
beq x1, x0, EXIT	00008263H
beq x0, x0, LOOP	FE000DE3H
EXIT: NOP	00000000H

Table 1: Program for multiplication of two numbers

5 Results

32-bit Pipelined Processor was designed , synthesized and implemented successfully. Its functionality was tested successfully by using multiplication.

5.1 Timing Report

Timing constraints was given as a clock period of 40ns and the worst negative slack was found to be 26.24 ns.There were no other timing violations. So the maximum frequency the circuit can operate is 72.7Mhz.

Design Timing Summary

Setup		Hold	
Worst Negative Slack (WNS):	26.245 ns	Worst Hold Slack (WHS):	0.022 ns
Total Negative Slack (TNS):	0.000 ns	Total Hold Slack (THS):	0.000 ns
Number of Failing Endpoints:	0	Number of Failing Endpoints:	0
Total Number of Endpoints:	996	Total Number of Endpoints:	996

All user specified timing constraints are met.

Figure 3: Timing Summary

5.2 Utilization Report

Summary

Resource	Utilization	Available	Utilization %
LUT	558	20800	2.68
LUTRAM	64	9600	0.67
FF	453	41600	1.09
IO	10	106	9.43

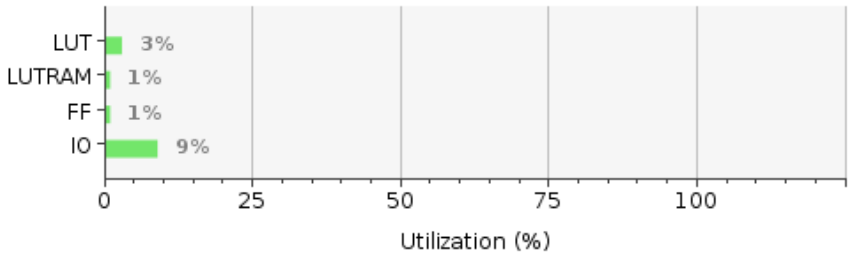

Figure 4: Utilization Summary

6 Simulation

6.1 Behavioral simulation

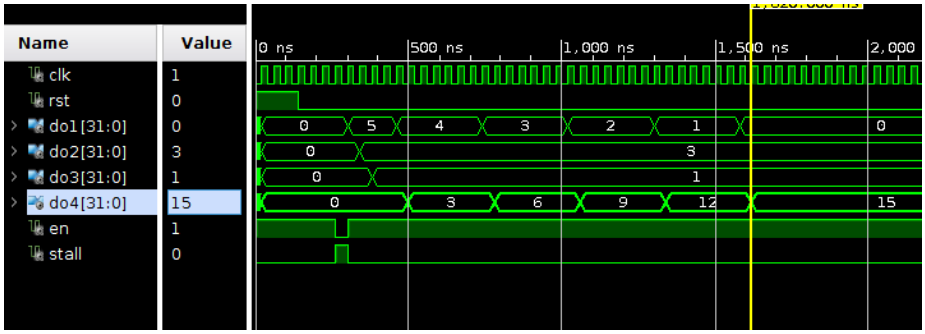

Figure 5: Behavioral simulation

6.2 Post implementation timing simulation

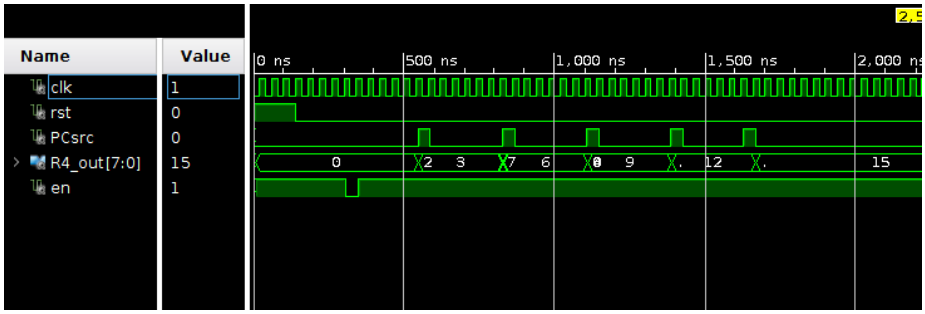

Figure 6: Post implementation timing simulation