Design and implementation of a Single Cycle 32-bit RISC-V processor Processor.

DOLA RAM, 15197, DESE

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1 Problem statement

Board. Target Device is Xilinx Artix-7 XC7A35T- ICPG236C (Family Artix-7, Part XC7A35T, Package CPG236, Speed Grade -1). The Processor is 32-bit RISC-V Processor. Processor should support basic arithmetic-logic instructions, branch instructions and load-store instructions. You need to implement only the user mode of RISC-V. Test the processor with a suitable algorithm, check if you can write the program in C and get the required assembly/binary code and use it. Design the Datapath block schematic first. Then do the HDL coding. Give the IO Constraints and Timing Constraints to achieve maximum delay performance. Do the Timing Analysis and Timing simulation with proper testbench. Refer to the User manual of BASYS3 Board for resources available, external circuit, and pin numbers where external resources are connected. Use LVCMOS33 IO standard on pins. You can do the pin assignment and give timing constraints using GUI or manually creating "xdc" file in proper format and adding it to the project.

2 Basic Block Diagram

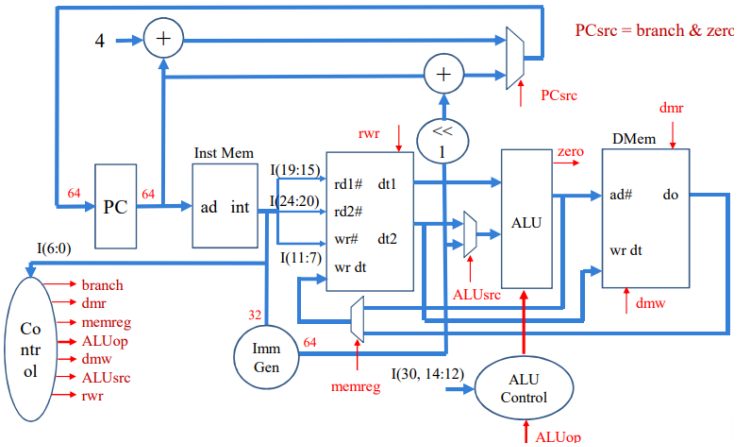

Figure 1: Data path and Control Signals.

3 CPU Specifications:

CPU specifications are:

- 32-Bit Address Space
- 32-Bit Separate Data Bus
- 32-Bit Program Counter
- 32 32-Bit Registers

4 Testing by Multiplication of two numbers

Assembly code	Instruction in hex
ld x1, 0(x2)	00013083H
ld x2, 1(x0)	00103103H
ld x3, 3(x0)	00303183H
LOOP: subx1, x1, x3	40308033H
add x4, x4, x2	00220233H
beq x1, x0, EXIT	00008263H
beq x0, x0, LOOP	FE000DE3H
EXIT: NOP	00000000H

Table 1: Program for multiplication of two numbers

5 Results

32-bit Single-cycle Processor was designed , synthesized and implemented successfully. Its functionality was tested successfully by using multiplication.

5.1 Timing Report

Timing constraints was given as a clock period of 40ns and the worst negative slack was found to be 24.01 ns.There were no other timing violations. So the maximum frequency the circuit can operate is 62.5Mhz.

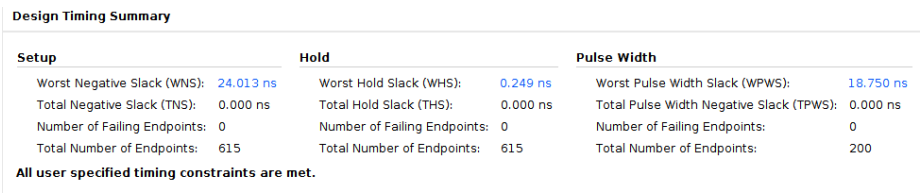

Figure 2: Timing Summary

5.2 Utilization Report

Name	Slice LUTs (20800)	Slice Registers (41600)	Slice (8150)	LUT as Logic (20800)	LUT as Memory (9600)	LUT Flip Flop Pairs (20800)	Bonded IOB (106)	BUFGCTRL (32)
CPU	375	144	119	311	64	30	10	1
ALU_Control1 (ALU_...)	17	5	15	17	0	1	0	0
CU (Control_Unit)	5	4	5	5	0	1	0	0
DMem1 (DMem)	128	0	45	64	64	0	0	0
PC1 (PC)	219	7	77	219	0	6	0	0
REG1 (REG_N)	6	128	69	6	0	0	0	0

Figure 3: Utilization Summary

Resource	Utilization	Available	Utilization %
LUT	375	20800	1.80
LUTRAM	64	9600	0.67
FF	144	41600	0.35
IO	10	106	9.43

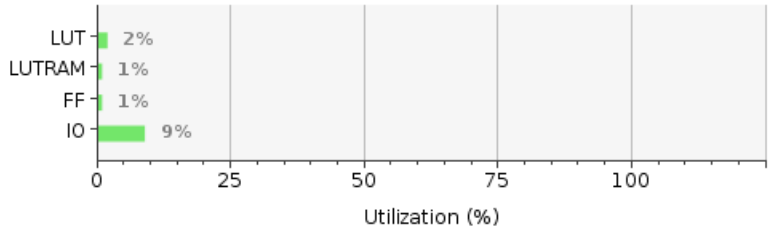

Figure 4: Utilization Report

6 Simulation

6.1 Behavioral simulation

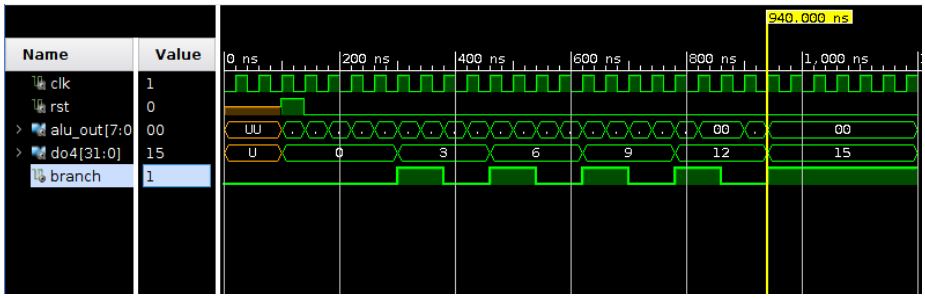

Figure 5: Behavioral simulation

6.2 Post implementation timing simulation

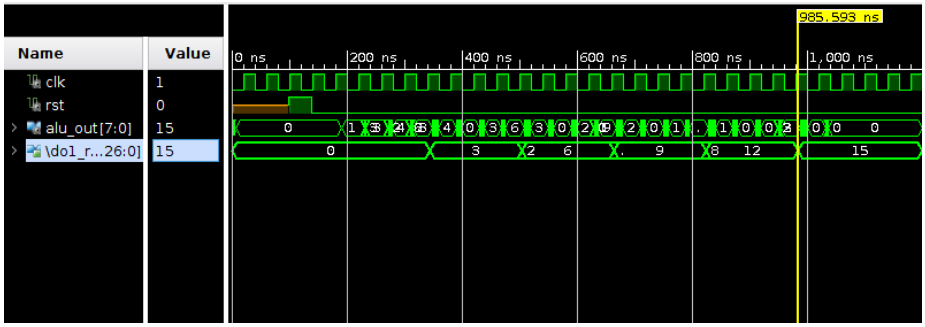

Figure 6: Post implementation timing simulation