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Optimization	"-O0”	"-O1”	“-O2”
# Dynamic Instructions	1326980	305135	261935
Num Mem Reads	354001	45582	44342
Num Mem Writes	73058	28950	27710
Num Reg Reads	2968155	728266	613716
Num Reg Writes	2512287	521319	439949
Forward Branches Taken	9010	8651	8001
Forward Branches Not Taken	461	11220	5210
Backward Branches Taken	41650	37569	39109
Backward Branches Not Taken	9741	1681	1801
4 Byte Block Hits	377632	52096	49918
4 Byte Block Misses	30243	22354	22052
4 Byte Block Hit Rate	92.59%	69.97%	69.36%
8 Byte Block Hits	383482	59712	57560
8 Byte Block Misses	24393	14738	14410
8 Byte Block Hit Rate	94.02%	80.20%	80.00%
16 Byte Block Hits	382199	62343	60231
16 Byte Block Misses	25676	12107	11739
16 Byte Block Hit Rate	93.71%	83.74%	83.70%
32 Byte Block Hits	371018	63907	61685
32 Byte Block Misses	36857	10543	10285
32 Byte Block Hit Rate	90.96%	85.84%	85.71%
64 Byte Block Hits	347467	63320	60971
64 Byte Block Misses	60408	11130	10999
64 Byte Block Hit Rate	85.19%	85.05%	84.72%
128 Byte Block Hits	296780	47661	45232
128 Byte Block Misses	111095	26789	26738
128 Byte Block Hit Rate	72.76%	64.02%	62.85%
256 Byte Block Hits	242527	11798	9715
256 Byte Block Misses	165348	62652	62255
256 Byte Block Hit Rate	59.46%	15.85%	13.50%

If I were building a processor and had to do static branch prediction, I would design a compiler that could do multiple compilation passes. By doing multiple passes keeping track of the number of forward and backward branches and the number of branch misses and hits programs can be compiled to minimize the number of branches taken in total and in many situations decrease the total instruction count.

From the results of the Shang statistics, if I built a system with a 256-byte direct-mapped cache, I would shoose the 16-byte block since it provides the highest hit percentage.

When compiling with optimization, using various techniques, the compiler will can speed up the program by reorganizing code to reduce branches and number of instructions. While these techniques may not be the most efficient with the use of registers and memory, or cache, it is clear that instruction structure plays a factor in program optimization.