

CMS TECHNICAL DESIGN REPORT FOR THE PHASE 1 UPGRADE OF THE HADRON CALORIMETER

This report describes the technical design and outlines the expected performance of the Phase 1 Upgrade of the CMS Hadron Calorimeters. The upgrade is designed to improve the performance of the calorimeters at high luminosity with large numbers of pileup events by increasing the depth-segmentation of the calorimeter and providing new capabilities for anomalous background rejection. The photodetectors of the CMS Barrel and Endcap Hadron Calorimeters, currently hybrid photodiodes (HPDs), will be replaced by silicon photomultiplier (SiPM) devices. The single-channel phototubes of the Forward Hadron Calorimeter will be replaced by multi-anode phototubes operated in a dual-anode configuration. The readout electronics for all three calorimeter systems will also be replaced. A new charge-integrating ADC, the QIE10, with an integrated TDC will be used along with a 4.8 Gbps data-link. The off-detector electronics will also be substantially upgraded to handle higher data volumes and improve the information sent to the calorimeter trigger system. The expected performance of these upgrades is discussed, including a detailed study of several Higgs and SUSY analyses. The planning for the implementation of this upgrade is presented, including construction, testing, and installation.

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Finally, we dedicate this technical design report for the phase 1 upgrade of the HCAL subdetectors to the memory of our colleague John Elias.

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Chapter 1

Overview of the Upgrade of the Hadron Calorimeters

The proposed upgrade of the CMS Hadron Calorimeters will support full performance of the CMS experiment at the high instantaneous luminosities and total integrated doses which are now predicted based on the strong performance of the LHC accelerator. This upgrade takes advantage of new technologies that have become available since the design and construction of the original calorimeters and improves the performance of the calorimeters as built, primarily through the replacement of the phototransducers and electronics. It will also address and mitigate many of the weaknesses that have been identified in the current systems.

1.1 Performance and Schedule of the LHC

The physics program at the Large Hadron Collider (LHC) began in 2009 with pp collisions at a center of mass (CM) energy of 7 TeV. By the end of 2011, a data sample with integrated luminosity of 6 fb^{-1} was collected by CMS. The CM energy was increased to 8 TeV and at the time of writing (August 2012) a further 11 fb^{-1} integrated luminosity has been delivered, with instantaneous peak luminosities approaching $7 \times 10^{33} \text{ cm}^{-2}\text{s}^{-1}$. The excellent performance of LHC through this period of operation is summarized in Fig. 1.1. Throughout this period, the LHC has operated with bunch trains with 50 ns bunch spacing.

Current planning for the LHC and injector chain foresees a series of three long shutdowns, designated LS1, LS2, and LS3. In LS1 (in the period 2013-2014), the CM energy will be increased to 14 TeV (or slightly lower). In the period through LS2 (2018), the injector chain will be improved and upgraded to deliver very bright bunches (high intensity and low emittance) into the LHC. In LS3 (2022), the LHC itself will be upgraded with new low- β triplets and crab-cavities to optimize the bunch overlap at the interaction region. The original performance goal for the LHC, to operate at an instantaneous luminosity of $1 \times 10^{34} \text{ cm}^{-2}\text{s}^{-1}$ with 25 ns bunch spacing, is likely to be achieved soon after LS1. Under these conditions, CMS will experience an average of about 25 inelastic interactions per bunch crossing (referred to as event pile-up). This is the operating scenario for which the CMS experiment was designed. Based on the excellent LHC performance to date, and the upgrade plans for the accelerators, it is anticipated that the peak luminosity will be close to $2 \times 10^{34} \text{ cm}^{-2}\text{s}^{-1}$ before LS2, and perhaps significantly higher after LS2. Delivering high bunch brightness will be more challenging with 25 ns bunch spacing than with 50 ns. While the plan is to operate at 25 ns after LS1, further 50 ns operation cannot be ruled out at this time.

As a result, CMS must be prepared to operate for the rest of this decade with average event pile-up ($\langle \text{PU} \rangle$) of 50 as a baseline, with the possibility that it may be significantly higher at the

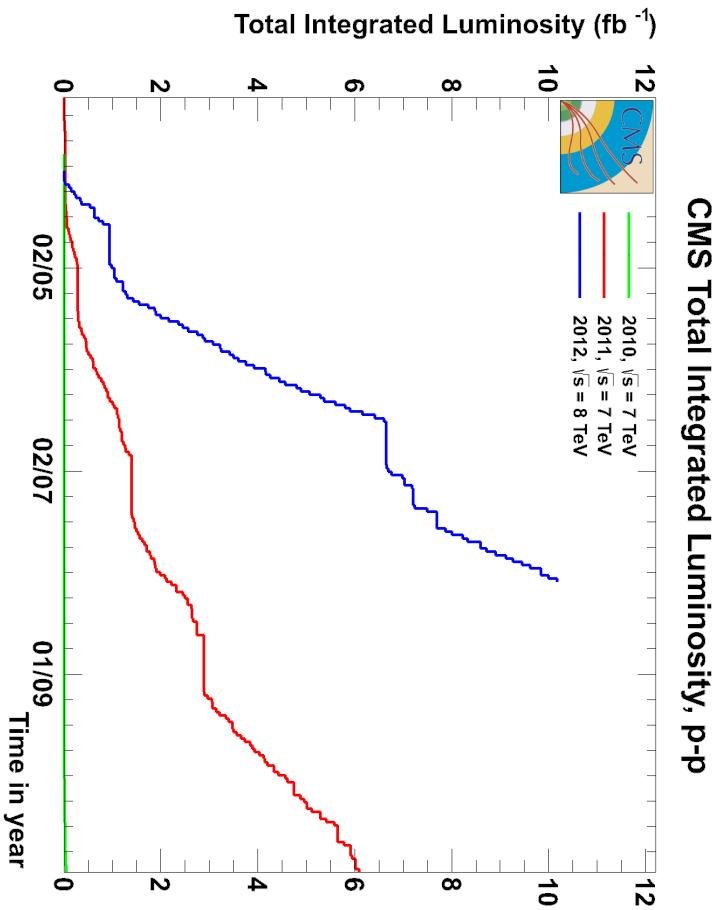


Figure 1.1: Luminosity performance of LHC over the period 2010-2012.

beginning of LHC fills. Higher PU causes increased fake rates in tracking, reduced resolution in calorimetry with contamination due to overlapping signals. The total integrated luminosity prior to LS2 will reach of order 200 fb^{-1} , with 500 fb^{-1} achieved by LS3. The goal for the High Luminosity LHC program (HL-LHC) is to deliver a further 2500 fb^{-1} beyond LS3. In this period $\langle \text{PU} \rangle$ will be well over 100 for the entire fill, with luminosity leveling employed. With the higher CM energy and very high luminosities beyond LS1, and with the recent discovery of a boson at a mass of 125 GeV [1], the CMS physics program will include both searches for new physics and at the same time measuring the couplings of the new boson in many decay modes. The detector performance, with good reconstruction efficiency at relatively low transverse energy, must be maintained even at a PU several times higher than the original design specification. This is the goal of the CMS upgrade program. Through LS2, three major upgrades are planned: a replacement of the pixel detector with a four-layer high-data-rate design, improvement to the L1-Trigger system with higher granularity and additional processing capabilities, and an upgrade to the photo-detectors and electronics for the hadron calorimeters (HCAL) to reduce background signals and improve measurement of jets and missing-energy at high PU. The HCAL upgrade is the subject of this document.

1.2 Review of the Existing Calorimeters

To set the upgrade in an overall context of the CMS physics program, it is useful to briefly review the design and operation of the current CMS hadron calorimeters. The CMS hadron calorimetry system (HCAL) has four major sections: the HCAL Barrel (HB), HCAL Endcap (HE), HCAL Outer (HO), and HCAL Forward (HF). The locations of each of these calorimeters are shown in the overall context of CMS in Fig. 1.2. The HB and Endcap HE calorimeters [2] are sampling calorimeters which use brass as the absorber and plastic scintillator as the

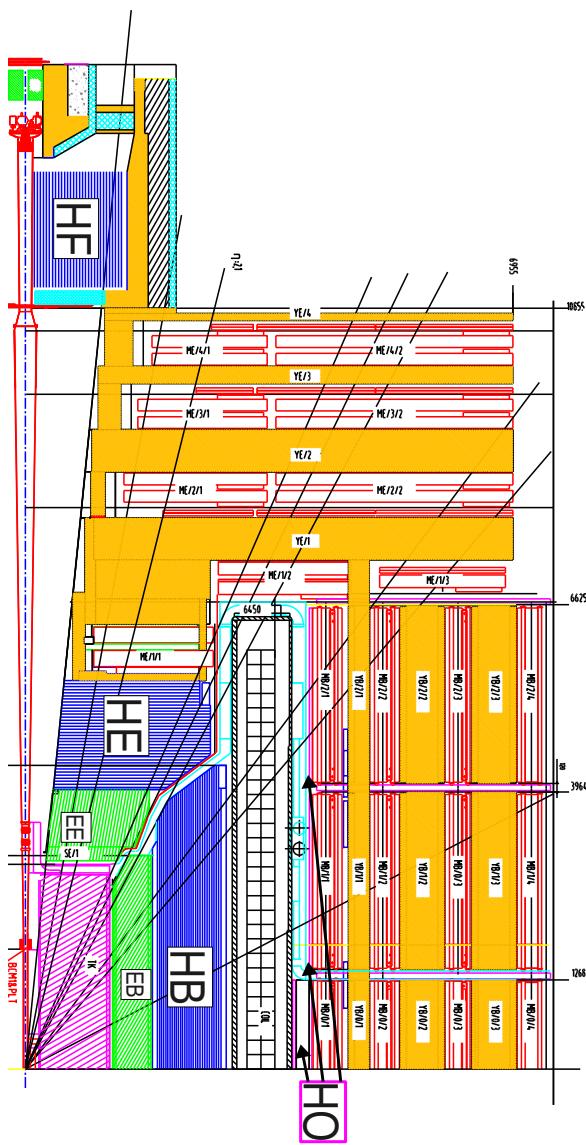


Figure 1.2: An r-Z schematic drawing of a quarter of the CMS detector showing the location of the HB, HE, HO, and HF calorimeters in CMS.

active material. Light from the plastic scintillator is wavelength-shifted and captured in WLS fibers which are fused to clear optical fibers for transport to the phototransducers and front-end electronics. The HCAL Outer calorimeter (HO), which functions as a tail-catcher for hadronic showers and is useful for muon identification, uses the same active material and WLS fiber as the HB and HE calorimeters but uses the steel return yoke and magnet material of CMS as absorber [3]. The modifications to the HO calorimeter and its readout will be carried out during LS1; these are not included as a part of this upgrade. The HB, HE, and HO calorimeters were all originally fitted with hybrid photodiode (HPD) transducers.

The HF is a Cherenkov calorimeter based on a steel absorber and quartz fibers which run longitudinally through the absorber and collect Cherenkov light, primarily from the electromagnetic component of showers which develop in the calorimeter [4]. The quartz fibers are inserted into the HF with a spacing of 5 mm and the fibers associated with a particular $\eta \times \phi$ region are bundled and the optical signal is converted to an electrical signal using a photomultiplier tube.

After the phototransducers, all of the hadron calorimeters share a common electronics chain. The signal from the phototransducer is integrated over 25 ns (the so-called “integration bucket”) and digitized by a QEIE8 ASIC [5] developed at Fermilab using a clock phased for the particular time-of-flight to each cell using a Clock-and-Control ASIC (CCA) developed for the purpose. The CCA aligns the digital data for the channels to a common clock and hands the data off to the Gigabit Optical Link (GOL) ASIC for transmission to the back-end electronics at a link rate of 1.6 Gbps. In the back-end electronics, the HCAL Trigger and Readout card (HTR) calculates trigger primitives which are then transmitted to the calorimeter trigger system. The trigger

primitives consist of an energy estimate for each bunch crossing for each projective volume in the calorimeter, summing the energy from any depth segments. The HTR card is also responsible to retain the data samples waiting for a possible Level 1 decision. On a Level 1 Accept, the HTRs transmit their data to a Data Concentrator Card (DCC) which then sends the event fragment into the central DAQ via SLINK64, otherwise the data samples are discarded if no Level 1 Accept is received.

The HCAL uses a continuous-readout front-end; there is no memory or pipeline in the front-end electronics. Instead, the QIE reading for every bunch-crossing is transmitted to the back-end electronics. This strategy has proven very useful, as the data-processing can be adjusted in the firmware of the back-end electronics and new features added without challenging and risky modifications to the front-end electronics. The upgrade program will maintain these strengths by retaining the same continuous-readout scheme.

1.3 Overview of the HF Upgrade

The upgrade is logically separated into two portions, one which applies to the HF and the other to the HB and HE calorimeters. These upgrades share many sub-components, such as the QIE10 ADC chip, but the installation schedules, the phototransducers, and the challenges which each face are all quite different. Both this chapter and the TDR as a whole will discuss first the HF calorimeter and then the HB and HE calorimeters as the upgrade of the HF calorimeter will be installed first chronologically.

By extending the reach of the calorimetry to high pseudorapidities ($3.0 < |\eta| < 5.0$), the HF plays an important role in identifying forward jets, determining missing transverse energy, and measuring the luminosity. Of the major modes of Higgs production at the LHC, Vector Boson Fusion (VBF) is the second-most dominant mechanism. Forward jets (especially in VBF) extend Higgs boson coupling measurements and complement the measurement of the light Higgs boson width. Since the HF extends the $|\eta|$ coverage to 5, it enables better missing E_T measurements (important for many searches for physics beyond the Standard Model). For these reasons, maintaining the design performance of the HF calorimeter in the presence of high-pileup is important for the CMS physics program. These aspects are discussed in more detail in Chapter 2.

The HF calorimeter uses Photomultiplier Tubes (PMTs) to collect the light from the quartz fibers. During initial operation of the detector in 2010, anomalous signals were identified which were associated with single muons or particle showers passing through the phototubes. These events produced anomalously large energy deposits which could be clearly identified in the low occupancy environment of initial operation. However, these anomalous signals become more-difficult to reject as the luminosity increases, as topological requirements become harder to apply. The most powerful technique for rejection of these signals has been based on timing, as the signal from the energy deposit directly in the PMT arrives before the signal from the calorimeter which must pass through the quartz fibers. Similarly, other classes of anomalous signals produce pulses which are very long in time compared with the normal Cherenkov pulse. However, the current timing technique depends on not having collisions in the bunches before and after a collision – this is true for the current operating conditions of LHC at 50 ns, but will not be true for future operation at 25 ns.

To ensure the desired performance of the forward calorimeter, several changes to the detector are required. The first change, which is already underway, is the replacement of the current Hamamatsu R7525 phototubes with Hamamatsu R7600U-200-M4 multi-anode tubes. The new

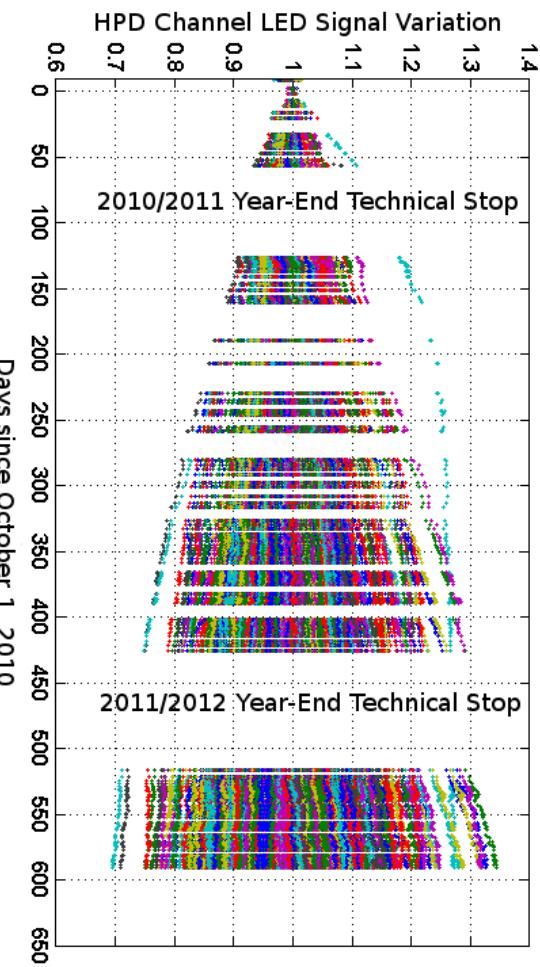


Figure 1.3: Divergence of the gains of individual HPD channels in the CMS HB and HE calorimeters (5184 channels) over a period of approximately two years as measured using the LED monitoring system. Detailed studies have indicated that these changes are consistent with photocathode migration in the HPD devices.

tubes have thinner optical windows and metal envelopes rather than glass. These changes have been shown to significantly reduce the rate of anomalous signals, though not to suppress them entirely. Further benefits are possible using the multi-anode output of the PMTs. With additional readout channels, it is usually possible to identify single-particle anomalous signals and even to recover the response for the channel rather than rejecting the energy deposit entirely, as is done now. The necessary electronics to support the additional channels is part of this upgrade. Another important capability brought by the upgrade will be a TDC capability in the ADC chip, allowing the determination of pulse arrival times and pulse widths for signals which are contained in a single charge-integration bucket, as required for 25 ns operation.

1.4 Overview of the HB and HE Upgrades

The HB and HE detectors currently use Hybrid Photodiode transducers (HPDs) which were chosen for their magnetic field tolerance and gain of $> 2 \times 10^3$. Each HPD is segmented, providing eighteen channels of optical-to-electrical conversion. During operation in the CMS magnet, a number of weaknesses have been identified, many of them related to the large electric field required for these devices (8 kV across a gap of 3 mm). The most significant of these is the appearance of electrical discharges in the device when high voltage is applied. This effect is enhanced by particular orientations and strengths of the magnetic field relative to the HPD device. This effect was particularly severe for the HO calorimeter, requiring significant reductions in voltage (from 8 kV to 6.5 kV) in much of the detector. While the discharge effect is much smaller in the HB/HE calorimeters, it is a significant source of high-amplitude noise and a risk to the longevity of the phototransducers. These discharges may be related to another significant effect presented in Fig.1.3, which shows the change in individual pixel response as monitored by the LED system over a period of nearly two years. This divergence in response appears to be due to photocathode migration effects. As no saturation of the effect has been observed, and the underlying process is not understood, the gain changes are worrisome. Cor-

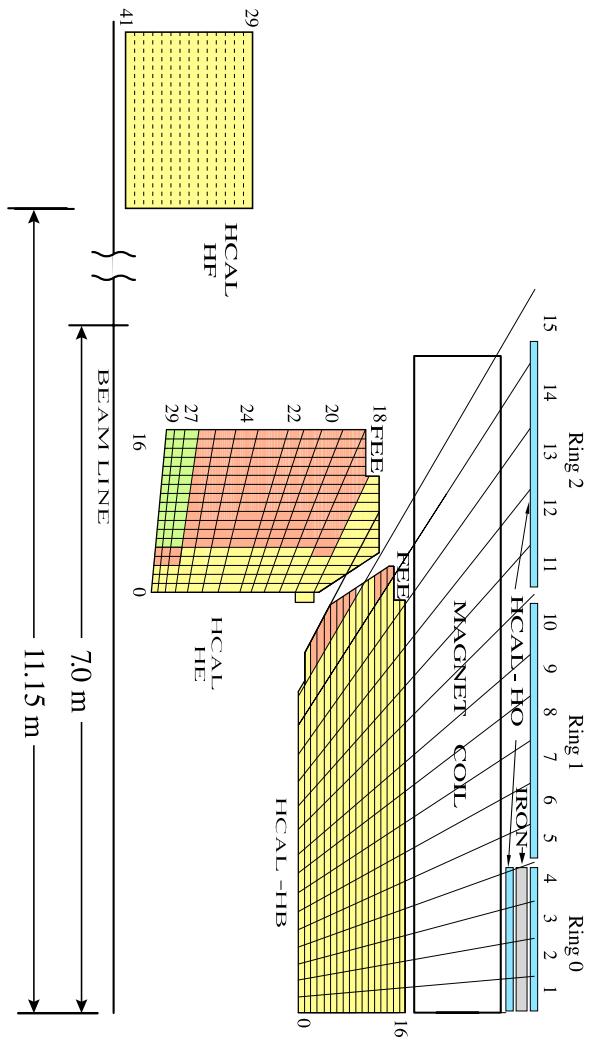


Figure 1.4: An r - Z schematic view of the CMS hadron calorimeters showing the locations of the HB, HE, HO, and HF calorimeters. The locations of the front-end electronics for the HB and HE calorimeters are indicated by “FEE”. The current depth segmentation of the HB and HE detectors is also shown.

rections can be made via the LED monitoring, but the decreases in response will raise the noise level in the calorimeter as the detector electronic noise is constant in units of collected charge while a decrease in response increases the GeV energy associated with that fixed amount of charge. The effect may also accelerate or change significantly. Recent developments have led to an ideal replacement for the HPD: the Silicon Photomultiplier (SiPM).

The SiPM is a multipixel Geiger-mode Avalanche Photodiode (APD) device which provides gains between 10^4 and 10^6 using an applied voltage less than 100 V and photon detection efficiencies in the range of 20% to 40%. The current from all pixels is summed and the device behavior is linear for small signals and can be corrected in the case where the pixel occupancy becomes high. The CMS HCAL R&D program has invested significant effort in the development of SiPMs which can replace the HPDs, bringing better and more stable performance to the HB and HE detectors. The devices are quite compact (a surface area of 1mm^2 to 9mm^2 is typical) and have low unit cost (less than 100 CHF). The HPDs of the HO subdetector will be replaced by SiPM devices during the LS1 technical stop, while keeping the existing electronics path.

The high performance of the SiPM devices, coupled with recent developments in data link technology, will allow a significant increase in depth segmentation in the HB and HE calorimeters. The current segmentation of the HB and HE calorimeters is shown in Fig. 1.4 with the segmentation indicated by the color/shading of the tile structure. The signal-to-noise performance of the HPD was not sufficient to support finer segmentation, nor were the particle-flow techniques, used to reconstruct jets of particles in the CMS detector, available to take full advantage of them at the time of the original calorimeter construction. With the improved gain of the SiPM, a segmentation with three depth segments in the barrel and four to five in the endcap, as shown in Fig. 1.5, becomes possible. This segmentation will allow better tracking of hadronic shower development which is important for particle-flow techniques which have been developed very successfully in recent years by the CMS collaboration. It will also allow

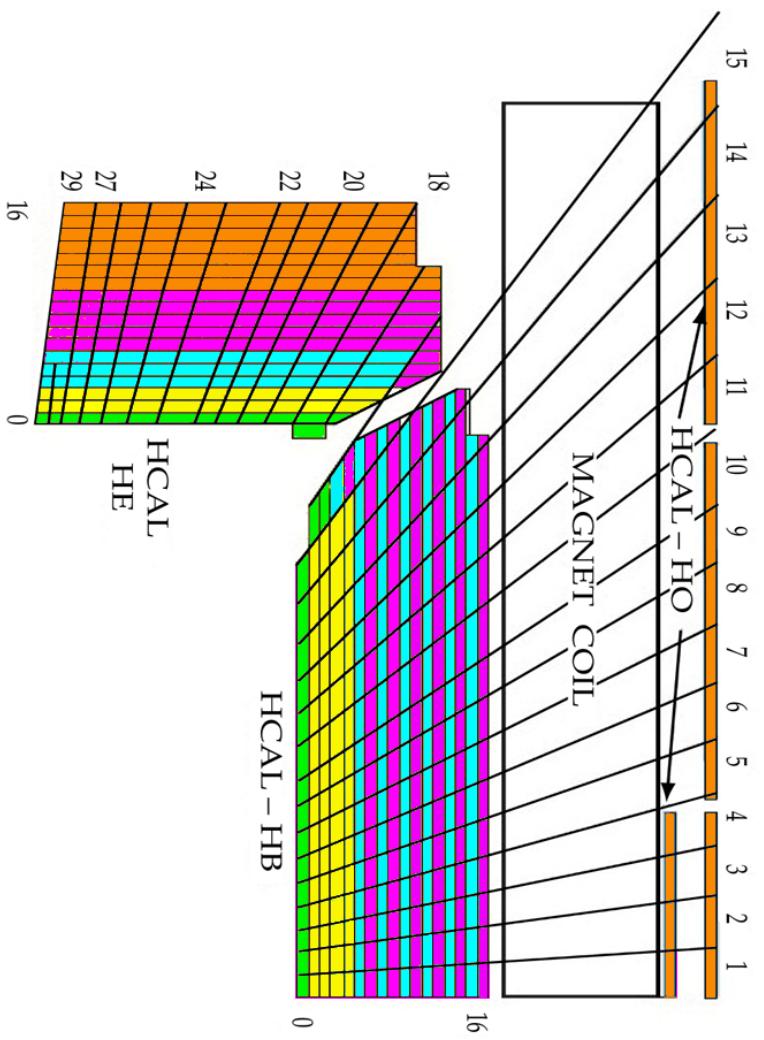


Figure 1.5: Depth segmentation structure which becomes possible with the use of SiPM photodetectors for the HB and HE calorimeters.

better management of the radiation damage which will occur in the high- η region of the HE calorimeter, reducing the response of the individual tiles. These differential response changes are mixed and lost as the light from all tiles are currently uniformly optically summed. By reading out smaller groups of tiles with individual SiPMs as a function of depth (particularly at high- η), the gain losses at high luminosity can be mitigated.

The longitudinal segmentation of the hadron calorimeter will provide shower profile information that is used to verify that electromagnetic particles identified in the ECAL have little energy in the HCAL. In particular, the segmentation suppresses the influence of pileup particles that contribute to the first layer of HCAL but not to deeper layers. Similarly, the deepest segment of HCAL can be useful for efficient identification of prompt muons and rejection of muons produced in the decay of hadrons in flight with isolation requirements that are robust against pileup. The deepest segment is not affected by the pileup particles and the excellent signal-to-noise of the SiPMs allows a tight selection on the energy deposit by the muon.

The location of the front-end electronics modules are indicated ("FEE") in Fig. 1.4. The HPDs, digitization electronics, and data link are contained in compact modules which plug into a backplane and mechanical assembly that is firmly mounted on the detector. When the CMS detector is open, these modules can be removed without disconnecting any other subdetector of CMS (e.g. ECAL or the silicon tracker). The upgrade replacement modules can thus be installed with minimal interference with the rest of CMS provided they occupy the same volume as the existing modules. The compact nature of the SiPM devices aids in meeting this requirement, but it remains an important design constraint for the HB/HE upgrades.

1.5 Strategies and Considerations for Upgrade Implementation

The HCAL Upgrade project will replicate and build on the success of the original construction process while addressing the differences in installation and commissioning between an initial construction project and an upgrade project. The use of common electronics in the construction of the original HCAL was an important cost-saving strategy and has proven highly advantageous for detector operations. Although the upgrade also uses common components, similar to the initial construction strategy, deployment of an upgrade into a working experiment is quite different from the original construction phase. This point drives the installation and commissioning strategy for the HCAL upgrades.

The current HCAL front-ends for all four major sections of the detector share most of their components – the integrator/ADC (QIE8), control and data-alignment ASIC, the data link, and the control module. The back-end electronics for the entire HCAL use identical hardware. This commonality saved resources during construction and has been extremely valuable during operations by minimizing the number of different systems which must be tracked and understood by operations personnel and allows pooling of spares.

The upgrade electronics design is similarly based on a number of common components. The electronics chain contains a number of new and common components: an enhanced integrator/ADC (QIE10), radiation-tolerant FPGAs for data alignment, a higher-bandwidth data link (GBT), and an improved control system (ngCCM/ngFEC). The data flow including these components for the case of the HF is shown in Fig. 1.6 and for HB/HE in Fig. 1.7, directly highlighting the similarities. The discussion of these topics is structured in the following way: the common aspects of the front-end electronics are discussed in Chapter 3, the requirements which are specific to each upgrade are discussed in Chapter 4 (HF) and Chapter 5 (HB/HE), and the back-end electronics, which are common for the whole upgrade, are discussed in Chapter 6.

The installation and commissioning plan for the HCAL upgrades is determined both by physics considerations and practical scheduling requirements depending on the duration and nature of the accesses required to make the installation. Access to the HF is relatively simple, as the full CMS detector does not need to be opened. In fact, the HF detector electronics can be accessed even during a short technical stop of LHC. Access to the HB and HE front-end electronics requires opening and closing CMS, a process which requires four to six weeks of work by itself.

The HF upgrades to allow effective background rejection at high luminosity and 25 ns bunch spacing will be very important for Higgs physics and searches for new physics phenomena. The multi-anode PMTs and necessary cabling for dual-anode readout will be installed in LS1. This will allow the installation of the upgraded HF front-end electronics in a typical year-end technical stop. The development schedule of the HF front-end electronics is thus advanced relative to that for HB/HE.

The installation of an upgrade into a functioning experiment must be done carefully to avoid reducing rather than improving the performance of the detector. While the front-end and back-end electronics were deployed simultaneously during initial construction, this has significant schedule risk for an upgrade. Instead, the HCAL Upgrade project plans the installation of the back-end electronics in advance of the front-ends. The back-end electronics is designed to be compatible with both the current front-ends and the upgraded front-ends. For the HF, the back-end electronics will be upgraded during LS1 and the HF readout will be switched entirely to the upgraded electronics for operations at a year-end technical stop after LS1. For the HB/HE, the back-end electronics will initially be deployed using split optical signals from

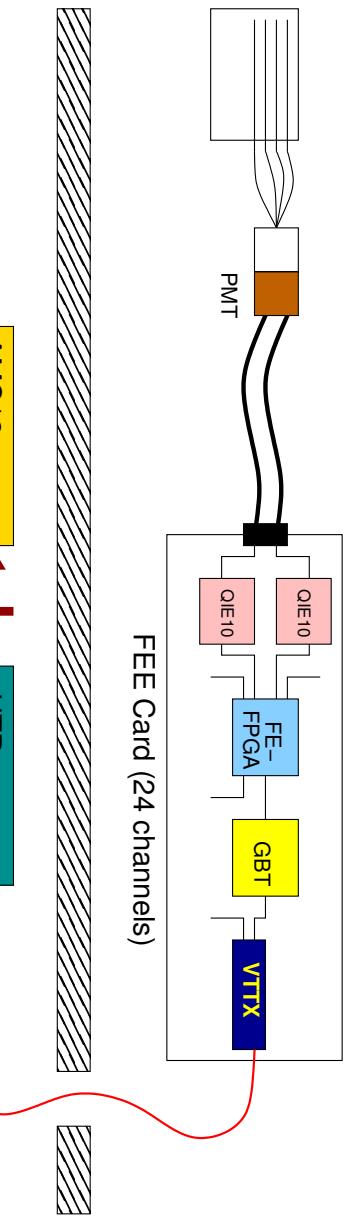


Figure 1.6: Overview of the upgraded HF detector focusing on the data path. The diagram shows the signal flow from the multi-anode PMTs, configured in dual-anode mode, through the ADC/TDC (QE10), the alignment and formatting (FE-FPGA), the data transmission (GBT/VTX), the trigger-primitive and pipeline electronics (uHTR) and the cDAQ link (AMC13). The control and local-DAQ paths are not shown in this diagram for simplicity.

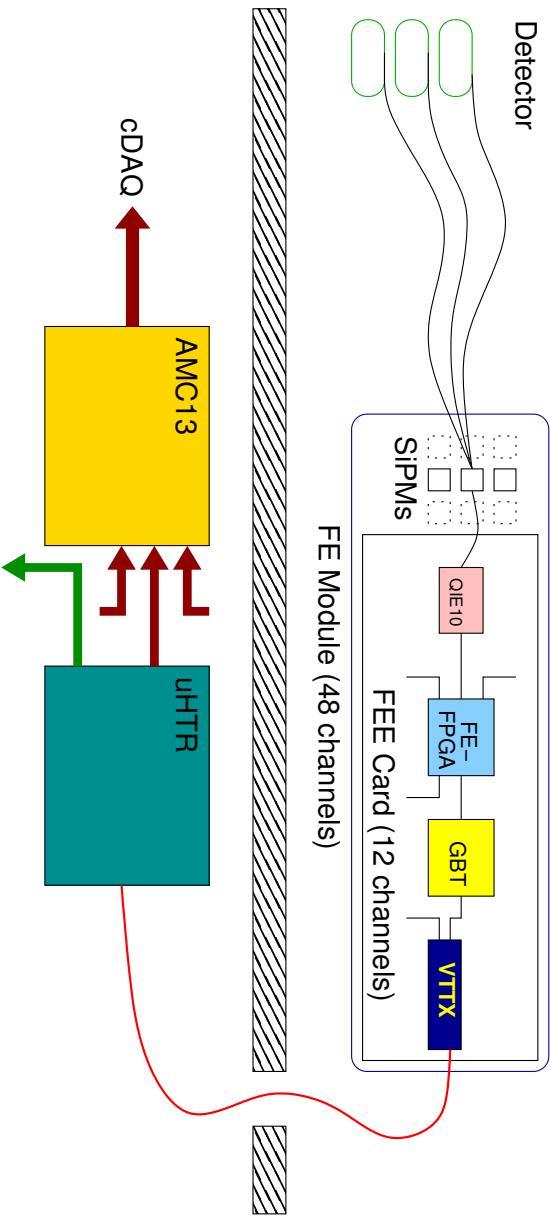


Figure 1.7: Overview of the upgraded HB/HE detectors focusing on the data path. The diagram shows the signal flow from the SiPM phototransducers through the ADC/TDC (QE10), the alignment and formatting (FE-FPGA), the data transmission , the trigger-primitive and pipeline electronics (uHTR) and the cDAQ link (AMC13). The control and local-DAQ paths are not shown in this diagram for simplicity.

the existing front-ends. This will allow commissioning of the HB/HE back-end electronics as well as the commissioning and deployment of an upgraded calorimeter trigger. These aspects will be discussed further in Chapter 6.

1.6 Radiation and Experimental Environment

The HB and HE Front-End Electronics (FEE) is inside the CMS solenoid, exposed to a 3.8-Tesla magnetic field and to radiation. The upgraded FEE must survive an integrated luminosity of 3000 fb^{-1} [6]. We have calculated the irradiation using the CMS Dose-Fluence Calculator, [7] assuming energy deposit on silicon. The results are in Table 1.1.

Table 1.1: HCAL FEE radiation levels (total ionizing dose (TID) and neutron and charged-particle fluence) for an integrated luminosity of 3000 fb^{-1} .

FEE type	Position [cm]	TID [Gy]	TID [rads]	1 MeV-equivalent neutron fluence [cm^{-2}]	charged hadron fluence [cm^{-2}]
HB	R=269, Z=429	14	1400	7×10^{11}	2.1×10^9
HE	R=261, Z=548	1.5	150	9×10^{10}	2.8×10^8
HF	R=300; Z=1200	1.5	150	2×10^{11}	6×10^8

Fluka simulations, which have been validated with neutron monitors installed at the hadron forward calorimeter and a Medipix detector installed at the cavern wall, provide similar results (M. Guthoff, private communication) to those obtained from the Dose Calculator. In both cases agreement was given within the uncertainties of systematic errors [8]. The ratio of dose rate between HB and HE has also been confirmed by observations of single-event upset (SEU) rates in the Clock-and-Control Module (CCM) used in HCAL during LHC operation. The SEU event effective cross-section is observed to be $0.078 \pm 0.004 \text{ pb}$ in HB and $0.012 \pm 0.002 \text{ pb}$ in HE, yielding an HB/HE ratio of 6.5 ± 1.1 which is in good agreement with the simulation prediction of ≈ 7.5 .

With safety factors, we summarize the assumed target levels for all HCAL FEE in Table 1.2.

Table 1.2: Target levels for all HCAL FEE.

TID	1 MeV-equivalent neutron fluence	charged hadron fluence
10 krad = 100 Gy	$2 \times 10^{12} / \text{cm}^2$	$10^{10} / \text{cm}^2$

Chapter 2

Design Performance of the Upgraded Detector

The performance gains of the upgraded detector originate from the superior characteristics of the new photodetectors to be installed in the barrel, endcap, and forward calorimeters and from the expanded functionalities of the proposed front-end and back-end electronics upgrades. The SiPM photodetectors with newly designed readout chips provide an order of magnitude higher signal-to-noise ratio in the barrel and endcap calorimeters. In the forward calorimeter the multi-anode signals provide redundant sampling of the light from a single calorimeter cell and high quantum efficiency for measuring Cerenkov signals while the new TDC capability allows rejection of many background events. This chapter reviews the use of the detector upgrades to increase the imaging and pattern recognition capabilities of the hadron calorimetry for the identification of signals and the rejection of backgrounds in an environment of 50 pile-up events per LHC bunch crossing as well as the impact of the upgrades for a selection of specific physics analyses.

In the area of detector performance, we investigate the introduction of precision timing measurements for every cell and anode in the calorimeter to suppress out-of-time and non-collisional beam backgrounds. The introduction of depth segmentation is also considered with the goal of maintaining high efficiency for particle identification in a high pile-up environment. The hit occupancy in the hadron calorimeter drops by two orders of magnitude from the front layers of scintillator directly surrounding the ECAL to the rear layers that sit in front of the muon systems. Hadron showers that are measured at multiple depths are more clearly identified and associated to a single high p_T charged or neutral hadron. Depth segmentation is also important when considering the long-term performance of the endcap region through 3000 fb^{-1} of LHC data-taking. The strong depth-dependent darkening of the scintillators and fibers from radiation in the endcap region can be compensated by re-weighting the energies measured at each depth as a function of the observed darkening to maintain uniform calorimeter response. Beyond the intrinsic performance of the HCAL detector, increasing the data bandwidth to the Level-1 trigger system and to the central data-acquisition systems are also investigated in terms of improving trigger efficiency performance for lepton/photon isolation and identification quantities, jet and missing transverse energy triggers, and related cross-triggers and to provide adequate data bandwidth of the full granularity readout to the high-level software trigger. The Level-1 trigger systems and the central data-acquisition system are in the process of developing higher bandwidth inputs to their systems in collaboration with the HCAL Upgrade proposal.

The sections of this chapter focus on a step-wise approach to understanding the performance of the upgraded detector and the optimization criteria and constraints involved in deciding the upgrade geometry and specifications. The choice of longitudinal segmentation is a central design issue for the HCAL Upgrades. We describe the procedure and supporting studies that went into the choice of the upgrade geometry. We first outline the general design constraints

on the choice of longitudinal segmentation and the introduction of precision timing measurements. We then describe the HE scintillator and fiber darkening studies and compensation methods. The next section is on object identification and, in particular, the impact of depth segmentation on particle flow quantities used in the CMS reconstruction and physics analyses. This is followed by a section on studies of background rejection using problematic background sources encountered in the 2012 LHC collision data. In the remaining part of the chapter, the cumulative improvements from the upgrades are implemented in benchmark physics analysis simulations that are foreseen to benefit from the data collected with the upgraded detector. The benchmark analyses studied are:

1. Higgs boson production via vector boson fusion with the Higgs boson decaying to τ -lepton pairs
2. Inclusively-produced Higgs bosons decaying to a pair of Z bosons with four-lepton final states
3. Supersymmetry (SUSY) signals corresponding with third-generation final states (which provide viable explanations for the stabilization of the electroweak energy scale)
4. A non-resonant diphoton plus missing transverse energy search, incorporating benefits of the pixel and HCAL upgrades.

These analyses passed through the full usual approval process for physics results within CMS.

2.1 Choice of Longitudinal Segmentation

The introduction of longitudinal segmentation is aimed at increasing the ability to separate showers and identify particle signatures in the lower occupancy regions behind the first layers of the hadron calorimeter. In the endcap region, depth segmentation makes it possible to compensate for the darkening of sensitive detector elements with depth.

Before presenting the results on the object identification, background rejection, and benchmark physics analyses, we include here a brief discussion of general design constraints on the choice of longitudinal segmentation and the inclusion of precision timing information.

Every individual scintillating tile from the 17(18) layers of scintillator in HB(HE) segmented in $\eta\text{-}\phi$ is instrumented with an individual optical fiber that carries the wavelength-shifted light of that tile to the edge of the detector to the location of the photodetector and front-end readout electronics. This allows complete flexibility to alter the longitudinal segmentation. The main constraints on the choice of longitudinal segmentation come from the performance optimization described below and in optimally matching the SiPM photodetection area and dynamic range to the range of expected light signals from energy depositions of particle showers. The total number of longitudinal segments is constrained by the power capacity of the readout boxes to approximately three segments in the HB and five in HE.

The primary considerations for a segmentation choice are:

- Impact on segmentation on Upgrade particle-flow methods for separating hadronic clusters
- Longitudinal isolation of electron and photon showers in the ECAL and muon tracks using HCAL information

- Uniform energy density for hadron showers as a function of readout depth, thus providing uniform SiPM signal magnitude across depths
- Energy resolution degradation with radiation damage to scintillators and WLS fibers (concern in HE only)
- Leakage current increase of SiPM with cumulative radiation dose at the location of the readout
- Number of readouts

A working optimization of the segmentation of HCAL has been developed for the physics studies described here. The choice of segmentation in the barrel is based mainly on the signal-to-noise ratio per depth where the finest segmentation of the front-layers into depths is chosen while maintaining the same signal-to-noise ratio of the current single-depth readout of the central barrel calorimeter. This mapping corresponds to a $\{1+4+12\}$, three-depth configuration for the barrel. Layer-0, the first depth, is unique and provides enough light due to its thickness and scintillator type to meet the signal-to-noise requirement with the single layer. The second depth consists of 4 layers, providing similar signal-to-noise ratio and a similar dynamic range requirement as depth-1 on the number of photons produced from the optical addition of the 4 layers. The rear depth consists of 12 layers and these layers will be interleaved with every other layer going to a separate SiPM device so as to equalize the splitting of the light yield in these layers. The dynamic range requirements of the rear layer with the splitting of the signals is similar to depth-1 and depth-2. The limitation to three depths in the barrel region is the baseline configuration for the front-end readout where power and cooling limitations constrain the total number of depths in the readout.

For the endcap region, the total number of depths is not as tightly constrained as in the barrel due to the decreased ϕ -segmentation from 5° to 10° for $1.74 < |\eta| < 3.0$. The segmentation in the endcaps is set to a $\{1+2+3+5+7\}$ five-depth configuration to match the radiation dose studies that were optimized to compensate for the darkening of the HE scintillator and fibers using offline analysis as discussed below.

The final segmentation of the calorimeter is determined by the construction of the optical-decoder unit (ODU) subassemblies in the readout modules. Further adjustments to the layer configuration can be implemented in the final module construction based on ongoing further studies without affecting the rest of the module design.

2.1.1 Radiation Dose Compensation in the Endcaps

The HE detector, particularly at large $|\eta|$, is exposed to a large flux of particles during operation. As $|\eta|$ increases, the average primary particle energy increases while the surface area of each HE scintillator tile decreases. As a result, the estimated TID for the HE scintillator tiles for 500 fb^{-1} of LHC collisions increases from 200 rad at $|\eta| = 1.5$ to 5 Mrad at $|\eta| = 3.0$ as seen in Fig. 2.1. The irradiation dose reduces light yield from scintillators. In order to compensate for the radiation damage of the scintillators by a re-weighting technique, the calorimeter must be split in several longitudinal depths. The optimal segmentation choice for this purpose was studied using simulation results from CMS-SW-4_2_8_SLHChcal with energy deposit information for each layer of the calorimeter. The rate of signal loss as a function of integrated dose was determined from bench tests with ionizing radiation sources [9].

This study identified a segmentation with a single-layer first depth, two-layer second depth, and three-layer third depth as optimal. Such a segmentation provides a uniform energy deposit/containment in each of the readout depths. This is important for resolution but is also

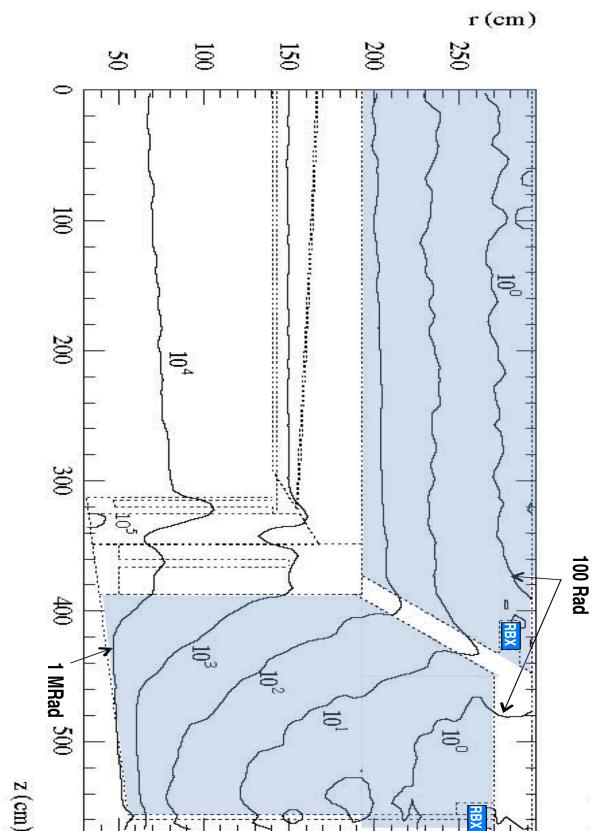


Figure 2.1: Radiation level contours in the HB/HE regions from FLUKA calculations after 500 fb^{-1} (in units of Gray).

naturally correlated with the integrated dose profile. The correlation between the dose profile and uniform energy density in the average shower makes the $\{1+2+3\}$ of the initial six layers of the calorimeter a robust choice. The arrangement of the last twelve layers is less crucial – results with segmentations $\{1+2+3+5+7\}$ and $\{1+2+3+12\}$ provide broadly similar resolutions. The five-depth segmentation has advantages for muon identification and particle flow techniques.

For the model of scintillator darkening used in the study, the pion resolution for $|\eta| < 2.5$ has no visible degradation up to 3000 fb^{-1} , while for $|\eta| > 2.65$ several depths cannot be recovered by the weighting technique at 3000 fb^{-1} as the darkening is greater than 95%. It is expected that an intervention to replace a subset of scintillator tiles will be required as part of the Phase 2 calorimeter upgrade. This upgrade is beyond the scope of this TDR and is expected to be in place for luminosities beyond 500 fb^{-1} .

Other measurements of scintillator darkening [10] suggest a higher rate of loss and neutron-damage of the scintillator is not considered in any study to date. As a result, the darkening could well be faster than the results in this study. Work is currently ongoing to compare detector response during current operations to provide information on this question. Based on preliminary results, the darkening appears more consistent with [10] than [9]. A comparison of the predictions of these models indicates that the identified segmentation will allow compensation of the scintillator radiation damage through 500 fb^{-1} , while a more-extensive intervention for operation up to 3000 fb^{-1} may be required. Studies on the observed and expected darkening and research and development on responses will continue as part of HCAL operations and the Phase 2 upgrade effort.

2.2 Precision Timing Performance Criteria

The required performance of the TDC timing in the QIE10 ASIC is determined by two use cases in the HCAL upgrade. In the HF, the TDC is crucial for identifying anomalous signals in the PMTs which are produced by particles passing directly through the PMTs. These signals arrive earlier than signals from the detector by 4-5 ns. The rise time of the HF signal is very sharp, as seen in Fig 3.2, which allows the HF to take advantage of TDC resolutions down to $\approx 1\text{ ns}$ which is the physical limit induced by shower development fluctuations in the calorimeter.

For the HB/HE, the TDC timing parameters were developed to be able to identify the bunch crossing for low energy pile-up energies down to 1 GeV relevant for lepton isolation and identification with finite timing resolution down to 0.5 GeV. This was achieved with a 100 fC threshold on the charge going into the QIE10 ADC/TDC chip. The 1 GeV scale is comparable to the minimum track momenta considered in isolation in the barrel region. Plots of the arrival time distributions of pile-up events for calorimeter cells with at least 1 GeV of energy are shown in Fig. 2.2. The hits are well contained in a single 25ns LHC bunch crossing and the simulation was done with multiple successive bunch crossing at a spacing of 25ns and an average of 50 pile-up events per crossing. For high energy pulses, the TDC achieves 0.5ns resolution, comparable to the same resolution achieved for high energy pulses using the pulse shape information from three successive 25ns ADC measurements.

2.3 Data and Monte Carlo Samples

All of the results presented in this chapter are based on the standard CMS software framework (CMSSW). Collision data samples have been processed using CMSSW_5_2_4 and the standard prompt reconstruction framework. Testbeam samples have been processed with the versions of CMSSW current during the year of data-taking, utilizing options for additional depth segments to be reconstructed within the standard CMS software.

For studies which are based on simulation, official versions of the CMS software supporting the full simulation of the Upgrade geometry in a high pile-up environment have been produced. Three different software release versions are used in the physics and object studies discussed below: CMSSW_4_2_8_SLHChcal14-patch3, CMSSW_4_2_8_SLHChcal15, and finally CMSSW_4_2_8_SLHChcal16. Many parameters are common to all releases, and there are also important differences detailed below.

The common aspects of these releases are higher signal-to-noise ratio from the use of the SiPM and QE10 readout in the barrel and endcaps and from the use of the QIE10 in the forward calorimeter, the introduction of depth segmentation in the barrel and endcap calorimeters, and the introduction of TDC timing in the barrel and endcap calorimeters.

The depth segmentation of the barrel and endcaps was fixed for these studies. The simulated samples were produced with separate energy measurements for every scintillator tile and these measurements were combined into readout channels for the reconstruction. Specific studies, such as the HE scintillator-darkening study discussed above, used the per-tile energies for optimization.

The SiPM performance is based on the test beam performance of the devices with a model verified to reproduce the test beam data and high-rate light pulse response from test stand evaluations of the SiPM devices. The model includes the SiPM pulse response including the Y-11 fiber decay time, the finite pixel count and the finite response time of the pixels - including a history of previous crossing light illumination on the pixels. The total pixel count is the per-

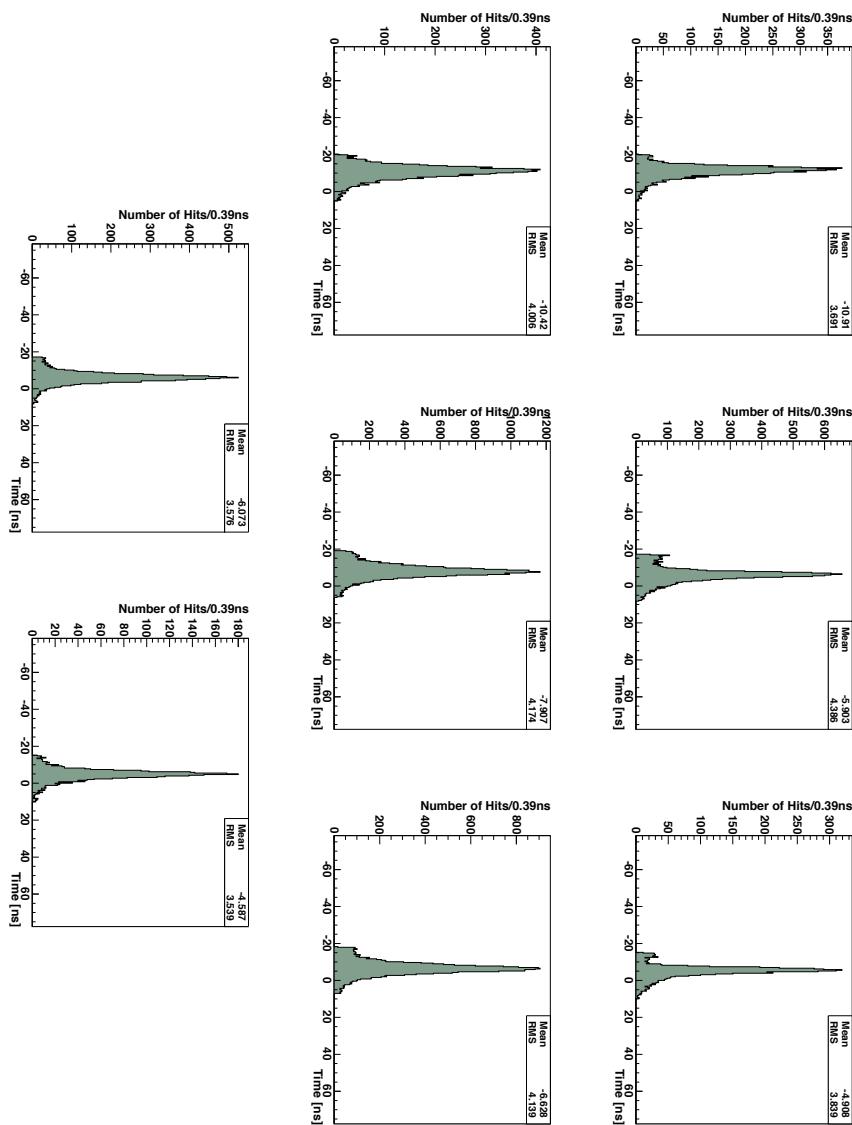


Figure 2.2: Arrival time distributions of simulated pile-up events for calorimeter cells with at least 1 GeV of energy with a simulation of the upgrade TDC measurements. The three barrel depths (top row) and five endcap depths (middle and lower rows) all show peaked distributions that are well contained within a single 25ns LHC bunch crossing.

depth count in a configuration where the signals from layers within a depth are optically added together and uniformly illuminate the SiPM devices. This is known as an optical decoding unit (ODU) model. For the barrel, the pixel count is approximated to be $4500 \times 4 \times 2$ to model the rear depth, consisting of 12 layers, in an ODU model. In practice, the rear section will consist of two electrically added devices. In the endcap, the SiPM pixel count is set to 4500×2 for each depth. In the outer HCAL, the SiPM pixel count is configured to 2500, but we have not included the HO in the reconstruction in order to minimize differences with the standard release geometry. The time response of pixels in the SiPM for barrel, endcaps, and the HO is set to 150ns, which is an order of magnitude slower than the current devices intended for use in the barrel and endcaps. The time response is an approximate model having fired pixels completely dead for 150ns and 100% responsive immediately after the 150ns time interval. The differences between the actual devices evaluated in test beam and the models used in the simulation were studied and found to have negligible impact on the calorimeter measurements. The signal-to-noise ratios are accurately modeled in the simulation based on unirradiated devices studied in test beam. The impact of the leakage current increase from radiation dose on calorimeter measurements from irradiated SiPM devices from test beam results and simulation are presented in a later chapter.

The HF region is modeled with single-anode PMTs with the assumption of perfect PMT background rejection using the multi-anode readout with TDC information. The multi-anode background rejection and hit recovery algorithms are described below. These methods have been shown in testbeam and collision operation to have high efficiency and are approximated as fully efficient in these studies.

The dynamic range of the front-end chip for charge measurements and the encoding of the digital output accurately follows the QIE10 specifications. The modeling of the timing discriminator in the QIE10 is done with a simple 100fC level discriminator. There is no hysteresis or filtering applied to the timing signals. We use a 6-bit TDC per 25ns bunch crossing and enable two special codes, one for pulses that remain above the threshold for the entire 25ns period and another for pulses that never have an upward transition across the threshold in the 25ns clock period. We model both rising and falling edge TDC measurements. For this study, the rising edge is studied in the barrel and endcaps.

Important differences are present in the three releases used for physics studies. The first MC production run was done with release CMSSW_4_2_8_SLHChcal4-patch3. This release spaced the HCAL hits energies at 50ns, while modeling the rest of the detector with a 25ns LHC bunch crossing. This difference was not intentional, but since the HCAL Upgrade TDC window has been demonstrated to correctly assign hits to the correct bunch crossing with high efficiency, the out-of-time pile-up reduction in the HCAL from 50ns is similar to the explicit timing window cut with 25ns hit spacing. The CMSSW_4_2_8_SLHChcal4-patch3 release did not include the HF region in the reconstruction, which placed an effective cut for jets to be within the $|\eta| < 3$ part of the calorimeter. This limitation did not significantly affect the high p_T analyses, but required a new release for Higgs vector boson fusion (VBF) production studies which contain a high percentage of forward jets.

Release CMSSW_4_2_8_SLHChcal5 includes the HF region in the reconstruction and reduces the hit spacing for the HCAL to 25ns. No explicit timing window is applied to the HCAL reconstruction, so the effects of 25ms bunch spacing with no timing window are present in these studies. For the CMSSW_4_2_8_SLHChcal4-patch3 and CMSSW_4_2_8_SLHChcal15 releases, the calorimeter reconstruction produces individual cells in $\eta\text{-}\phi$ for each depth. In the particle flow reconstruction, the depth dimension is suppressed by adding cells into projective towers in the HCAL barrel and endcaps. This reduction procedure allows for the same algorithms to be applied as in the standard detector geometry. The benefits of higher signal-to-noise and the cell-by-cell zero suppression are present in the particle flow reconstruction, but no explicit use of depth segmentation is used. For the full depth-segmented particle flow algorithm with a 25ms timing window applied, a third software release, CMSWW_4_2_8_SLHChcal16, was made.

The step-wise approach to increasing the complexity of the HCAL Upgrade geometry in the simulation and reconstruction enables the analysis results to better separate performance changes due to different elements of the upgrade and reconstruction algorithms. We, therefore, highlight differences in the analyses based on the release version and correspondingly what aspects of the HCAL Upgrades are present in the simulation and reconstruction. All of the HCAL upgrade MC samples are built on top of the Pixel Phase 1 detector configuration. The analyses compare the differences between the HCAL+Pixel Phase 1 detector to the Pixel-only Phase 1 detector and to the Standard geometry (no upgrades) detector. This approach was taken in order to understand the incremental benefit of the HCAL upgrades with respect to the Pixel Phase 1 detector upgrade with a common set of physics analyses.

2.4 Object Identification

The performance optimization of the upgraded detector is considered in the context of how the hadron calorimeter is configured in online operations and in physics analysis. Extensive development of particle-flow techniques leveraging the precision silicon tracking system and the high-granularity, high-resolution electromagnetic calorimeter have changed the emphasis on the function of the hadron calorimetry within the tracking acceptance: the focus is on particle isolation and identification rather than total calorimetric energy measurements, with the important exception of the neutral hadron energy measurements where hadron calorimeter energy resolution are still dominant.

One of the most difficult challenges for particle-flow is the presence of high minbias pile-up, populating incrementally the innermost parts of the detectors and calorimeters. In 25ns LHC operation where there is a strong overlap of calorimeter pulses into successive bunch crossings, the out-of-time calorimeter clusters are completely outside of the realm of particle-flow methods as the tracking system is limited to in-time track reconstruction. Out-of-time calorimeter energy depositions must be rejected based on timing information. For the hadron calorimeter, the hit density as a function of depth was studied as a starting point for understanding how one could leverage the deeper, lower occupancy depths with the increased signal-to-noise ratio of the SiPM readout to do particle identification in a high pile-up environment. Figure 2.3 is an event display for a single 100 GeV pion simulation in the environment of 50 pile-up events per 25ns bunch crossing showing the multi-depth energy deposition pattern in the barrel hadron calorimeter.

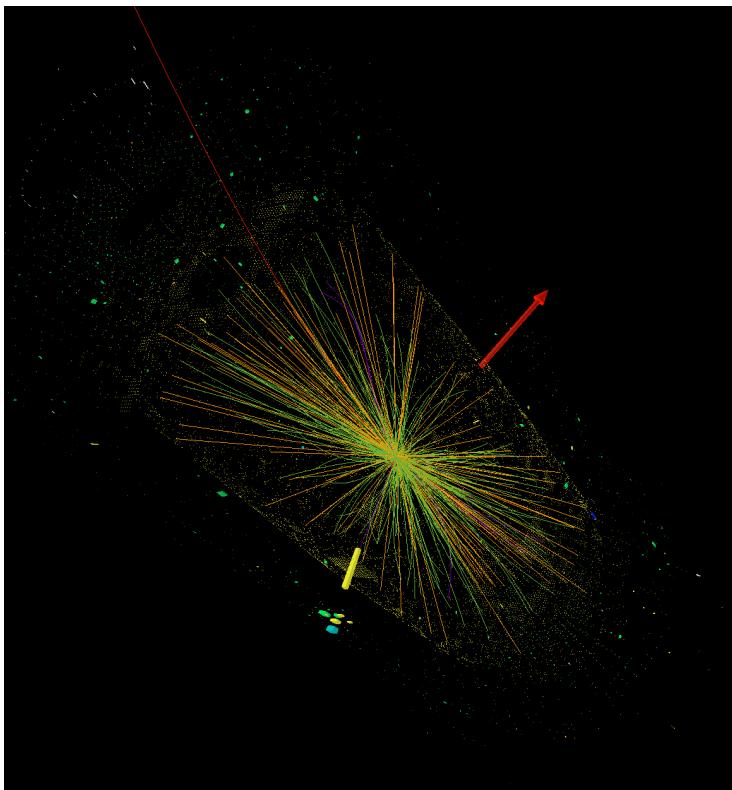


Figure 2.3: Event display of a single 100 GeV pion simulation in the environment of 50 pile-up events per 25ns bunch crossing showing the multi-depth energy deposition pattern in the barrel hadron calorimeter directly behind the energy cluster in the electromagnetic calorimeter.

The transverse and longitudinal shapes of hadronic showers vary greatly from shower to shower. The ability to separate two closely spaced showers depends, therefore, on the observed transverse widths of the energy clusters and the fluctuations of the cluster widths as the showers develop longitudinally. To study these properties, a “supercluster” algorithm was developed to form the longitudinal association of transverse clusters. Transverse clusters associate hits energies independently for each depth of the calorimeter. Each transverse cluster has a width in η and ϕ , a depth coordinate, and an $\eta\text{-}\phi$ cluster position. A supercluster forms the longitudinal associate of transverse clusters and therefore has a transverse cluster multiplicity, an η and ϕ width and cluster positions, as well as additional properties such as the maximum depth of a transverse cluster in the supercluster. Comparisons of the barrel and endcap supercluster widths in η and ϕ are shown in Fig. 2.4 for three different software reconstruction release versions: `CMS-SW-4-2-8-SLHChca14-patch3`, `CMS-SW-4-2-8-SLHChca15`, and `CMS-SW-4-2-8-SLHChca16`. The difference between the three releases is described in section 2.3. Significant improvement in the behavior of the clustering is achieved with the Upgrade PFlow (`SLHChca16`) and that this improvement is related to the timing window cut. The degradation of out-of-time pile-up is seen in the `SLHChca15` release with 25ns time spacing in HCAL compared with `SLHChca14-patch3` with 50ns time spacing in HCAL. Figure 2.5 shows the hit multiplicities and cluster multiplicities in HCAL superclusters for each of the three reconstruction releases. The anomalous hit count in the endcap clusters indicate the particle flow clustering is failing in that region in a high pile-up environment. The Upgrade PFlow eliminates the anomalous hits in the endcap region. Figure 2.6 shows the maximum depth of a cluster in a supercluster for different supercluster energy thresholds in the barrel and endcap calorimeters. Higher energy particles tend to penetrate deeper into the HCAL.

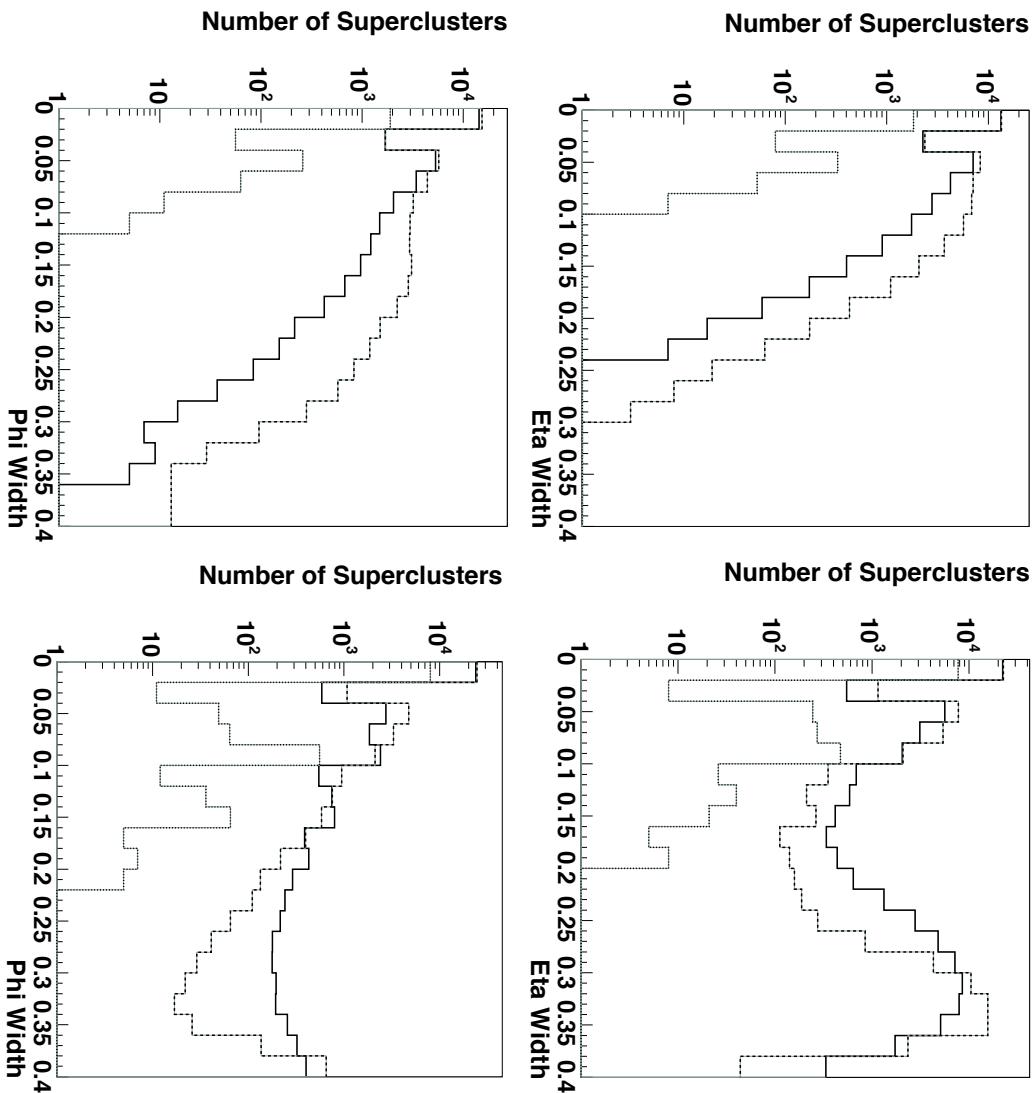


Figure 2.4: Comparisons of the barrel (left) and endcap (right) supercluster widths in η (top) and ϕ (bottom) are shown for three different software reconstruction release versions. The solid line shows the performance of standard particle flow with 50 pileup events and a bunch-spacing of 50 ns, the dashed line shows the degradation of performance for 50 pileup events and a bunch-spacing of 25 ns, and the dotted line shows improvement with particle flow configured to take full advantage of the HCAL depth segmentation.

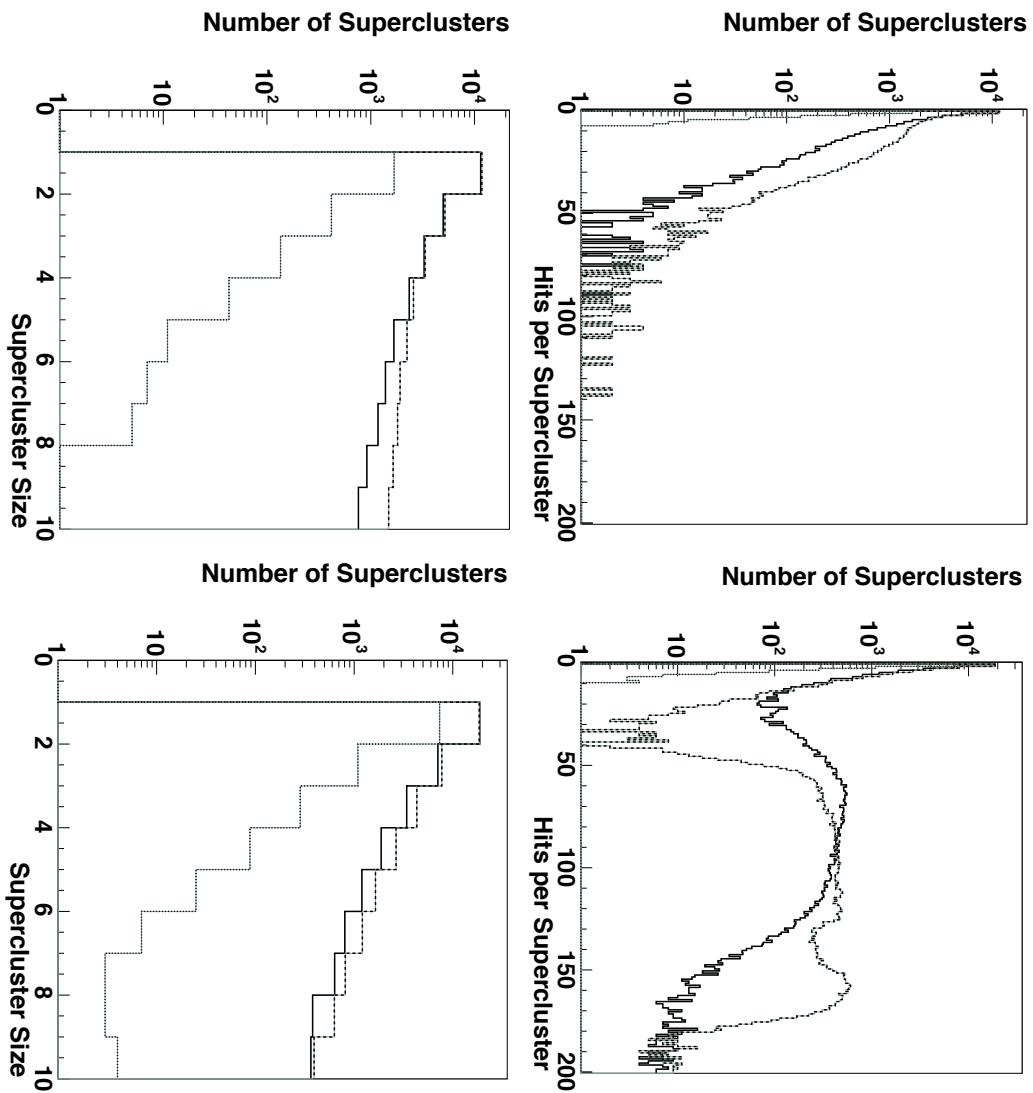


Figure 2.5: Comparisons of the barrel (left) and endcap (right) hit multiplicities (top) and cluster multiplicities (bottom) in HCAL superclusters are shown for three different software reconstruction release versions. The solid line shows the performance of standard particle flow with 50 pileup events and a bunch-spacing of 50 ns, the dashed line shows the degradation of performance for 50 pileup events and a bunch-spacing of 25 ns, and the dotted line shows improvement with particle flow configured to take full advantage of the HCAL depth segmentation.

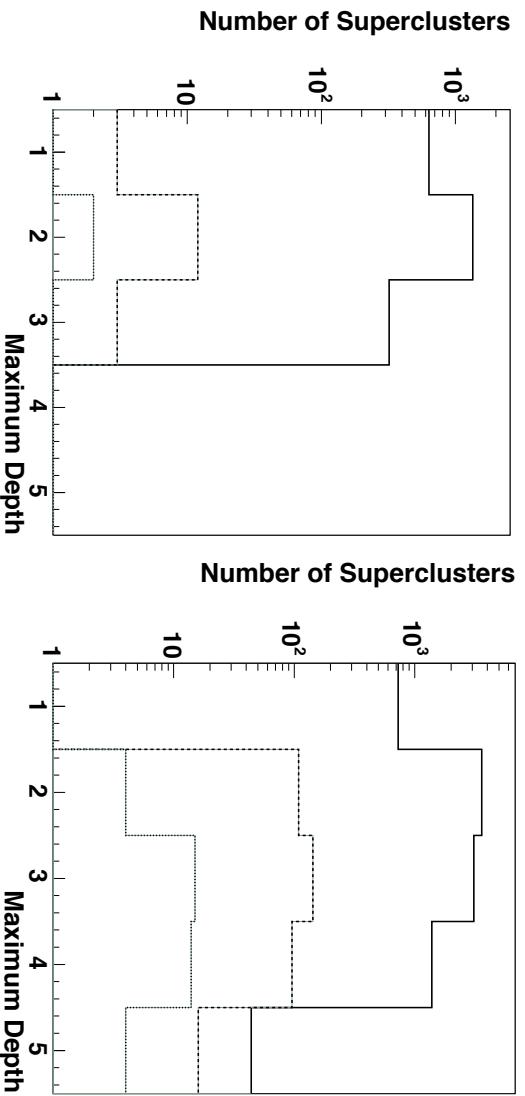


Figure 2.6: The maximum depth of a cluster in a supercluster for all superclusters (solid line), superclusters above 5 GeV (dashed line), and superclusters above 10 GeV (dotted line) in the barrel (left) and endcap (right) calorimeters. Higher energy particles tend to penetrate deeper into the HCAL.

2.5 Background Rejection

The upgraded HCAL detector design provides additional handles to bring known LHC background sources under control and to better reject a variety of backgrounds that impact physics performance. A dedicated discussion of background rejection with the Upgraded HF is described in Section 2.5.1. For the HCAL barrel and endcaps, the Upgraded detector was evaluated in terms of the background rejection factor for a Monte Carlo simulation of the beam halo at $\sqrt{s} = 14$ TeV.

2.5.1 Background Rejection in the Forward Calorimeter

Signal production in the HF calorimeter is based on Cerenkov light. Cerenkov photons, produced in the plastic-cladded quartz fibers of HF by showering particles, are converted to analog and then digital signals by using photo-multiplier tubes and HCAL front-end electronics. The Cerenkov signal from the HF calorimeter has a fast production and collection time (<10 ns full width at the base). This includes an inherent \sim 1.2 ns difference between electromagnetic showers (from the front of the calorimeter) and the hadronic showers (produced much deeper in the absorber) since the quartz fibers are read out from the back of the detector [4].

In HF modules exposed to test beams and to proton-proton collisions at P5, various sources of non-physical (TeV) signals were identified with the leading effects due to charged particle punch-through from late developing showers and Cerenkov light from decay muons traversing the glass window or envelope of the PMT. Cosmic rays and beam halo are also a source of spurious light in the PMTs. The magnitude of spurious signals produced from particles traveling through the PMT glass windows is proportional to the path length of the particle in the glass and number of particles passing through. This guided the choice of replacing current thick-windowed, glass-envelope, fine-mesh dynode PMTs with a new generation of tubes where the structure (thinner window and a metal casing) contains significantly less glass. Further, the PMTs are proximity focused devices, limiting the cross-section to particles traversing the dynode structure.

In addition, the replacement tubes are quad-anode PMTs, providing a redundancy of up to four in verifying the consistency of the signal from a single HF tower. After LS1, the new PMTs will be operated with jumpers as a single anode device. Once new front-end electronics is installed, jumpers will be changed to give 2-anode readout. Four anode readout will remain in reserve should it be needed at the high luminosities after LS2 and the performance of both techniques are discussed below, with an emphasis on the planned 2-anode readout.

The light from a tower of HF (after passing through the light mixer) uniformly illuminates both photocathodes, yielding equal signals in the each anode, within the constraints of Poisson statistics. In contrast, a stray muon traversing the glass window produces a non-physical signal in one anode. Signals from particles passing through the PMT also generally appear 4-5 ns early compared with signals from the detector, as light signal from the detector must pass through the quartz fiber at a speed well below that of the relativistic muons or shower particles. Non-physical signals can thus also be identified by timing. Once a signal is identified as non-physical, the true tower response can be determined from the other valid readout.

The new PMTs were tested at the CERN H2 test-beam facility with standard HCAL front-end electronics in two modes: (1) particles were aimed directly at the windows with no calorimeter connections, and (2) a mock-up HF (similar to what we have in P5) was read out to evaluate calorimeter performance. Both tests used muon and electron beams of various energies. Without applying any algorithm to reject spurious signals, the thin-window PMTs reduced the

magnitude of the spurious muon signals by a factor of four.

Using the test beam data, several background rejection and signal recovery algorithms were developed exploiting the multi-anode readout. Channel-to-channel response variations within a PMT were measured and used for correction over the face of the PMT; for the two-channel readout configuration a $\sim 12\%$ variation consistent was observed, as shown in Fig. 2.7). This variation is consistent with that expected for Poisson variations in the number of photons hitting each of the two channels, given the signal amplitude.

For the two-channel readout configuration, the separation of spurious PMT-window hits is shown in Fig. 2.7. The algorithm used to identify spurious signals is based on the ratio of the ordered signals (denoted as S_1 and S_2 , where $S_1 > S_2$). Several other algorithms have also been developed (e.g. based on ratios and means). The two-channel algorithms have on average 92% efficiency for identifying spurious PMT hits with negligible misidentification rate.

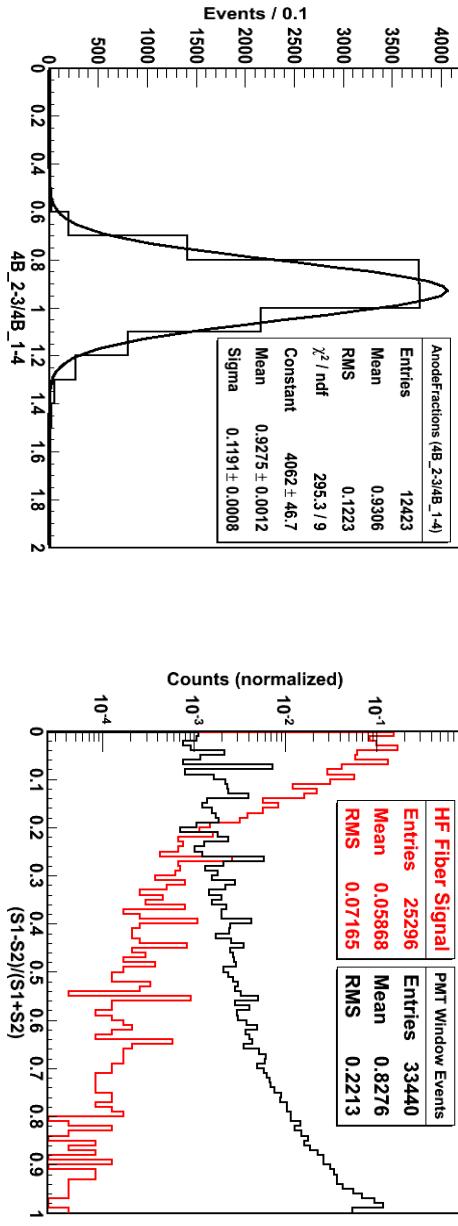


Figure 2.7: Channel-to-channel variations for two-channel readout obtained from data collected at the CERN H2 beam tests (left). The RMS of the distribution indicates the uncertainty in the resulting signal. Distribution of an identification parameter for spurious signals based on two-channel readout obtained from data collected at the CERN H2 beam tests (right). The red distribution shows the signal produced by electron showers, whereas the black distribution shows the PMT signal produced by muons traversing the PMT glass.

An example of recovery at the few photo-electron level is shown in Fig. 2.8 from test beam data. The same algorithm is applied to spurious PMT hits and to the calorimeter signal. The signal is virtually unaffected by the recovery algorithm, whereas the spurious PMT hits are corrected by the algorithm, even without the use of timing information.

As discussed above, spurious signals generally appear 4-5 ns before the signal from the calorimeter. This characteristic has been used to reduce the effect of these spurious signals during 2010-2012 LHC operation. The phase relationship between the LHC clock and the QIE integration clock in HF has been adjusted to shift the charge from spurious events out of the integration window for the bunch-crossing in which they occurred and into the previous LHC bucket. Since the LHC has been operating with 50 ns bunch-spacing during 2010-2012, there are no collisions during the 25 ns periods when the spurious signals arrive. In the Level-1 trigger, these empty buckets have been disabled, which removes much of the effect of the spurious signals. Similarly, only the bunch-crossing of interest is used to determine the energy in HF for HLT and reconstruction, also suppressing the impact of the spurious signals.

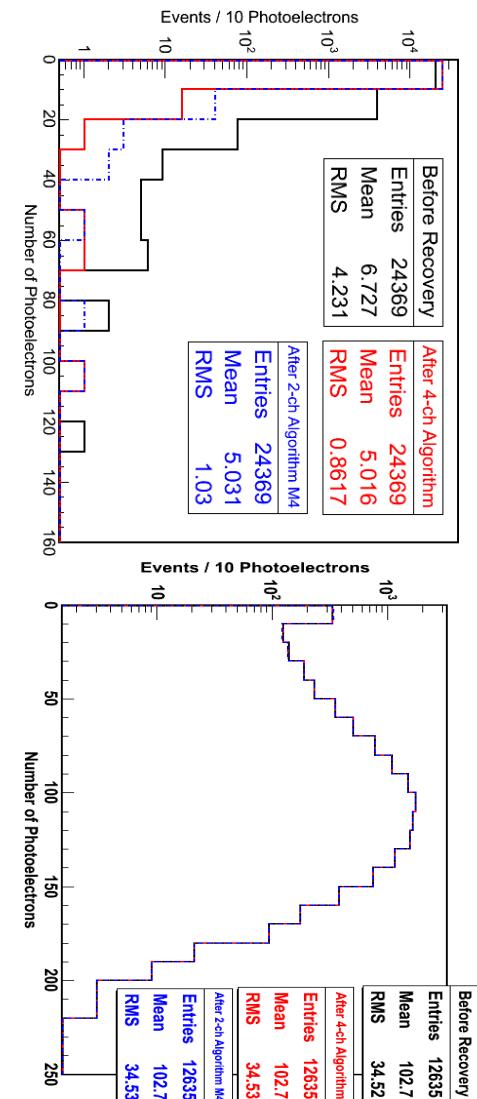


Figure 2.8: Distribution of photo-electrons for spurious (left) and true calorimeter signals (right). Black, red, and blue histograms are, respectively, for no identification, four-channel identification and recovery, and two-channel identification and recovery. The algorithms eliminate the high-side tail of PMT hits with more than 92% efficiency, whereas they do not alter the genuine calorimeter signal.

After LS1, however, the LHC will shift to operation with every 25-ns bucket filled to reduce the occupancies of the tracking detectors as luminosities increase further. The techniques used during 2010-2012 will no longer be available to suppress the impact of spurious signals. To avoid having Level-1 trigger on the wrong bunch-crossing, it will be necessary to shift the integration phase to keep both the spurious signals and the true signals in the same integration window. Similarly, spurious signals cannot be excluded during reconstruction by any clock phase choice.

The impact of this change on the Level-1 trigger has been estimated by considering the performance of 24 upgrade PMTs which have already been installed in the CMS detector. Figure 2.9 shows the jet spectrum derived from a study of minimum-bias events considering only the out-of-time energy measurements (not from a collision bunch). The spectrum is dominated by muon/shower effects which have been shifted out of the collision bunch by adjusting the integration phase. This spectrum of fake jets is in addition to any spectrum from collisional energy.

Unlike the current QIE8 ADC, the new QIE10 to be deployed with the same upgrade which will provide multi-anode readouts being designed to have a built-in TDC which will allow recognition of early pulses by using adjustable thresholds for the signal. This new functionality, available at the L1 trigger level, will distinguish pre-triggers from spurious PMT hits and fully suppress the rate of jets shown in Fig. 2.9. The fine adjustment of the timing of true calorimeter signals within a bunch crossing will allow us to reject other out-of-time background, such as beam halo events.

The new TDC will record two times for each pulse: the crossing of adjustable thresholds, in the negative direction of the signal, and in the return of the signal in the positive direction. By combining information from a local cluster of channels, a decision can be made whether to generate a L1 trigger primitive or not and whether to use one anode or all for the energy measurement. The TDC functionality of the QIE10 has been optimized with test-beam studies including an adapter card accommodating both two- and four-channel readout options. The application of the TDC will allow the full spectrum of fake jets shown in Fig. 2.9 to be rejected.

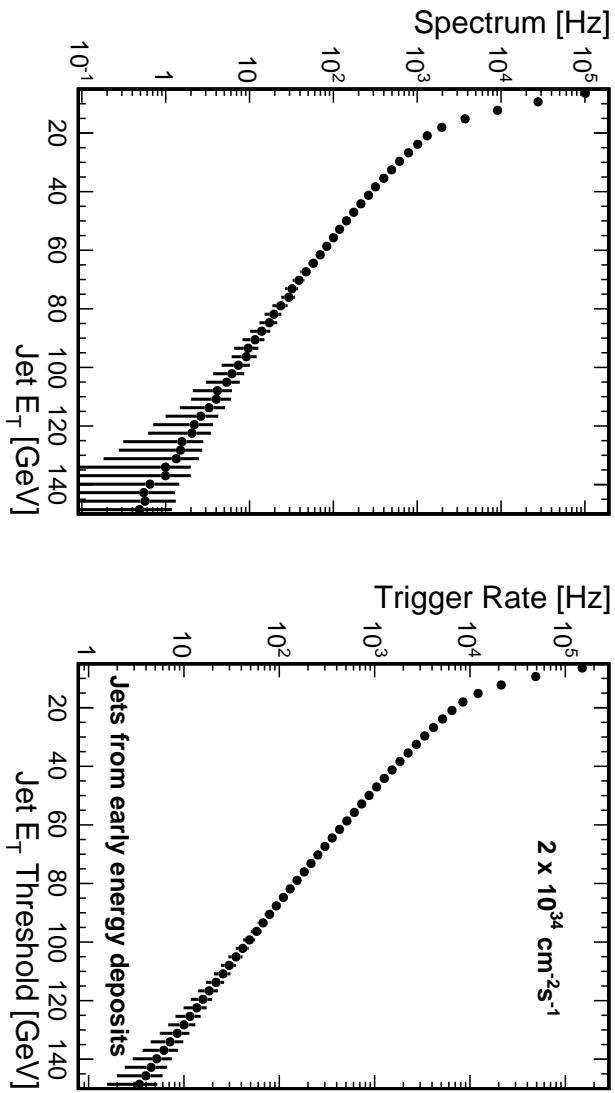


Figure 2.9: The spectrum of fake jets in HF induced by out-of-time energy deposits at an instantaneous luminosity of $2 \times 10^{34} \text{ cm}^{-2} \text{s}^{-1}$. The spectrum was determined using 2012 $\sqrt{s} = 8 \text{ TeV}$ collision data by consideration of out-of-time signals observed in minimum-bias events for a set of 24 upgrade-type PMTs already installed in the HF. Thus, this figure accurately represents the fake rate for the detector after PMT replacement but before the dual-anode readout with TDC is installed.

2.5.2 Background Rejection in the Barrel and Endcap Calorimeters

The TDC functionality of the QIE10 discussed in Section 2.5.1 also provides a powerful rejection power of non-collision backgrounds such as beam halos and cosmic ray particles in the barrel and endcap calorimeters. The beam halo particles are produced in upstream of the detector when beam protons suffer collisions and traverse the calorimeter in parallel to beam protons; therefore, signals from beam halo particles are on average about 6 ns earlier than those from particles produced in proton-proton collisions. Furthermore, cosmic ray particles hit the calorimeter randomly in time.

The correlation of time versus energy for particles measured in the barrel calorimeter in three different depths in simulation samples are shown in Fig. 2.10. While the average time does not depend on the measured energy at energies beyond 20 GeV, the time shifts toward positive values at lower energies. This is due to the fact that it takes longer time for smaller pulses to pass the TDC threshold which is set to 100fC in this simulation study. In subsequent studies, corrections are applied on reconstructed hit time as functions of its energy.

Figure 2.11 shows the reconstructed hit time versus energy correlation for particles from collisions and beam halos at $i\eta=1$ and 10 corresponding to $\eta = 0.04$ and 0.83 respectively. At $i\eta=1$, the beam halo particle timing is about 6ns earlier than that for collision particles, while at $i\eta=10$ there are two groups of beam halo hits corresponding to muons that are traveling in the $-z/+z$ -direction. While earlier beam halos are about 15ns separated from collision particles, later beam halos are overlapping with collision particles and the hit topological information provides a further discrimination against beam halos.

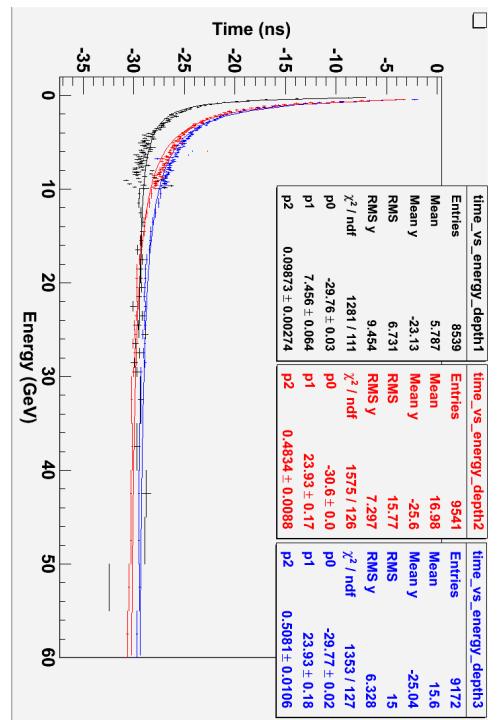


Figure 2.10: The energy versus time correlation for particles produced in in-time collisions and measured in three depth segmentation of the barrel calorimeter.

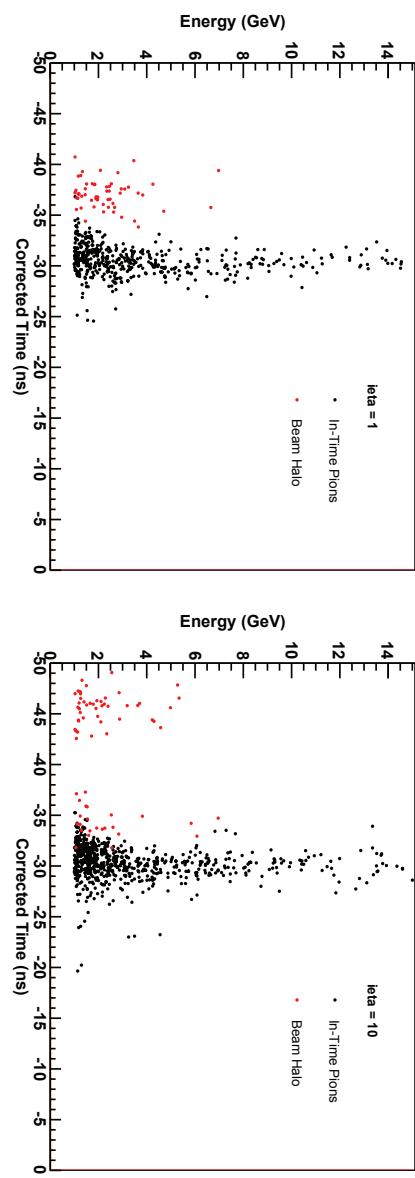


Figure 2.11: The time versus energy correlation for particles produced in in-time collisions (black) and for beam halos (red) at $i\eta=1$ and 10 .

2.6 Full Analysis Results in Higgs Physics

The performances of the vector boson fusion (VBF) $H \rightarrow \tau\tau$ and the inclusive $H \rightarrow ZZ \rightarrow 4l$ analyses using the foreseen HCAL upgrade, in addition to the Pixel Phase 1 upgrade, are studied [11]. These studies are performed using simulated Monte Carlo signal samples generated at $\sqrt{s} = 14$ TeV with 50 overlapping collisions per event. The bunch-crossing interval is 25 ns. The VBF selection increases in signal efficiency by a factor of 2.4 in the upgraded HCAL geometry. For the $H \rightarrow ZZ \rightarrow 4l$ analysis the lepton reconstruction sees a 30% reduction in the HCAL upgrade geometry, per lepton, in the isolation variable energies and a factor of 3 reduction in the amount of HCAL energy directly behind reconstructed electrons with respect to the Pixel Phase 1 scenario.

2.6.1 VBF $H \rightarrow \tau\tau$

The potential improvements from the HCAL upgrade for an analysis optimized for SM Higgs boson production through vector boson fusion (VBF) using final states with tau pairs are assessed. An analysis similar to the reference analysis [12] has been used, with a few small

changes where needed to account for the different conditions. A comparative study of the performance of VBF-tagging is done in the context of the $e\mu$ tau-pair final state in the scenario of the combined HCAL and Pixel Phase 1 upgrade (HCAL Upgrade) and the scenario without upgrades (Standard Geometry). The analysis has not been re-optimized for the higher pile-up conditions or the higher beam energy.

The following samples simulating the production of a SM Higgs boson of mass $m_H = 125$ GeV through vector boson fusion (VBF) and decay to tau pairs have been used:

1. ./VBF_HToTauTau_M-125_14TeV-powheg+pythia6
/Summer12-UpgradeStdGeom2_DR428_PU50-DESIGN42_V17S-v1
2. ./VBF_HToTauTau_M-125_14TeV-powheg+pythia6
/Summer12-UpgradeHCAL_PixelPhase1_DR428_R2_PU50-DESIGN42_V17S-v1

2.6.1.1 Lepton selection

In the $e\mu$ channel the selection requires a muon with $|\eta| < 2.1$ and an electron of opposite charge with $|\eta| < 2.3$. The muon and electron are required to have $p_T > 20$ GeV and $E_T > 10$ GeV or $p_T > 10$ GeV and $E_T > 20$ GeV respectively. Electrons are required to have a high value of a multivariate discriminator based on track quality, cluster shape, and kinematic quantities. Muons are identified using the particle-flow algorithm [13–15]; in addition they are required to have a χ^2/ndof of the global track fit smaller than 10, at least one segment in the muon detector that has been included in the global track fit, muon track segments in at least two stations of the muon detector, at least one hit in the pixel detector, and hits in more than 5 layers of the inner track detector. The electron and muon candidates are required to have a distance from the selected primary vertex of $d_z < 0.1$ cm along the z direction and $d_0 < 0.02$ cm in the perpendicular plane. In addition, we require the ratio of the energy in the hadronic calorimeter to the energy in the electromagnetic calorimeter (H/E) to be less than 0.12 (0.10) in the barrel (endcap) region.

The selected muons and electrons are also required to be isolated. The isolation is based on particle-flow candidates; all photon and neutral hadron candidates and all charged candidates (including charged hadrons, electrons, and muons) which have been associated to the selected primary vertex are considered. For the muon isolation the photon and neutral hadron candidates are required to have a transverse energy of $E_T > 0.5$ GeV. All transverse energy (momentum) deposits of these candidates in an isolation cone of size $\Delta R = \sqrt{(\Delta\phi)^2 + (\Delta\eta)^2} < 0.4$ in the vicinity of the selected muon (electron) are considered. The lepton itself is excluded by comparing the shared track when comparing to charged particle-flow candidates and by using a veto cone depending on the lepton and on the type of particle-flow candidates in consideration. To account for the energy of additional neutral particles due to the presence of pile-up $\Delta\beta$ corrections are applied. The transverse momenta of all charged hadron particle-flow candidates within the isolation cone, which do not fulfil the primary vertex restriction, are summed; for these candidates no threshold on the momentum is required for the electron isolation, while for the muon isolation they are required to have $p_T > 0.5$ GeV and to lie outside an inner veto cone of $\Delta R_{inner} > 0.01$. This sum is corrected by a factor of 2:1 to account for the amount of neutral energy with respect to the amount of charged energy in the isolation cone. A relative combined isolation variable is then defined as:

$$I_{\text{rel}} = \frac{\sum p_T(\text{charged}) + \max(\sum E_T(\text{neutral}) + \sum E_T(\text{photon}) - \Delta\beta, 0)}{p_T(\mu \text{ or } e)} \quad (2.1)$$

where $p_T(\text{charged})$ corresponds to the transverse momentum of all charged particle candidates, $E_T(\text{photon})$ and $E_T(\text{neutral})$ correspond to the transverse energy of the photon and neutral hadron candidates and $\Delta\beta$ corresponds to the energy estimate of neutral particles due to pile-up as described above. The restrictions on the value of I_{rel} in each of the signal samples are chosen to have approximately the same efficiencies for this cut as in the reference analysis. In the absence of a full study of the background processes in each scenario, these cuts have not been optimized for the best performance. The values of the cuts for muons and electrons are summarized in Table 2.1. Figure 2.12 shows the distribution of I_{rel} for electrons and muons. In the HCAL Upgrade, the isolation variables see less HCAL energy due to a reduction of out-of-time pile-up and an improvement in the signal-to-noise ratio in a finer granularity detector readout. The reduction is greatest in the muon isolation quantity in the endcap region where 37% less energy is observed in the isolation variable in the HCAL Upgrade relative to the standard geometry.

Table 2.1: Summary of the cuts applied on I_{rel} in each sample.

	HCAL Upgrade	Standard Geometry
Muon	$ \eta < 1.5$	1.02
	$ \eta \geq 1.5$	1.17
Electron	$ \eta < 1.479$	1.08
	$ \eta \geq 1.479$	0.69
		0.74
		0.66

2.6.1.2 Topological selection

In order to discriminate the Higgs boson signal from background events like W bosons in association with jets or $t\bar{t}$ events, a restriction is applied on the linear combination

$$p_\zeta^{\text{cut}} = 0.85 \cdot p_\zeta^{\text{vis}} - p_\zeta^{\text{miss}} \quad (2.2)$$

where p_ζ^{vis} is the transverse momentum of the combined four vector of the two selected leptons projected onto their bisector in the transverse plane and p_ζ^{miss} is the projection of the transverse missing energy vector on the same bisector [16]. Again, the restriction in each sample is chosen to have approximately the same efficiency for this cut as in the reference analysis. The requirements are $p_\zeta < 75$ GeV in the HCAL Upgrade and $p_\zeta < 145$ GeV in the Standard Geometry scenarios respectively.

2.6.1.3 Jet selection

The reconstruction of jets in the event is crucial for selecting events with a VBF-like topology. Jets are clustered from all particle-flow candidates using the anti- k_T algorithm [17, 18] with an opening parameter of $R = 0.5$. They are required to have a corrected transverse momentum greater than 30 GeV and to be within $|\eta| < 5.0$. The jets are required to be separated by a distance larger than $\Delta R > 0.5$ from the selected leptons. A multivariate discriminator is used to distinguish jets belonging to the hard interaction from jets originating from pile-up which is especially important in a high pile-up environment. This discriminator is based on the compatibility of the combined tracks with the selected primary vertex, jet shape variables, and the multiplicity of both neutral and charged components within the jet. Figure 2.13 shows that the rate of selecting jets from pile-up is significantly lower in the HCAL Upgrade scenario than in the Standard Geometry scenario; the application of the discriminator against pile-up

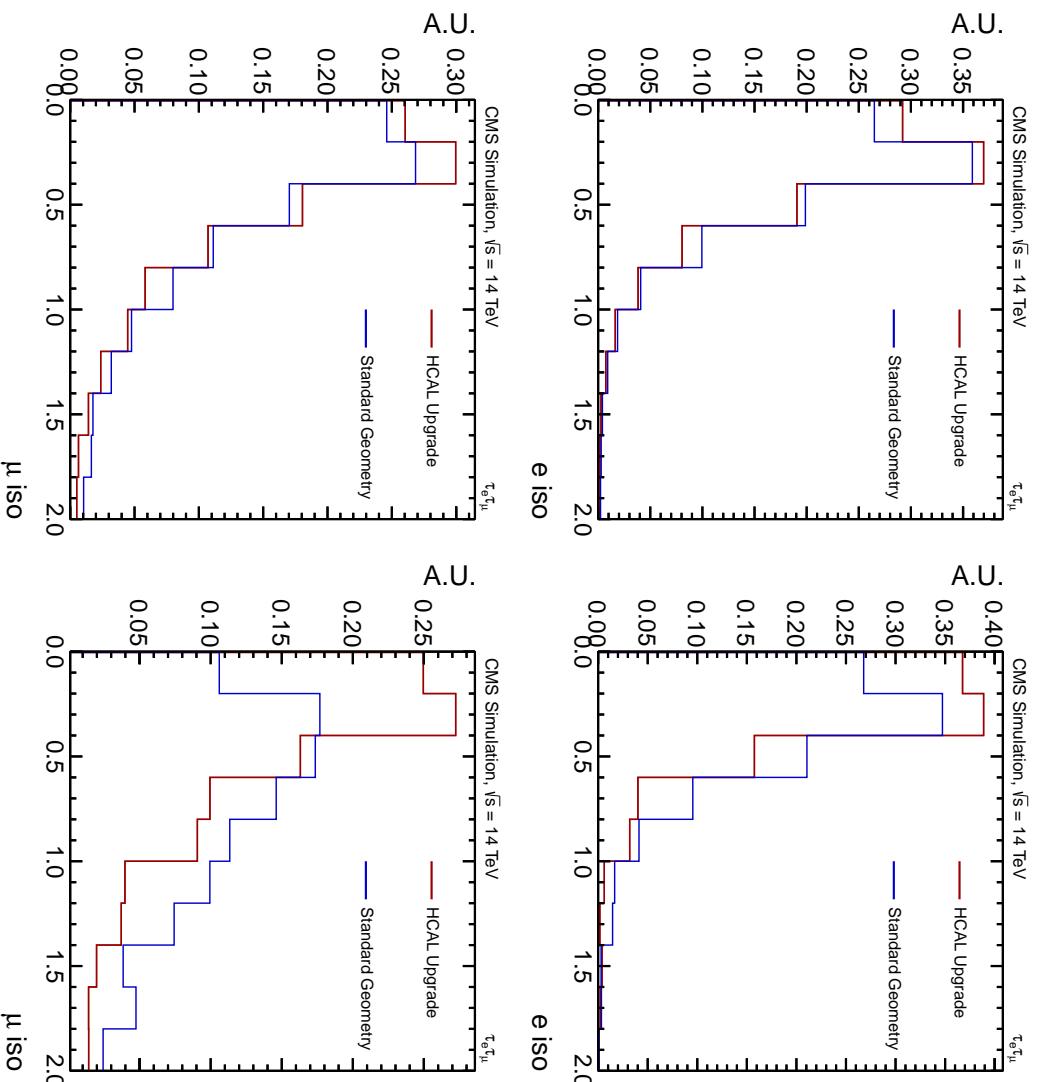


Figure 2.12: Distribution of the relative isolation variable defined in Equation 2.1 for electrons with $|\eta| < 1.479$ (≥ 1.479) on the upper left (right) and for muons with $|\eta| < 1.5$ (≥ 1.5) on the lower left (right). All histograms are normalized to an area of 1.

jets provides further improvement in each case. Using generator-level information, a jet is identified as a pile-up jet in this context if there is no generator jet within a distance $\Delta R < 0.3$ of the selected jet. This is confirmed in the higher multiplicity of reconstructed jets in the Standard Geometry sample as shown in Fig. 2.14, which is further exacerbated when the discrimination against pile-up is not applied. The comparison of the reconstructed jet p_T with the generator p_T for jets matched to generator jets in Fig. 2.15 shows a smaller spread for the response in the HCAL Upgrade scenario.

2.6.1.4 VBF selection

In order to exploit the topology of Higgs boson production through vector-boson fusion, a selection based on jets is applied [19]. Two or more jets satisfying the jet selection described above are required, including the requirement on the discriminator against pile-up jets. In order to isolate the efficiency of VBF selection for jets genuinely from the prompt interaction for the purposes of this study, the jets are additionally required to be matched to generator jets within a

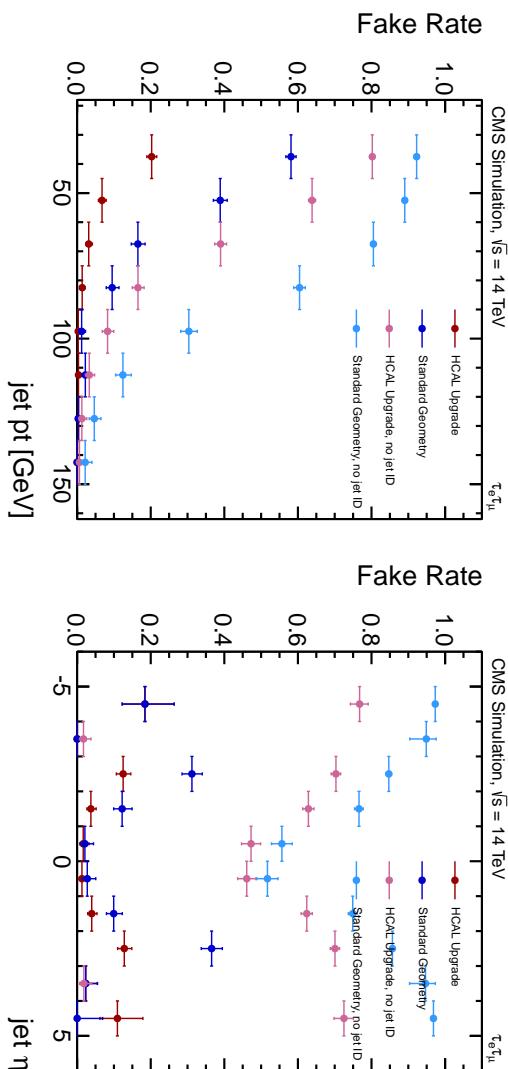


Figure 2.13: Ratio of jets not matched to generator jets to all jets passing the selection as a function of the reconstructed jet p_T (left) and η (right). The comparison between the Standard Geometry and HCAL Upgrade is shown both with and without the application of the multivariate discriminator against jets from pile-up in the jet selection.

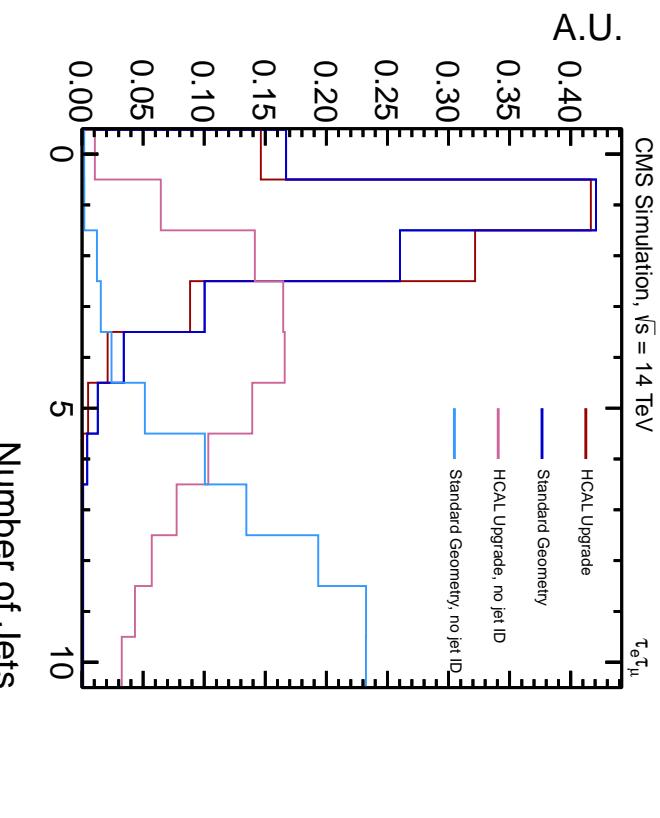


Figure 2.14: Number of reconstructed jets in selected events with $p_T > 30$ GeV and $|\eta| < 5.0$. The comparison between the Standard Geometry and HCAL Upgrade is shown both with and without the application of the multivariate discriminator against jets from pile-up in the jet selection. All histograms are normalized to an area of 1.

distance $\Delta R < 0.3$. The VBF selection requires also that there are no such jets in the rapidity gap between the two jets with the highest transverse momentum, and that the jets are in opposite hemispheres. The invariant mass of these two jets is required to be greater than 600 GeV, and

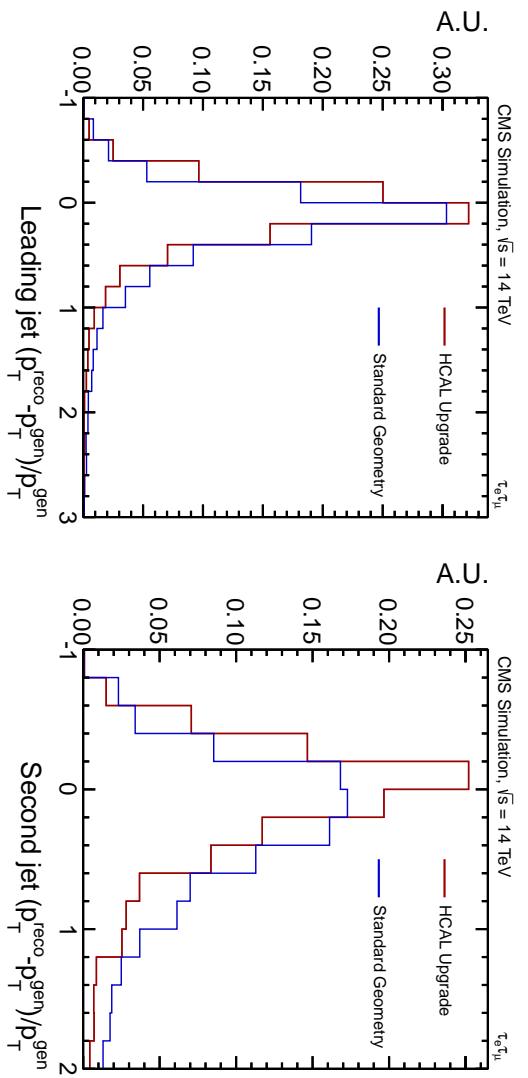


Figure 2.15: Difference between the reconstructed jet p_T and generator jet p_T divided by the generator jet p_T for selected jets matched to generator jets for the leading jet when there is at least one selected jet in the event (left) and for the sub-leading jet when there are at least two selected jets in the event (right). The full width at half-maximum for the Upgrade and Standard Geometry are 0.40 and 0.47 respectively for the leading jet and 0.47 and 0.73 respectively for the sub-leading jet. All histograms are normalized to an area of 1.

the absolute difference in pseudorapidity between them is required to be greater than 4.0. The distribution for these two variables is shown in Fig. 2.16. Figure 2.17 shows the distribution of the tau-pair invariant mass $m_{\tau\tau}$ in the two scenarios after applying the VBF selection. As in the reference analysis, a maximum likelihood technique [20] is used to reconstruct $m_{\tau\tau}$ from the observed momenta of the visible tau decay products and the reconstructed missing transverse energy. The improved resolution for missing transverse energy with the Upgrade translates to a 25% better resolution for $m_{\tau\tau}$.

2.6.1.5 Results

The performance of jet reconstruction and identification is better with the Upgrade, with the rates for selecting jets from pile-up being significantly lower in the Upgrade scenario. The selection efficiency for events passing the VBF selection normalized to the inclusive selection efficiency is found to be 11% in the HCAL Upgrade scenario and 4.6% in the Standard Geometry scenario. The Upgrade thus provides a potential improvement in the efficiency for a VBF signal by a factor of 2.4.

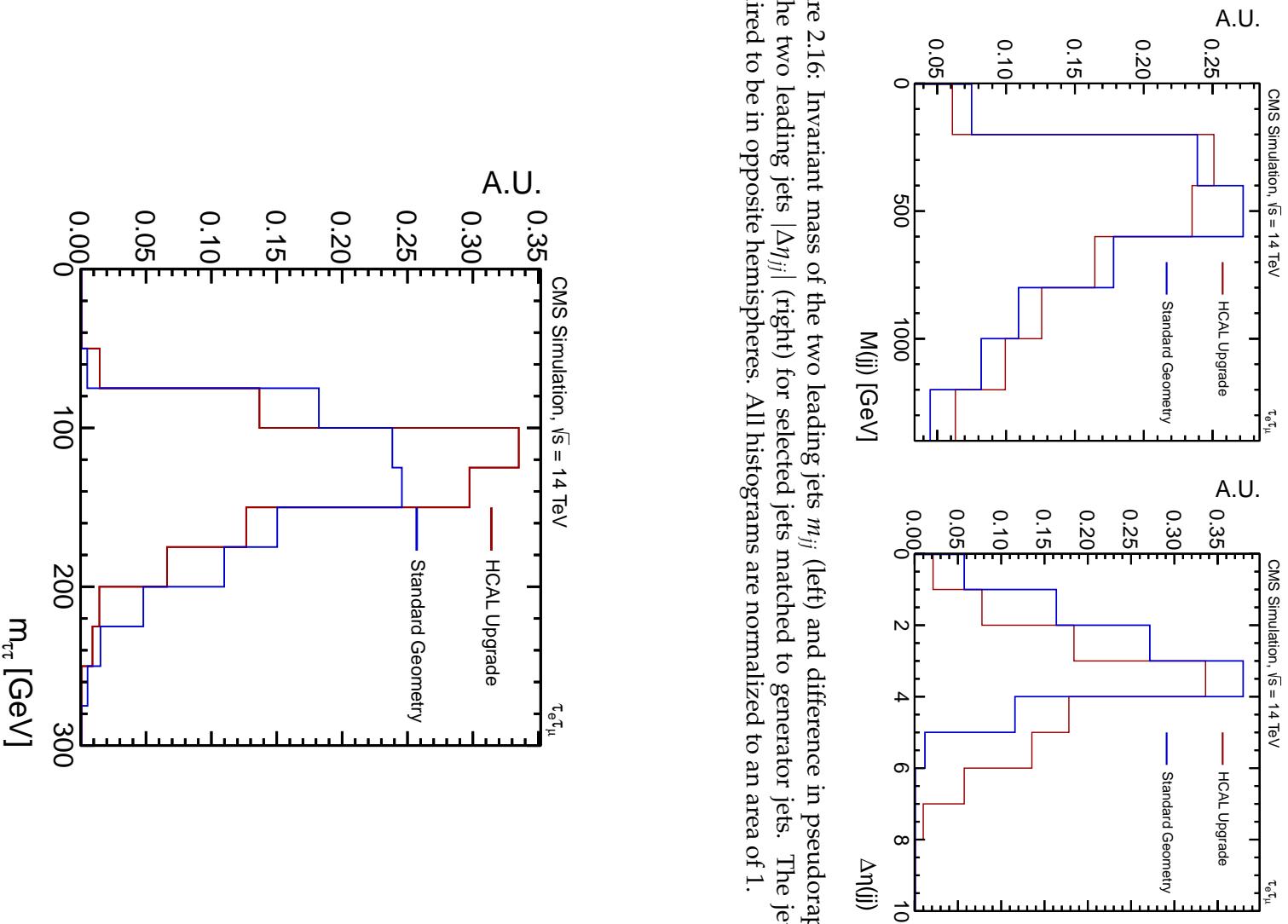


Figure 2.16: Invariant mass of the two leading jets m_{jj} (left) and difference in pseudorapidity for the two leading jets $|\Delta\eta_{jj}|$ (right) for selected jets matched to generator jets. The jets are required to be in opposite hemispheres. All histograms are normalized to an area of 1.

Figure 2.17: Tau-pair invariant mass $m_{\tau\tau}$ for events passing the VBF selection. All histograms are normalized to an area of 1.

2.6.2 $H \rightarrow ZZ$ for $Z \rightarrow \mu^+\mu^-, e^+e^-$

The CMS collaboration is proposing an upgrade to the existing hadronic calorimeter (HCAL). The upgrade will mainly consist of a more refined segmentation of the calorimeter and new readout electronics, with the consequence of a significantly lower noise and a better timing. This study aims to study the performances of the analysis used for the Higgs boson search in the $H \rightarrow ZZ \rightarrow 4l$ ($l = e, \mu$) channel, with the introduction of the HCAL upgrade, with respect to the previous scenario, i.e. with only the Pixel Phase 1 detector upgraded. The analysis is optimized for the search of a Higgs boson in the mass range $110 \text{ GeV} < m_H < 160 \text{ GeV}$. The analysis, due to lack of time and missing background Monte Carlo samples, has not been optimized to the different beam conditions under which the Pixel upgrade will be operated, namely a higher center-of-mass energy $\sqrt{s} = 14 \text{ TeV}$ and a higher number of overlapping events, pileup (PU). Instead we have compared the effects of the HCAL and Pixel upgrades [21] on the signal selection efficiency. As benchmark we have used a Higgs boson MC sample with $m_H = 125 \text{ GeV}$. The search essentially relies on the reconstruction and identification of leptons well isolated from other particles in the event. One or both Z bosons can be off-shell.

2.6.2.1 Analysis

The beam conditions in which the Phase 1 Pixel detector and the upgraded HCAL will be operational will be significantly different with respect to the present conditions. LHC will operate at a higher center-of-mass energy $\sqrt{s} = 14 \text{ TeV}$ and with possibly a higher pileup. Moreover, the current sub-detectors will suffer degradation.

For these reasons, two dedicated Higgs boson Monte Carlo (MC) samples (both with $m_H = 125 \text{ GeV}$) have been used for this study:

1. [/GluGluToHToZZTo4L_M-125_14TeV-powheg-pythia6
/Summer12-UpgradePhase1.DR428-PU50-DESIGN42_V17S-v1](https://github.com/cmstpcdm/Pythia6/tree/Summer12-UpgradePhase1.DR428-PU50-DESIGN42_V17S-v1)
2. [/GluGluToHToZZTo4L_M-125_14TeV-powheg-pythia6
/Summer12-UpgradeHCAL_PixelPhase1.DR428-PU50-DESIGN42_V17S-v2](https://github.com/cmstpcdm/Pythia6/tree/Summer12-UpgradeHCAL_PixelPhase1.DR428-PU50-DESIGN42_V17S-v2)

The first one (1) contains the simulation of the Pixel Phase 1 detector, while the second one (2) simulates the upgraded HCAL detector together with the Pixel Phase 1.

The 2012 reference analysis [22, 23] has been used, but a few simple modifications were necessary due to the different beam conditions. In the 2012 reference analysis, a complete reconstruction of the individual particles is obtained via the particle flow (PF) technique. This technique uses the information from all CMS sub-detectors to identify and reconstruct the particles emerging from each collision event. Electrons are reconstructed within the geometrical acceptance $|\eta^e| < 2.5$ and for $p_T^e > 7 \text{ GeV}$. The reconstruction combines the information from the clusters of energy deposits in the ECAL and the trajectory in the inner tracker. In particular, the trajectories are fitted, for electrons, with a Gaussian sum filter. Their identification relies on a multivariate technique which combines observables sensitive to the amount of bremsstrahlung along the electron trajectory, the geometrical and momentum matching between the electron trajectory and the associated clusters, as well as shower-shape observables. In order to further improve the separation between electrons and charged hadrons, some tracking observables are also used, using either the dedicated CMS electron tracking based on a Gaussian-Sum Filter (GSF) or the standard Kalman Filter (KF) tracks:

- $f_{brem} = (\rho_{in} - \rho_{out}) / p_{in}$, with the GSF track, that is a measure of the Bremsstrahlung emission, which helps in discriminating against charged hadrons.

- χ^2_{GSF}
- $hits_{KF}$
- χ^2_{KF}

The information carried by these variables is maximized using a multivariate analysis (Boosted Decision Tree, BDT) where the signal and background samples for the training have carefully been chosen. The training of the BDT was performed on a $W + 1$ -fake electron sample, directly taken from data, for the background. For signal, a mixture of Monte Carlo $H \rightarrow ZZ \rightarrow 4e$ samples (with masses: 115-120-130-140 GeV) was used. Because of the different beam and detector conditions, the cut on the BDT output used in the 2012 analysis has been replaced with the requirement for the BDT output to be greater than 0. In addition, all electrons must have 0 or 1 expected missing inner hits in order to reject conversions. Henceforward electron ID designates electron candidates selected among the basic electron objects, according to the techniques and cuts just described. Moreover, within the HCAL upgrade scenario, an additional cut on the ratio of the energy released in the hadronic calorimeter over the energy released in the electromagnetic calorimeter, H/E , for single reconstructed electrons had to be introduced. With the HCAL upgrade, indeed, many more soft electrons are reconstructed. This leads to an excess of the number of electrons passing the selection criteria, for a large fraction of the events (Fig. 2.18).

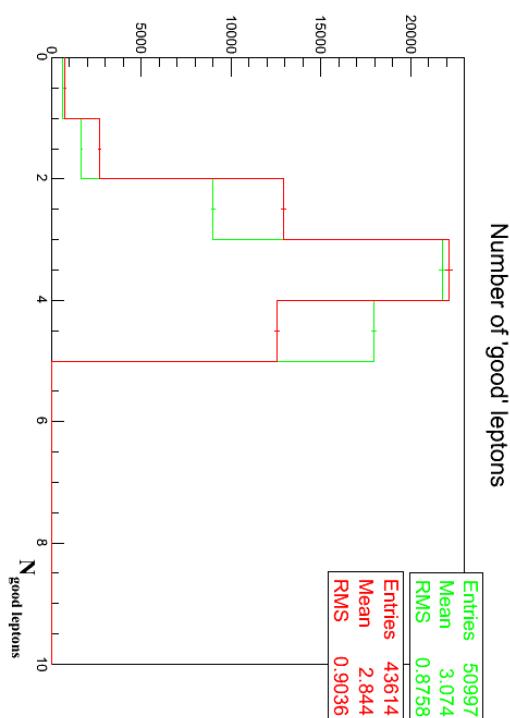


Figure 2.18: Number of electrons passing all selection requirements, (in the $H \rightarrow 4e$ channel analysis), before any additional requirement on the H/E ratio. In red, the Phase 1 Pixel detector scenario; in green, the HCAL upgrade scenario. Plots are normalized to the number of entries in the HCAL upgrade scenario.

The particle-flow isolation variable for electron identification shows less energy in the isolation cone for signal candidates. This effect is the same for muons and electrons and is described in detail below in the discussion of the 4μ final state. After adjusting for the shift in the isolation variable, as determined from muons, to the electron selection, and additional tightening of the H/E cut was needed. The cut of $H/E < 0.05$ in the Pixel+HCAL Upgrade geometry is approximately equivalent to a cut of $H/E < 0.15$ in the Pixel Phase 1 scenario, as shown in Fig. 2.19. Once the requirement $H/E < 0.05$ is introduced for electrons in the HCAL upgrade scenario and the electron PF isolation variable is tightened, the excess is not present anymore, as is visible in Fig. 2.20.

Muons are reconstructed within $|\eta^\mu| < 2.4$ and for $p_T^\mu > 5$ GeV. The reconstruction combines

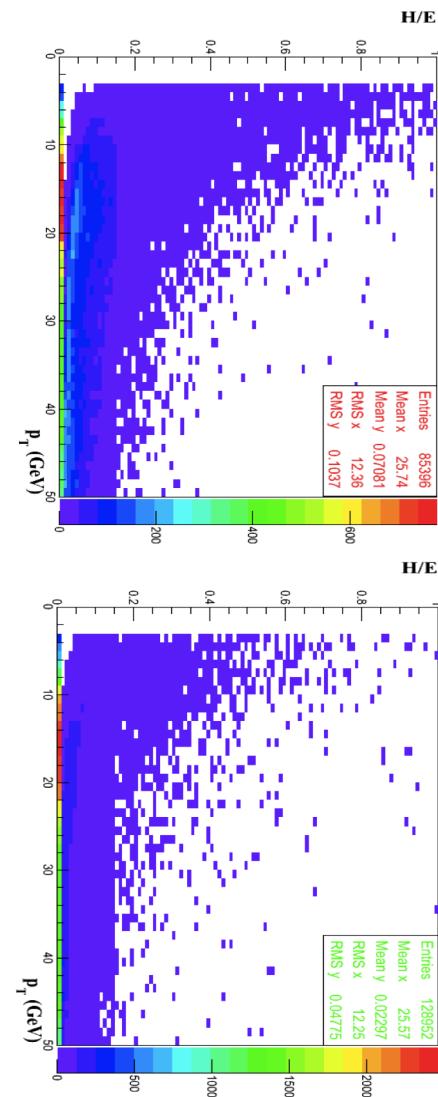


Figure 2.19: The H/E versus the p_T of reconstructed electrons in the Phase 1 Pixel detector scenario (left) and the HCAL upgrade scenario (right). An $H/E < 0.05$ cut in the HCAL upgrade scenario is equivalent to an $H/E < 0.15$ in the Phase 1 Pixel detector scenario. The HCAL upgrade scenario with its increased signal-to-noise performance and out-of-time pile-up suppression has roughly a factor of 3 less HCAL energy behind reconstructed electrons.

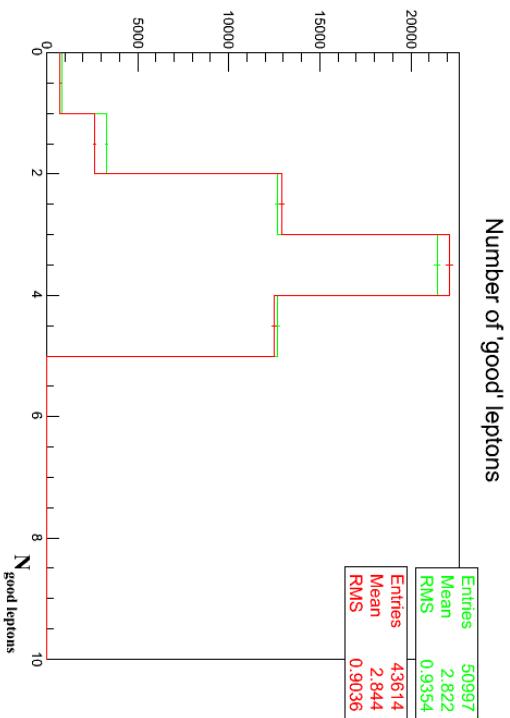


Figure 2.20: Number of electrons passing all selection requirements, (in the $H \rightarrow 4e$ channel analysis), with the addition of the cut $H/E < 0.05$ in the HCAL Upgrade scenario. In red, the Phase 1 Pixel detector scenario; in green, the HCAL upgrade scenario. Plots are normalized to the number of entries in the HCAL upgrade scenario.

the information from the silicon tracker and the muon spectrometer. The PF muons are selected among the reconstructed muon track candidates by applying minimal requirements on the track components in the muon system and taking into account a matching with small energy deposits in the calorimeters.

The isolation of individual leptons ($l = e, \mu$) is measured relative to their transverse momentum (p_T^l), by summing on all the particles (charged and neutral) reconstructed within a cone of $\Delta R < 0.4$ around the lepton direction (as reconstructed at the interaction vertex):

$$R_{ISO}^l = (\sum p_T^{\text{charged}} + \text{MAX}[0, \sum E_T^{\text{neutrals}} + \sum E_T^\gamma - \rho \cdot A_{eff}]) / p_T^l$$

The $\sum p_T^{\text{charged}}$ is the scalar sum of the transverse momenta of the charged hadrons originating from the primary vertex, where the primary vertex is defined as the vertex with the highest sum of p_T^2 of its constituent tracks. The $\sum E_T^{\text{neutrals}}$ and the $\sum E_T^\gamma$ are the sums of the transverse energies of the neutral hadrons and of the photons respectively. Finally, the term $\rho \cdot A_{eff}$ subtracts an estimate (obtained using a *jet area* technique) of the transverse energy of neutral particles within the isolation cone, coming from pileup of additional pp collisions. In the 2012 $H \rightarrow 4l$ reference analysis, muons and electrons are considered isolated if $R_{ISO}^l < 0.4$. At higher \sqrt{s} and PU, as in the samples under study, the value of this isolation variable increases significantly and will need to be adjusted for optimal use in a high pile-up environment. For this study, we have not changed the definition of R_{ISO}^l , but have loosened the cuts on this quantity to maintain signal efficiency.

In the upgraded HCAL scenario, the increase in R_{ISO}^l is typically 30% less than in the Pixel Phase 1 scenario. This is mostly due to the improved readout electronics of the HCAL upgrade, in addition to the refined segmentation of the calorimeter. In order to be coherent, different cut values have been decided for the two scenarios. In the Pixel Phase 1 scenario, muons and electrons have been considered isolated if $R_{ISO}^l < 5.0$. On the other hand, in the HCAL upgrade scenario, a tighter cut has been chosen, requiring $R_{ISO}^l < 3.5$. This improvement could have significant consequences on background rejection, since a tighter cut on the leptons isolation could significantly reduce the background contamination. Unfortunately this effect cannot be quantified as the relevant Monte Carlo background samples, with the proposed upgrades and the different beam conditions, were not available for this study.

The electron and muon pairs from Z decays should originate from the primary vertex. This is ensured by requiring that the significance of the impact parameter to the event vertex, $SIP_{3D} = \frac{IP}{\sigma_{IP}} \text{ satisfies } |SIP_{3D}| < 4$, for each lepton. The IP is the lepton impact parameter in three dimensions at the point of closest approach with respect to the primary interaction vertex and σ_{IP} is the associated uncertainty.

Using well identified and isolated leptons, a $4l$ candidate is then selected. The lepton isolation requirements suppress the $Z + \text{jet}$, $Zb\bar{b}$ and $t\bar{t}$ backgrounds. The requirement on the significance of the impact parameter to the event vertex further suppresses the $Zb\bar{b}$ and $t\bar{t}$ backgrounds. When building the Z candidates, a Z candidate is formed by a lepton pair with the same flavour and opposite charge (l^+l^-). The lepton pair with the invariant mass closest to the nominal Z mass is denoted Z_1 and it's required to have $40 \text{ GeV} < m_{Z_1} < 120 \text{ GeV}$. Then, considering all remaining leptons, a second l^+l^- pair, with mass denoted m_{Z_2} , is required to satisfy $12 \text{ GeV} < m_{Z_2} < 120 \text{ GeV}$. The 12 GeV cut provides an optimal sensitivity for a Higgs boson mass hypothesis in the range $110 \text{ GeV} < m_H < 160 \text{ GeV}$. If more than one Z_2 candidate satisfies all the criteria, the ambiguity is resolved by choosing the lepton pair with highest p_T . Among the four selected leptons forming the two Z candidates, at least one should have $p_T > 20 \text{ GeV}$ and another one should have $p_T > 10 \text{ GeV}$. To reduce background from leptons originating

from hadron decays in jet fragmentation, or from the decay of low-mass hadronic resonances, it's required that any oppositely charged lepton pair chosen among the four selected leptons (irrespective of flavour) satisfies $m_{l^+l^-} > 4$ GeV. The phase space for the search for the SM Higgs boson is finally defined by restricting the mass range to $m_{4l} > 100$ GeV.

2.6.2.2 Comparative Results

After tightening the cuts in the HCAL Upgrade scenario on (1) the isolation of the single leptons by 30% and (2) the $H/E < 0.05$ for electrons, no changes in the number of selected leptons in each event are expected with respect to Phase 1 Pixel detector scenario. This is confirmed from the distributions in Figures 2.20 and 2.21.

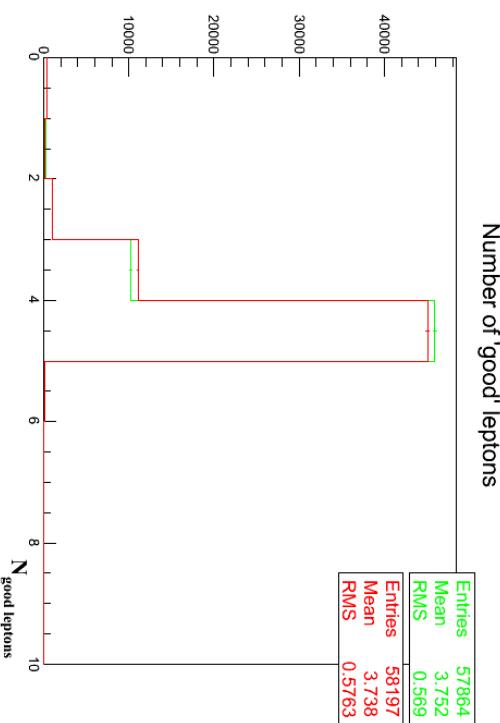


Figure 2.21: Number of muons passing all selection requirements, (in the $H \rightarrow 4\mu$ channel analysis). In red, the Phase 1 Pixel detector scenario; in green, the HCAL upgrade scenario. Plots are normalized to the number of entries in the HCAL upgrade scenario. The lepton isolation has been tightened by 30% in the HCAL upgrade case without reduction in efficiency.

Comparable efficiencies are obtained for all channels, with differences being smaller than 3%. A summary of efficiencies obtained for both scenarios (upgraded HCAL and Phase 1 Pixel detector) is reported in table 2.2.

Table 2.2: Efficiencies for the $H \rightarrow ZZ \rightarrow 4l$ analysis, with the upgraded HCAL and with the Phase 1 Pixel detector. The ratio of the efficiencies is close to unity for all three final states after tightening isolation and identification requirements.

Channel	Overall Efficiency		Efficiency ratio
	HCAL upgrade	Phase 1 geometry	
$H \rightarrow 4\mu$	$(36.1 \pm 0.2)\%$	$(36.0 \pm 0.2)\%$	1.00
$H \rightarrow 4e$	$(10.5 \pm 0.1)\%$	$(10.2 \pm 0.1)\%$	1.03
$H \rightarrow 2e2\mu$	$(20.9 \pm 0.1)\%$	$(20.3 \pm 0.1)\%$	1.03

The HCAL Upgrades enable the tightening of lepton isolation and identification cuts aimed at lowering backgrounds while maintaining high signal efficiency in the $H \rightarrow 4l$ analyses. The quality of the lepton selection and the reconstruction of the Z candidates are unchanged by the tighter selection cuts in the HCAL Upgrade geometry. This is confirmed by the m_{Z_1} and m_{Z_2} distributions, respectively shown in Fig. 2.22 and in Fig. 2.23, which have identical mean values and widths in the two scenarios (Pixel Phase 1 and HCAL upgrade). Similarly, the m_{4l} distribution is identical in the two scenarios, as shown in Fig. 2.24.

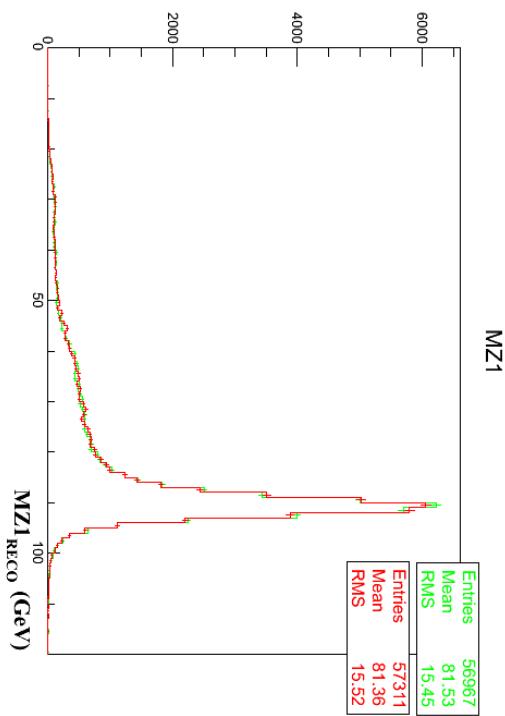


Figure 2.22: Distribution of m_{Z_1} for signal events in the $H \rightarrow 4\mu$ channel analysis. In red, the Phase 1 Pixel detector scenario; in green, the HCAL upgrade scenario. Plots are normalized to the number of entries in the HCAL upgrade scenario. The quality of the lepton selection and the reconstruction of the Z candidates are unchanged by the tighter selection cuts in the HCAL Upgrade geometry.

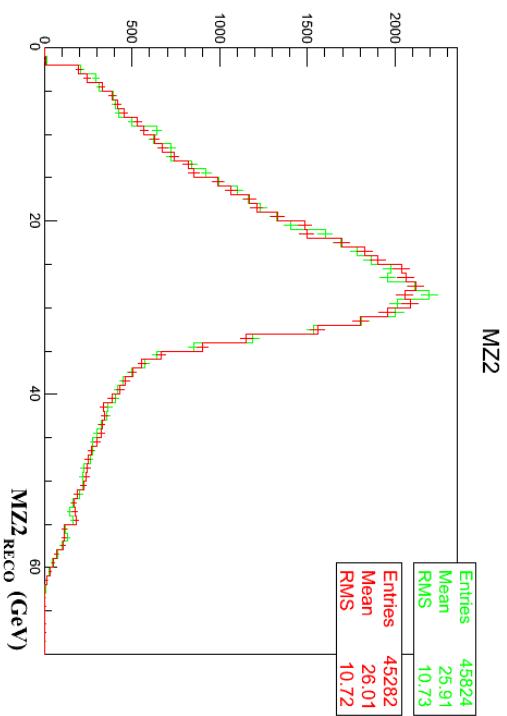


Figure 2.23: Distribution of m_{Z_2} for signal events in the $H \rightarrow 4\mu$ channel analysis. In red, the Phase 1 Pixel detector scenario; in green, the HCAL upgrade scenario. Plots are normalized to the number of entries in the HCAL upgrade scenario. The quality of the lepton selection and the reconstruction of the Z candidates are unchanged by the tighter selection cuts in the HCAL Upgrade geometry.

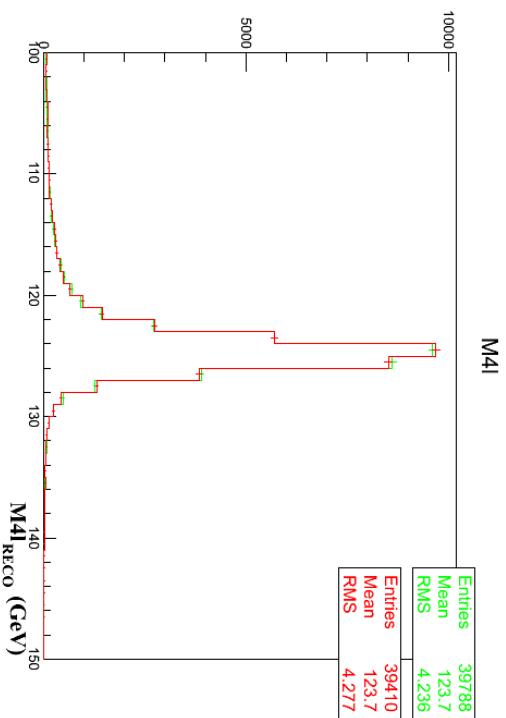


Figure 2.24: Distribution of $m_{4\ell}$ (in the $H \rightarrow 4\mu$ channel analysis), in a Higgs boson Monte Carlo sample with $m_H = 125$ GeV, at $\sqrt{s} = 14$ TeV. In red, the Phase 1 Pixel detector scenario; in green, the HCAL upgrade scenario. Plots are normalized to the number of entries in the HCAL upgrade scenario. The quality of the lepton selection and the reconstruction of the Z candidates are unchanged by the tighter selection cuts in the HCAL Upgrade geometry.

2.6.2.3 Conclusions

The upgrade of the hadronic calorimeter is expected to significantly improve the performance of lepton identification and isolation in a high pile-up environment. The amount of HCAL energy measured behind reconstructed electrons is found to be a factor of 3 smaller in the HCL Upgrade geometry. This allows a tightening of the H/E cut by a factor of 3 for the same electron signal efficiency. A similar improvement in the isolation variable allows for a tightening of 30% in the particle-flow isolation, retaining the same efficiencies as the previous scenario. This expected reduction in background contamination cannot be quantified in this study, due to the missing Monte Carlo samples with the appropriate detector upgrades and beam conditions. Nevertheless this study shows that, with the introduction of the HCAL upgrade, identical signal selection efficiencies for $H \rightarrow 4\mu$, $2e2\mu$, and 4μ can be obtained using a 30% tighter H/E cut on the isolation value of each of the 4 leptons and a factor of 3 tighter H/E cut for electrons.

2.7 Full Analysis Results in the Search for Supersymmetry

The performances of an inclusive third-generation supersymmetry (SUSY) search and a diphoton plus missing transverse energy search are evaluated with full simulation in a high pile-up environment for standard and upgraded geometries of the hadron calorimeter (HCAL) [24]. The inclusive third-generation search selects a final state with a single lepton, missing transverse energy (MET), and a high multiplicity of jets, using b-tagging methods to measure the heavy-flavor content of the event. The HCAL Upgrade geometry is shown to improve the particle-flow jet p_T resolution, which in turn improves the missing H_T resolution. The signal-to-background of the third-generation SUSY search is improved in the HCAL Upgrade geometry for events with large missing H_T and large H_T . The search in the diphoton plus missing transverse energy topology also sees an improvement in the \cancel{E}_T resolution in the HCAL Upgrade geometry. The mismeasurement tails in the high \cancel{E}_T region of the analysis are reduced. The HCAL Upgrade improvements come from a reduction of out-of-time pile-up energies and an improvement in the signal-to-noise ratio and a finer granularity of the detector readout.

2.7.1 Third-Generation SUSY Search

This analysis is based on a search for Supersymmetry (SUSY) in final states with a single lepton, b-quark jets, and missing transverse energy (\cancel{E}_T) at $\sqrt{s} = 7$ TeV with 2011 data [25]. We apply the search to full simulation of the standard and upgraded geometries of the hadron calorimeter (HCAL) at $\sqrt{s} = 14$ TeV with an average of 50 pile-up events every 25ns LHC bunch crossing. The purpose of the search is to maintain high efficiency and low backgrounds for selecting light gluinos decaying to light third-generation squarks, which then decay to top and bottom quarks. In addition, this analysis is also suited for the detection of direct production of third-generation squarks (\tilde{t}) at high luminosity as given by the planned upgrade. In a high pile-up environment, the total energy in the collision has the potential of overwhelming new physics signals unless the sensitivity to pile-up is reduced for quantities that measure the level of hadronic activity in the event. The HCAL Upgrades have the potential of reducing out-of-time pile-up through the use of calorimeter TDC timing measurements and by improving the signal-to-background ratio of energy measurements in a finer granularity readout. In particular, particle-flow jets can be improved through better separation of hadronic clusters and their association to individual particles.

2.7.1.1 Analysis

This analysis focuses on the detection of signal events with significant hadronic activity, quantified by the scalar sum of the transverse momenta of selected jets H_T , and missing transverse momentum \cancel{E}_T , which is calculated with the CMS particle-flow algorithm [26, 27], combining information from different sub-detectors to reconstruct all visible particles. The absolute value of the vectorial sum of these particles is defined as \cancel{E}_T .

2.7.1.2 Monte Carlo Samples

The search is repeated on Monte Carlo full simulation of the detector in the Standard, Pixel, and Pixel+HCAL geometries. Simulated events are produced with the GEANT4 package [28] for the full detector simulation in the Standard, Pixel, and Pixel+HCAL geometries.

The production and the decay of $t\bar{t}$ pairs and vector bosons in association with the production of hard jets are generated using MADGRAPH [29]. The produced parton events are then passed to PYTHIA6 [30] with tune Z2 [31] for simulating parton showers, multiple interactions and fragmentation processes. The decay of τ leptons is simulated using TAUOLA [32].

SUSY mass spectra and branching ratios have been calculated at the electroweak scale using the renormalization group equations implemented in the SOFTSUSY package [33], interfaced to PYTHIA6. The low mass scenarios LM6 and LM9 [34] are used as cMSSM benchmark scenarios. The following background samples for $t\bar{t}$ + jets and Drell-Yan ($\mu^+ \mu^-$) + jets and signal samples for LM6 and LM9 have been used:

1. ./PYTHIA6_Tauola_TTbar_TuneZ2star_14TeV
/DYToMuMu_M_20_TuneZ2star_14TeV_pythia6
/PYTHIA6_SUSY_LM6_sfshht_14TeV
/PYTHIA6_SUSY_LM9_sfshht_14TeV
/Summer12-UpgradeStdGeom2_DR428-PU50-DESIGN42_V17S-v1
2. ./PYTHIA6_Tauola_TTbar_TuneZ2star_14TeV
/DYToMuMu_M_20_TuneZ2star_14TeV_pythia6
/PYTHIA6_SUSY_LM6_sfshht_14TeV
/PYTHIA6_SUSY_LM9_sfshht_14TeV
/Summer12-UpgradePhase1_DR428-PU50-DESIGN42_V17S-v1
3. ./DYToMuMu_M_20_TuneZ2star_14TeV_pythia6
/PYTHIA6_SUSY_LM6_sfshht_14TeV
/PYTHIA6_SUSY_LM9_sfshht_14TeV
/Summer12-UpgradeHCAL_PixelPhase1_DR428-PU50-DESIGN42_V17S-v1
4. ./PYTHIA6_Tauola_TTbar_TuneZ2star_14TeV
/Summer12-UpgradeHCAL_PixelPhase1_DR428_R2-PU50-DESIGN42_V17S-v1

where samples (1) are in the standard, samples (2) are in the Pixel Upgrade, and samples (3) and (4) are in the Pixel+HCAL Upgrade geometries. The reconstruction software release version for the Pixel+HCAL Upgrade samples is CMS-SW-4-2-8-SLHChc14-patch3 for the Drell-Yan + jets and LM6/LM9 signal samples. This reconstruction software introduces a 50ns spacing for HCAL hits relative to the 25ns spacing for all other subdetectors. This difference in time spacing is an approximate model for time window suppression applied with the HCAL Upgrade TDC measurements. The $t\bar{t}$ + jets background sample is reconstructed with release CMS-SW-4-2-8-SLHChc15 where all hits are spaced at 25ns and no timing window is applied. Differences in performance for the $t\bar{t}$ + jets sample come from intrinsic signal-to-background improvements with finer granularity in the detector readout.

2.7.1.3 Event Selection

Muon candidates [35] are required to have $p_T(\mu) > 20\text{ GeV}$ and $|\eta| < 2.1$, and its reconstructed track must have an impact parameter $d_0 < 0.02\text{ cm}$ in the transverse plane with respect to the beam spot and $|d_z| < 1.0\text{ cm}$ with respect to the primary vertex along the z direction. In addition, the muon is required to be isolated within a cone of size $\Delta R = 0.3$. The relative combined isolation of the muon, defined as the sum of the transverse energy E_T (as measured in the electromagnetic and hadron calorimeters) and the transverse momentum p_T (as measured in the silicon tracker) of all reconstructed objects within this cone, excluding the muon, $I_{\text{rel}}^{\text{comb}} = \sum_{\Delta R < 0.3} (E_T + p_T)/p_T(\mu)$, is required to be $I_{\text{rel}}^{\text{comb}} < 0.15$.

The reconstruction of jets is based on the CMS particle-flow algorithm. Extra energy clustered into jets due to pileup is taken into account with an event-by-event correction to the jet four-vectors. Jets are reconstructed from particle-flow candidates using the anti- k_T clustering

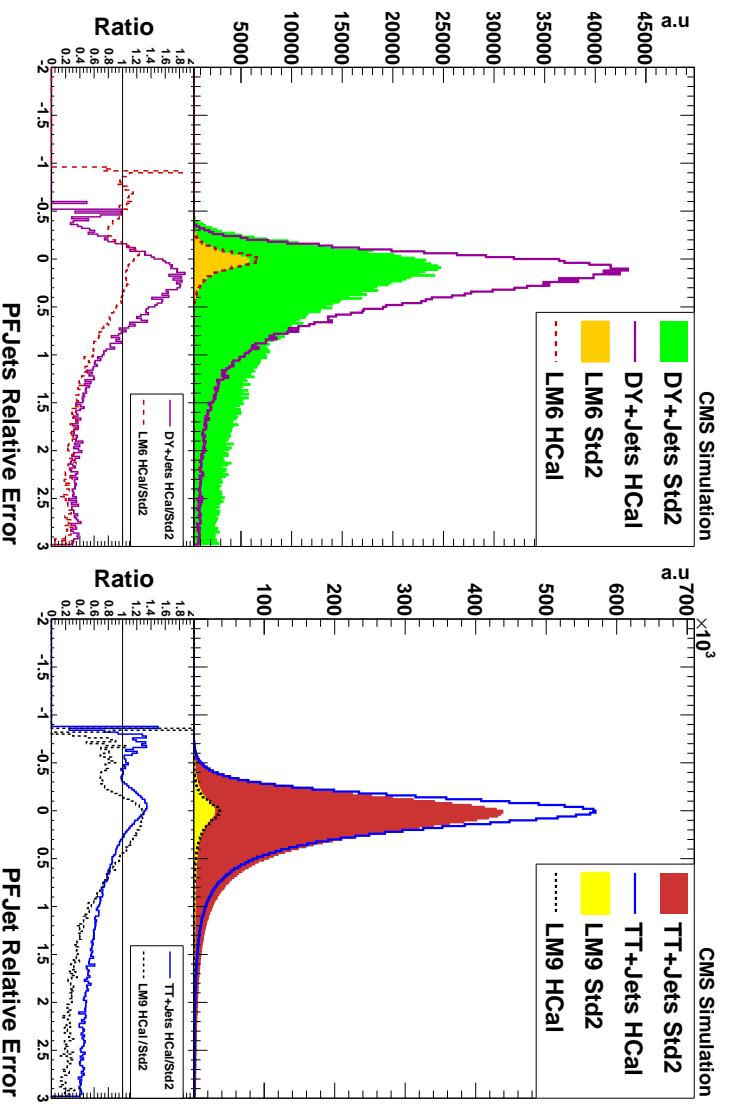


Figure 2.25: The distributions of the relative error on the particle-flow jet p_T measurement as compared to generator jets with a $\Delta R < 0.3$ matching parameter. The Drell-Yan ($\mu^+ \mu^-$) + jets (green) background and the LM6 (yellow) signal are plotted on the left for the standard (solid histogram) and Pixel+HCAL Upgrade (open histogram) geometries. The $t\bar{t}$ + jets (red) background and the LM9 (yellow) signal are plotted on the right for the standard (solid histogram) and Pixel+HCAL Upgrade (open histogram) geometries. Ratios of the distributions are shown underneath. The relative error on the particle-flow jet p_T measurement is improved in the Pixel+HCAL Upgrade geometry for background and signal samples.

algorithm [36] with a distance parameter of 0.5. Different corrections are applied on the raw jet energy to obtain a relative uniform response across the detector in η and an absolute calibrated response in p_T [37]. At least four jets with $p_T > 40$ GeV and $|\eta| < 2.4$ passing different quality criteria in order to suppress noise and spurious energy deposits are required, which are spatially separated from a selected lepton by $\Delta R > 0.3$.

The missing transverse energy is reconstructed by summing up the transverse momentum vectors of all particle-flow objects.

2.7.1.4 Comparative Results

Several improvements are observed in the HCAL Upgrade geometry relative to the standard geometry in hadronic event quantities. Figure 2.25 shows the relative error on the p_T measurement of particle-flow jets with respect to generator jets, defined as $(p_T - p_T^{gen})/\rho_T^{gen}$ with a $\Delta R < 0.3$ matching parameter between generator and reconstructed jets. Large mismeasurement tails are observed in the standard geometry, where the corresponding tails in the HCAL Upgrade geometry are substantially reduced. Improvements are seen in both the signal and background samples. The relative improvement in the $t\bar{t}$ + jets sample is lower than in the Drell-Yan sample due to the lack of a timing window in the $t\bar{t}$ + jets sample to better suppress out-of-time pile-up.

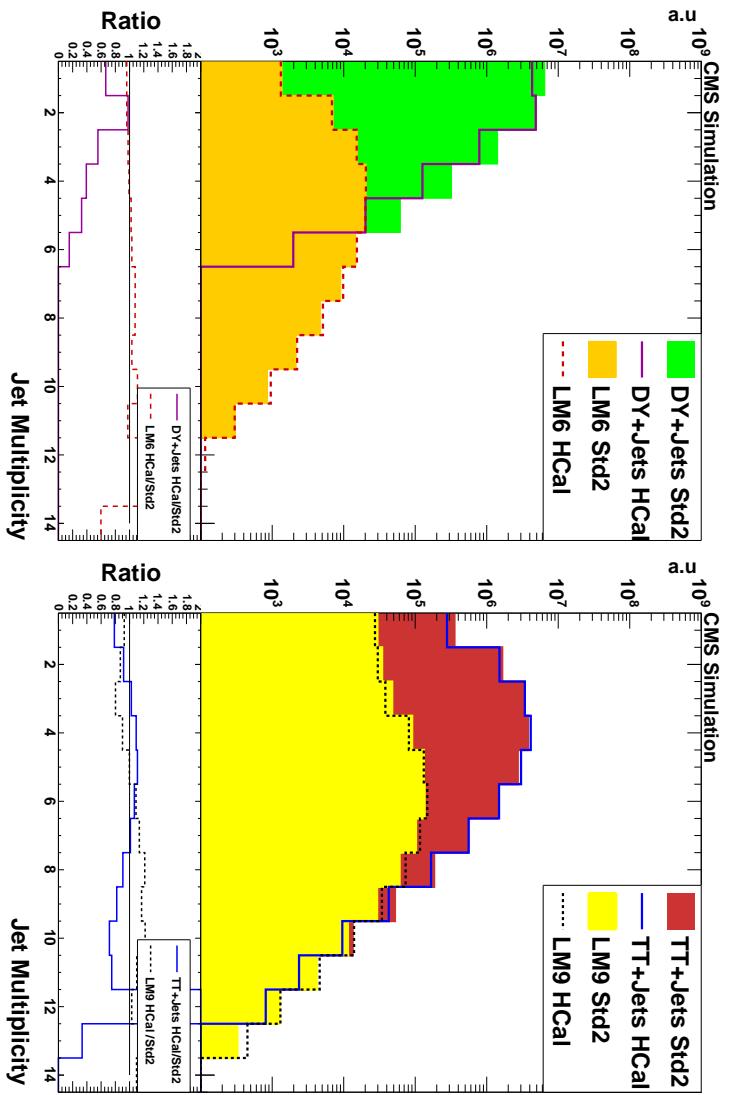


Figure 2.26: The jet multiplicity distributions are plotted for Drell-Yan ($\mu^+\mu^-$) + jets (green) background and the LM6 (yellow) signal on the left and $t\bar{t}$ + jets (red) background and the LM9 (yellow) signal on the right for the standard (solid histogram) and Pixel+HCAL Upgrade (open histogram) geometries. Ratios of the distributions are shown underneath. The decrease in the jet multiplicities for the Pixel+HCAL Upgrade geometry indicates a reduction in the number of pile-up induced jets entering the event selection.

As one of the signal properties of the SUSY events is a high number of jets with $p_T > 40$ GeV, the application of jet identification to reduce the number of pile-up jets entering the event selection is important. Even with the application of pile-up suppression in the jet ID, the HCAL Upgrade samples additionally demonstrate a lower number of pile-up induced jets into the jet multiplicity distributions, as shown in Figure 2.26.

The improvement in the relative error on the particle-flow jet p_T measurement and the reduction in the number of pile-up induced jets with a $p_T > 40$ GeV directly improve the relative error of the particle-flow \cancel{E}_T measurement. A comparison of the relative error on the \cancel{E}_T measurement as determined from the generator-level quantity for events with intrinsic non-zero \cancel{E}_T is shown in Fig. 2.27 from $t\bar{t}$ + jets and the LM9 signal for standard and Pixel+HCAL Upgrade geometries. A substantial narrowing of the relative error distributions is observed for signal and backgrounds for the Pixel+HCAL Upgrade geometry.

The SUSY search analysis focuses on the large \cancel{E}_T and large H_T region of the event selection. The \cancel{E}_T distributions are shown in Fig. 2.28.

With a selection cut of $\cancel{E}_T > 60$ GeV applied, the H_T distribution of the selected events is shown in Fig. 2.29. The generator-level H_T distributions are also plotted in Fig. 2.29 for the background processes and show closer agreement with the Pixel+HCAL Upgrade geometry.

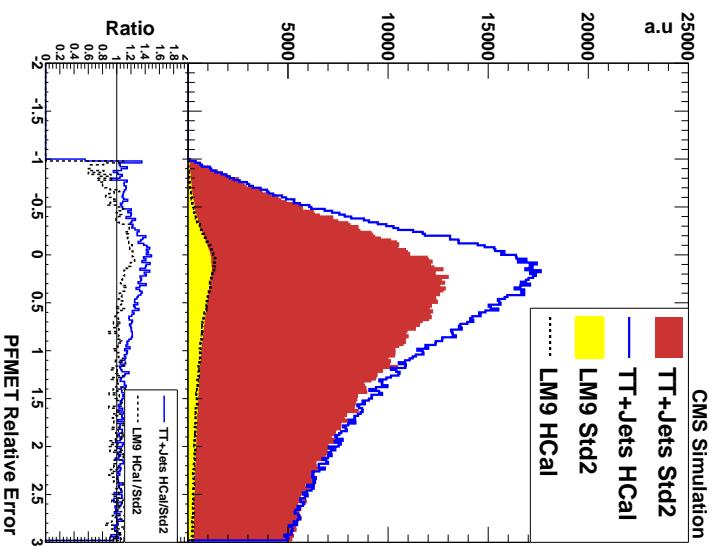


Figure 2.27: The distributions of the relative error on the particle-flow \cancel{E}_T measurement as compared to the generator value for events with intrinsic non-zero \cancel{E}_T . The $t\bar{t} + \text{jets}$ (red) background and the LM9 (yellow) signal are plotted for the standard (solid histogram) and Pixel+HCAL Upgrade (open histogram) geometries. Ratios of the distributions are shown underneath. The relative error on the \cancel{E}_T measurement is improved in the Pixel+HCAL Upgrade geometry for background and signal samples. The intrinsic \cancel{E}_T of the Drell-Yan ($\mu^+\mu^-$) + jets background is small, and, therefore, the relative error is not plotted.

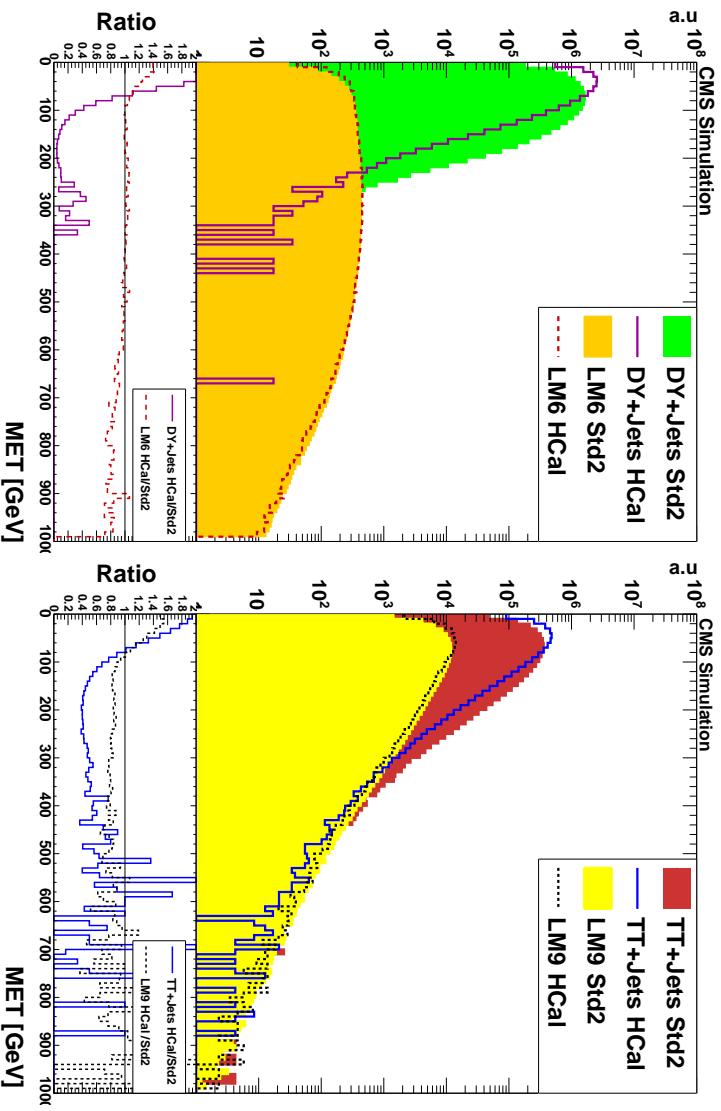


Figure 2.28: The \cancel{E}_T distributions are plotted for Drell-Yan ($\mu^+ \mu^-$) + jets (green) background and the LM6 (yellow) signal on the left and $t\bar{t}$ + jets (red) background and the LM9 (yellow) signal on the right for the standard (solid histogram) and Pixel+HCAL Upgrade (open histogram) geometries. Ratios of the distributions are shown underneath. There is a reduction in the amount of high \cancel{E}_T background relative to signal in the Pixel+HCAL Upgrade geometry.

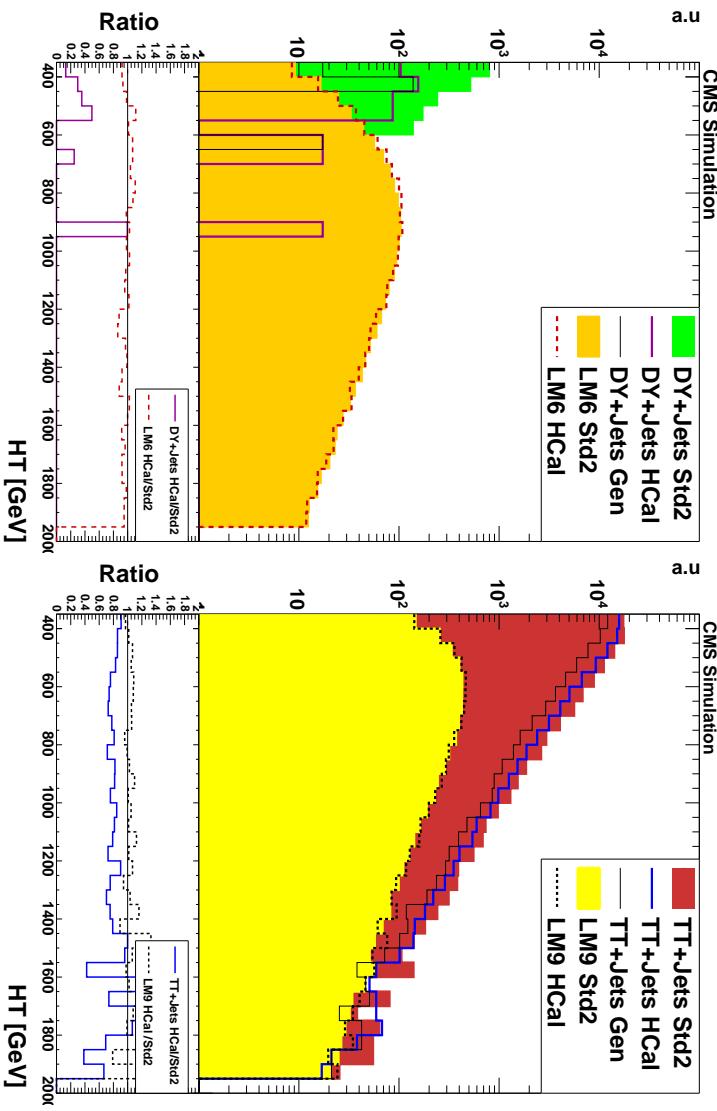


Figure 2.29: The H_T distributions for events with $\cancel{E}_T > 60 \text{ GeV}$ are plotted for Drell-Yan ($\mu^+ \mu^-$) + jets (green) background and the LM9 (yellow) signal on the left and $t\bar{t}$ + jets (red) background and the LM9 (yellow) signal on the right for the standard (solid histogram) and Pixel+HCAL Upgrade (open histogram) geometries. The generator-level H_T distribution for the backgrounds are superimposed (solid black line) for the background processes and show closer agreement with the Pixel+HCAL Upgrade geometry. Ratios of the distributions are shown underneath. The signal-to-background ratio of events with large \cancel{E}_T and large H_T is improved for the Pixel+HCAL geometry relative to the standard geometry.

2.7.1.5 Conclusions

The impact of the upgrade Pixel+HCAL geometry on the search for third-generation supersymmetry in the single lepton, b -jets, and \cancel{E}_T channel is evaluated in a high pile-up environment. For the two major backgrounds to the third-generation SUSY search, $t\bar{t} + \text{jets}$ and Drell-Yan ($\mu^+\mu^-$) + jets, the signal-to-background is improved in the HCAL Upgrade geometry relative to the standard geometry in the large \cancel{E}_T , large H_T region of the event selection.

2.7.2 Two Photons and Missing Transverse Energy

The proposed Phase 1 Pixel and HCAL Upgrades can provide several benefits to SUSY analyses with photons and missing transverse energy (MET) compared with the current detector geometries. This study examines the improvement to the measurement of missing transverse energy (MET) under high pile-up conditions at the nominal LHC energy of 14 TeV.

2.7.2.1 Analysis

The SUSY search in the $\gamma\gamma + \cancel{E}_T$ channel looks for diphoton events with large \cancel{E}_T as a signature of new physics. As the SM does not predict many processes to have two photons and large true \cancel{E}_T , the majority of the events in the \cancel{E}_T distribution comes from the mismeasurement of events without true \cancel{E}_T . The only irreducible background, SM processes with two photons and true \cancel{E}_T , comes from $W\gamma\gamma$ and $Z\gamma\gamma$ which have very small cross-sections.

The distribution of the \cancel{E}_T measurement for p_T -balanced events with diphoton candidates is computed using two methods. The first method is to estimate the \cancel{E}_T distributions with Monte Carlo simulation accounting for each of the contributing background processes and using the full simulation to estimate the \cancel{E}_T measurements. The second method is to extract a data-derived sample of the p_T -balanced events and to re-weight the contribution of the \cancel{E}_T distribution for these events according to the total p_T of the diphoton candidate. The re-weighting is done to remove the bias imposed by the high resolution electromagnetic (ECAL) calorimeter measurement for electromagnetic (EM) energy depositions. The di-EM sample can be a selection of Z bosons decaying to a pair of electrons or an inclusive QCD multijet sample with a pair of di-EM candidates that fail the isolation criterion for photons, photon candidates that fail the isolation criteria and called “fakes.”

The following background samples for γ +jet, $\gamma\gamma$ -box, Drell-Yan (e^+e^-) + jets, and QCD multijets have been used:

1. /PYTHIA6_g_PhotonPt25to250_TuneZ2star_14TeV
/PYTHIA6_ggbox_diphotonPt25to250_TuneZ2star_14TeV
/DYToEE_M_20_TuneZ2star_14TeV_pythia6
/QCD_Pt_800to1000_TuneZ2star_14TeV_pythia6
/QCD_Pt_600to800_TuneZ2star_14TeV_pythia6
/QCD_Pt_470to600_TuneZ2star_14TeV_pythia6
/QCD_Pt_300to470_TuneZ2star_14TeV_pythia6
/Summer12-UpgradeStdGeom2_DR428-PU50-DESIGN42_V17S-v1
2. /PYTHIA6_g_PhotonPt25to250_TuneZ2star_14TeV
/PYTHIA6_ggbox_diphotonPt25to250_TuneZ2star_14TeV
/DYToEE_M_20_TuneZ2star_14TeV_pythia6
/QCD_Pt_800to1000_TuneZ2star_14TeV_pythia6
/QCD_Pt_600to800_TuneZ2star_14TeV_pythia6

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/QCD_Pt_470to600_TuneZ2star_14TeV-pythia6
/QCD_Pt_300to470_TuneZ2star_14TeV-pythia6
/Summer12-UpgradePhase1_DR428-PU50-DESIGN42_V17S-v1

3. /PYTHIA6_g_PhotonPt25to250_TuneZ2star_14TeV
/PYTHIA6_ggbox_diphotonPt25to250_TuneZ2star_14TeV
/DYToEE_M_20_TuneZ2star_14TeV-pythia6
/QCD_Pt_800to1000_TuneZ2star_14TeV-pythia6
/QCD_Pt_600to800_TuneZ2star_14TeV-pythia6
/QCD_Pt_470to600_TuneZ2star_14TeV-pythia6
/QCD_Pt_300to470_TuneZ2star_14TeV-pythia6
/Summer12-UpgradeHCAL_PixelPhase1_DR428-PU50-DESIGN42_V17S-v1

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where samples (1) are in the standard, samples (2) are in the Pixel Upgrade, and samples (3) are in the Pixel+HCAL Upgrade geometries. The reconstruction software release version for Pixel+HCAL Upgrade samples is CMS SW-4-2-8-SLHCCh14-patch3. This reconstruction software introduce a 50ns spacing for HCAL hits relative to the 25ns spacing for all other subdetectors. This difference in time spacing is an approximate model for time window suppression applied with the HCAL Upgrade TDC measurements.

2.7.2.2 Event Selection

Events passing the selection are classified into four types of events based on the photon candidates. These contain: diphoton ($\gamma\gamma$), dielectron (ee), electron-photon ($e\gamma$), and fake-fake (ff). The selection criteria to identify the photon candidates are listed in Table 2.3.

Table 2.3: Photon identification cuts for diphoton plus missing energy analysis.

	Photons	Electrons	Fakes
p_T (leading/sub-leading)	$> 40/25 \text{ GeV}$	$> 40/25 \text{ GeV}$	$> 40/25$
$ \eta $	< 1.379	< 1.379	< 1.379
Combined Isolation ($dR < 0.3$)	$< 6 \text{ GeV}$	$< 6 \text{ GeV}$	$> 6 \text{ GeV}$
H/E	< 0.05	< 0.05	< 0.05
$\sigma_{ij\eta j}$	< 0.011	< 0.011	< 0.011
Pixel Seed	No	Yes	No

QCD multijet events can contribute diphoton events, either through direct diphoton or multijet production where one or more jets are misidentified as photons. To model the QCD background, a template is created using either dielectron or fake-fake events. Both sets of selections are dominated by intrinsically p_T -balanced processes with no true E_T and have E_T distributions that are primarily due to mismeasurement. As the source of mismeasurement is primarily due to the finite resolution of hadron energy measurements, the size of the fake E_T is correlated with the magnitude of the vector sum of the transverse momenta of the two photon candidates. To more accurately model the shape of the E_T distribution, each bin is reweighted based on the ratio of the di-EM p_T between the dielectron and the fake-fake events. The template E_T distribution is then normalized to the number of events in the signal selection based on the region with $E_T < 70 \text{ GeV}$.

Electroweak processes can contribute to the diphoton signal through W pairs or Z decays to electrons, where electrons are misidentified as photons. To determine the amount of this contribution a study was performed to determine the fake rate for photons due to electron misidentification.

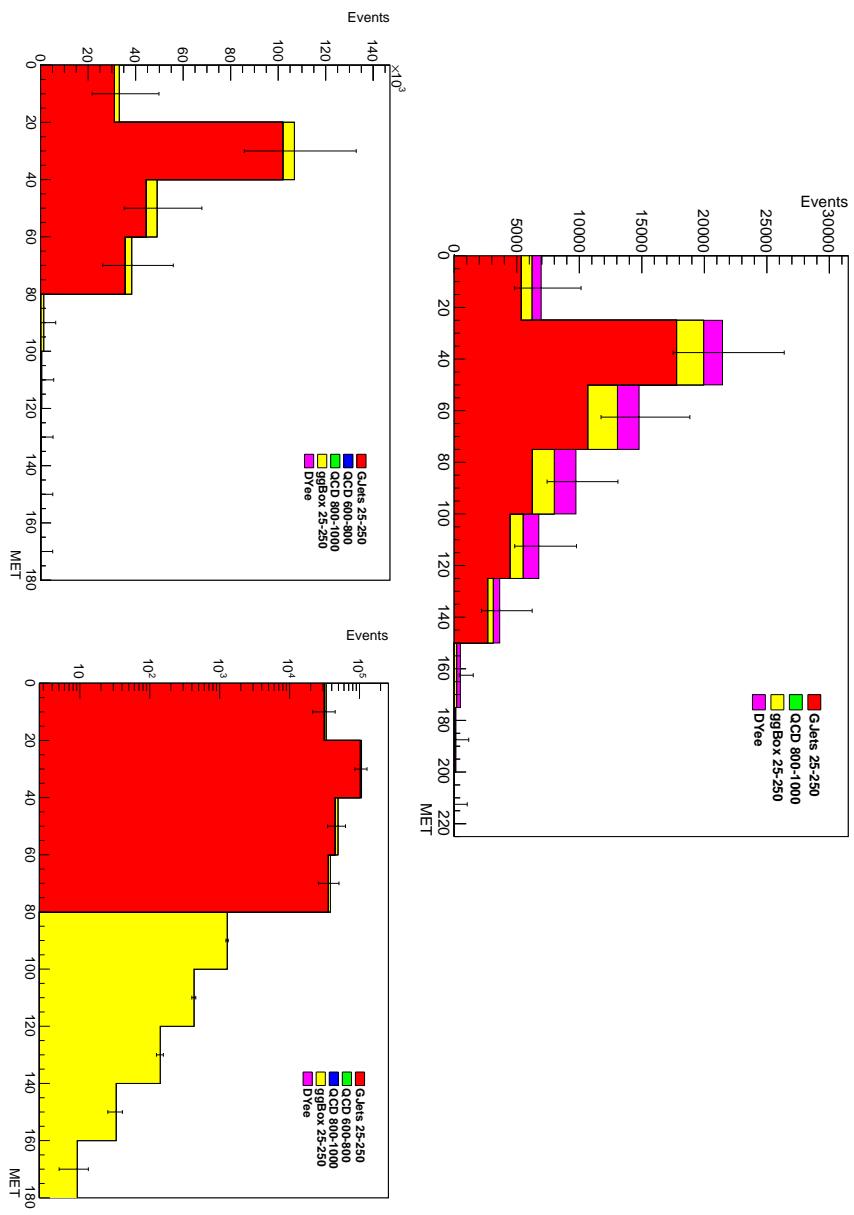


Figure 2.30: The \Z_T distributions for the final signal selection are shown for the standard (top) and Pixel+HCAL (bottom) Upgrade geometries. The spectrum for the upgrade geometry is shown in both linear (left) and logarithmic y -axis scales. The Pixel+HCAL Upgrade geometry has an order of magnitude fewer high \Z_T events above 100 GeV as compared with the standard geometry and negligible contributions from Drell-Yan (e^+e^-) due to the improved photon identification in the Pixel Upgrade geometry.

The photon fake rate was determined by measuring the amount of misidentified electrons in the $e\gamma$ events. This is done by fitting the Z peak in the ee and $e\gamma$ samples. The ratio of Z events in the two samples can then be used to determine the fake rate.

To examine the overall effect on the background for the upgrade with respect to the current geometry, a plot of the \Z_T distribution was generated using the diphoton events from the QCD, photon + jets, and Drell-Yan MC samples.

2.7.2.3 Results

The \Z_T distributions for the final signal selection are shown in Fig. 2.30 for the standard and Pixel+HCAL Upgrade geometries. In the standard geometry, the \Z_T distribution extends to 180 GeV and has a mean of 62 GeV. The Pixel+HCAL Upgrade geometry has an order of magnitude fewer high \Z_T events above 100 GeV as compared with the standard geometry and negligible contributions from Drell-Yan (e^+e^-) due to the improved photon identification in the Pixel Upgrade geometry. The combination of the Pixel and HCAL Upgrades provides significant improvement in the analysis performance through complementary reductions in background processes producing fake high \Z_T in a high pile-up environment.

Chapter 3

Common Front-End Electronics Aspects

As discussed in Chapter 1, the electronics will be very largely common across the HB, HE and HF sub-detectors. Keeping the designs similar allows sharing of resources, reduces the overall engineering needed and simplifies long-term maintenance (technical expertise, spares, etc.) This chapter describes three major components of the FEE which are common across the designs: the Charge (Q) Integrator and Encoder (QIE) ASIC, the Front-End Field-Programmable Gate Arrays (FE-FPGAs), and the CERN-developed Gigabit Transceiver (GBT) data and control links. The data flow path through these components is illustrated in Fig. 3.1. This chapter also discusses the DC-DC converters which will be used in the development of the front-end electronics for all of the HCAL upgrades. The back-end electronics, which is also common across the upgrade projects, is described in Chapter 6.

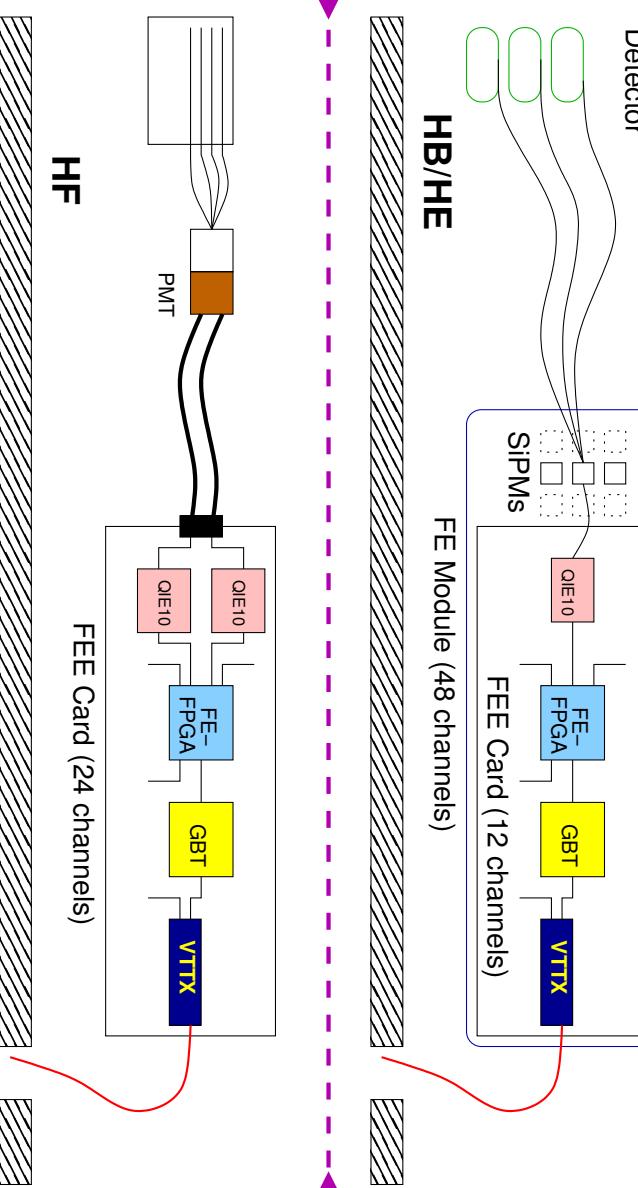


Figure 3.1: Overview of the HB/HE (top) and HF (bottom) data flow paths after the upgrade, showing the common front-end components: Charge (Q) Integrator and Encoder (QIE10), front-end FPGA (FE-FPGA), and the data link GBT (serializer)/VTTx (dual optical transmitter module).

3.1 The Charge (Q) Integrator and Encoder (QIE version 10)

One of the challenges in high-energy collider physics calorimetry is to make precision measurements of energy in a high rate environment over a wide dynamic range while maintaining good low energy sensitivity. Due to photo-statistics, calorimeters typically have poor resolution at low energy, with the resolution improving to an intrinsic limit with increasing energy. This poses an optimization challenge, since the number of bits required to span the dynamic range is significantly larger than is needed to satisfy the precision at the highest energies. HCAL currently meets this challenge with a charge-integrating ASIC, the QIE8, and plans to use an upgraded version of this device, the QIE10, in its upgraded system.

The QIE10 is the latest device in a family of fast, wide dynamic range, dead-timeless ADCs developed for use in high-energy physics experiments [38]. The QIE10 will differ from previous generation chips by incorporating TDC information in the digital output. It is being targeted for use in both the CMS HCAL and Atlas TileCal sub-detectors. A generic chip is being developed to satisfy the requirements of both experiments, but a CMS specific development cycle may be needed if the generic chip does not satisfy all of the HCAL requirements.

3.1.1 Properties of Front-End Signals

Signals from the calorimeter tend to be fast, making signal processing without shaping quite challenging. Figure 3.2 shows the measured pulse shape (energy vs. time) from (a) the scintillating tiles as used in HB/HE/HO, and (b) the steel-quartz fiber Cerenkov detector in HF. Using a charge integrator provides a distinct advantage in the handling of the fast signals from the detector, as long as signal arrival time and pulse shape information can be determined.

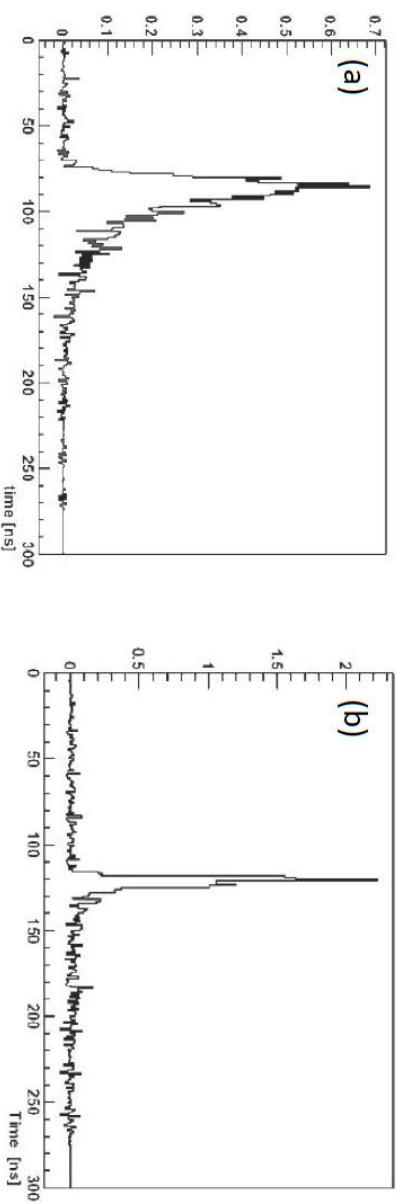


Figure 3.2: Average pulse shapes from a 30 GeV electron impacting directly on an HB wedge (a) and a 50 GeV pion impacting on HF (b), as measured in a testbeam at CERN. These pulse shapes are obtained using the original photodetectors for HB and HF and the full electronics chain including the QIE8. The QIE8 integration has been removed by comparison of multiple testbeam events and an external TDC which measures the phase between the integration clock and the particle arrival. The polarity of the HF signal has been inverted for simpler comparison between HB and HF.

The upgraded photodetectors for HF are quad-anode Hamamatsu PMTs (R7600-200-M4) that produce fast, negative polarity pulses, while HB and HE will have SiPMs that produce positive polarity pulses. The QIE integrates negative polarity signals in its non-inverting input amplifier and positive polarity pulses in its inverting input amplifier. While the specific SiPM device has not yet been selected, the general performance parameters have been determined

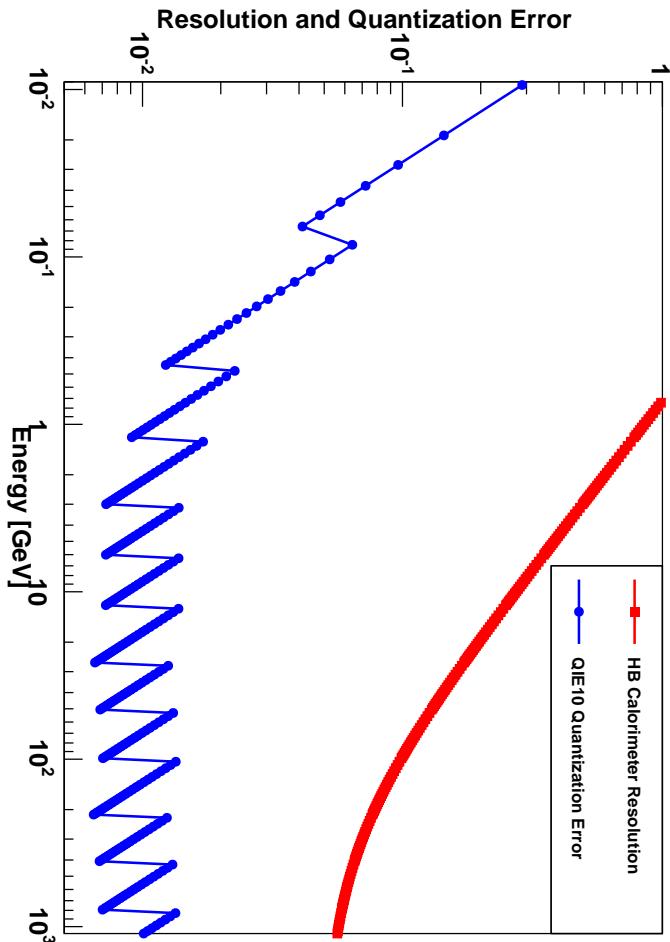


Figure 3.3: HCAL Detector Resolution (solid red curve) and QIE digitization error (blue line with points) versus energy.

(see Section 5.1). The rise time of the SiPM pulse is approximately 2-5 ns while the PMT pulse is faster, approximately 1-2 ms. The SiPM pulse fall time is 20 ns coming from the decay time of the wavelength shifter (WLS) fiber. The PMT signal decay time is 2-5 ns due to the fast nature of Cherenkov signals.

The gain and photo-detection efficiency of the SiPM are substantially larger than that of the HPD for which the QIE8 was designed. To accommodate larger signals from SiPM devices, the sensitivity of the QIE10 least significant bit (LSB) is 3 fC/LSB on both inputs. The QIE10 RMS noise is less than 2 fC. The LSB is set such that there is good signal/noise discrimination for single photoelectrons (10 fC) and so that the MLP calibration signal, (≈ 50 fC), in the tile-fiber calorimeter can be measured with a significance of at least 10 standard deviations.

We specify the largest signal that the electronics should be able to handle to be 1.1 TeV in a single HB/HE channel, which corresponds to 33,000 detected SiPM photoelectrons. The dynamic range from 3 fC to 330 pC requires a 6-bit mantissa for the QIE10 and covers the wide capabilities of the SiPM while maintaining a constant term of 2-3% for large signals, significantly less than the intrinsic detector resolution (see Fig. 3.3). The inverting input (positive input current) is not intended for PMTs with long cables, and has lower input impedance (~ 10 ohms). In addition, this impedance changes somewhat as a function of input amplitude. The dynamic input impedance produces a small amount of amplitude-dependent pulse-shape variation (“time slewing”). This has been simple to correct for in the existing QIE8, and the effect is smaller in the QIE10 due to the smaller electronic gain and faster transistors.

Unlike the HPD and previous generation HF PMT, the SiPM and upgrade HF PMT gains are more closely matched. This allows for the QIE10 sensitivity and dynamic range of inverting and non-inverting inputs to be identical and simplifies the chip design. The HF signal input (non-inverting) differs from the SiPM input (inverting) by having a very small change in in-

put impedance over the QIE10 dynamic range. The constant input impedance is required to provide proper termination of the 5 m cable from the HF PMTs. With a nominally $20\ \Omega$ input impedance, a $30\ \Omega$ series resistor is required to terminate a $50\ \Omega$ cable.

For the upgrade HF PMT signals, the single photoelectron peak occurs at 38 fC for a PMT gain of 4.5×10^5 at an operating voltage of 650 V including the factor of 2 signal reduction from back-termination for the 5 meter-long $50\ \Omega$ coaxial cables between the PMT bases and the QIE10 input. With the same sensitivity for the LSb as with the SiPM (3 fC), the single photoelectron peak occurs at 13 ADC counts with a significance of over 10 standard deviations. With the same dynamic range specification as with the SiPM, the maximum signal for dual(single) readout of the HF PMTs is 35 (17) TeV, corresponding to 8700 photoelectrons.

The pedestal mean of 18 fC (6 LSB counts), and a 4-bit programmable DAC is needed to adjust the pedestal mean in the range 6 - 30 fC in steps of 1.5 fC . The ability to adjust the pedestal within the first linear decoding range of the QIE10 is operationally important for equalizing pedestal means and simplifying online zero suppression calculations.

Timing discrimination of the pulse arrival time is a vital addition to the QIE10 ASIC, especially for the Cherenkov calorimeter where the entire pulse is integrated within 25 ns and therefore no information as to the pulse arrival time within the integration clock can be derived. This is especially useful information to help suppress out-of-time signals in HF. Similarly, for the SiPM signals, high luminosity operation will increase the occupancy of neighboring bunch crossings and reduce the sensitivity to the pulse arrival time determined from the multi-bucket pulse shape. The speed of the HF pulse and the characteristics of the backgrounds require a TDC resolution of at least 800 ps to provide clean separation between nominal and out-of-time signals.

3.1.2 QIE10 functions

The structure and signal flow through the QIE10 is diagrammed in Fig. 3.4. The QIE splits the input signal from a photo-sensor into four ranges that are scaled by factors of 8, with each range integrating a scaled fraction of the current via a bank of capacitors. The output voltage of a capacitor is presented to a comparator. The output from all comparators forms a thermometer code that is used to determine which capacitors voltage should be digitized by the pseudologarithmic Flash-ADC. The FADC bin size doubles several times over its full range, so that the bin size at the top of the FADC is 8 times the bin size at the bottom of the FADC. Since the four integrator ranges are also scaled by a factor of 8, the end result is that the QIE resolution (the FADC bin size divided by the signal magnitude) is held between 0.7% and 1.4% over most of the dynamic range as shown in Fig. 3.3.

The dead-timeless operation is achieved by switching the input current through four banks of nearly-identical integrating capacitors and comparators. The capacitor identification bit identifies the integration phase of the chip. The digital output result for a given integrated input pulse has a four clock period latency ($4 \times 25\text{ ns}$), due to the four functions (integrate, compare, digitize, reset). The wide-dynamic range is spanned with scaled sensitivity ranges, with larger currents being mapped onto less sensitive/lower precision ranges. The advantage of this QIE solution is that it provides precise digitized information of the integrated pulse every 25 ns over a wide dynamic range with minimal impact of clock jitter or arrival time information. Alternative voltage-sampling techniques typically require shaping and extending the pulses to allow multiple measurements over several 25 ns periods, which introduces additional pile-up dependency. The digital information from each channel also is quite sparse and can fit within the required bandwidth of the existing fiber plant.

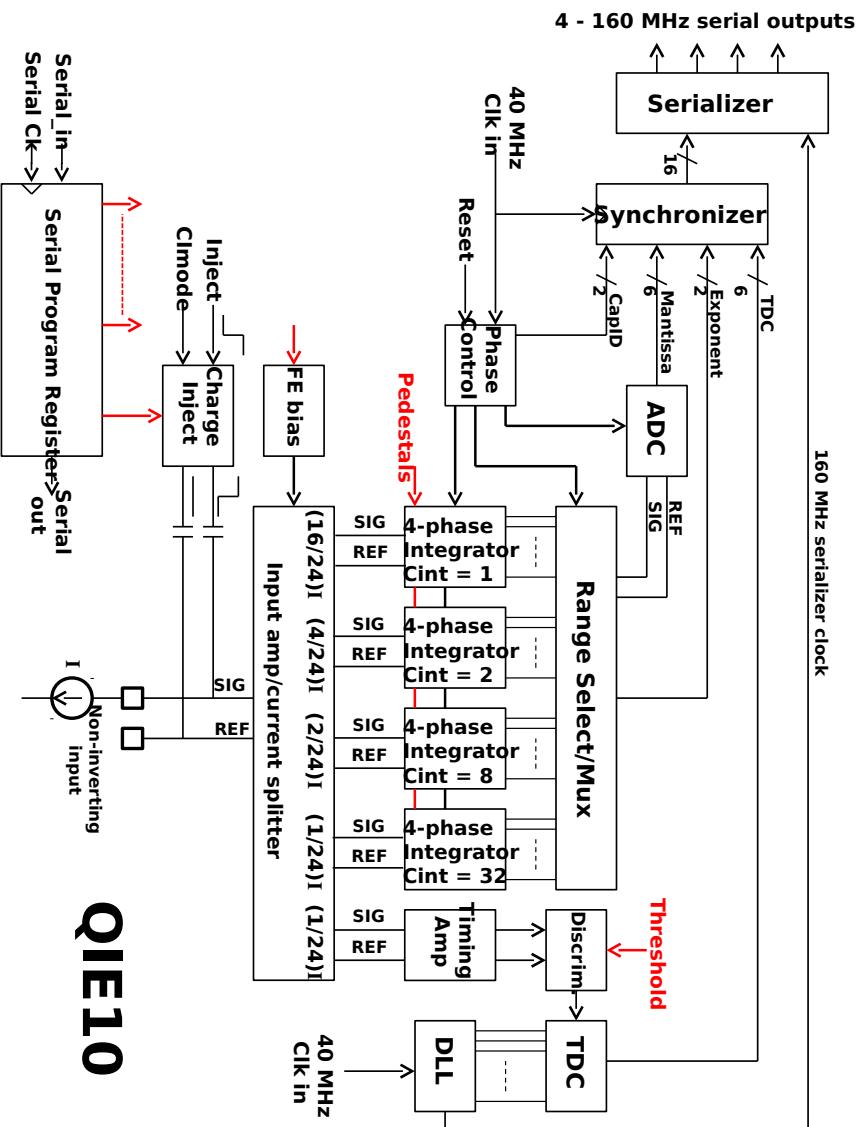


Figure 3.4: Block diagram of the functionalities incorporated in the QIE10.

3.1.3 QIE10 Sensitivity and Dynamic Range

Based on the requirements of the upgraded HCAL subdetectors described above, the nominal minimal charge sensitivity of QIE10 is 3.2 fC/bin, while the maximum charge that can be digitized is approximately 340 pC, yielding a nearly 17-bit dynamic range. The QIE10 spans the full 17-bit dynamic range by advantageous remapping of the required resolution onto a compressed pseudo-logarithmic scale. The result is a 17-bit dynamic range compressed onto 8 bits of data (6-bit FADC mantissa + 2-bit range exponent).

Table 3.1 shows the ideal QIE10 response mapping of input charge to output code, assuming a pedestal of 0 and ignoring some range overlap. In reality, each range will require a gain and offset calibration constant. Figure 3.3 shows the quantization error for the 4 FADC sensitivity regions and 4 ranges.

3.1.4 QIE10 Timing

The QIE10 incorporates timing information for signal into the output data; this feature was not available in the predecessor QIE chips. The QIE produces digital TDC information based on the rising edge of the pulse and a discriminated level output for off-chip processing for pulse width determination. An 8-bit programmable threshold will be used to set the discriminator threshold. The step size of the threshold DAC is determined by an external resistor, allowing the discriminator thresholds to be tuned separately for HB/HE and for HF. An external resistor

Table 3.1: Ideal QIE10 response mapping of input charge to output code

Range (Exp)	Input Charge	ADC Code (Mant.)	Sensitivity (Q/bin)
0	0 fC - 48 fC	0 - 15	3.2 fC/bin
0	48 fC - 170 fC	16 - 35	6.4 fC/bin
0	170 fC - 426 fC	36 - 56	12.8 fC/bin
0	426 fC - 580 fC	56 - 63	25.6 fC/bin
1	580 fC - 964 fC	0 - 15	25.6 fC/bin
1	964 fC - 1937 fC	16 - 35	51.2 fC/bin
1	1937 fC - 3985 fC	36 - 56	102.4 fC/bin
1	3985 fC - 5214 fC	56 - 63	204.8 fC/bin
2	5214 fC - 8286 fC	0 - 15	204.8 fC/bin
2	8286 fC - 16.1 pC	16 - 35	409.6 fC/bin
2	16.1 pC - 32.5 pC	36 - 56	819.2 fC/bin
2	32.5 pC - 42.3 pC	56 - 63	1638 fC/bin
3	42.3 pC - 66.9 fC	0 - 15	1638 fC/bin
3	66.9 pC - 129 pC	16 - 35	3276 fC/bin
3	129 pC - 260 pC	36 - 56	6552 fC/bin
3	260 pC - 339 pC	56 - 63	13.1 pC/bin

of 10k provides a step size of 24 fC (8 LSB) and a range going from 0-6120 fC. This configuration, appropriate for HB/HE, allows for timing measurements of minimum ionizing (MIIP) particles and provides a dynamic range up to approximately 20 GeV, well above the typical energy of pileup particles. A TDC in the QIE will convert the rising edge discriminated signal into 6-bit digital output, providing a TDC with 500 ps bins. The discriminator levels (rising and falling edges) will also be sent off the device to the FPGA for additional pulse width determination.

3.1.5 QIE10 Coupling

The QIE10 will be operated in a DC-coupled configuration for both the SiPMs and the upgrade PMTs. AC coupling is challenging due to the inherent undershoot of the pulse, which is especially problematic at high luminosity. This can decrease the QIE bias voltage (pegging the QIE pedestal at zero) and require a significant recovery time for the device. DC coupling has some challenges with the SiPM which are addressed in the design. The leakage current for the SiPM increases with radiation damage, resulting in a radiation-induced pedestal shift and an increase in pedestal width. While some amount of pedestal shift can be compensated for via the pedestal DAC, the increase in pedestal width requires an increase in the mean pedestal to avoid negative saturation of the QIE, regardless of the coupling choice. Because of the pseudo-logarithmic nature of the QIE, a pedestal increase in the QIE could potentially change the sensitivity scale at which the QIE is operating thereby degrading the resolution. However, studies with irradiated SiPM devices indicate that the resolution effects are minimal with the chosen QIE10 binning.

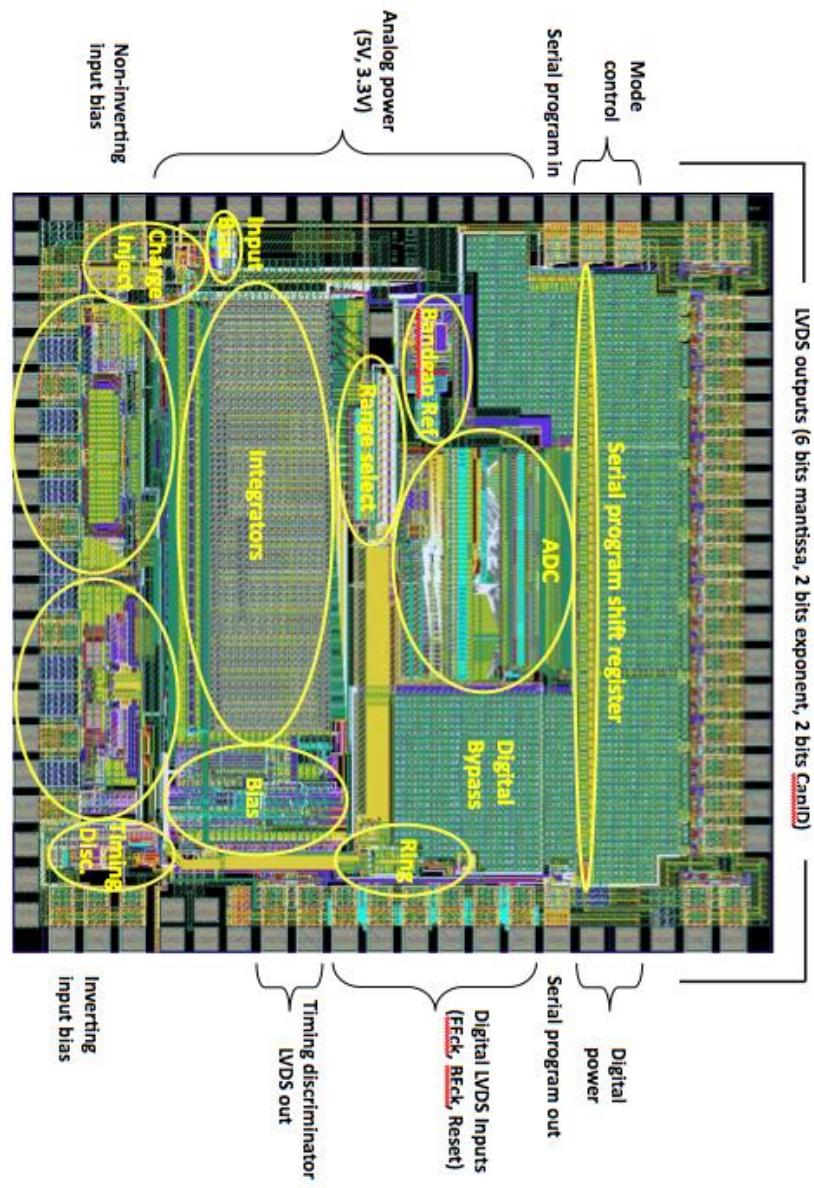


Figure 3.5: Layout of the first full QIE10 prototype chip. The final version of this chip will include a 6-bit TDC and serial data inputs and outputs.

3.1.6 QIE10 Inputs and Outputs

A serial programmable register is incorporated into the QIE10 to set pedestals, integration clock phasing, threshold for timing discriminator, and charge injection circuit selection. The output data are essentially a floating-point number (6-bits FADC, 2-bits range) along with phase information (2-bits capacitor identification) and 6-bits of TDC. The serial data output are sent out via LVDS lines at 160 MHz. The serial outputs carry the 6-bits of mantissa and 2-bits of range information as well as the 2-bits of CapID and 6-bits of timing information. The output of the timing discriminator is also available as an LVDS output to allow external circuitry for pulse counting and pulse-width determination.

The GBTX ASIC discussed below (Section 3.3) will provide the analog integration clock for the QIE10. The GBTX will be capable of delivering individually programmable 1 ns-steps in clock delay per QIE10. A QIE Reset signal will start the CapID rotation at 0. Alignment of QIE Reset will be synchronized to the QIE integration clocks. This resetting and alignment of the QIEs is critical for synchronizing the detector and will be performed during the LHC dump orbit gap based on the Bunch-Count-Zero signal from the fast-control system.

A charge injection calibration circuit has been included in the QIE10 design. This circuit will be used to verify gain stability and for in situ calibration of the ADC. It is also a useful diagnostic tool for debugging problems in the front-end readout chain.

3.1.7 QIE10 Fabrication Process

The QIE10 also differs from its predecessors in that it is required to survive in a high radiation environment (100 Gy ionizing radiation and $2 \times 10^{12} \text{ n/cm}^2$). The QIE8 was fabricated in the AMS 0.8 micron silicon bi-CMOS process. In previous radiation testing, that process showed serious CMOS threshold voltage shifts starting at neutron fluences of $2 \times 10^{12} \text{ n/cm}^2$. The fabrication process that was chosen for QIE10 is the AMS 0.35 micron Silicon-Germanium bi-CMOS (3.3 V and 5 V) process. This smaller transistor feature size makes the transistors faster and less susceptible to threshold shifts but necessitates careful design incorporation of SEU mitigating layout, which is part of the specification and test program for the QIE10 prototypes [39]. Bi-polar transistors are used in the splitters because bi-polar transistor matching is much better than CMOS. Most of the QIE functions operate on 3.3 V, but the 5 V is needed in order to “stack” several processes (input amp, the splitter, the current switch, the integrator, the ADC) that require some minimum voltage to operate.

Due to the increase in channel count in HB, HE, and HF in the upgraded detector, the QIE10 footprint/pin-count will need to be compact and the device will have to be low power. Currently, a 64-pin Thin Quad Flat Pack (TQFP) is considered sufficient for the device. The power dissipation for the final chip design is estimated to be 350 mW.

A prototype version of the chip with most of the required functionality (but without the TDC) has been fabricated. The chip layout is shown in Fig. 3.5. The TDC and serial data output will be incorporated into the submission of the QIE10 design anticipated for November 2012. The series of QIE10 prototyping is shown in Table 3.2.

Table 3.2: QIE10 ASIC prototypes (past and planned)

Prototype version	Notes
proto1	Achievements: migration to AMS 0.35um SiGe BiCMOS process on the analog input stage
proto2	Achievements: input impedance matched to new photosensors; ADC with greater dynamic range (100k:1); irradiation tests
proto3	Submitted in November 2011. ADC and encoder, timing discriminator, but no TDC. Low yield due to electrostatic discharge on inputs. Ringing on timing circuit.
proto3b	Submitted in May 2012. Non-inverting input only. Fixes: Electrostatic Discharge protection on inputs. Repair ringing on timing circuit. Not yet tested
proto4	Submission expected in November 2012. Non-inverting input only. 6-bit TDC. Parallel outputs.
proto5 = CMS pre-production version	Submission expected in February 2013. Non-inverting and inverting inputs. Serial outputs.
ready for production	November 2013. HF case.[39]

3.1.8 Testing Program

The QIE10 is required to survive in a radiation environment that is roughly ten times worse than the environment the QIE8 will see. The QIE10 is expected to survive a total ionizing radiation of 10 kRad and a fluence of 1 MeV-equivalent neutrons of $2 \times 10^{12} \text{ n/cm}^2$ through 3000 fb^{-1} . Typical testing exposures for ionizing dose and displacement damage studies would

be 3-10 times the levels expected in the experiment (Table 1.2). For QIE10, this radiation dose requirement translates into a testing exposure of 30 kRad and $5 \times 10^{12} \text{ n}/\text{cm}^2$ with no degradation in performance. Bit error rate limits similar to QIE8, better than 10^{-12} , are required. The bit-error-rate limit set for the QIE8 was 10^{-14} , and the QIE10 should be required to perform at a similar level.

Besides the testing of the QIE10 for its behavior under radiation, the full set of characteristics defined in the specification will be tested in bench tests and/or testbeam evaluations. In the case of QIE10 testing for the HF upgrade, testbeam evaluations may be performed at FNAL as the H2 area will not have beam available in 2013. However, chip performance can be well-qualified with bench testing and testbeam evaluations to understand system issues. Production chips will be tested for a reduced set of criteria to identify and reject any bad-quality chips.

3.1.8.1 QIE10 Radiation testing

The plan for radiation testing the QIE10 is similar to the program previously conducted for the QIE8. The QIE8 radiation studies were done in stages, with initial tests being done on simple test devices to verify the viability of the process. Initial studies included measuring SEU cross-sections using various transistor layouts in simple shift registers, studying the degradation in V_{be} and beta for bi-polars, measuring increases in leakage currents and threshold voltage shifts for CMOS test transistors, and testing for destructive single event effects such as latch-up. Later studies focusing on system level single event effects and performance degradation were conducted with final versions of the chips/board.

For the QIE10, initial tests were conducted to measure the effect of displacement damage and total ionizing dose on bipolar and CMOS transistors for the AMS Silicon Germanium 0.35 μm BiCMOS process [40]. Various test devices (NPN bipolar, NMOS, PMOS, NMOSP, PMOSN with standard and enclosed layouts) were exposed to 200 MeV protons (only 5 kRad due to machine problems, corresponding to $8 \times 10^{10} \text{ p}/\text{cm}^2$) at Massachusetts General Hospital (MGH), $5 \times 10^{12} \text{ n}/\text{cm}^2$ 1 MeV equivalent neutrons from a reactor at Lowell, Massachusetts, and a Co-60 1 MeV gamma source (45 kRad) at Brookhaven National Laboratory. With protons, the NPN transistors beta did not change, but there was a small (few mV) shift in V_{be} . Under gamma irradiation, the beta for the NPN did not change at high current density (nominal operating point) but deteriorated at low current densities, which is consistent with an introduced constant leakage current. NPNs showed no change under neutron exposure. The CMOS transistors had small (10-30%) changes in sub-threshold leakage with standard or enclosed layouts from 5kRad proton exposure. For gammas, the NMOS transistors showed a small sub-threshold current increase with little change for PMOS transistors. Under neutrons, some NMOS sub-threshold current increase was observed. Enclosed layouts do not provide significant radiation immunity.

A test of SEU mitigating layouts for digital sections of the chip was conducted on three 105-bit shift registers with differing layouts that were exposed to 200 MeV protons at MGH. Three different layouts were used on a single chip that could be exposed to beam: “vanilla” or standard layout, SEUSS (Redundant Single Event Upset Suppression System (Fermilab) [41]), and DICE (Dual Interlocked Storage Cell - (CERN) [42]) layouts. Problems with noise-induced SEU made tracking the overall fluence of the beam difficult, so absolute cross sections could not be determined. However, because the layouts were on the same chip, relative SEU tolerance could be measured. The DICE layout was the most robust, with no upsets seen. The rate of upsets in the SEUSS register was approximately ten times higher than the rate limit determined for DICE and about a factor of four lower rate than the standard/vanilla layout.

The results of these tests have guided the ASIC designer to use standard layout (no enclosed layouts) and DICE mitigation for the critical circuits of the QIE10. Currently in the design, DICE SEU mitigation layout is used in the ring counter, the shadow (readback) control register, and the output pipeline that shifts the data out of the chip. No mitigation is used in the ADC/TDC section of the chip. For reference, the only SEU mitigation layout included in the QIE8 design was in the ring counter.

More thorough SEU testing is needed to measure the QIE10 SEU cross section. Prototype 3 does not include the shadow or serial output registers, so the only bits that can be monitored are 2-bits for capacitor identification, the 6-bits of mantissa (if the pedestal is set much higher than pedestal noise to force a delta function, and the 2 range bits). This intermediate test could provide additional feedback to the chip designer, but would not be in time to provide design changes (additional SEU mitigation) for the November 2012 Prototype 5 submission. A more rigorous SEU test of the Prototype 5 chip is planned for spring 2013.

3.1.8.2 QIE10 Chip testing

The planned QIE10 chip tests are similar to the ones conducted on QIE8. Benchtop measurements include the following:

- Charge injection with DC current, logarithmic sweeps with plots
- Charge injection with the QIE10 internal charge injection DAC
- Charge Injection with an externally-generated charge pulse
- Charge sharing measurement with an external charge injection swept through event clock
- Study of range transition regions, bin widths (differential non-linearity)
- Pedestal stability and noise
- Capacitor rotation and resets

After thoroughly studying a small number of chips on the bench, the QIE10s will be packaged. The preferred package (preferred because it makes assembly and board rework easier) is a 64-pin QFP or TQFP package. Packaged chips will be sent through a robotic chip tester that will be used to select chips for mounting on PC boards. Although checks performed by the robotic chip tester are somewhat less rigorous than precision bench top measurements, the large number of chips necessitates this approach. Selection parameters will include the input impedance (large/small input pulses), pedestal mean value and RMS, capacitor rotation, gains as measured by the internal charge injection circuit and as determined by an external charge injector (ADC response and range bits), and range bit toggling, capacitor identification bit rotation. Chip yields for the QIE8 have typically been in the 60-80% range, which is fully acceptable and the same rate is expected for the QIE10.

3.2 Front-End FPGAs

Radiation-tolerant Field-Programmable Gate Arrays are effective replacements for the ASICs which were used in the original HCAL FE electronics for control and data flow functions. In the upgrade FE, FPGAs are used for data alignment and formatting, managing the configuration of QIE chips, performing a falling-edge TDC calculation for the HF, and for system integration tasks. An FPGA is also used in the ngCCM to support the redundancy system.

The familiar SRAM-based FPGAs produced by Xilinx and Altera are not appropriate choices

for the HCAL front-end electronics due to their relatively high sensitivity to radiation. Instead, the ProASIC3L series FPGA from Microsemi (formerly Actel) is planned for use in the HCAL upgrade electronics. The ProASIC3 series includes ProASIC3, ProASIC3E, ProASIC3 nano, and ProASIC3L [43]. These FPGAs have been extensively studied by multiple groups to characterize their behavior under radiation and the results of these tests validate their use in the HCAL front-end electronics environment. Of particular value are the extensive studies documented in [44].

The main features of these FPGAs are:

- flash-based FPGA
- non-volatile (i.e. the FPGA maintains its configuration even when powered-off, thus it does not need an external PROM, a difference from the more-familiar SRAM-based FPGAs)
- power consumption is considerably lower than popular SRAM-based FPGAs
- reprogrammable (minimum of 1000 times).
- flash-based user ROM (1 kbit)
- Dual-Port SRAM (up to 504 kbits)

These FPGAs are have lower performance than SRAM-based FPGAs in terms of clock speed (350 MHz compared with 500+ MHz). However, this performance difference is not a concern for the intended use in the HCAL FEE.

The leading concern in a radiation environment is Single Event Latchups (SEL), because they can have a destructive effect. According to studies from the manufacturer, SEL have been observed at linear energy transfer (LET) levels of $86.9 \text{ MeV cm}^2/\text{mg}$ and higher at room temperature and at an operating temperature of 125°C [45]; another study [44] has observed SEL at LET levels of $55 \text{ MeV cm}^2/\text{mg}$ and higher. The typical LET for nuclear interaction in silicon, by far the most abundant material around the sensitive nodes of the chip, is around $16 \text{ MeV cm}^2/\text{mg}$ [46] which is far below the thresholds observed to cause SEL. However, there are other materials in the chip that can lead to recoils with larger LET. The probability for such recoils to be produced is proportional to the abundance of the heavier element in the chip (copper, tungsten, etc) and to the cross-section of the specific nuclear interaction leading to their production. Since these heavier elements are much rarer than Silicon, their contribution to the overall single-event-upset (SEU) rate is normally negligible. For destructive events such as SEL even a small cross-section is worrisome, and it is interesting to know the maximum LET of fragments produced by nuclear interaction of hadrons with these heavier materials. The worst configuration is the fission of tungsten [47], which could produce fragments with a LET of up to $45 \text{ MeV cm}^2/\text{mg}$. Thus, the ProASIC FPGAs have been characterized as safe from SEL for LET below $55 \text{ MeV cm}^2/\text{mg}$ and are thus considered safe for our application where the maximum plausible LET would be $45 \text{ MeV cm}^2/\text{mg}$.

Having found that ProASIC3 FPGAs are immune from SEL in the LHC environment, the second issue to study is the tolerance to the total dose of ionizing radiation. Over the expected total ionizing dose (TID) of 10 krads, ProASIC3 FPGAs remain fully functional – they do not exhibit an increase in power consumption or a deterioration in maximum clock frequency [44, 48]. Additionally, the flash-based FPGA configuration and the flash-based user ROM are not upset by radiation [44, 49] in the LET range of interest (up to $45 \text{ MeV cm}^2/\text{mg}$).

Irradiation tests with protons and heavy ions have shown the effects listed [44, 48, 49] and discussed below:

- **Single-Event-Effect (SEE) in the programming circuitry:** CMS will avoid this problem, likely due to a Single Event Gate Rupture in the charge-pump circuitry used to reprogram the flash cells, by not reprogramming the FPGAs when exposed to heavily ionizing radiation. Reprogramming the FPGA will only be allowed when there is no beam in the accelerator. We are investigating a protocol to comply with this limitation. The basic concept will be that reprogramming the FPGA shall require an explicit human intervention to be performed in the experimental cavern. As persons can access the experimental cavern only when there is no beam, this will automatically ensure that the FPGA is reprogrammed under the same conditions.
- **SEE in the Phase Locked Loop (PLL):** This effect has been observed for LET higher than $10 \text{ MeV cm}^2/\text{mg}$ [44] and it is therefore a possible effect in CMS. A power-cycle would be needed to recover normal operations. According to [49], it is sufficient to power-cycle only the PLL, while this is not clear in [44]. Any PLL in commercial-grade FPGAs or ASICs is expected to have a similar behavior.

The following additional effects are present in any commercial grade FPGA or ASIC and do not represent particular disadvantages for this series:

- **SEU and single-event transients (SET) in the custom logic:** These effects can be mitigated using triple-module-redundancy and safe finite-state-machine style in the FPGA logic. These techniques were used with the Actel A54SX16 anti-fuse FPGA in the current HCAL front-end and no SEU effects have been observed. Commercial design tools can now assist the designer in these tasks.
- **SET in the IOs:** These effects can be mitigated by triplication of the critical FPGA inputs and outputs.
- **SEU in the Dual-Port SRAM:** This effect can be mitigated through Error Detection and Correction (EDAC) codes or by avoiding the use of the internal SRAM for functions which will be used during collisions.

We conclude that the ProASIC3 FPGAs are good candidates for the HCAL FEE. Critical FPGA functions should not use the ProASIC3 PLL, as it has been shown that it is sensitive to SEE. Note that if a SEE is produced in a ProASIC3 PLL, the part of the FPGA which does not use a PLL clock will not be affected.

Given the extensive device-level testing which has been completed on the ProASIC3 series, no additional device-level testing is planned by the HCAL group. Instead, the group will focus on system tests which validate both the device itself and the firmware design to be used. These validation plans are discussed more completely in Section 4.4 and Section 5.8 for the HF and HB/HE front-end designs specifically and will include the use of the CERN IRRAD facility and in-situ testing in the CMS cavern where possible.

3.3 Gigabit Transceiver (GBT)

The upgrade FEE plans include the use of the GBT and Versatile Link technologies, under development at CERN [50, 51]. These technologies are tolerant to radiation levels greater than the HCAL exposure levels. The GBT is an optical data link technology providing bidirectional 4.8 Gb/s serial communication with the capability to receive “parallel” data with an arbitrary phase, at the frequency of the LHC or at multiples of 2, 4, 8. Additionally the GBT can recover the frame clock, can reduce the jitter from an input clock, and distribute phase-controlled clock signals. The data rate (bandwidth) available to the user is lower than the 4.8 Gb/s line rate,

and depends on how the GBT is configured as discussed below. The primary component of the GBT technology is the GBTX (Gigabit Data and Timing Transceiver) ASIC which will be used in the FEE along with the laser driver (GBLD) and transimpedance optical receiver (GBTIA) ASICs. The Versatile Link project provides receiver diodes and VCSELs appropriate for 4.8 Gb/s operation in an LHC radiation environment which are packaged either as transceiver (VTRX) or a dual transmitter (VTTX) in an SFP+ form-factor.

The GBTIA and GBLD chips have been fully validated including radiation testing during 2011. Concerning the GBTX, pre-production prototypes were submitted in August 2012, and the design has been validated with extensive simulations. Fully-packaged chips are expected at CERN for testing in February 2013. HCAL has contributed to the development of the GBTX ASIC supplying the design of the 8b10b encoding portion. The Versatile Link project includes the identification and packaging of laser drivers, receiver diodes, and VCSELs appropriate for The GBTX accepts parallel input data in common LVDS logic levels or with the lower-power but less-common SLVS logic levels. LVDS is compatible with commercial components (including FPGAs) and with the present development of the QIE10. The GBTX parallel outputs are SLVS logic levels which are not directly compatible with commercial electronics. In order to match them to the other components of the HCAL FEE, we will use a simple level-translation ASIC developed by the CERN microelectronics group. The GBT technology will be used in the ngCCM and in the readout module, in different configurations.

The ngCCM will use the GBT link in bidirectional mode, with Forward Error Correction. This mode allows to transmit 82 bits at every cycle of the LHC clock. These bits are sufficient for the control functions, and the use of Forward Error Correction will minimize the error probability. This is important because a single bit error in the control path can affect many readout channels for many clock cycles. In this mode, the GBT system can be configured over the GBT link itself. The counting room electronics will use the LHC clock to transmit commands to the ngCCM; the ngCCM GBTX will recover the LHC clock and provide it as a system clock for the entire RBX or HF front-end crate.

The upgrade Readout Modules will use a number of GBT links in a different configuration, i.e. as transmitters only (see Fig. 3.6), with the standard Ethernet-style 8b10b encoding as the baseline option. The 8b10b encoding is used in the existing HCAL data links and can be decoded with pre-built logic resources in the back-end electronics. In this mode, the GBT link can carry 88 bits of user data at every cycle of the LHC clock. The readout modules will transmit ADC and TDC data over these 88 bits. The GBTX offers a third encoding mode (“wide frame mode”) capable of transmitting 112 bits at every cycle of the LHC clock. Although not strictly necessary, the readout modules may have an option to use the wide frame mode for additional monitoring and TDC. Similarly the readout module will be organized in such a way that if there is a need to change the GBTX configuration to FEC mode, only some TDC data will be lost. This functionality is provided through reprogramming of the FE-FPGAs which are responsible for the data formatting.

In the baseline plan, the readout GBTX ASICs will be clocked from the ngCCM GBTX, via the backplane (an equivalent scheme is in use in the existing HCAL FEE). The GBTX provides eight output clock signals, in sync with their master clock, with a phase control in steps of 50 ps spanning the whole LHC clock period. These clock signals will be distributed to the QIE10 ASICs. The design for the front-end cards requires one GBTX ASIC for every six QIE10 ASICs, so the number of GBTX output clocks is sufficient.

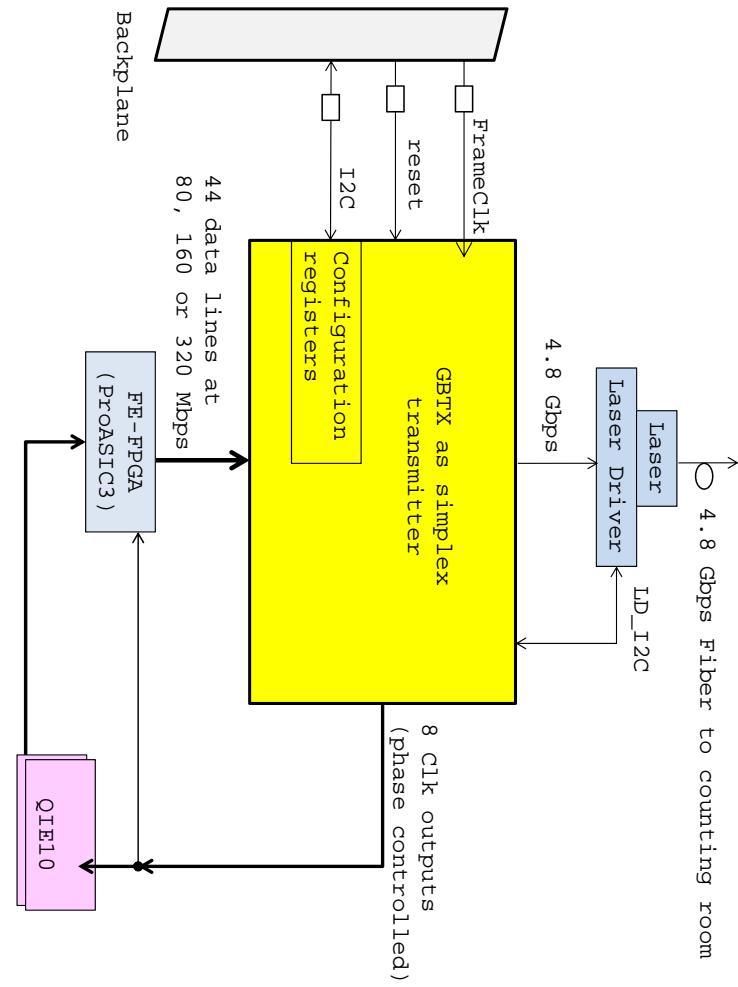


Figure 3.6: Block-diagram showing the use of the GBTX in the readout module.

3.3.1 GBTX testing

The test plan for the GBTX ASIC includes these tests:

1. validation of the ASIC design
2. radiation-tolerance tests
3. production tests

All tests will be performed on packaged ASICs, which are expected to be available in CERN in February 2013. Wafer-level or naked die tests are not relevant as the packaged chip will include a crystal oscillator and some passive parts, which are required for the proper behavior of the ASIC. Additionally, the complex structure of the ASIC and of its inputs and outputs would make this task too difficult.

The validation of the ASIC design requires testing all functions, testing the tolerance of the ASIC to small variations of its input voltages and testing the immunity from noise (amplitude noise and phase noise or jitter, on the power pins and on the signal pins). The GBTX tests will be performed in the facilities of the CERN ESE group, which owns the ASIC tester Sapphire(TM) from the Credence company. The ASIC tester is normally connected to all IOs of the Device Under Test, which allows it to accurately measure the device outputs. Unfortunately the ASIC

tester available at CERN has a maximum data rate of 800 Mbps, so it cannot test directly the 4.8 Gbps GBTX signals. For this reason, a more complex test setup has been developed, as shown in Fig. 3.7.

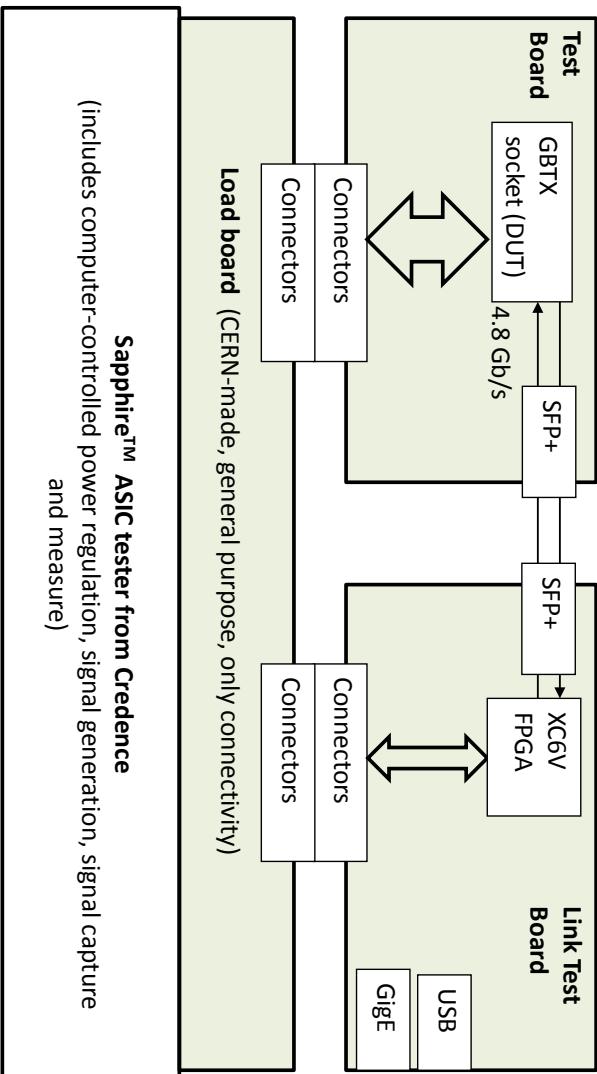


Figure 3.7: Setup for the validation and production tests of the GBTX ASIC

The ASIC tester will control all inputs and read all outputs except the 4.8 Gbps signals, which will be connected to a commercial FPGA. The test procedure is controlled by Verilog testbench files which are loaded into the ASIC tester. These testbench files define the electrical signals as on the stimulus of the device, and capture the device outputs and compare them to the expected signals from the testbench. The validation test is expected to take about four months after the packaged ASICs will be available at CERN. GBTX samples will be available to CMS HCAL at the end of the validation tests, provided that no major problems are found.

The second test is the radiation tolerance of the GBTX. The tolerance to total ionization dose will be tested with an X-ray machine available in the CERN-ESE group. Tests of SEE require a heavy ion facility, such as the Cyclotron at Louvain la Neuve (Belgium) which has been regularly used by the CERN ESE group for this purpose. The irradiation test setup is a variation of the setup shown in Fig. 3.7. The ASIC tester cannot be taken to the irradiation facility, so the setup will include the Test Board (in the radiation area), connected via optical fibers to the Link Test Board (outside the irradiation area).

The production test of the GBTX will be carried out to identify manufacturing defects on individual devices. During these tests, the design itself is not validated but instead a subset of the validation tests are used to identify defective chips, focusing on minimizing testing time while identifying defective chips with high probability.

CMS HCAL has contributed to the GBTX test with the development of the Test Board and of the Link Test Board. HCAL personnel will be part of the team in charge of the tests described

above.

3.4 DC/DC Converters

The HCAL upgrades involve an increase in channel count without a proportionally large increase in power use. For example, the HB upgrade will triple the channel count and add TDC data which together increase the data volume by a factor five, but the power is constrained to increase by less than a factor three. This is particularly challenging as several of the components in the upgrade use lower voltages (e.g. 1.5 V core voltage of the GBTX) which are inefficient to supply over long cables through linear regulators. The existing FEE use the linear regulator L4913 with a dropout voltage of almost 1 V, available with fixed output voltages of 2.5 V, 3.3 V, and 5.0 V. Much of the power is regulated as 5 V from a 6.5 V input, which gives an efficiency of $5\text{ V}/6.5\text{ V} = 77\%$. If we build the upgrade FEE with linear regulators, the efficiency of the 2.5 V regulation would be at most $2.5\text{ V}/3.5\text{ V} = 71\%$. The efficiency to regulate 1.5 V for the GBTX would be even lower.

In this situation, the use of DC-DC converters in the upgraded front-end electronics has the following advantages:

- increased conversion efficiency, reduced power dissipation in the electronics
- reduced current in the LV-cable, reduced power dissipated in the LV-cables
- reduced power required from the external power supplies, which reduces the cost of new power supplies (in the case of HB/HE) or allows the reuse of existing supplies (in the case of HF).

Our need for DC-DC converters which properly function in the environment described in section 1.6 is a good match to the developments of CERN DC-DC converters [52, 53]. The CERN DC-DC converter is composed of a radiation-hard ASIC, which contains the switches and related control logic, and a mezzanine which supports advanced sensing, filtering and shielding structures.

We have tested [54] a few prototypes of such DC-DC converters with our existing front-end electronics. In the initial configuration, we placed the DC-DC converters over the QIE card in a location close to the position of the original linear regulators. This location is far from the QIE chips, in order to minimize noise coupling. We ran multiple tests, using the standard HCAL test stand DAQ framework, with each test corresponding to a different capacitance placed at the input of the QIE8. This input capacitance emulates the effect of the capacitance of a photosensor connected to the QIE8 inputs. The range of capacitance used in these tests cover the types of photosensors of the existing and upgraded HCAL FE. We have found satisfactory behavior, in particular the system noise (DCDC curve in Fig. 3.8) does not increase significantly compared to the noise found with linear regulators.

In a second test, we moved the DC-DC converter to a location within 25 mm of the QIE chips in order to study the worst-case condition. We have found a satisfactory behavior, as the system noise in this new configuration (DCDC 25 mm) does not increase significantly, also shown in Fig. 3.8.

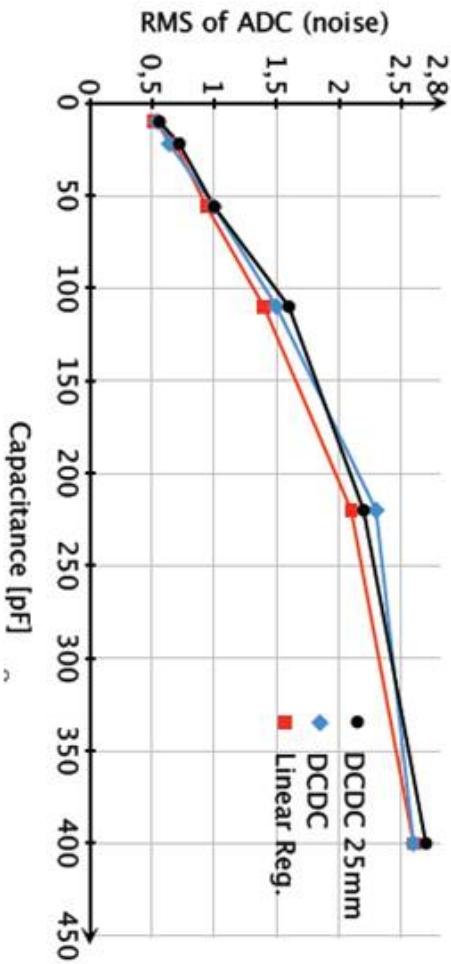


Figure 3.8: Results of a test of a DC/DC-converter prototype with a QIE8 card and comparing to results from the original linear regulators. The DC/DC converter prototype was placed in the position of the original linear regulators as well as near the QIE8 chip (at a distance of 25 mm, indicated by "DCDC 25 mm"). The capacitance on the horizontal axis emulates the effect of the photosensor at the QIE8 input.

Chapter 4

Forward Calorimeter Front-End Upgrades

The key elements of the HF Phase 1 upgrade are the installation of multi-anode PMTs and the provision of new electronics capable of handling the additional channels and providing TDC measurements along with the integrating ADC measurements. As discussed in Section 2.5.1, dual-anode readout is expected to be sufficient for background rejection, compared to a four-anode readout which would be significantly more expensive. However, the design maintains the possibility to eventually switch to four-anode readout should that prove necessary.

The HF upgrade will begin with phototube and cable replacement during LS1, as well as the installation of the upgraded back-end electronics. These steps will allow the installation of the HF front-end electronics during a typical three month year-end technical stop, as the necessary phototube boxes and electronics racks can be accessed without opening the core of CMS.

The HF absorber and quartz fibers are exposed to a high rate of radiation and the quartz fibers experience a loss of transparency as a result. These effects and possible responses for the forward CMS detector region beyond 500 fb^{-1} are under study by the CMS Phase 2 Forward Calorimeter working group and are outside the scope of this report.

This chapter will discuss the specific aspects of the HF Phase 1 upgrade, using the common components described in Chapter 3. The back-end electronics upgrades are described in Chapter 6.

4.1 Phototubes and Cabling

The first step of the HF upgrade program involves the replacement of the current PMTs (Hamamatsu R7525) [55] with PMTs that have thinner square front window, metal jacket and multi-anode photo-cathode (Hamamatsu R7600U-200-M4) [56]. Since the calorimeter signal is carried to the PMTs through a light guide system, and each anode signal is result of photo-electrons produced on the corresponding photo-cathode surface segment, the analog signal from these PMTs can be read out independently through appropriate PMT baseboard design.

The baseboard features a voltage divider designed following the manufacturer recommendation with a total divider resistance of $2.75 \text{ M}\Omega$. The maximum PMT operating voltage is 900 V, with an expected HF nominal operating voltage of 600 V providing a gain of 1.5×10^5 . The baseboard houses 10 nF bypass capacitors between all dynodes and the voltage divider ground connects to the phototube box safety ground. For better performance at high signal rate, the last two dynodes have boost power supply inputs for providing additional current at the nominal voltages for these dynodes (8% and 16% of cathode HV).

Following the installation of the new multi-anode PMT's during LS1, it will be necessary to read out these PMT's with the existing HF electronics. Due to the limited channel count of the

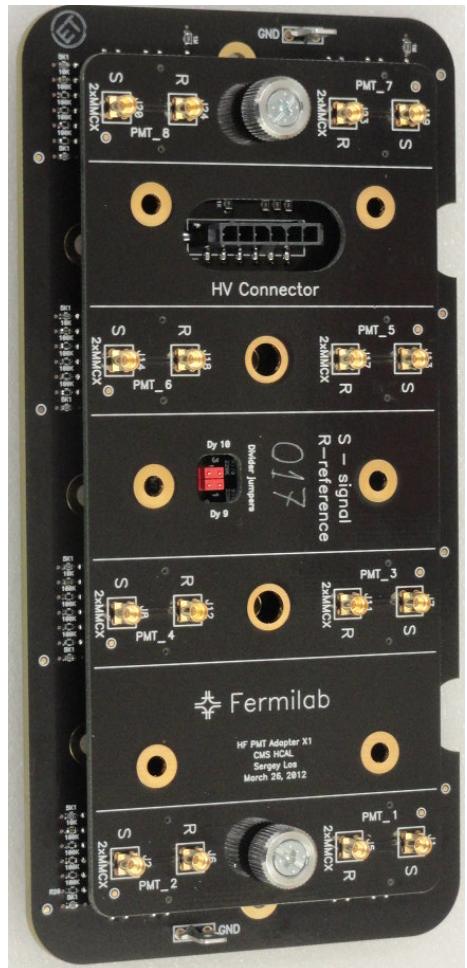


Figure 4.1: Adapter board for single-anode readout of HF PMT system shown mated to the base board. For dual channel operation, this adapter board can be removed and replaced by another with sixteen pairs of MMCX connectors.

existing electronics, the anodes of the four anode PMT's will be ganged into a single channel. Later when the new electronics are available, the PMT boxes will be reconfigured to allow multi-anode readout. In order to facilitate the transition to multi-anode readout, the ganging of anodes and connections to cables within a PMT box is handled by a separate adapter circuit board, pictured in Fig. 4.1. The adapter board can be easily dismounted from the base board along with the internal cable assembly.

The adapter board uses through-hole MMCX signal connectors and attaches to the base board via screw/standoff retainers. The shortest possible connections for critical signals are used in the overall design of the readout boards in order to lower series inductance. Conductors belonging to different grounds do not overlap, which decreases the AC coupling between grounds. Finally, to prevent surface discharges, the ground planes are located on the internal layers of the adapter board.

The signal cables that connect the readout boxes to the front-end electronics will need to be replaced in order to support multi-anode readout. Because of space constraints at both the electronics and the PMT boxes, a cabling solution with high connection density is required. This cabling requirement precludes simply augmenting the existing cables. Cable adapters at the FEE crates will be used to transition from the new cables to the existing electronics. When the new electronics are available, the adapters will be removed and cables will be connected directly. This will greatly reduce the work necessary to transition to the new electronics.

In addition to having sufficient connection density the cabling solution must be robust enough to survive in the harsh radiation environment in UXC and must not degrade the detector performance. After considering several possible designs and providers, a cabling solution has been identified which satisfies our requirements. Prototypes of the entire cabling system from PMT to QIE were evaluated both in the lab and at testbeam [57]. Figure 4.2 compares the pulse performance of the upgrade cabling solution to the original HF cabling solution, showing that the upgrade cabling meets the signal integrity requirements. The components of this cabling system are shown in Fig. 4.3 and include components within the PMT box, long (5 meter) cables which connect the PMT boxes to the FEE, and the temporary adapters which will be used before the upgraded FEE is available.

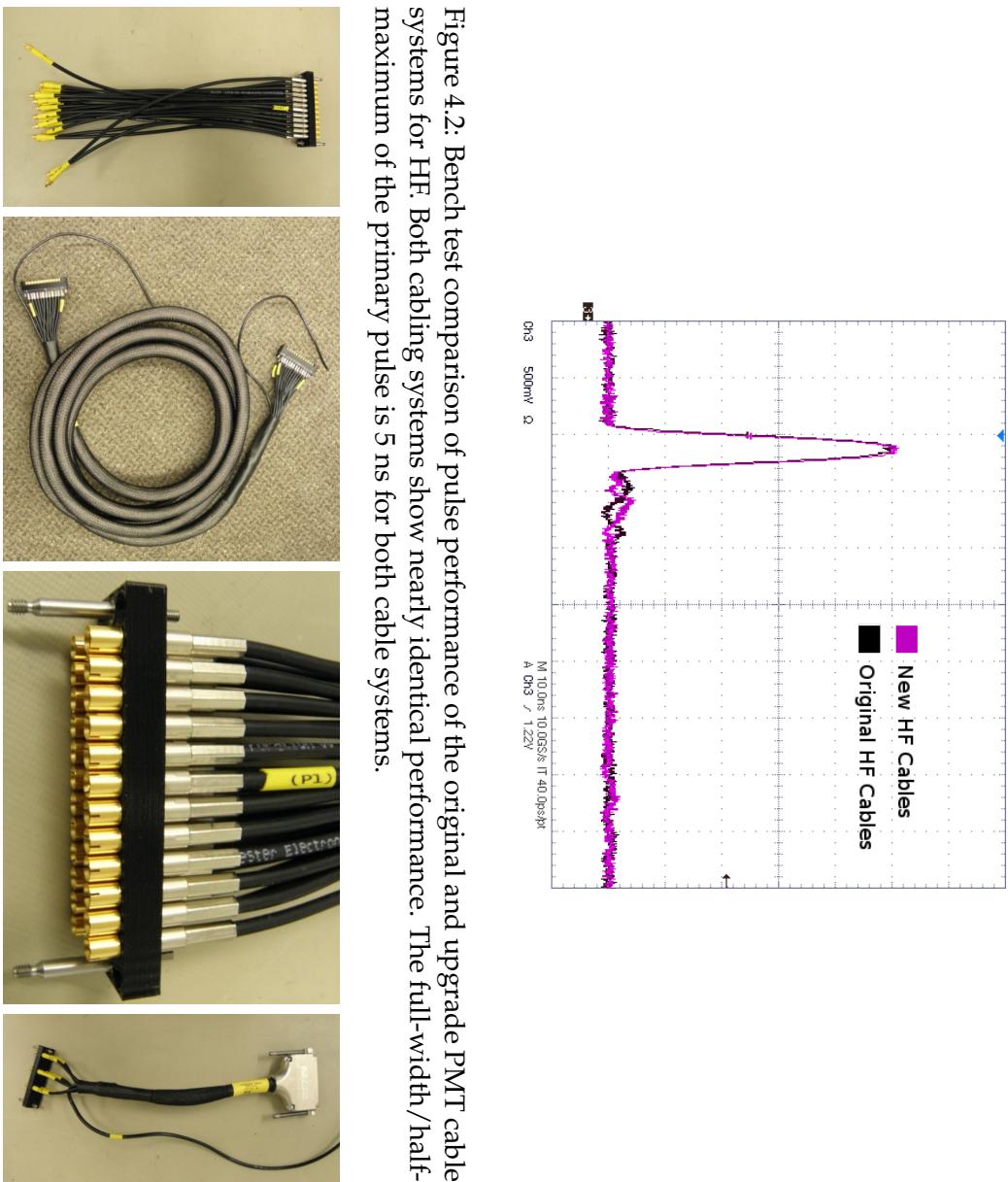


Figure 4.3: Components of the upgraded HF PMT cable system showing, from left, the pigtail cable which connects the adapter boards to the outside of the PMT box, the long (5 meter) cable which connects the PMT box to the FEE, a detail of the 24-coax connector, and the adapter cable which will be used in the period after the installation of the PMTs and before the upgraded FEE is available.

In addition to the electrical performance, the mechanical properties, robustness, and dimensions of the cabling were evaluated. Given that the cable volume will be substantially increased, a detailed evaluation was performed to confirm that the proposed solution was feasible given the space constraints within the HF shielding and support structures. We found that the cabling solution with its excellent properties of pliability, minimal bend radius, and cable density, was sufficient to allow the quadrupling the number of signals which would be necessary for quadrupole readout as shown in Fig. 4.4. Also, as the cables are sufficiently easy to handle, a PMT box can be replaced during a short technical stop if necessary.

Some of the HF mechanical structures will need to be modified to accomodate the new cables. On the upper level of the HF support structure, it is foreseen to augment the cable storage capacity next to the HF racks by adding additional trays. Sufficient space is available and the area is easily accessible. On the lower levels the current front end cable storage area is insufficient and will require additional cable support under the lower level floor. This area

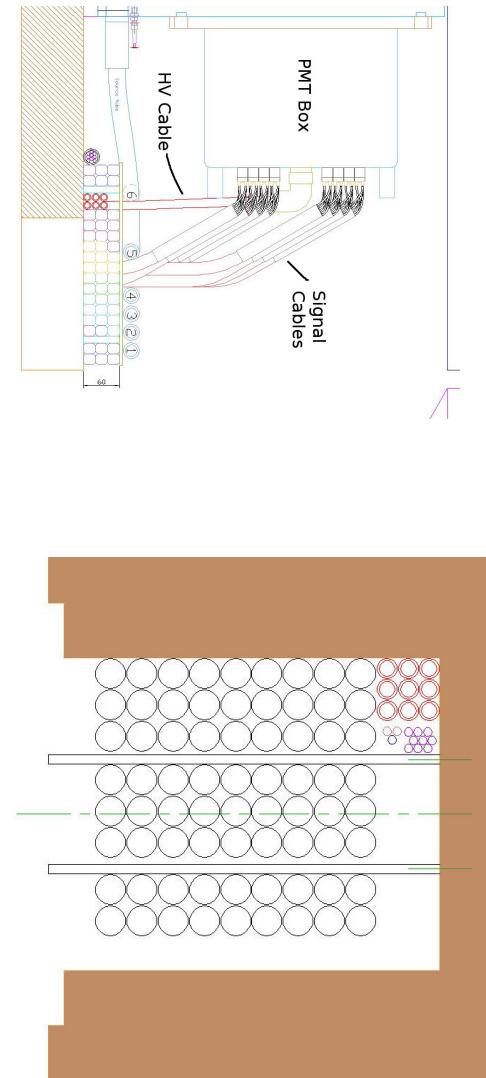


Figure 4.4: Mechanical drawings showing the cable arrangements after the upgrade at the critical choke point for the cables connecting the PMT boxes to the FEE (left) and the cross-section of the cables at the cable port in the HF shielding (right). These drawings are made for a possible future four-anode readout of HF and demonstrate that the cabling solution meets our full mechanical requirements.

is difficult to access while the HF detectors are in the maintenance garages at the ends of the collision hall. The planned access to this cable storage area will require temporary removal of floor panels. The relationship between the PMT boxes, the electronics racks, and HF support structures can be seen in Fig. 4.5.

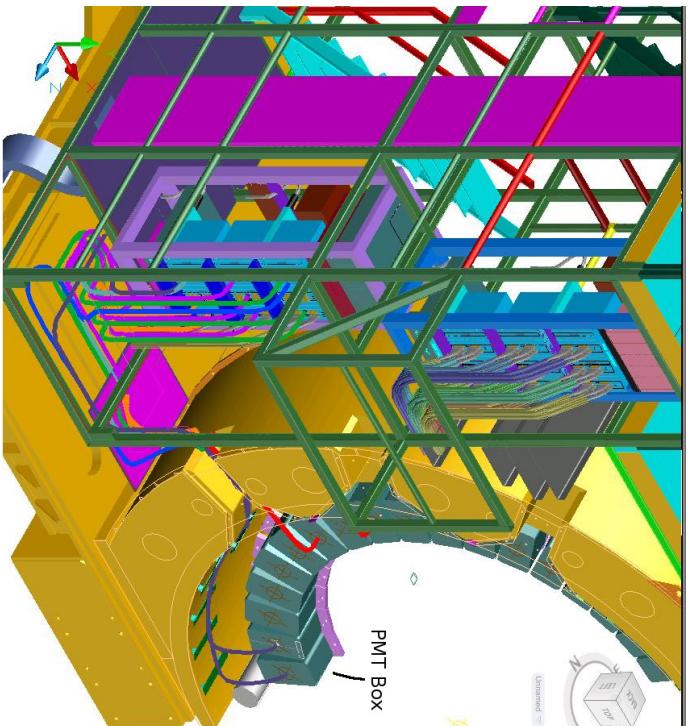


Figure 4.5: CAD Drawing showing the relative locations of the electronics racks (e.g. the purple cage left of center), the PMT boxes (green semicircle at right), and the mechanical portion of the HF table (yellow and green volumes). For illustration, only a portion of the full set of cables are shown.

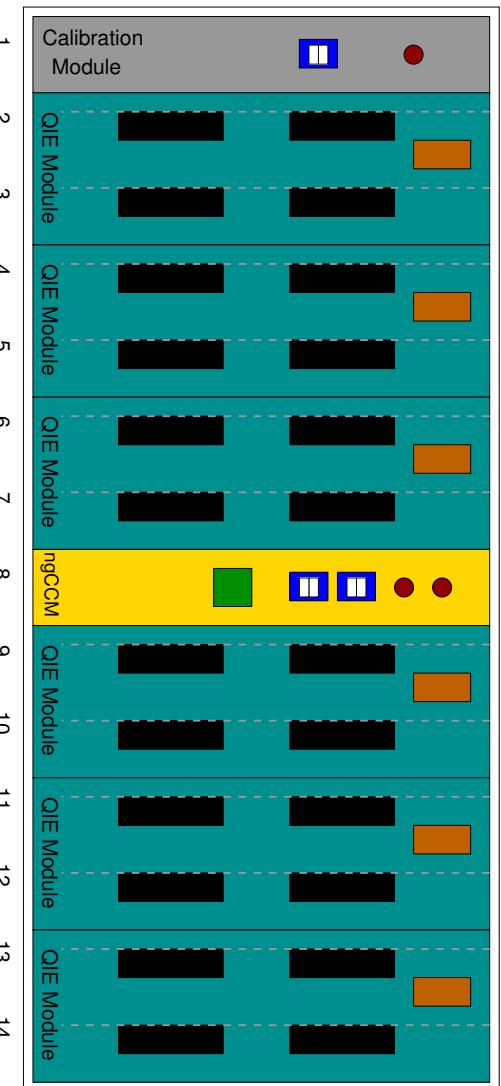


Figure 4.6: Drawing of an HF front-end crate showing the six QIE10 modules (12 cards), the ngCCM, and the calibration module. The location of the two cards within each module is indicated by light dashed lines.

4.2 Front-end Electronics

The front-end electronics for the HF upgrade will be organized in Eurocard-style crates, similar to the arrangement of the previous design. Due to the size of the front-end cable connector, each card will occupy 1.2 inches of horizontal space, as opposed to the 0.8 inches typical for VME and used in the original HF electronics. The crate layout is shown schematically in Fig. 4.6. Twelve slots are for six QIE10 modules, each holding two QIE10 cards, which digitize and process the signals from the PMTs. In the center of the crate is the clock and control module, the ngCCM, and on the far left is the calibration module responsible for LED-based and laser-based calibration and monitoring. Twelve crates of electronics, six at each end of CMS, will be required to readout the full HF subdetector.

4.2.1 QIE Cards

Each QIE card will be responsible for 24 channels of analog data. To process the full set of signals from HF in the case of dual-anode readout, 144 cards will be required. The analog signals will be integrated and digitized by 24 QIE10 chips. These QIE10 chips will then be connected to one of two FPGAs which provide several functions: data alignment across the channels on the same fiber link, calculation of the CapId matching condition, and management of the configuration bitstreams. Each FPGA will be connected to three GBT link chips for the final data transmission, for a total of six GBT link chips on each card and three VersaLink dual optical transmitters (VTTx). A schematic view of the data flow within the HF FE Card is shown in Fig. 4.7.

Mechanically, the HF FE cards will be combined in pairs to form modules. The two cards of a module will share a single 12-fiber MTP output which will be fed by through an MTP-LC fiber break-out. This allows the optical connections to be compact and reduces the risk of damage during handling as only one connector need be touched to remove the module. The arrangement of cards into two card modules with standoffs between the cards also increases the mechanical robustness of the system. Mechanical drawings of the individual card and module concepts are shown in Fig 4.8. Half the QIE10 chips will be mounted on the back-side

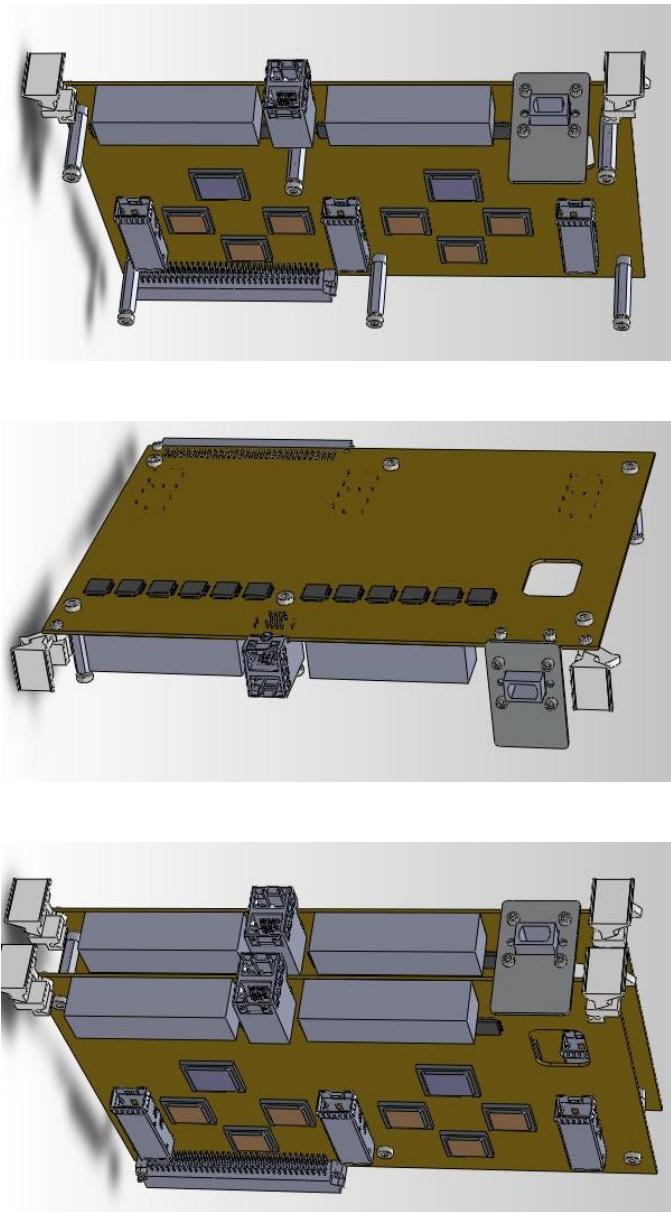
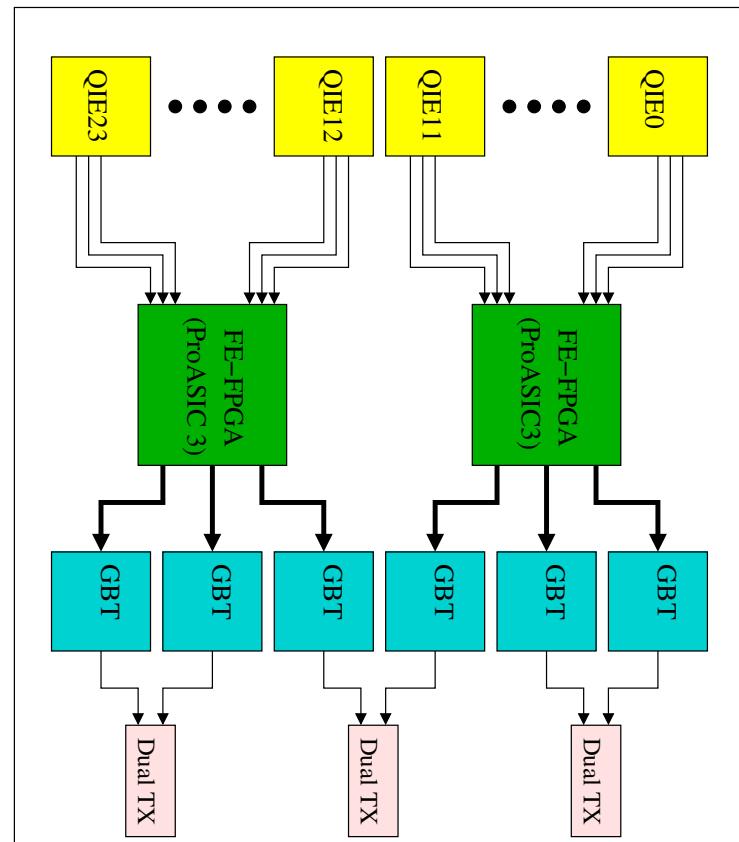


Figure 4.8: Mechanical drawings of an HF FE card front (left figure) and back (center figure) as well as two-card HF FE module.

Figure 4.7: Schematic view of the data flow within an HF front-end card.



of the cards and the front-panel mechanics will be arranged to avoid risk of damage to the QIE10 chips during module handling. The layout of the card will be arranged to allow the replacement of VTTx transmitter modules without requiring modification to the board.

The HF FE-FPGA will receive the discriminator output from the QIE10 and will use it to create a falling-edge TDC as well as identifying cases with multiple pulses within the same 25 ns window. The ProASIC3 FPGAs can run at 320 MHz (8 times the LHC frequency) and use flip-flops clocking on either the rising or falling edge of the clock. Thus, a 4-bit TDC (1.66 ns bins) can be implemented in the FPGA using a 320 MHz clock from the GBT and applying standard techniques, without use of the FE-FPGA PLL. The TDC is automatically started on each rising edge of the 40 MHz LHC clock and stopped by a falling edge on the discriminator output. One of the sixteen codes of the TDC is reserved for the case where no falling edge is observed, resulting in 15 total bins across 25 ns. Alternatively, the internal PLL of the FE-FPGA could be used to produce the 320 MHz from a slower clock provided by the GBT, with the rest of the techniques the same. With the use of the internal PLL, a 90°-phase clock could be produced, allowing a 5-bit TDC (0.80 ns bins) if required.

The LHCb collaboration has reported the development of such a 4-bit TDC on a single ProASIC3 FPGA as part of development work for their electronics upgrade. The design has been tested on hardware, and it shows practically no dependence on temperature (the measured variation is less than 0.007 count per degree Celsius). The LHCb design uses the FPGA integrated PLL for clock multiplication, but does not use gate delay (which explains the weak dependence on temperature). The PLL is susceptible to single-event effects under radiation as discussed in Chapter 3. In case of SEE on a PLL during data-taking, the TDC functionality can be compromised until a power-cycle is performed, but this will not affect the other functionalities, like the read out of ADC data, so it is a failure that can be isolated from the critical functions. According to manufacturer documentation, PLL SEE can be easily identified and reset without power-cycling the full chip. This functionality will be tested during system irradiation evaluation as described in Section 4.4.

The final decision on the use of the PLL will be made based on testbeam evaluation of the performance of the TDCs and the results of irradiation SEE studies. As the use of the PLL is determined by the firmware loaded into the FPGA, the circuit design will be completed in a manner to support, but not require, its use. This will allow the decision to be made based on the final observed performance and radiation tolerance without delaying the production of the hardware.

The three links attached to each FPGA will form an organizational group. As described in Chapter 3, the GBT data link will carry 88 bits of user data for every LHC bunch crossing. For the HF, two of the links will be dedicated to the ADC and rising-edge TDC data using the same data format as used in HB/HE. The third link in a triplet will be responsible for the pulse-width/falling-edge TDC information. The “ADC” links will each handle the data for six channels as shown in Table 4.1.

As discussed in Chapter 3, each QIE10 has a 2-bit rotating capacitor id (CapId) counter. All of these are sent to the FE-FPGA where they are checked for alignment, and reduced to a single consensus CapId for the six channels carried on a link and a bit identifying if there was a mismatch between any of the QIEs. When a CapId mis-alignment is identified due to power up or SEU, it should be corrected during the next orbit gap when the QIE is reset. Should a QIE device fail such that it is not possible for the CapIds to match, that QIE will be masked in the FE-FPGA such that the disagreement of the remaining functional channels can be tracked.

Table 4.1: GBT Link Data Format for the HF Upgrade for the primary fibers. Abbreviations listed in the data format are defined as follows: RE TDC (Rising-edge TDC produced within the QIE10); CapId (Capacitor ID for the capacitor used in this sample); CE (to indicate that the CapIds of all channels on the link are not the same); BC0 (Indicates that this sample is from the bunch with number zero in the orbit. Used for latency/phase alignment of the data links).

Byte	7	6	5	4	3	2	1	0
0								8b10b Comma Character
1			RE TDC 0[3:0]			CapId		CE
2							QIE ADC 0	BC0
3							QIE ADC 1	
4							QIE ADC 2	
5							QIE ADC 3	
6							QIE ADC 4	
7							QIE ADC 5	
8					RE TDC 1			RE TDC 2
9		RE TDC 3[1:0]						RE TDC 0[5:4]
10			RE TDC 4[3:0]					RE TDC 3[5:2]
11				RE TDC 5				RE TDC 4[5:4]

The third fiber of the triplet will provide data for twelve channels and use the data format shown in Table 4.2. The data format includes both the falling-edge TDC measurement from the FE-FPGA and information about the number of rising or falling edges observed within the 25 ns time window. This information is valuable for identifying and rejecting various types of anomalous noise and beam background which can generate long pulses or multiple spikes in the window if they overlap with true energy deposits. The arrangement of fibers in triplets will allow the initial operation of the system with only the ADC fibers if necessary as discussed below.

An important benefit of the ADC card design as shown is that it will be possible to reformat the data if required through reprogramming of the FE-FPGA. As an example, this would allow the reorganization of the data if an optical link failed and a replacement would not be possible for some time. In this situation, it would be possible to operate with the ADC data only on the operable data links, leaving out some or all of the TDC data.

Table 4.2: GBT Link Data Format for the HF Upgrade for the fibers which carry falling edge TDC data. Sufficient reserved space is available to accomodate a five-bin falling edge TDC. Abbreviations listed in the data format are defined as follows: FE TDC (Falling-edge TDC determined by the FPGA); TDC STS (Indicates if no edge was detected or if multiple edges were detected within a single bunch crossing); BC0 (Indicates that this sample is from the bunch with number zero in the orbit. Used for latency/phase alignment of the data links).

Byte	7	6	5	4	3	2	1	0
0								
1				Comma Character				
2	FE TDC A1			FE TDC A0				
3	FE TDC A3			FE TDC A2				
4	FE TDC A5			FE TDC A4				
5	FE TDC B1			FE TDC B0				
6	FE TDC B3			FE TDC B2				
7	FE TDC B5			FE TDC B4				
8	TDC STS A3	TDC STS A2	TDC STS A1	TDC STS A0				
9	TDC STS B1	TDC STS B0	TDC STS A5	TDC STS A4				
10	TDC STS B5	TDC STS B4	TDC STS B3	TDC STS B2				
11			Reserved (00)					

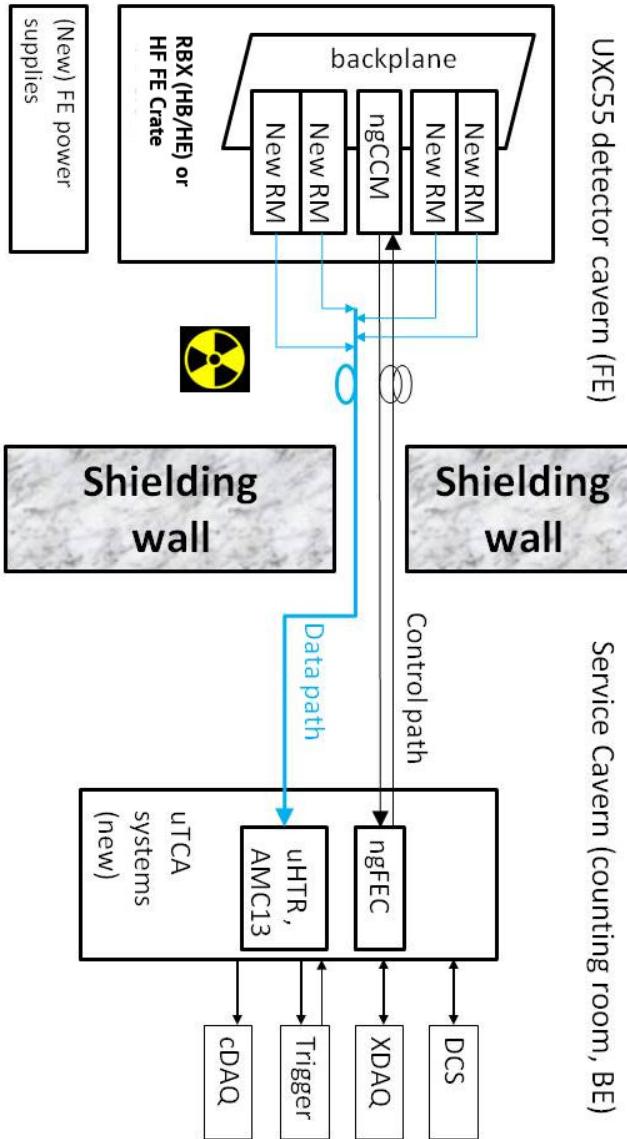


Figure 4.9: Block diagram of HCAL electronics. The diagram does not show the twisted pair links, the redundancy ngCCM links and the HV and LV cables.

4.2.2 Front-end control module (ngCCM)

The architecture of the Upgrade FEE remains similar to the existing FEE. As a consequence, slow control and fast control will be handled by the new-generation Clock-and-Control Module (ngCCM). The resulting scheme is shown in Fig.4.9, where the backplane of the FE-crates is accessible and can be changed if needed.

The ngCCM requirements are:

1. deliver a good quality clock (to be cleaned up again in the GBTxTs)
2. provide an orbit signal to the rest of the FE, to enable the marking of the data to maintain data synchronization. (QIEREST)
3. provide reset capabilities for the FE (RESET)
4. forward an input warning-test-enable (WTE) signal for calibration purposes
5. read out its own voltages and temperature
6. provide I2C communication for configuration of the GTBX, QIE10, and FE-FPGA chips
7. improve the robustness of the system.

These requirements are identical to requirements for the control of the HB/HE upgraded system, though the HB/HE system has additional requirements related to the SiPMs. As a result, the same architectural design will be used for both the HF and HB/HE ngCCMs, though the physical realization of the ngCCMs will be different as determined by the crate or readout-box in which the controller must sit.

In order to meet the first five requirements, the ngCCM will communicate with the counting room using two single-mode optical fibers (Corning SMF-28) and a twisted pair patch cable (four pairs). In the existing HF FE-crate, the slow control is implemented over the twisted pair patch cable, with an optocoupler on the CCM for noise reduction. During the operations of the existing HCAL, anomalous behavior was observed which was determined to be due to SETs in the optocouplers. The optocouplers are needed to provide electrical isolation, but essentially all optocouplers are sensitive to SET, so for the upgrade we will use the twisted pair patch cable for driving static electrical levels, which can be easily made immune from SETs with low-pass filters. In the upgrade, fast control and slow control will be merged and implemented over 4.8 Gbps bidirectional GBT links [50, 51]. The two existing single-mode fibers are expected to work at this data rate without problems (J. Troska, private communication). We intend to use the GBT in its Forward-Error-Correction mode, which is the most robust mode against noise and radiation-induced errors. Section 6.9 describes how the ngCCM will interact with the control room systems.

Regarding the requirement for robustness, the existing HF has one HF CCM per FE-crate with no redundancy and no connections between CCMs. A failure of part of a CCM causes the loss of a significant number of detector channels, and such an occurrence would be a severe fault. Intervention to the HF FEE will be possible during short technical stops, so a failed HF ngCCM could be replaced during such a stop. On the other hand, a broken fiber will be difficult to replace and at this time it is not clear if we can lay down spare fibers. For this reason a redundancy scheme can be effective to improve the overall robustness. The ngCCM design allows to build a system robust against individual failures of part of a ngCCM and certain failures of the optical fiber plant. A more robust design is achieved by adding redundancy, using a bidirectional port to connect adjacent ngCCMs. This port allows to establish a link (“redundancy link”) which connects bidirectionally each ngCCM to one of its neighbours, thus creating pairs of interconnected ngCCMs. Any of the two ngCCMs within a pair is capable to take over the control of the other ngCCM. The realization of the HF ngCCM will be on Eurocard-style format.

The resulting ngCCM scheme is shown in Fig. 4.10, where the redundancy elements are shown in grey. If there are no failures, the GBTx will communicate with the backplane with only I2C drivers and level shifters in between, but without FPGA intervention. The I2C signals in the backplane will be driven by GBTx parallel (“E-link”) signals. I2C signals have duration of many microseconds, while the GBTx E-link signals have a period of 25 ns and function in Double-Data Rate mode; we will obtain the desired behavior sending identical values on many consecutive clock cycles and on the two semi-periods related to each DDR cycle. The redundant scheme (grey components in Fig. 4.10) can cover a certain number of failures, including (but not limited to) failures of a GBT link. The redundant links will use optical fibers in order to avoid any problem of ground loops and of tolerance to magnetic fields. The requirements on the optoelectronic parts are compatible with developments from the Versatile Link project [51], in particular with the custom optical transceiver VTRX. For the encoding of the redundancy link we are investigating a scheme with a ProASIC3 FPGA.

The ngCCM is designed in such a way that its FPGA is reprogrammable after installation, and this feature adds flexibility and redundancy. The key components of the ngCCM design have been validated using a HB/HE-format prototype discussed in Section 5.5.

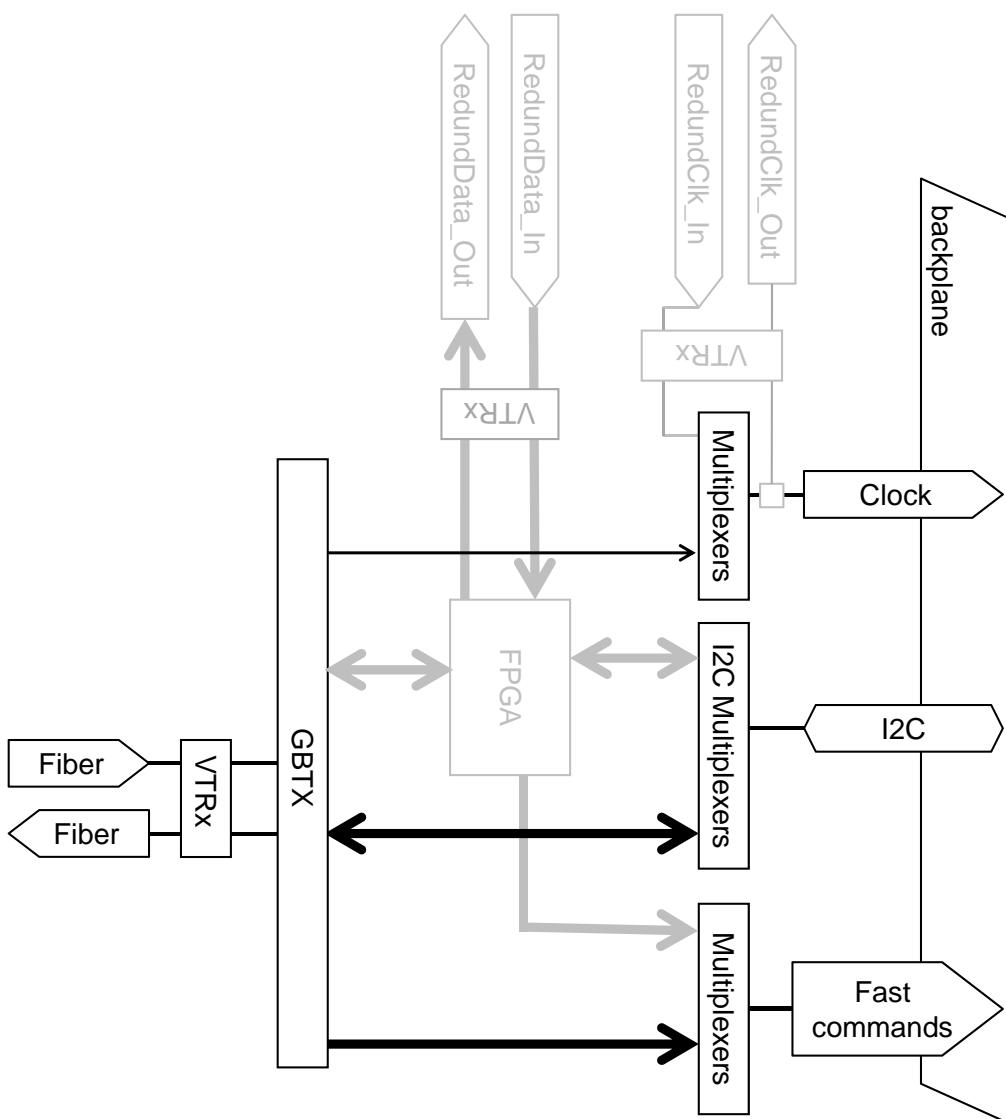


Figure 4.10: Simplified block diagram of the ngCCM. The redundancy elements in grey are discussed in the text.

4.2.3 Calibration module

Each front-end electronics crate will contain one calibration module. The calibration module contains an LED pulser for the PMT boxes read out by the crate as well as a laser light distribution system. The design of the LED pulser is the same as that used in the original HF calibration module. The controls for the pulser, however, will be significantly enhanced from those in the original calibration module. In particular, the calibration module will be able to use the CMS global Warning-Test-Enable signal to generate LED pulses during the LHC orbit

gap. This will allow monitoring of the phototube gain during CMS global operations. This capability was added relatively late to the current HCAL calibration and monitoring system and the LED pulser controls were not properly set up to allow the LED to fire during orbit-gap operations. The pulser controls will also be adjusted to allow for high-intensity “soaking” of the PMTs, which is important to pre-condition them for high-current operation. Otherwise, the PMTs will exhibit a short-term drift in gain when the average current drawn rises, as has been observed over the last few years of LHC operation.

4.3 Optical Fibers, Cooling, and Low-Voltage Power

As discussed above, the full functionality of the HF upgrade will require the use of twelve optical fibers per front-end module, while limited functionality will be available with eight fibers per module. The current HF optical fiber plant uses eight-fiber ribbons, while the front-end module and the uHTR will both naturally use twelve-fiber MTP connectors. While it is possible to re-use the eight-fiber ribbons with various fiber breakouts or patch-panels on both ends, it has been determined to be more cost-effective as well as simpler and safer to install a full set of 12-fiber ribbons for the HF upgrade.

The 12-fiber ribbons will be installed in parallel with the existing fiber plant, allowing for a safe transition from one set of optical fibers to the other. The installation of the optical fibers requires the HF to be on its risers, not in the garage. This configuration is unusual during extended technical stops and blocks other activity on the CMS detector as CMS must be in the closed configuration. The installation of the 12-fiber ribbons during LS1 may serve as contingency in the global CMS schedule, with a goal to have the fibers installed as soon as possible without undue pressure on the global schedule.

The layout of the HF front-end racks is shown in Fig. 4.11. Each of the two HF subdetectors hosts four readout racks, two tall racks on the upper portion of the HF structure and two shorter racks on the lower portion. The assignment of readout crates, AC-to-DC converters, and DC power supplies are shown as well.

It is currently estimated that a HF crate will require 330 W of power. With six crates on each HF, the low voltage system will need to deliver approximately 2 kW of power per HF, roughly a 66% increase over that of the existing HF FEE. The existing LV system consists of a single CAEN EASY crate per HF, with each crate containing four A3100 modules. For the upgrade, an additional CAEN EASY crate will be added to each HF and two additional A3100 modules, allowing each A3100 to power a single crate. Each A3100 can deliver 500 W to a crate, including power loss in the cables between the EASY crate and readout crate.

When considering the cooling of the electronics, the addition of a second EASY crate provides a second benefit by balancing the heat load across racks better. As a result, approximately 1 kW of power will be dissipated in each rack, 660 W from electronics crates and 200 W for an EASY crate or 350 W for the AC/DC converter. The heat exchangers in the HF racks are rated for 2 kW heat dissipation, so additional heat exchangers will not be necessary, even in the case of an increased power loss.

4.4 Test Program

As with all CMS projects, the HF front-end will go through the electronics design review (EDR) process before production begins. The EDR will review both the functionality of the electronics

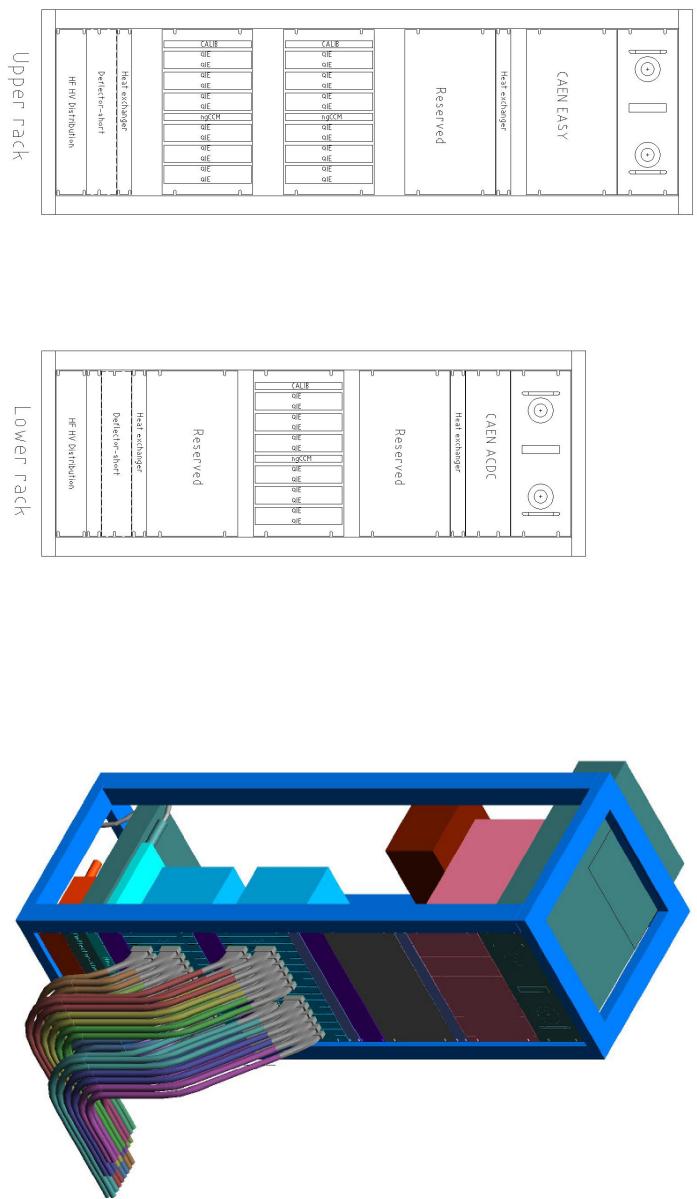


Figure 4.11: Layout of the on-detector racks of HF after the upgrade (left), showing the locations of the readout crates, AC/DC converters, and the DC power supplies (EASY crates), as well as the reserved space in case of future upgrades. There are a total of eight racks on the two HF subdetectors, four upper and four lower. On the right, a 3d view of an upper rack showing the signal cables leaving the front of the rack.

and its robustness including radiation tolerance. To prepare for the EDR, several tests will be made on the front-end electronics.

The primary functionality test will be a testbeam evaluation of the electronics during May 2014. The H2 beam test zone at the CERN North Area will be used for these tests. The tests will evaluate the behavior of the front-end with a partial HF-style calorimeter and also check the behavior of the front-end for muons and showers directed into the phototubes. Similar tests in previous years were important for understanding the anomalous signals seen in the detector and these tests will validate the solutions provided by the upgraded electronics. The possibility of 25 ns structured-beam tests will be discussed with the SPS run coordinators. The test will include the use of final pre-production ngCCM and readout electronics as well as the production back-end electronics.

The radiation tolerance of the design will be evaluated in tests at the CERN IRRAD facility. The crucial individual components (QIE10 and GBT) will be previously tested separately as discussed in Section 3.1.8 and Section 3.3.1. In preparation for the EDR, a radiation system test will also be performed at CERN IRRAD including the final FE-FPGA firmware. The tests will be performed with continuous readout, allowing the evaluation of single-event upsets as well as total dose effects. The test will include both the HF electronics cards and the ngCCM.

These tests, along with bench tests at Fermilab and elsewhere, will provide the basis for the EDR and approval for production of the front-end electronics. After the EDR, an additional validation will be performed using a partial crate installed on the HF platform and operating in parallel to the current 1.6 Gbps electronics. Given the time required for production and

burn-in of the front-end electronics, this test cannot be completed before the EDR and still allow installation on schedule. The test will allow very thorough testing of the software and firmware of the ngFEC and the FE-FPGAs, guaranteeing a fully-functional support system for the HF front-ends before installation begins at the end of 2015.

4.5 Installation and Commissioning

The installation of the HF front-ends is organized for the 2015/2016 year-end technical stop (YETS) of LHC. During a YETS, approximately two and half months would be available for installation work, assuming minimal holiday breaks. In preparation for the installation, all signal cables and optical fibers will be installed during LS1 as well as the full backend readout for the upgraded detector. The full crates of front-end electronics will be assembled and burned-in at CERN Building 904 for a minimum of four months in advance of installation.

In B904, the crates will each be connected to a PMT box for one week and validated with pedestals, LEDs, and lasers. Each crate will also be operated over the full four month period for pedestal and test-pulse operation to verify stability. The data written during these tests will be used to test all the offline reconstruction and High Level Trigger (HLT) code required for the multi-anode readout and TDC data inclusion.

The installation work required during the YETS in detail is:

- Replacement of PMT box adapter boards to switch from single-anode to dual anode readout. This task requires approximately 4 days of effort on each HF and can be completed in parallel with other activities.
- Removal of the existing HF electronics crates and cable adapters (3 days/HF).
- Installation of the additional EASY crates on each HF (1 day/HF).
- Installation of upgrade front-end electronics and connection to the PMT boxes and back-end electronics. This work is estimated to require approximately one day per crate with parallel work on both HFs. Thus, crate installation will require 12 days (two and a half weeks) of activity.

The commissioning of the detector will begin immediately with the installation of the first upgrade front-end electronics crates. Tests will include pedestal, LED, laser, and test-pulse runs. The HLT will also be commissioned with the full readout data format required to contain the TDC data and the multi-anode readout. It is expected that one month will be available for the full-detector commissioning after all crates are installed.

Chapter 5

Barrel and End-cap Front-End Upgrades

The HCAL barrel and endcap calorimeters are sampling calorimeters with a brass absorber and plastic scintillator as the active material. The light produced in the plastic scintillator is absorbed in Kuraray Y11 wavelength-shifting (WLS) fibers and re-emitted as green light, some of which is captured within the fiber. The light which is captured in the fiber propagates along the fiber to where the WLS fibers are spliced to clear fibers which carry the signals to photo-transducers. The structure of the calorimeter, including the tiles and fibers, is shown in Fig. 5.1.

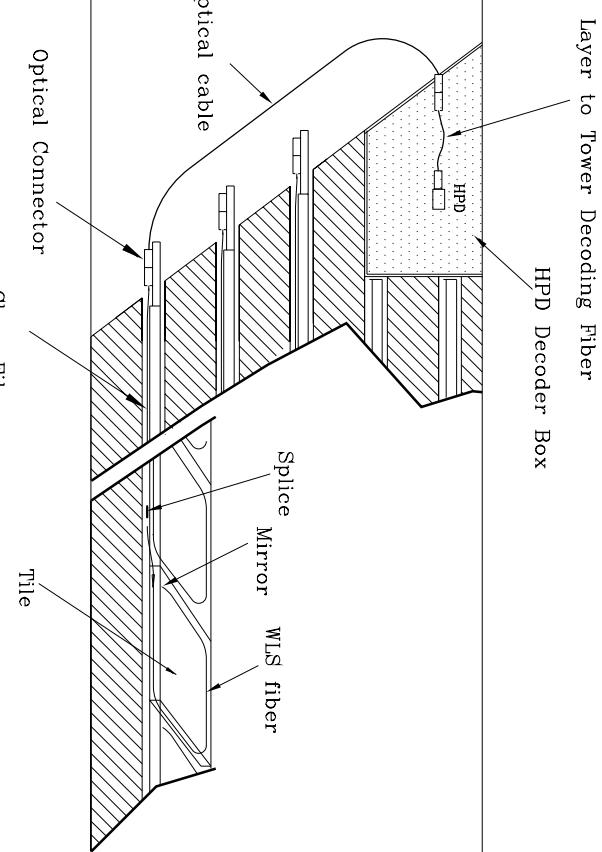


Figure 5.1: Structure of CMS barrel hadron calorimeter, showing the absorber, the plastic scintillator tiles, the wavelength-shifting fibers, and the location of the readout boxes.

HCAL barrel and endcap front-end upgrade is constrained to keep much of the existing infrastructure intact, including the readout boxes (RBX) enclosure and backplane, the power cables, the cooling pipes, and the copper cables and optical fibers connected to the off-detector electronics. The HB and HE each have 36 RBXs mounted on the detector. Given these strong constraints, the architecture of the upgraded readout modules (RMs) cannot be too different from the existing modules. The upgrade to the HB and HE systems involves the replacement of the RMs with new ones that use SiPM photosensors and which allow for depth segmentation. This chapter describes the aspects of the HB and HE front-end upgrade, including the SiPMs, the RMs, the control module (ngCCM), and the calibration module. The matching back-end

electronics upgrades are described in Chapter 6.

5.1 SiPM Photodetectors

SiPMs are a rapidly emerging technology that replace photomultipliers and other photodetectors for many applications, and are becoming quite common in commercial applications such as PET scanners. They have low operating voltage, high gain, large dynamic range, insensitivity to magnetic fields, and good radiation tolerance. They are now very suitable for application in the CMS central HCAL detectors, having been tested in parts of the CMS HO calorimeter [6] and used in other calorimeter applications like CALICE [58]. A large installation of 60,000 SiPMs has also been added to the T2K near-detector [59]. They are physically very small, being a few mm² in area and therefore give us the opportunity to increase the calorimeter readout segmentation. They operate at a modest reverse bias voltage of \approx 80 volts which allows local bias voltage generation via Cockcroft-Walton generators. They are able to withstand the expected radiation dose of \approx 10¹² n/cm², E>100 keV. Their large gain provides robust electrical signals that reduce the importance of electrical noise and allow for signal splitting for TDC measurements. Their increased effective quantum efficiency and ability to detect single photoelectrons improves the ability to calibrate and monitor the calorimeters.

SiPMs are pixelated APDs that operate in Geiger mode. Each pixel of the SiPM is separated from the bias voltage by a current limiting quench resistor. The absorption of a photon of proper wavelength can excite an avalanche that causes the struck pixel to discharge. The firing of a pixel causes its capacitor to discharge, creating a quantized charge output from the SiPM depending on the number of pixels that discharge.

5.1.1 SiPM Simulation

In order to understand the requirements for SiPMs for the HCAL upgrade, we have developed a simulation model of the basic properties of the SiPM and used GEANT to generate single pions to explore potential issues. The Geiger-mode nature of the SiPM means that each micro-pixel has a dead time during which the impact of a second photon will result in a smaller or zero charge signal from the device. Each SiPM also has a finite number of micro-pixels. As a result, the main issues studied were saturation and recovery time, considering the energy of a primary pion incident on the calorimeter and the presence of various levels of pile-up event background.

5.1.1.1 Sensor Model

We model the SiPM sensor with individual micro-pixels. The model includes parameters for the gain, its temperature dependence, the micro-pixel recovery time constant, and a simple optical cross-talk ansatz. There is also a fast analytic generator if one is not interested in the micro-pixel recovery behavior. We typically use an ADC simulation where the charge from the sensor is rounded down to a charge corresponding to a QIE code, but we can also use an “analog” type mode. We model the photon detection efficiency by attenuating the number of photons before passing them to the SiPM model, so that the SiPM model operates on “photo-electrons” which represent all photons which would impinge on the device and cause a Geiger cascade if the hit pixel is live.

Using this model, we can scan the input versus output of the sensor as can be seen in Fig. 5.2a. From this one sees the saturation of the sensor signal where the blue curve diverges from the diagonal at around 20% occupancy. The saturation is monotonic and one can correct for it,

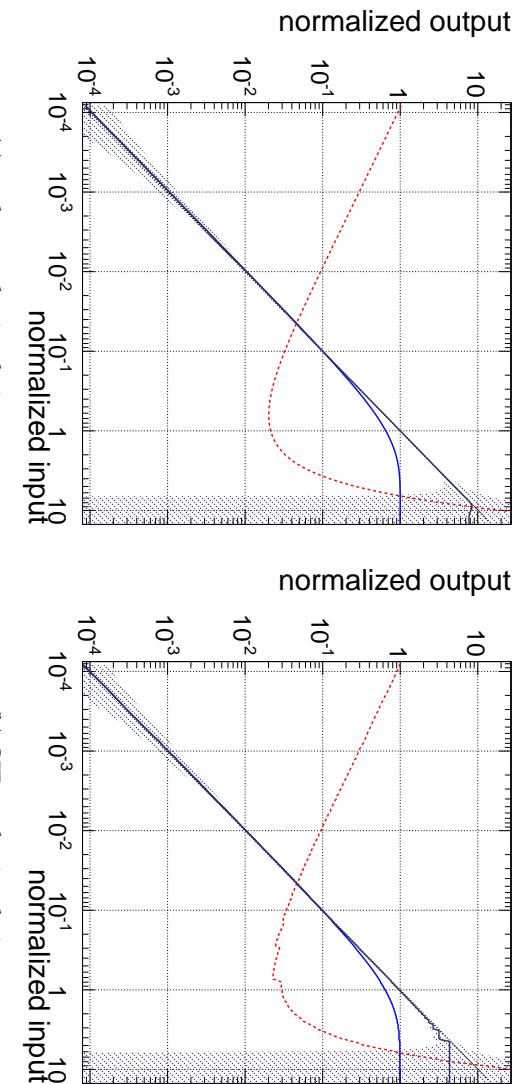


Figure 5.2: Output signal as a function of input “photon-electrons” both normalized to the number of micro-pixels in the sensor. The blue curve is the raw output. The black curve applies a basic correction for saturation. The red dashed curve is the fractional uncertainty of corrected measurement, showing the $1/\sqrt{N}$ effect of photostatistics at low amplitude and the uncertainty due to the saturation at high amplitude.

provided that all the analog signal in a given channel comes from a single SiPM device. The black curve in Figure 5.2a shows the result of this correction scheme. The uncertainty on the measurement after correction has two components. One comes from the Poissonian counting uncertainty on the number of photons and the second comes from the discrete nature of the SiPM pixels. These uncertainties cause the error on the correction to decrease as $1/\sqrt{N}$ as expected and then to blow up quickly as the slope of the saturation decreases at around $3 \times$ the number of micro-pixels in the device. When using the QIE simulation, there is a third source of uncertainty that comes from the quantization of the QIE. This is visible in Fig. 5.2b as the “jagged” portion of the error curve between 0.1 and 1.0 normalized input. Elsewhere, the error is dominated by the photostatistics (low amplitude) or the saturation effects (high amplitude). Figure 5.2b represents a 12,100 pixel sensor with a gain of 10 fC/photoelectron coupled to our QIE model.

Using the model described above we can study a toy calorimeter tower to understand the interaction of SiPM parameters with pile-up and a simplified physics signal. We can study different depth segmentations and SiPM configurations by adjusting the layers combined into a single SiPM and the number of SiPMs combined into a single readout channel. We thus compare different SiPM parameters and readout configurations against the basic physics signals discussed below to evaluate acceptable performance.

5.1.1.2 Signal and Pileup Models

The signal we use are the layer-by-layer GEANT4 energy deposits corresponding to the central tower of either a 500 GeV or 1 TeV charged pion. These energy deposits are derived from the standard CMSSW geometry and individual events are collected to form a signal library. We evaluate the response of the calorimeter to these large energy hadronic events.

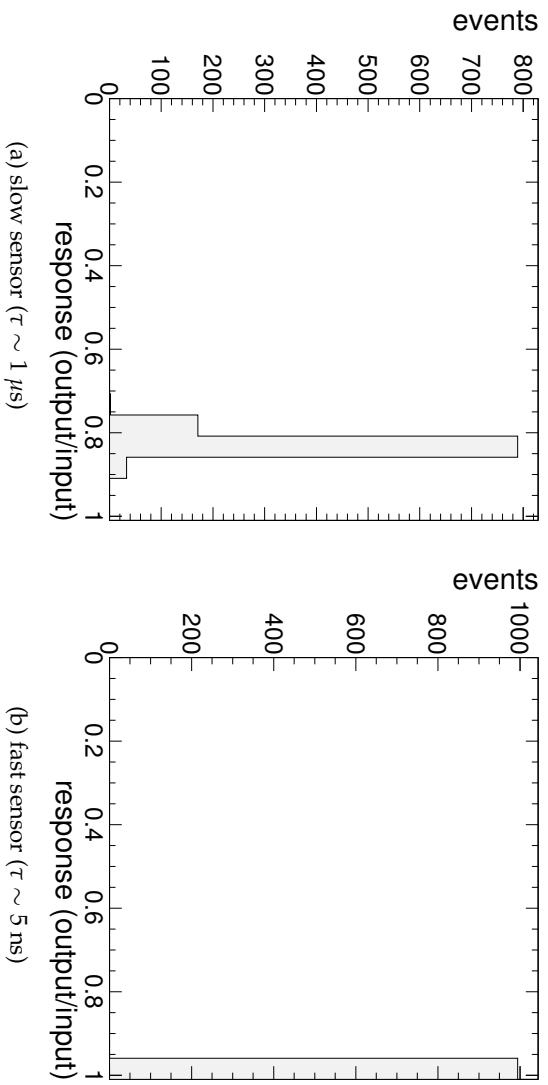


Figure 5.3: Response of a slow and fast SiPM to a test pulse after accumulating the pileup (50 interactions at 25 ns crossing) for $10 \times \tau$.

The pileup library is derived from layer-by-layer GEANT4 energy deposits of minimum bias simulation. In this case the layer-by-layer spectrum is extracted from simulation and used as a template to generate the energy deposits of a random minimum bias event using a toy simulation. We are able to simulate pileup for a full millisecond prior to the physics signal. This allows us to study the effects of the pixel recovery from the pileup-generated photon flux into the sensors.

5.1.1.3 Results

In general, we found that a one-to-one matching of readout channels and SiPMs is more forgiving in terms of dynamic range requirements of the SiPM and tolerance to pile up. We demonstrated that recovery time of the SiPM micro-pixels must be fast-enough to keep up with the pile-up rate. The sensors with pixel recovery times on the order of a micro-second have a significant baseline shift because of pile-up preceding the physics signal. Figure 5.3a shows the shift of 20% in the response of the slow ($\tau_{\text{av}} \sim 1 \mu\text{s}$) SiPM at only 50 interactions per 25 ns crossing as compared to a fast sensor, Fig. 5.3b, with a recovery time constant of a $\sim 5 \text{ ns}$. This would represent a significant shift in the response of the calorimeter over the course of a single run or fill.

The other key sensor characteristic is pixel density. If many photons arrive in a short time at the sensor, then it will go into saturation. If each SiPM is separately read out, correction of the saturation is possible with reduced precision as the signal increases. When summing the charge from multiple SiPMs in a single readout channel, it is best to keep the signal from each SiPM in linear region (below 20% occupancy). One can see the effects of pixel count on the saturation in Fig. 5.4, where the lower density sensor has a longer tail that extends out from unity. For one-to-one readout configuration, this tail could be corrected if it is above 0.6.

Interestingly, the pixel recovery time also plays a role in the dynamic range. Figure 5.2a have an assumption that the light arrives at the sensor as a delta function in time, however in truth it is distributed over 50 or more ns. For the very fast sensors, a micro-pixel can fire and recover and fire again, perhaps as many as 3 times during the scintillation time. This multiplies the

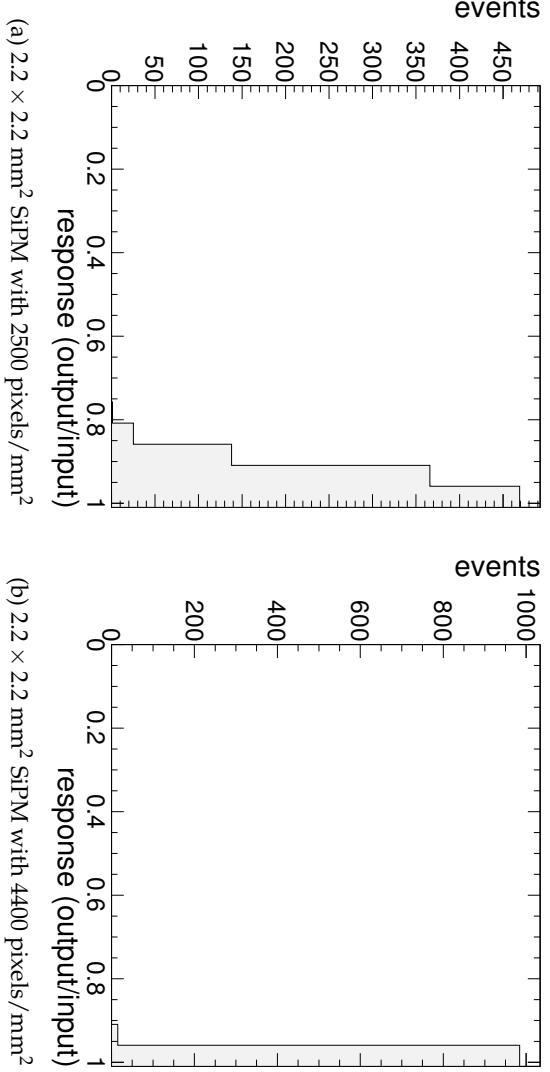


Figure 5.4: Response of two SiPMs with different pixel densities to 1000 GeV pion test pulses.

number of photons that a sensor can measure during a 25 ns integration time and extends the linear dynamic range as seen in Fig 5.5. At the same time, it distorts somewhat the shape of the scintillation pulse because the highest density of photons arrive quite early and push the sensor into saturation. As the cells recover the pulse has become considerably less bright so the tails of the distribution are accentuated by the response characteristics of the device. This distortion is however small and should have minimal effect given the charge-integration electronics of the QIE.

We conclude from these simulation studies that one of the key characteristics of a SiPM sensor is its pixel recovery time. This should be as small as possible, but generally less than the bunch crossing frequency to avoid a significant shift in response as a function of pile-up conditions. We also conclude that a large pixel density is critical. We find that when adding many separate SiPMs in a single readout channel the pixel density must be larger than $4400/\text{mm}^2$ and the recovery time $\tau < 5 \text{ ns}$. When reading out each SiPM individually, we can go as low as $2500/\text{mm}^2$, which puts 11k pixels on a device of size 2.2 mm^2 , and a recovery $\tau \sim 10 \text{ ns}$.

5.1.2 SiPM Equivalent Circuit

The equivalent circuit for the Hamamatsu $15 \mu\text{m}$ $500 \text{k}\Omega$ MPPC is shown in Fig. 5.6. This device is a candidate SiPM and we will discuss its properties in some detail below. In Fig. 5.6, C_1 is the pixel capacitance and R_1 is the quenching resistor. When the pixel C_1 discharges, the charge stored in it flows to R_{18} , a 10 Ohm resistor that represents the input impedance of the QIE10. C_4 represents the other 21608 cells in parallel with C_1 . C_2 is stray capacitance of the cell. C_3 is the parallel stray capacitance of the other cells in parallel, and R_3 is the parallel resistance of the quenching resistors of the other cells in parallel. C_8 is the parallel device capacitance of the guard rings and package. C_{12} is a local bypass capacitor to hold the bias voltage when there is a cell discharge. Important parameters are C_1 and R_1 which control the recovery time. Increasing the depletion depth will reduce C_1 and hence reduce the gain as well as speeding up the recovery time. Decreasing R_1 too much has a tendency to increase afterpulsing and make the SiPM more unstable.

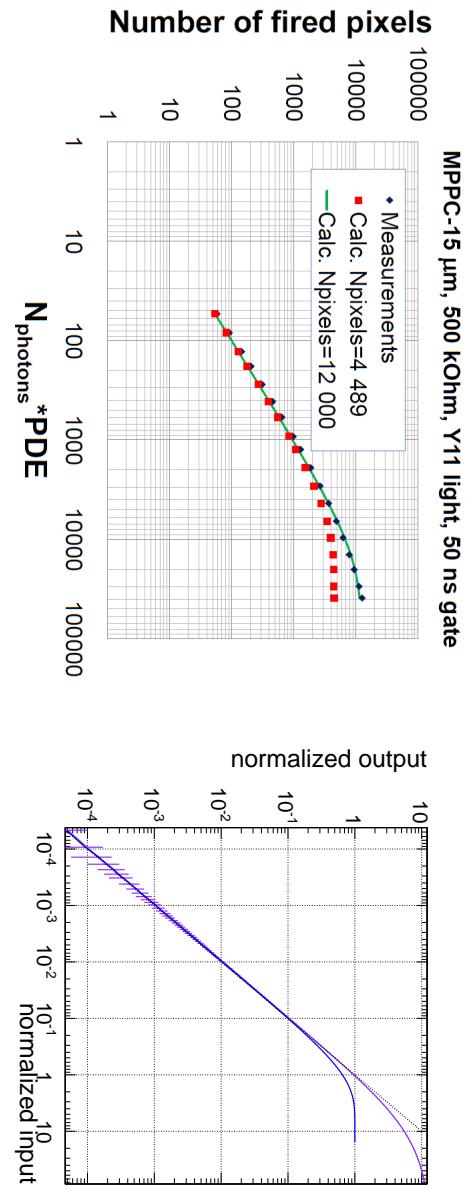


Figure 5.5: Demonstration of the dynamic range expansion of a fast-recovering SiPM able to fire multiple times during the Y11 wavelength-shifter pulse shape. The left figure shows results from simulation of a SiPM with $\tau = 4$ ns where the blue “light” has a δ -function time profile and the purple has the time profile of Y11 wave shifter and a 50 ns integration of SiPM signal. The right figure shows the result from bench tests of a candidate SiPM.

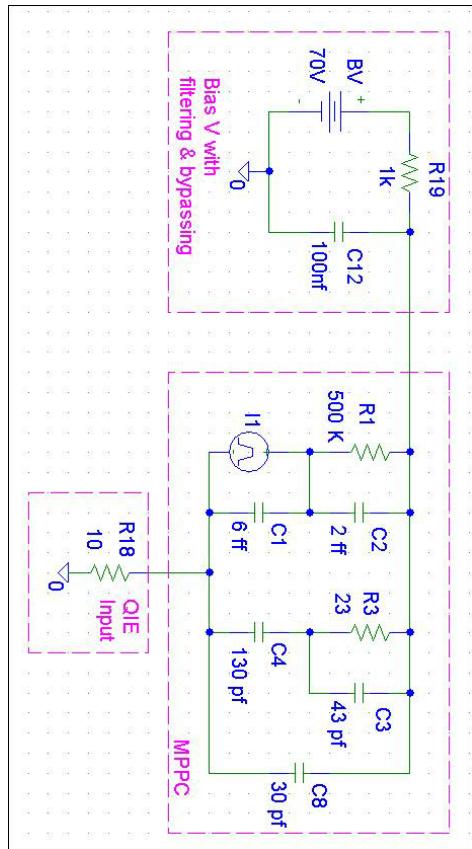


Figure 5.6: Equivalent circuit for the Hamamatsu 15 μm 500 $\text{k}\Omega$ MPPC, showing the circuit relationship of the key parameters pixel capacitance (C_1) and quenching resistor (R_1). These are discussed along with the other portions of the circuit in Section 5.1.2.

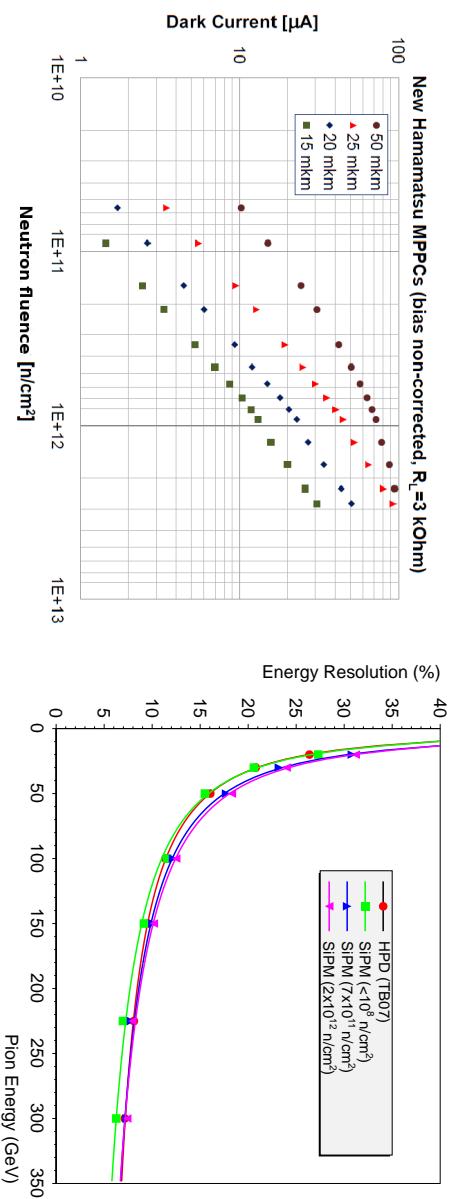


Figure 5.7: Effects of neutron-exposure on the MPPC leakage current (left) and detector resolution from simulation(right). The leakage current is shown for a 1 mm^2 device on exposure to neutrons and currents scale with area for larger devices.

5.1.3 Radiation Tolerance

As pointed out in Section 1.6, the expected lifetime dose to the SiPM is about $7 \times 10^{11} \text{ cm}^{-2}$ (1 MeV neutron equivalents), and 14 Gray of ionizing dose. With appropriate safety factors, we require tolerance to $2 \times 10^{12} \text{ cm}^{-2}$ neutrons and 100 Gray. We have studied the effects of neutron radiation on SiPM devices using the CERN IRRAD facility and an Am-Be laboratory source and the effects of ionizing radiation using the CERN IRRAD facility.

The neutron dose causes bulk damage in the SiPM. This has the effect of increasing the leakage current, which is dominated by micro-pixel discharges of the SiPM. The leakage current is thus directly related to the gain of the device. A reasonable maximum leakage current that can be accommodated is $200 \mu\text{A}$. Beyond that, the SiPM will heat significantly, which increases the leakage current, leading to an unstable operating situation. The plot on the left in Fig. 5.7 demonstrates the increase in dark/leakage current as a function of neutron dose for 1 mm^2 Hamamatsu MPPCs of various cell size. We see that the 15 micron cell size device has $25 \mu\text{A}$ at $2 \times 10^{12} \text{ cm}^{-2}$ dose, corresponding to $120 \mu\text{A}$ for a $2.2 \times 2.2 \text{ mm}$ square device.

The effect of such a leakage current on the detector resolution for pions is shown on the right of Fig. 5.7. The simulation and testbeam data both show the response for pions which deposit no energy in the ECAL calorimeter, which is somewhat better than the average response for the CMS calorimeter as whole. At the design criterion of integrated luminosity ($2 \times 10^{12} \text{ n}/\text{cm}^2$), the calorimeter resolution at lower energies is slightly worse than with the HPD ($119\%/\sqrt{E}$ versus $108\%/\sqrt{E}$), but this is not expected to be significant for physics.

The presence of increased leakage current causes a voltage drop in the HV filter resistor to the pixel, and hence a reduction in the applied overvoltage. If this is not corrected for by increasing the bias voltage, there will be a drop in the gain. We set a maximum limit of the reduction in that the gain multiplied by the photon detection efficiency (PDE) of the SiPM should be at least 60% of its original value. Fig. 5.8 shows the effect of the apparent decrease in $\text{gain} \times \text{PDE}$. We see that the $15 \mu\text{m}$ $500 \text{ k}\Omega$ MPPC (green data points) survives to $2 \times 10^{12} \text{ cm}^{-2}$ neutrons with only 20% loss of signal. It is also worth noting that this effect can be recovered by increasing the bias voltage, although at the cost of increasing the leakage current.

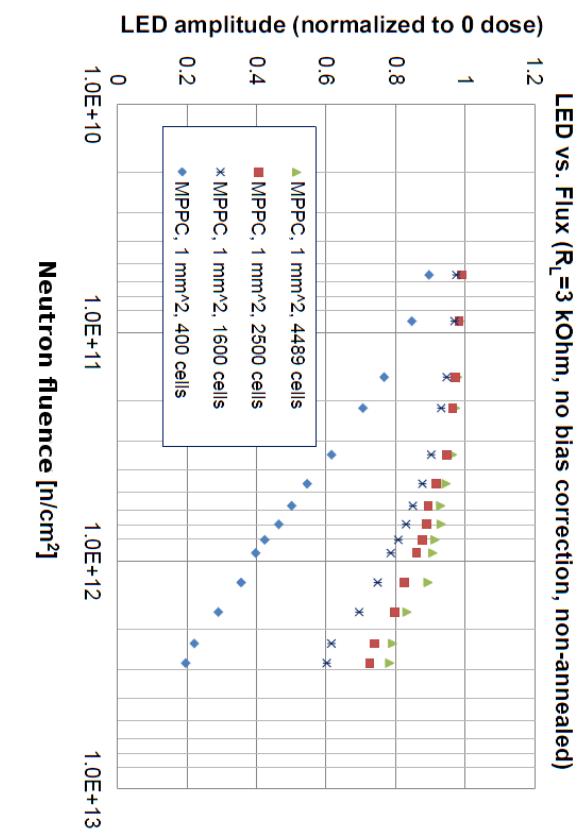


Figure 5.8: Change in Gain \times PDE after exposure to neutrons.

We have seen that the presence of epoxy encapsulation causes an enhanced sensitivity to neutrons. The neutron interacts with the hydrogen of the epoxy, causing ionization and resulting light. This creates spurious noise events. Therefore we have moved to encapsulation techniques that do not use epoxy. Additionally we have seen that some SiPMs have intrinsic sensitivity to neutrons. Our final choice of SiPM will include evaluation of the presence or severity of this sensitivity.

Fast neutrons produce neutron-nucleus elastic collisions in silicon with a cross-section of several barns. The recoil nuclei can pick up a detectable amount of energy from neutron collisions. Their energy can reach several tens of keVs and can produce thousands of electron-hole pairs due to ionization process. Such large number of electron-hole pairs can be easily detected especially in structures with avalanche multiplication of charge carriers. This effect is known in literature as a nuclear counter effect. The rate of the detected events depends on the thickness of the detectors active volume. In most cases the active volume is proportional to the thickness of the depletion region. The thickness of the depletion region of a typical SiPM is rather small: 2.5 μm . The SiPMs operate in Geiger mode and their single pixel response does not depend on the ionization produced inside the SiPM pixel – a single electron-hole pair results in the same pulse as thousands. As a result, the nuclear counter effect rate in SiPMs is expected to be small and signals induced by neutrons in the SiPMs are expected to be equal to their single photoelectron pulse.

This expectation was confirmed for most of the SiPMs studied during our R&D efforts; SiPMs from KETEK, FBK and Zecotek had very low nuclear counter effect rates and the induced signals had single electron amplitudes. However, this was not the case for Hamamatsu MPPCs. In Fig. 5.9 one can see oscilloscope screenshots of the signals induced by neutrons in a KETEK SiPM (upper channel) and Hamamatsu MPPCs (bottom channel). The SiPMs were irradiated by 1 MeV neutrons at the CERN IRRAD-6 facility. At this facility neutrons are produced by 24 GeV protons hitting the marble wall. The sensitivity of Hamamatsu SiPMs to neutrons was also studied using an Am-Be neutron source ($E_n=1\text{-}10 \text{ MeV}$). Fig. 5.10 shows an example SiPM response to a neutron from Am-Be source.

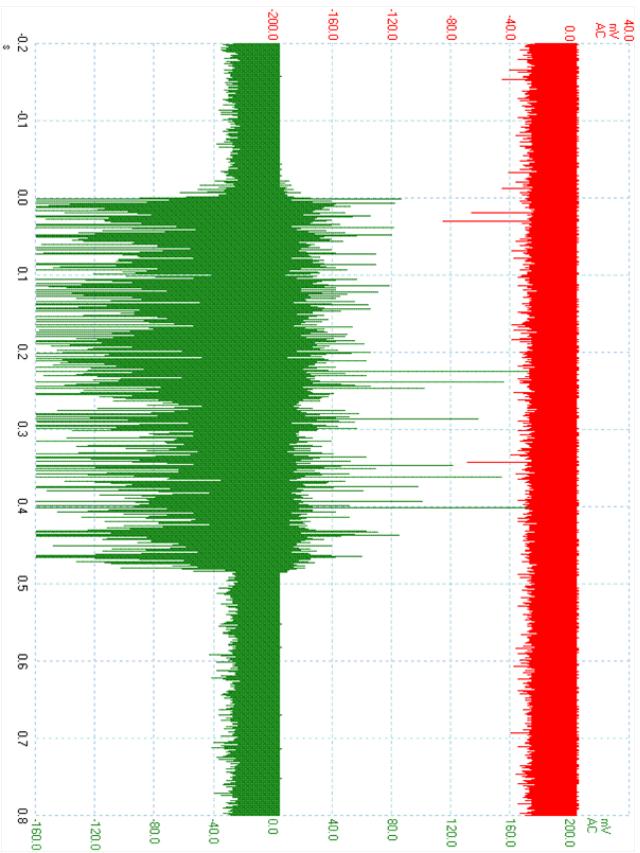


Figure 5.9: Screenshot of the signals induced by 1 MeV neutrons in 1 mm^2 KETEK (top) and Hamamatsu (bottom) SiPMs. Screenshots were taken during beam burst from CERN PS accelerator (time scale is in seconds, amplitude scale is in mV). The signals from SiPMs were amplified by fast amplifiers.

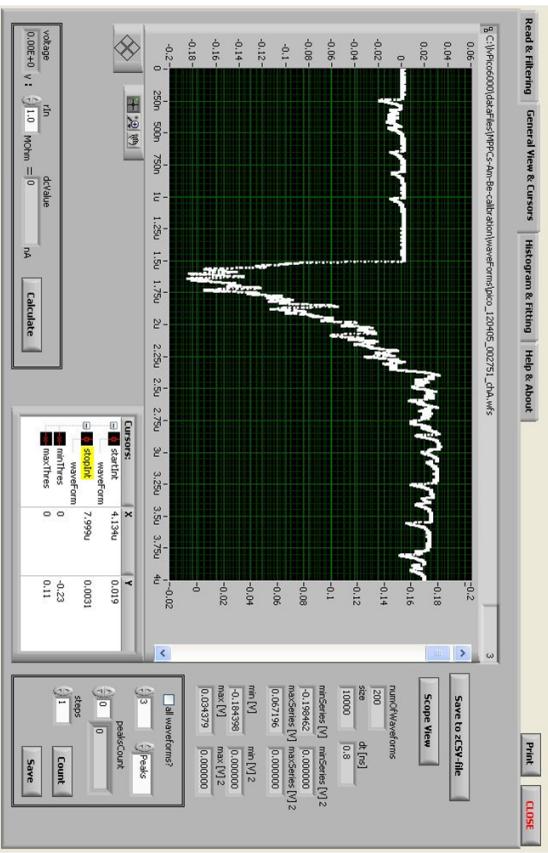


Figure 5.10: The Hamamatsu SiPM response to the neutron from Am-Be source.

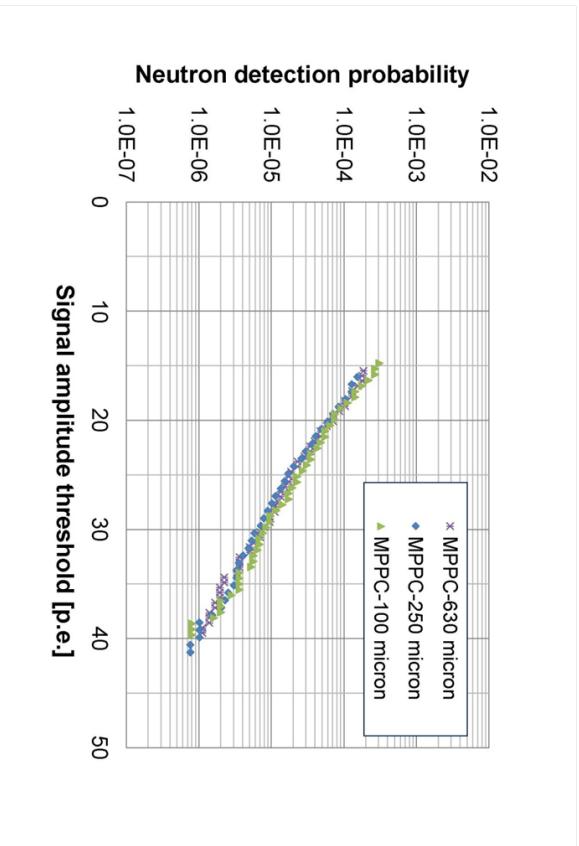


Figure 5.11: The measured probability to detect neutrons from Am-Be source by $3 \times 3 \text{ mm}^2$ Hamamatsu SiPM, as a function of the discriminator threshold. The Hamamatsu SiPMs had different thickness of silicon bulk (630, 250 and 100 μ)

From Fig. 5.10 one can see that the duration of the signal is much longer than the duration of the SiPM single electron pulse. Such long signals can be due to the carriers diffusing to the SiPM pixel volume from non-depleted silicon bulk. Typical diffusion time can be estimated as $\approx 1\mu\text{s}$. This corresponds to $\approx 35\mu\text{m}$ diffusion length for holes in silicon. All SiPMs produced by Hamamatsu have fast pixel recovery time (4-15 ns). The charge carriers produced in non-depleted silicon bulk can slowly diffuse to the micro-pixel depleted volume and cause multiple firing of a single SiPM micro-pixel. The neutron-induced SiPM signals reach several hundreds of electrons in amplitude.

Figure 5.11 shows the measured probability that neutrons from Am-Be source cause signals in Hamamatsu SiPMs as a function of the discriminator threshold. Taking into account the neutron flux in the HB RBX ($2 \times 10^4 \text{ n/cm}^2$ at $L = 10^{35} \text{ cm}^{-2}\text{s}^{-1}$ and the SiPM sensitive area ($\approx 5 \text{ mm}^2$), one can estimate the HCAL trigger rate of $\approx 10^{-3} \text{ Hz}$ per Hamamatsu SiPM for a 40 photo-electron (2 GeV) threshold. For a KETEK SiPM, this rate will be at least six orders of magnitude smaller.

5.1.4 SiPM Specifications and Candidates

The gain of the SiPM is closely related to the properties of the QE10, already discussed in Section 3.1. The QE10 has least count of 3.2 fC, and full scale of 339 pC. The single photoelectron should be observable as it provides a convenient calibration. As the electronic noise (before neutron damage) will be approximately 0.7 least counts, the single photoelectron should be 3 least counts above pedestal to provide good separation. One photoelectron should produce 10 fC of charge or 60,000 electrons – implying a gain of 60,000. To check what the full scale signal of 339 pC corresponds to, we note that the calorimeter provides about 30 photoelectrons per GeV, folding in the SiPM PDE of about 17% at 500 nm wavelength. Therefore 1 GeV is 180,000 electrons or 300 fC. Full scale is $339,000 / 300 = 1130 \text{ GeV}$ per 25 ns timeslice per readout channel. This is a good match to our physics requirement.

The number of effective pixels is a function of the actual number of pixels and the speed of recovery time. As discussed above, the light pulse from the calorimeter is about 40 ns wide, there is an opportunity for pixels to be re-fired, if the recovery time is fast. As shown Fig. 5.5, the fast (3.3 ns) Hamamatsu 15 μm 500 k Ω pixel MPPC achieves an effective number of micro-pixels 2.7 times larger than the physical number of micro-pixels. As a result, we require a recovery time of at most 10 ns and at least 20K micro-pixels per SiPM.

We are testing devices from several vendors. For this report we concentrate on Hamamatsu and KETEK devices. In Table 5.1, we summarize the required specifications and the characteristics of several of the best devices studied to date. The Hamamatsu 15 μm 500 k Ω device meets our specs with the exception of sensitivity to spurious noise events caused by neutrons. We are working with the vendor to reduce it. The KETEK 15 μm 400 k Ω would meet our specifications with a reduced gain and increased photon-detection-efficiency. We are working with this vendor to understand these issues.

Table 5.1: SiPM Specs and candidate SiPM values. Neutron exposure is 2×10^{12} neutrons of 1 MeV equivalent damage, unless noted otherwise. (^aFor these devices neutron exposure was to 1.6×10^{12} . ^bKETEK device parameters are scaled from tested 1X1 mm² device.)

Parameter	Spec Value	Hamamatsu 15 μm 500 k Ω	^a KETEK 20 μm 400 k Ω	^{a,b} KETEK 15 μm 500 k Ω
Size	2.2 mm ² or 2.5 mm round	2.2X2.2	2.2X2.2	2.2X2.2
Gain	6×10^4	2×10^5	9×10^5	5×10^5
Effective number pixels (per device)	> 20K per device	58K	12K	44K
Recovery Time RC	< 10 ns	4 ns	29 ns	8 ns
PDE at 515 nm	> 15%	18%	21%	12%
Leakage Current (after 2E12 n)	< 200 μA	120 μA	900 μA	388 μA
Fractional Gain X PDE (after 2E12 n)	> 65%	80%	80%	85%
ENF	< 1.4	1.3	1.2	1.1
Optical Cross Talk	< 15%	15%	15%	10%
Neutron noise sensitivity	NO	yes	no	no
Bias Voltage	< 100 V	75 V	25 V	29 V
Operating temp	22°C	22°C	22°C	22°C
Temperature Dependence	< 5% per °C	4%	1%	1.5%

5.1.5 SiPM Packaging

To simplify the construction of readout modules and to protect the SiPMs, the individual devices are packaged in eight-SiPM arrays in a ceramic carrier, as shown in Fig. 5.12. The carrier provides separate bias voltage and signal pins for each SiPM in the array. The entire ceramic package is covered by a quartz window which protects the wire bonds and front surface of the SiPM. Epoxy encapsulation for protection of the wire bonds and SiPM surface, which is commonly used in industrial and commercial applications, was abandoned after it was discovered that the epoxy caused spurious signals when the SiPM operated in a neutron-rich environment as discussed above.



(a) 3D CAD model of SiPM ceramic carrier

(b) Photograph of carrier loaded with SiPMs

Figure 5.12: Ceramic carrier for the SiPMs.

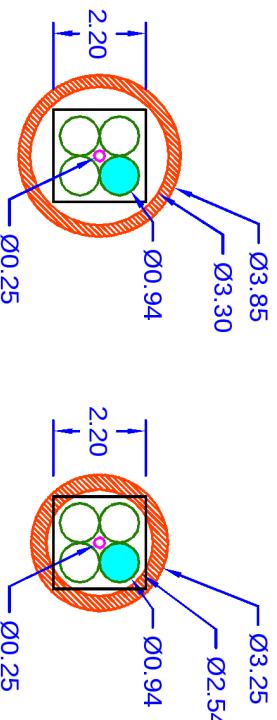


Figure 5.13: Four optical fibers carry waveshifted scintillation signals from the calorimeter to the SiPM. Each of these fibers has a diameter of $940 \mu\text{m}$. At the center of the grouping is a $250 \mu\text{m}$ diameter minicalibration fiber. The SiPM perimeter is indicated for $2.2 \text{ mm} \times 2.2 \text{ mm}$ square format SiPM and two formats of cylindrical optical mixer, with outer diameters of 3.25 mm and 4 mm .

5.2 Optical Mixers

Given the performance characteristics of the pixels of the SiPM, it is important to spread the light from all input fibers as uniformly as possible across the SiPM surface. This helps to maximize the photon-detection efficiency and the rate performance of the SiPM.

Given the depth segmentation planned for the HB and HE subsystems, multiple optical fibers are mapped onto a SiPM device of $2.2 \text{ mm} \times 2.2 \text{ mm}$ cross sectional area. Figure 5.13 shows the arrangement of optical fibers for a four-fiber combination, arranged in a two-by-two format, and the perimeter of the SiPM. These fibers are of $940 \mu\text{m}$ diameter. In the interstice at the center of the grouping is inserted much smaller diameter calibration fiber of $250 \mu\text{m}$ diameter, used for providing an optical calibration and timing pulse to the SiPM.

Numerous optical mixing strategies were studied and tested, having various cross sections, materials and surface preparations. The simple solution of a cylindrical cross section, cladded-fiber mixer proved to be superior to all other methodologies. The basic format for HB is shown in Fig. 5.14, in which 3.25 mm diameter cylindrical optical mixers are mounted and registered in an aluminum “mixer” support plate. The fibers themselves have a vinyl polymer core and a single, thick fluoro-polymer cladding. The fibers are glued into the plate. The surfaces of the mixer plates receive a final optical finish through a diamond fly-cutting procedure.

The optical transmission through the mixer is tested using a Y11 waveshifter fiber of $940 \mu\text{m}$ diameter optically excited through the sidewall using a blue-violet LED. This excitation is similar to that of the waveshifting of scintillation light in a HCAL megatile. The waveshifting fiber

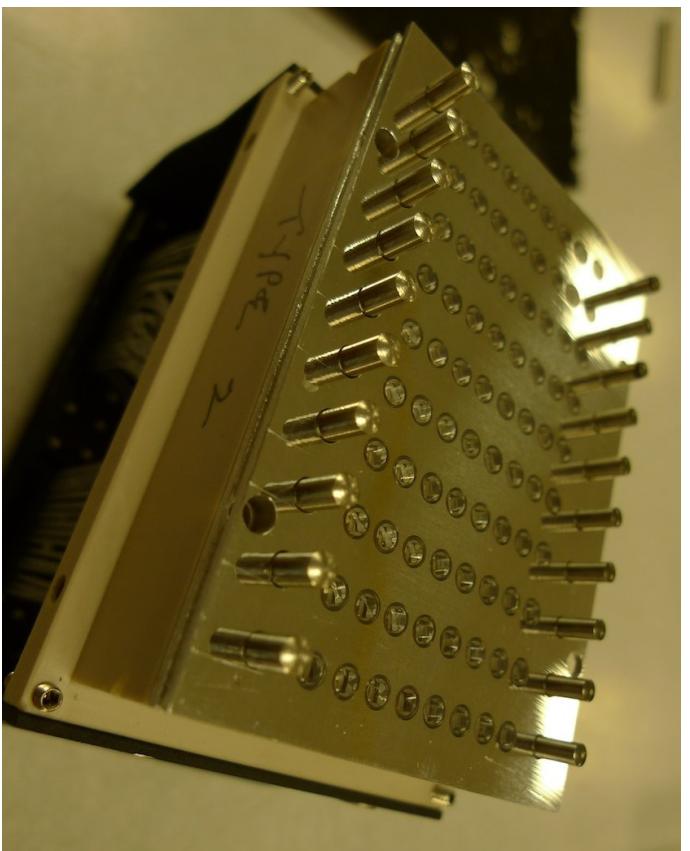


Figure 5.14: An aluminum mixer plate used for HB testbeam evaluation. The plate supports 80 optical mixers in an arrangement that allows them to be registered with 1×8 linear arrays of SiPM. The thickness of the mixer plate (and hence the axial length of the optical mixers) is 4 mm.

is coupled through a ferrule to a clear fiber waveguide, and the light from the Y11 source propagates to the end of the clear fiber, where it emerges into and passes through an optical mixer under test. The light transmitted through the mixer is detected by a P/N diode on the far side. The current in the P/N diode can be measured with and without the mixer; the ratio gives the transmission efficiency. The transmission is typically in the 85% range, dominated by the effect of the additional optical interface added in the system, which has an effect of 5-10%.

SiPM devices operate most effectively when uniformly illuminated, so the distribution of light output from the optical mixer is also important. The optical profile of a mixer is studied by replacing the P/N diode with a fiber-optically coupled CCD. With the CCD sensor, the optical profile of the light, with and without mixing, can be studied. In the top row of Fig. 5.15, the left column shows a direct CCD image of an excited fiber (of a grouping of four) in the absence of optical mixing. The middle column then presents the corresponding spatial intensity profile from the digitized light information from the CCD. The right column shows a histogram of the intensity recorded in all of the individual CCD pixels. This indicates that the pixels illuminated by the input fiber are clustered near 210 counts.

Using the reference established by the fiber without mixer, the performance of optical mixer candidates can be evaluated systematically. The middle row, left column, of Fig. 5.15 shows the direct CCD image of same input fiber, excited at the same level as before, but now seen through an optical mixer of 3.25 mm diameter and 4 mm axial length. The image appears to be much more “dim”, which is just what is intended. The same amount of input light intensity is now distributed across a much larger area, as can be seen quantitatively in the middle row of Fig. 5.15. The measurements for optical mixers of 3.85 mm diameter \times 6 mm length are shown in the bottom row of Fig. 5.15.

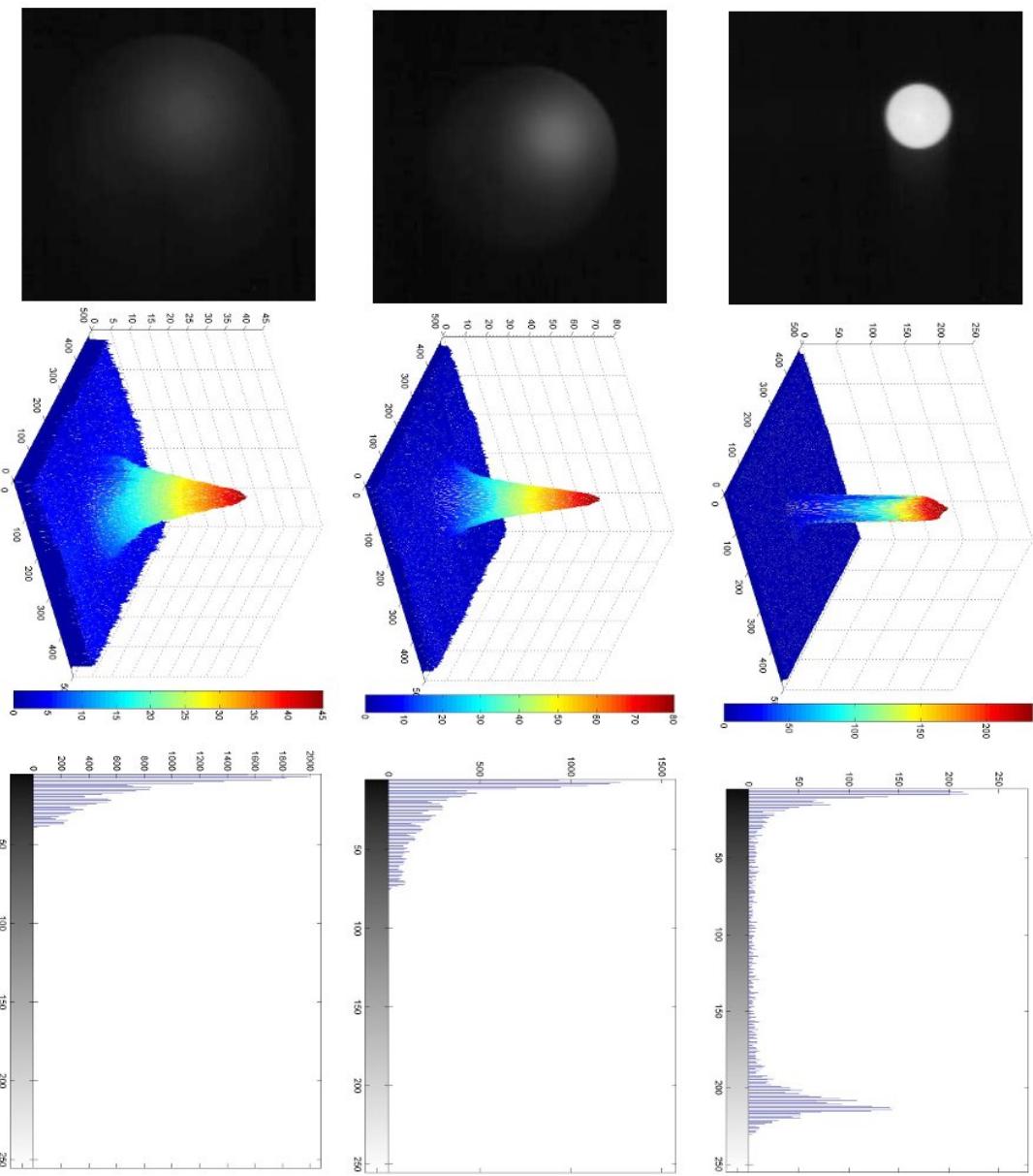


Figure 5.15: Image (left column), intensity profile (center column), and pixel amplitude histogram (right column) of the light from a $940\text{ }\mu\text{m}$ optical fiber directly coupled to CCD imager (top row). Results are also presented as seen through an optical mixer of 3.25 mm diameter and 4 mm length (middle row) and 3.85 mm diameter and 6 mm length (bottom row). Intensity is in least counts and corresponds to the light intensity detected per pixel on the CCD.

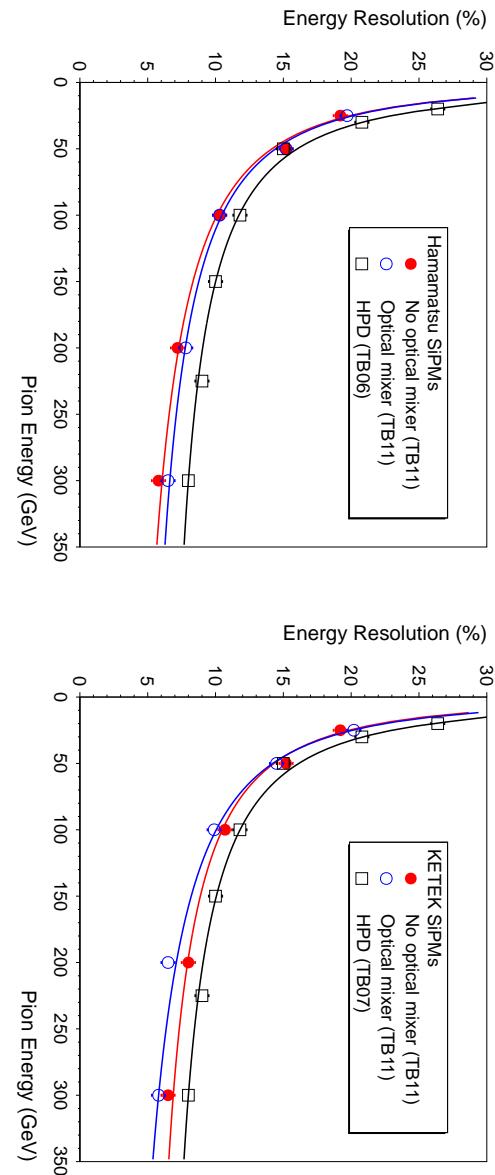


Figure 5.16: Pion energy resolution for Hamamatsu and KETEK SiPM readout modules in the H2 test beam (2011) compared with results with HPD from 2006 (TB06)[60].

The optical mixers developed so far are able to remove any significant impact on calorimeter performance, as demonstrated in testbeam studies discussed below. A number of additional tests will be performed on the mixers, including studying longer mixers as well as radiation tests on the mixers during and after exposure to gammas, protons and neutrons. Additional studies on thermal stability (from -20°C to 60°C , allowing for a tracker cooling accident or an RBX overheat) and humidity will also be performed. The mixer design will be finalized with the completion of the layer segmentation choice and validated using both simulation and testbeam.

5.3 SiPM Testbeam Studies

In October 2011, the HCAL group made test beam studies of the SiPM readout concept in the H2 beam at CERN. The H2 testbeam area contains two production barrel hadron calorimeter wedges and a production ECAL supermodule can be mounted in front of one HB wedge. The calorimeters are mounted on a rotating table and the cell of the calorimeter directly exposed to the testbeam can be varied.

For the October 2011 test, four phi slices were instrumented. Two slices were instrumented with HPDs, and two slices had various candidate SiPMs. Each SiPM-instrumented readout module was able to read out four towers around $\eta = 0.6$. Each of these $\eta - \phi$ towers were read out with four longitudinal depths: layer 0, layer 1+2, layer 3+4+5+6, and layers 7 to 16. To read out the eight fibers of the last depth, 2 SiPMs were employed, each viewing four fibers. The charge signals from those SiPMs were combined electrically at the input of the QIE front end electronics. The other three depths were read directly into QIE channels.

Two SiPMs listed in Table 5.1 were studied in detail: the Hamamatsu 2.2 mm^2 MPPC with $15\text{ }\mu\text{m}$ pitch micro-pixels and $500\text{ k}\Omega$ quench resistors, and the KETEK SiPM with micro-pixel pitch of $20\text{ }\mu\text{m}$ and $400\text{ k}\Omega$ quench resistors. Readout modules were constructed from SiPMs of both types and installed into the HB facility at H2. With these prototype readout modules, we demonstrated that a four-depth readout is viable and does not degrade energy resolution by the summation of four times as many electronics channels. Fig. 5.16a and Fig. 5.16b show

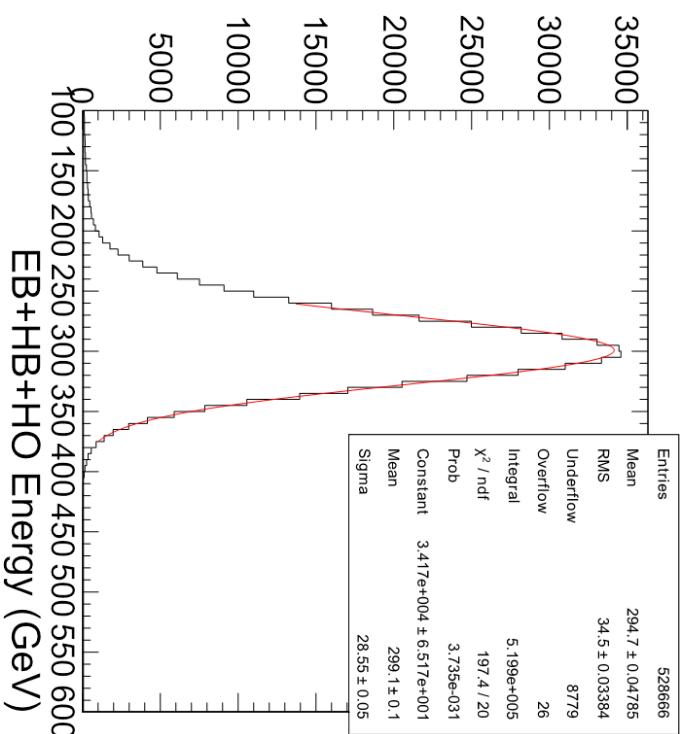


Figure 5.17: Energy distribution for 300 GeV pions, where sum of ECAL + HCAL + HO was formed. The HCAL was instrumented with KETEK SiPMs with light mixers.

measured energy resolutions for the HB when fitted with Hamamatsu MPPCs and KETEK SiPMs respectively.

Fig. 5.17 shows 300 GeV pion energy distributions where ECAL+HCAL+HO were summed, and as expected there are no significant tails to the distribution. The HCAL was instrumented with KETEK SiPMs with light mixers.

As described earlier, the first of the four longitudinal depths was a single layer of scintillator, with a single optical fiber carrying the light to the SiPM. We tested two cases, the first where the fiber went directly to the SiPM, illuminating an area corresponding to the 0.93 mm diameter of the fiber. In this case most of the pixels of the 2.2 mm square SiPM did not view the light from the calorimeter. The second case studied was where the fiber went into a light mixer such that most of the pixels were illuminated by the light. Fig. 5.18a shows the case for KETEK, where the solid line is without a light mixer. We see that the presence of the light mixer substantially increases the dynamic range of the readout. Fig. 5.18b shows the same thing for the Hamamatsu MPPCs. Here we do not see the striking effect of the light mixer. This is because the Hamamatsu device had substantially more effective pixels. These signals did not saturate the number of pixels available in the 0.93 mm diameter area.

The research and development program on the SiPMs has been highly effective and comprehensive, including the evaluation of devices from more than fifteen manufacturers. Near-candidate SiPMs have been identified and proven from two manufacturers and we expect to have final candidate devices available by the end of 2012, allowing a vendor selection as early as the middle of 2013 though additional time is available in the schedule for final parameter adjustments and vendor cost-competition.

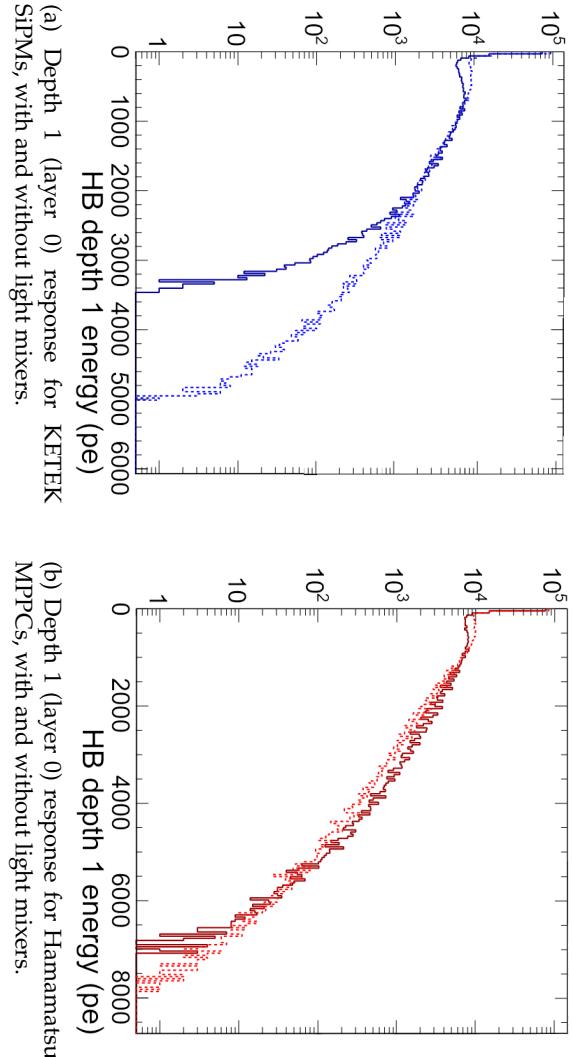


Figure 5.18: Number of photo-electrons recorded for depth 1 for KETEK and Hamamatsu SiPMs. Two cases are shown, without and with light mixers.

5.4 Readout Module

As discussed in the chapter introduction, the RM contains the phototransducers and the front-end electronics chain. In detail, the functions of the RM are:

1. receive analog light pulses from the calorimeter scintillators via optical fibers and organize into calorimeter tower segments for readout via an Optical Decoder Unit (ODU)
2. transform the calorimeter signal from light to electrical pulse (SiPM/SiPM card)
3. digitize the calorimeter electrical signal (QIE10/QIE card)
4. format the digital data (FE-FPGA/QIE card)
5. serialize the digital data and convert into optical data and drive it off the RM to the back-end electronics (GBT/QIE card)
6. provides bias voltages for the SiPMs, control voltages for the Peltier coolers that stabilize the SiPM temperatures, and readback of critical temperatures, voltages, and currents of the electrical system. (Bias-Control Board)

A readout Module (RM) consists of an ODU, one SiPM Mounting Board hosting eight SiPM arrays, one SiPM Control Board and four QIE10 Boards. Each of these tasks is accomplished by the RM component indicated in parentheses.

The detector connects to the RM via a set of multi-fiber optical connectors which connect to the ODU. Each optical connector carries the signals from all eta values of a given scintillator layer and the role of the ODU is to remap these signals to collect the light from the appropriate layers to the correct phototransducer. The SiPM, described previously, receives the light from the calorimeter segments and converts it into electrical pulses. The electrical pulses are received on QIE boards where integration and timing measurements are performed by QIE10 chips and the digital results are transferred to an FE-FPGA. The FE-FPGA is responsible for data formatting and for interfacing between the ngCCM and the QIE chips. The data output to the counting room is performed via a GBT chip and Versatile Link transmitter also residing on the QIE board.

The SiPM control board performs many functions. It supplies the the bias voltages for the array of SiPMs and provides for the readback of the SiPM leakage currents. The control board is also important in the temperature management for the SiPMs, as it supplies the control voltages for the Peltier coolers and provides for readout of temperatures used for the Peltier control feedback loop.

The design of all the boards is not finalized, as the final ASICs are not yet available. However, a prototype HB RM design was completed for a 64-channel, 80-SiPM used in the testbeam evaluation described in Section 5.3 which shows the key elements of the mechanical design as realized in a full module. The layout of the components an RM can be seen in Fig. 5.19 which can be compared directly with the prototype RM in Fig. 5.20.

Although functionally the same as the HB RM, the HE RM is mechanically different. The optical cables from the HE calorimeter enter the RM at an angle rather than head-on as for HB and the heat extraction occurs in the center of the RBX rather than on the top and bottom surfaces. The board-level components are expected to be identical for HB and HE, which was a successful strategy in the original detector electronics.

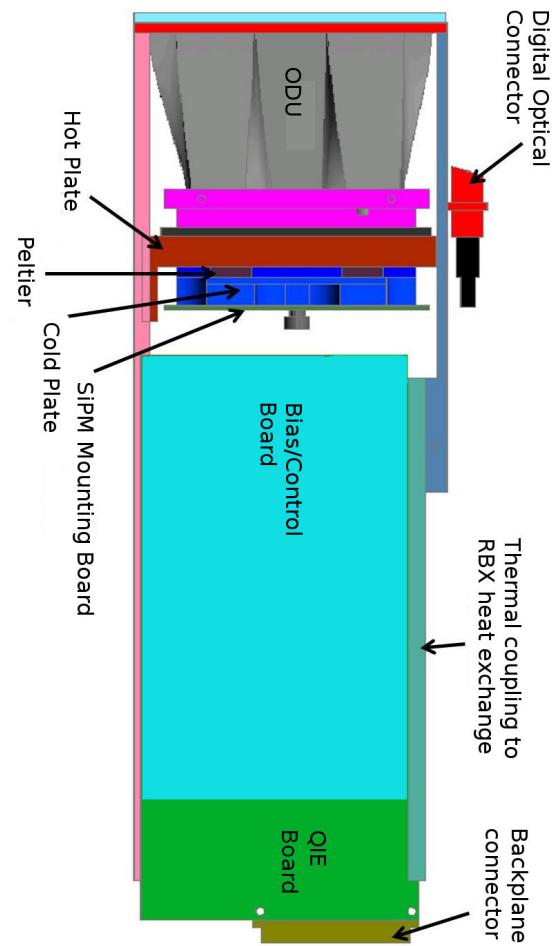


Figure 5.19: Side view (upper) and plan view (lower) of the design of the HB RM. In the lower view, location of the four QIE boards and the SiPM control board is shown. Note that three of the QIE boards connect to existing RBX backplane connectors. The fourth is a daughter board.

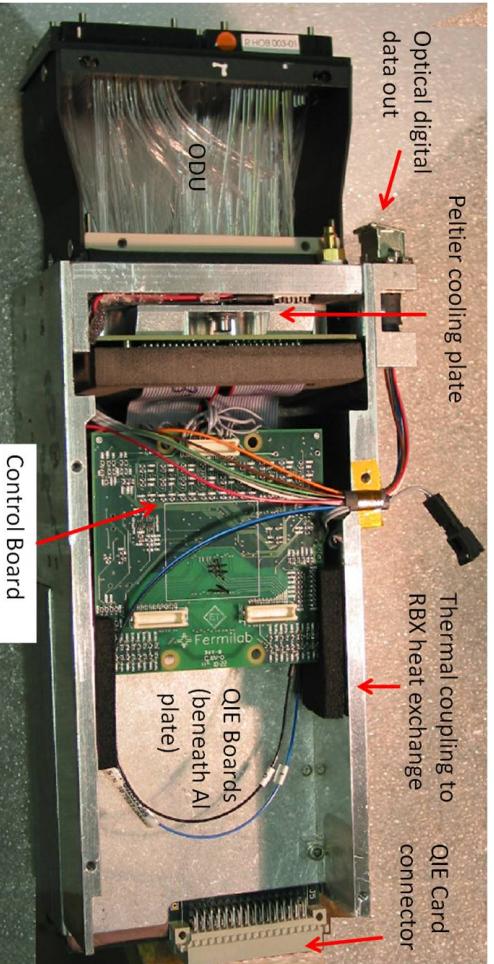


Figure 5.20: Photograph of a Prototype HB RM used at 2011 Testbeam. Besides being used for SiPM tests, the prototype was also used to explore mechanical issues. The SiPM control board for the final RM is envisioned to be full length.



(a) Detail of ODU. On the left optical connectors for cables from the calorimeter can be seen.

(b) Detail of ODU. The surface that mates to the SiPMs can be seen as well as alignment dowel pins.

Figure 5.21: The HB ODU. Optical cables attach to the ODU and the internal fibers are then routed to create calorimeter readout segments ($\eta/\phi/\text{depth}$).

5.4.1 Optical Decoder Unit

Connectorized optical cables carry light signals from the calorimeter scintillator tile layers to the ODU which is the front part of the RM. The optical cables are attached to connectors on the ODU. Fibers from each ODU connector location are routed to create calorimeter optical tower segments. These fiber bundles from each segment are then optically connected to the SiPM arrays. Each SiPM receives the light from one bundle. The detail of the ODU assembly, including the structure of the fiber interconnections, is shown in Fig. 5.21. The ODU technology was used very successfully in the original HPD-based HCAL readout.

5.4.2 SiPM Mounting Board

The SiPM arrays are placed in sockets on a SiPM Mounting Board in the RM. The SiPM power is distributed via the sockets. The board also has connectors to allow the passage of the SiPM signals to the QIE boards, to provide the bias voltages for the SiPMs as well as the output path for leakage current measurements. In the situation where multiple SiPMs are combined into a single readout channel, the electrical combination is performed on the SiPM mounting board before the signal is sent to the QIE.

5.4.3 SiPM Control Board

The SiPM control board has several functions. It supplies the bias voltages for the array of 64 SiPMs in the RM. Each has an independently settable bias voltage and an independently readable leakage current. The individual voltages and currents are accessed via I_C transactions from the backplane, connected to the control board over a jumper cable. The design and performance of these functions have been validated in the HO SiPM upgrade, which has similar requirements to the the HB/HE upgrade.

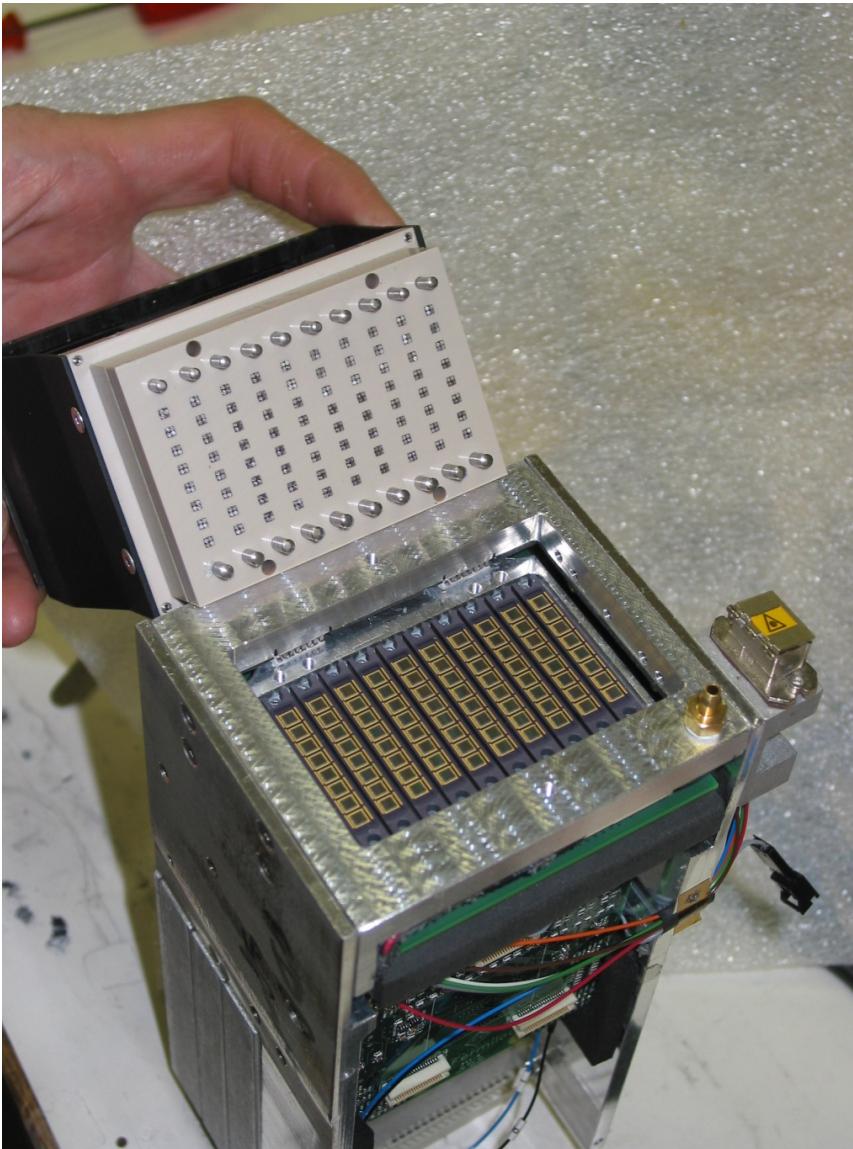


Figure 5.22: The prototype RM with the ODU separated from the rest of the mechanics. One can see the SiPM array and the fiber bundles that will optically mate to them. Alignment dowels are visible.

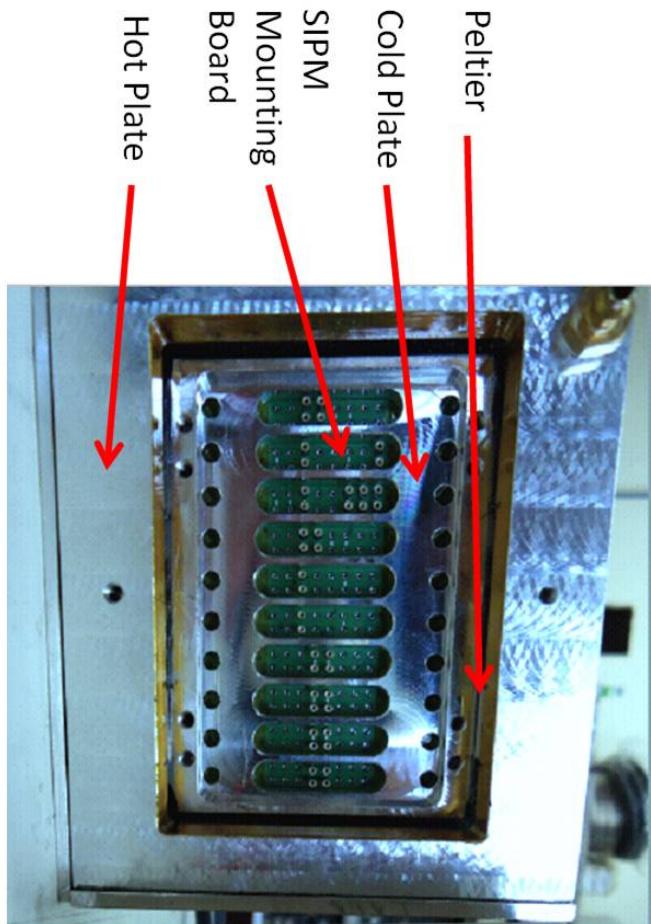


Figure 5.23: The structure of the SiPM cooling and SiPM Mounting board. The SiPM packages are not mounted but would insert into the sockets of the mounting board. One of the four Peltier coolers is seen.

The control board also supplies the voltages for the four Peltier-effect coolers. The Peltier cooler power supply can provide a maximum of 3 A at 5 V. There is a hardware under-temperature cutoff circuit to avoid temperature excursions below a set temperature which can be adjusted to the local dew point value. Accidental commands to the SiPM control board could cause the Peltiers to cool too much, with the resultant danger of condensation. The hardware limit cuts off current to the Peltiers when a local temperature measurement reads too low. This protection is done locally with no intervention required by the ngCCM or DSS systems. The control board also provides readout of the temperatures used for the Peltier control feedback loop.

Table 5.2 shows values of many of the SiPM control board parameters.

Table 5.2: SiPM Control Board Parameters

SiPM Control board parameter	
Bias Voltage (BV) Range	0–100 V
BV Setting Resolution	25 mV
BV Current Limit (per channel)	100 mA
Leakage Current Full Scale	40 mA
Leakage Current Least Count	10 nA
Temperature Resolution	0.018°C

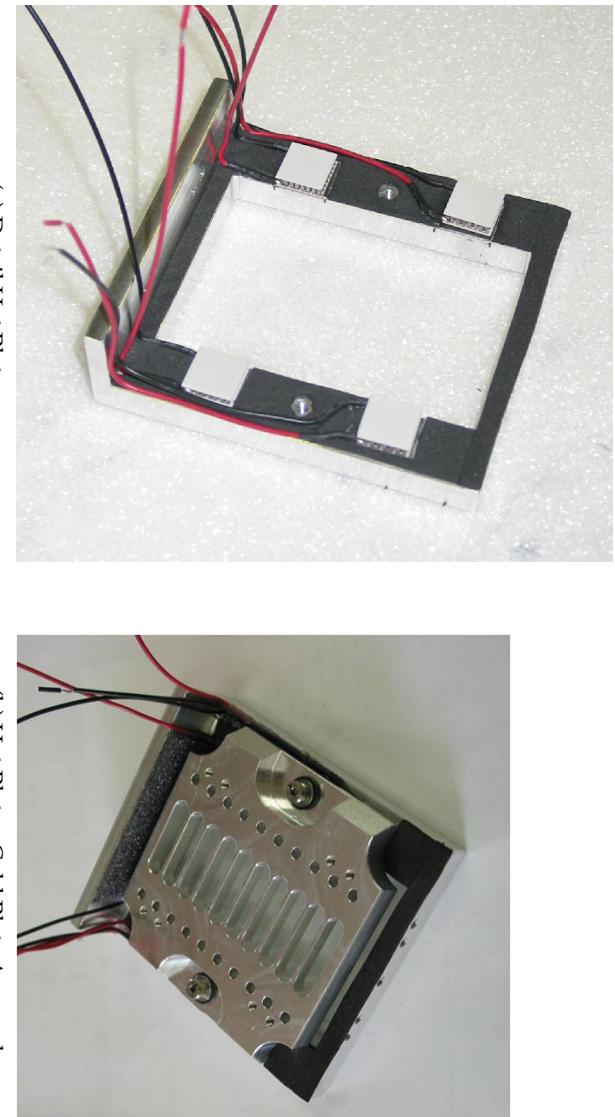


Figure 5.24: The Hot and Cold Plates for the Peltier Cooling System. Note the 4 Peltiers on the Hot Plate.

5.4.4 Peltier Cooling

The Peltier system is used to stabilize the temperature of the SiPMs and optionally to reduce it somewhat to limit the effect of single-pixel noise in neutron-damaged SiPMs. The Peltier cooling system consists of two plates and a set of four Peltier-effect devices. One plate, called the hot plate, is thermally coupled to the RBX cooling system which receives the heat from the Peltier devices. On the other side of the Peltiers is the cold plate which is thermally coupled to the SiPM mounting board. The Mounting board is also optically connected to the fibers from the ODU, a connection which does not have large thermal conductivity. Figure 5.24a and Fig. 5.24b show details of the Hot Plate and the Cold Plate. The Hot Plate has four Peltier-effect devices attached to it. The “foot” on its bottom of the picture is the thermal coupling to the RBX cooling system.

The Peltier set voltage determines the amount of power removed from the cold plate and hence the temperature. The control loop sequence is done via slow control software through the ngCCM. The local temperature is read out through the SiPM control board, and a correction voltage is calculated in the slow control software. The new correction voltage is downloaded into a SiPM control board register and a DAC generates Peltier voltages. We have found the system to be very stable, oscillating around one least count.

Figure 5.25 shows temperature stability for a similar control structure built into the HO calorimeter at P5. The blue curve shows temperature stability over a two hour period. The stability is about \pm one least count which is 0.018°C .

The maximum power that can be supplied to the Peltier system is 15 W. In a test setup, we found that 8 W total could be removed from the SiPM mounting board at the cost of running the Peltier system at the full 15 W. In this case the temperature drop between the outside and the SiPM mounting board was between 25 and 30 $^\circ\text{C}$. Most of the heat load onto the SiPM mounting board came from the ODU fibers.

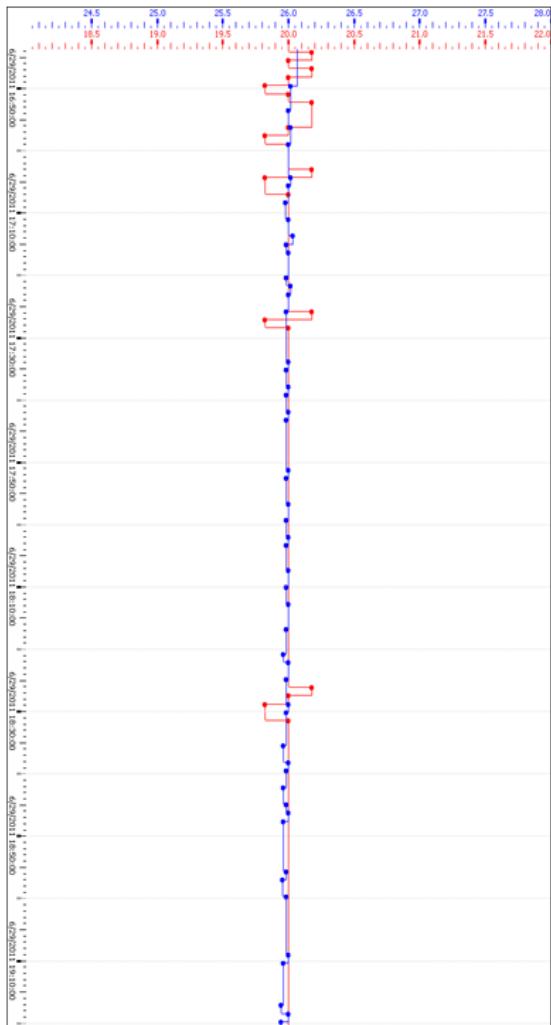


Figure 5.25: Readback temperature from the SiPM Mounting Board (HO System) over a 2 hour period. Note the stability is about one least count which is 0.018°C .

5.4.5 QIE Board

There are four QIE boards in each RM. Fig. 5.26 shows the overview of the QIE board. The board contains twelve channels of readout. Electrical signals from the SiPMs enter and are integrated by the array of twelve QIE10s (six on each side of the board), where TDC measurements are also performed. As discussed in Chapter 3, each QIE10 has a 2-bit rotating capacitor id (CapId) counter. All of these are sent to the FE-FPGA where they are checked for alignment, and reduced to a single CapId and error bits. The ADC, TDC, CapId, and error data are sequenced by the FE-FPGA into frames as shown in Table 5.3. While in the HF, a falling-edge TDC is provided by the FE-FPGA, this functionality is less-useful in the HB and HE where the pulse length is longer and less data bandwidth is available. The frames are transferred to the GBT where the data is serialized by the GBT that then sends the data to the Versatile Link [51], labelled VL in the Fig. 5.26. This VL contains a driver chip and a 850 nm laser diode that drives the serial optical data off detector to the counting house.

As discussed above, the individual CapId values for each QIE are not sent, but only a consensus CapId for the six QIEs on a link is sent along with a bit identifying if there was a mismatch between any of the QIEs. When a CapId mis-alignment is identified due to power up or SEU, it should be corrected during the next orbit gap when the QIE is reset. Should a QIE device fail such that it is not possible for the CapIds to match, that QIE will be masked in the FE-FPGA such that the disagreement of the remaining functional channels can be tracked.

5.5 Front-end Control module

As already discussed in this chapter, the architecture of the Upgrade FEE remains similar to the existing FEE. As a consequence, slow control and fast control will be handled by the new-generation Clock-and-Control Module (ngCCM) which must support the same set of backplane connections and core functions as the current CCM.

The ngCCM requirements are :

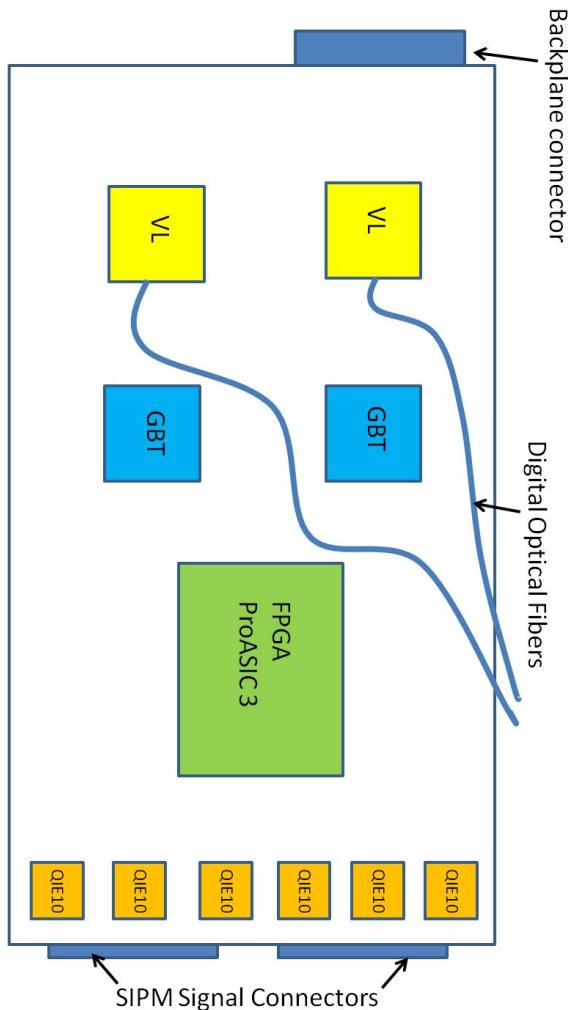


Figure 5.26: Conceptual Design of QIE Board. There are twelve QIE10 chips on the board, six on each side. Most other components are on the top. Voltage regulators and other support electronics not shown.

Table 5.3: GBT Link Data Format for the HB/HE Upgrade.

Byte	7	6	5	4	3	2	1	0
0					8b10b Comma Character			
1		TDC 0 [3:0]			CapId		CE	BC0
2					QIE ADC 0			
3					QIE ADC 1			
4					QIE ADC 2			
5					QIE ADC 3			
6					QIE ADC 4			
7					QIE ADC 5			
8					TDC 1			TDC 0 [5:4]
9		TDC 3[1:0]				TDC 2		TDC 3[5:2]
10			TDC 4[3:0]					
11				TDC 5				TDC 4[5:4]

- TDC – Rising-edge TDC produced within the QIE10
- CapId – Capacitor id for the capacitor used for this sample.
- CE – Indicates that the CapIds of all channels on the link are not the same.
- BC0 – Indicates that this sample is from the bunch with number zero in the orbit.
- Used for latency/phase alignment of the data links.

1. deliver a good quality clock (to be cleaned up again in the RM GBTX_S)
2. provide an orbit signal to the rest of the FE, to enable the marking of the data to maintain data synchronization. (QIEREST)
3. provide reset capabilities for the FE (RESET)
4. provide a warning-test-enable signal for calibration purposes
5. read out its own voltages and temperature
6. provide I2C communication for configuration of the GTBX, QIE10, and FE-FPGA chips
7. provide I2C communication for the bias voltage setting of the SiPMs and the Peltier control loop (including temperature monitoring)
8. improve the robustness of the system.

Except for requirement (7) which is unique to the SiPM-based system, the requirements for the HB/HE ngCCM are identical to those for the HF ngCCM and the same architecture discussed in Section 4.2.2 will be used and the same ngFEC described in Section 6.9 will be used for the counting-room component of the control system. For the HB/HE ngCCM realization however, the mechanical and electrical interface to the backplane must remain the same as on the existing HCAL.

An HB/HE ngCCM prototype Rev1 [61] has been designed and manufactured. Fig. 5.27 shows the four cards before the module assembly. The Rev1 prototype contains the full functionality of the final ngCCM except that it uses a Xilinx Virtex-5 FPGA and a commercial PLL as a GBTX emulator as the final GTBX is not yet available.



Figure 5.27: The four ngCCM Rev1 cards before the module assembly.

Using the prototype, the following functionalities have been tested successfully:

- local programming of the FPGAs
- stable operation of the 4.8 Gb/s GBT link
- transmission of fast commands from the ngFEC prototype to the RBX backplane with stable latency
- I2C cycles from the ngFEC prototype to an I2C target connected to the backplane
- remote programming of the ProASIC3 FPGA over the GBT link.

The Rev1 of ngCCM is not radiation-tolerant because some of the custom radiation-tolerant components (VTRx, GBTx, DC-DC converter) are not yet available. Once they become available, we will use them on the next ngCCM prototype. For other components (line drivers, multiplexers, etc) we use commercial components and will validate in system tests that they can tolerate the HCAL FEE radiation levels.

Returning to the robustness of the system, another challenge is transferring the heat from the hottest components to the RBX metal chassis. Water cooling is available on the RBX chassis, but does not reach the ngCCM enclosure. Cooling fans will not be used because of the magnetic field. We have studied how the PCB can transfer heat more efficiently and we have designed a solution in ngCCM Rev1. In this solution, the PCB has exposed metal around the edge of the board on the signal layers of the board (including on the top layer). The exposed metal of these layers is connected with a row of tightly spaced vias and transfers heat from the core of the board to the edge. The board should be mounted in contact with the exposed metal, in order to transfer the heat to the chassis. This solution may apply to both RM and ngCCM.

5.6 Calibration Module

Each RBX will also contain one calibration module. The calibration module contains an LED pulser for the SiPMs as well as a laser light distribution system. Fibers from the calibration module will connect to each of the interstitial microfibers in the light mixers, allowing LED or laser signals to be delivered to the SiPMs. The design of the LED pulser will be same as that used in the original HB/HE calibration module. The controls for the pulser, however, will significantly enhanced from those in the original calibration module. In particular, the calibration module will be able to use the CMS global Warning-Test-Enable signal to generate LED pulses during the LHC orbit gap. This will allow monitoring of the SiPM gain during CMS global operations. This capability was added relatively late to the current HCAL calibration and monitoring system and the LED pulser controls were not properly set up to allow the LED to fire for orbit-gap operations. The calibration module will also include PIN diodes for monitoring the light delivered, using the same QIE10+GBT readout chain which is used elsewhere in the detector electronics.

5.7 Powering

The existing RBX, with its four RMs and a CCM, consumes about 90 Watts, and the cooling pipes can remove up to 300 Watts per RBX. The upgrade RBX will process about 4 times as many data (3 times ADC data plus additional TDC data), but it is constrained to consume only 3 times the power of the existing RBX. The breakdown of the estimated power usage is given in Table 5.4. This estimate is based on a backplane voltage of 9 V, providing a good safety margin for the backplane capacitors with a maximum rating of 16 V.

One important area for consideration in saving power for the FEE design is in the provision of the low voltage power. Each RBX receives the power ("Low Voltage") via two cables (LV-cables). The resistance of the installed LV-cables and their corresponding return paths is about $0.2\ \Omega$ per LV-channel (0.1Ω for the two circuits together). The GBTx requires 1.5 V voltage, other GBT parts require 2.5 V. The QE10 requires most of its power at 3.3 V and a small contribution at 5 V. With such a range of voltages, linear regulators are not efficient and the DC-DC converters discussed in Section 3.4 are an effective solution.

A proper use of these DC-DC converters in HCAL requires careful studies of the margins be-

Table 5.4: Estimated power usage, assuming 192 channels and 32 data fibers per RBX. This estimate is based on an RBX backplane voltage of 9 V.

Component	per component [W]	per RBX [W]
QE10 (with TDC)	0.4	80
GBTX (as transmitters only)	0.7	22
Laser diode and laser	0.4	13.2
GBTX and VTRX (in the ngCCM)	1.7	1.7
ProASIC3 FPGA (in the RM + calibration module)	1.5	24
ngCCM redundancy link (FPGA, VTRX)	1	1
SiPM Control Card	5	20
Calibration module	1	10
Glue logic, clock distribution	-	5
Total before regulator efficiency	-	177
Voltage regulators (80%-efficient)	-	44
Peltier coolers (no regulator)	2	8
Total RBX power dissipation	-	229
Cable power loss (25A across 0.1Ω)	-	62
Total power at supply (11.5V)	-	291

tween their input voltage and their maximum absolute voltage (which is not known at this time). In order to transfer the maximum power while minimizing the current (i.e. minimizing the losses on the LV cables), we need to feed the DC-DC converters with a voltage close to the maximum (11V). On the other hand, we must avoid over-voltages, which can have destructive effects. Under the design in Table 5.4, at full current, the voltage drop in the LV-cables will be 1.2 V, so the output of the external power supplies must be ~10.2 V if we want 9 V on the backplane and at the DC-DC converter. The risk is that if an RBX reduces suddenly the absorbed current, its input voltage will rise to ~10.2 V and may damage the DC-DC converter depending on its final rated voltage. The current design is within the specifications, but we are considering reducing any risk using a combination of these ideas:

- reduce somewhat the maximum resistance of the LV-cable set, in order to reduce the voltage needed from the external power supplies;
- upgrade the protection circuitry ("LV Module" a.k.a. "LV box") already mounted in the rear side of the present RBXs or (as the LV Module is physically difficult to access) add protection circuitry elsewhere in the connection of the LV to the RBXes;
- reduce the operating voltage of the DC-DC converters, in order to reduce the voltage needed from the external power supplies, which is easy to implement, but reduces the advantage of DC-DC converters over linear regulators.

The first pre-production prototype of the DC-DC converter ASIC is expected to be delivered to CERN in August 2012. The mezzanine board has already been developed.

The existing external power supplies are CAEN A3016 modules which can deliver up to 8 V. To deliver higher voltages, we need to change the power supplies. We expect the replacement modules, which may be upgraded versions of existing designs, to fulfill the following requirements:

- Magnetic field and radiation tolerant [at least as CAEN A3050]
- Two Channels, individually controlled and protected
- No "Remote Sensing" input required

- VMax and IMax set by trimmer for each channel
- Interlock capability
- Screw Lock output connectors
- Power 300 W / channel
- Max Output voltage across the plus and minus connectors = 14 V.
- The module should be able to work at -2 V from ground.

5.8 Test Program

As with all CMS projects, the HB/HE front-end will go through the electronics design review (EDR) process before production begins. The EDR will review both the functionality of the electronics and its robustness including radiation tolerance. The QIE10, GBT, and FE-FPGA will be comprehensively validated by standalone tests as well as operation in the HF upgrade for a year before the HB/HE EDR. As a result, the tests will focus on the SiPMs and system tests.

The SiPM components have been the target of an extended series of bench and beam tests as discussed above. The final production candidate SiPMs will tested at the CERN IRRAD facility to the design criteria of $2 \times 10^{12} / \text{cm}^2$ neutrons and 10 kRad of ionizing dose. The SiPM components will be validated to meet the requirements of Table 5.1 after irradiation.

The primary system functionality test will be a testbeam evaluation of the electronics during October of 2015. The H2 beam test zone at the CERN North Area will be used for these tests. The tests will evaluate the behavior of the front-end with two fully-instrumented HB wedges and include an EB supermodule and readout of HO as well. The tests will validate the detector behavior for hadrons and muons and allow comparison of trigger and reconstruction algorithm performance between data and simulation. The possibility of 25 ns structured-beam tests will be discussed with the SPS run coordinators. The test will include the use of final pre-production ngCCM and readout electronics as well as the production back-end electronics.

In previous upgrade projects, significant benefits have been obtained from parasitic or test operation of a small prototype in the CMS environment. For the evaluation of the HB/HE readout modules, the HF platform provides an excellent environment. Access to HF is much simpler than access to the HB or HE readout boxes and there is sufficient space on the platform to install and cool a standard RBX. As shown in Table 1.1, the radiation levels in the HF FEE and the HE FEE are quite similar. The RBX will be populated by a full set of modules: four readout modules, a calibration module, and anngCCM. This test will validate the design of the module, the firmware of the FE-FPGA, the performance of the system under irradiation, and will also validate the necessary control and readout software and firmware in the back-end. This test is planned to occur during LHC operations in 2016 using the final design electronics.

The radiation tolerance of the full HB/HE system will be evaluated in tests at the CERN IRRAD facility. Each of individual components and the integrated system will have been validated previously for HF. However, it is important to carry out a full system radiation including the final FE-FPGA firmware. The tests will be performed with continuous readout, allowing the evaluation of single-event upsets as well as total dose effects. The test will include the HB RM, the HE RM, and the ngCCM.

5.9 Installation and Commissioning

The HB/HE electronics, while accessible during a long stop where CMS is opened, is generally inaccessible for years at a time. This mandates a strong burn-in and validation period for the electronics modules. This is a stronger requirement than for HF, where access is generally simpler and can be done during any beam stoppage of four hours or more. In HB or HE, a broken module is likely irreparable for two years or more. As a result, all upgrade RMs will undergo operation and burn-in for at least five months before detector installation in the Underground Service Cavern (USC). Delivery of the first third of the HB/HE RMs is expected at CERN by January 1 2017 to fill the testing pipeline.

To achieve the full set of tests at B904, it will be necessary to construct burn-in RBXes. These RBXes will be used only at CERN B904 for burn-in and must contain backplanes and allow cooling of the modules. The detailed mechanics are likely to be different than those of the true RBXes, as the same mechanical constraints will not apply. These tests will include pedestal, LED, and test-pulse runs as well as calibration of QIE10 ADC and TDC bin parameters. The testing program will also include determination of all SiPM bias-voltage/gain curves and the Peltier control parameters for each RM. All of measured parameters will be incorporated in the HCAL tables of the CMS Online Master Data Store (OMDS).

The installation process for the modules will require the following steps to be taken for each RBX:

1. Disconnection of the analog optical cables from the scintillator tiles from the RMs. These cables must be handled carefully as they become stiff from irradiation and time and cannot be flexed significantly.
2. Disconnection of all digital optical fibers and the control RJ45 cable from the CCM.
3. Removal of all modules from the RBX
4. Installation of the ngCCM and the new readout modules
5. Connection of the ngCCM to the ngFEC and to its neighbor
6. Connection of the digital data fibers from the RMs to the back-end electronics (uHTRs)
7. Connection of the analog optical cables from the scintillator tiles to the new RMs.

After the connection of the digital data fibers (step 5), but before the analog cables are connected, each box will be checked thoroughly with LED, laser, test-pulse, and pedestal runs. The ngCCM will be fully checked, including a test of the redundancy link with its neighbor. It may be necessary to install RBXes in pairs as a result of this requirement. The full test before re-connecting the analog optical cables allows any necessary intervention to be completed before reconnecting the fragile analog cables.

After the analog cables are connected, the system will be checked using the radioactive source system. The radioactive source system allows the insertion of a Co-60 source on the end of a wire into each layer of the calorimeter. This test is the only way to validate that the connections from each layer have been properly re-connected. All other tests will observe only sums of layers, leaving it uncertain if a single layer is misconnected.

The details of the installation schedule and process for the HB and HE RMs will be developed in concert with the CMS Technical Coordination group. In the case of the HB, careful planning will be necessary to complete the work without disturbing the dry insertion of the tracker.

Chapter 6

HCAL Back-end Electronics Upgrades

6.1 Requirements

The roles of the back-end electronics in the HCAL Upgrade follow the same structure as that used in the original electronics for the hadron calorimeter.

- Receive a continuous stream of ADC and TDC data from the front-ends over a set of optical links. For the upgraded front-end electronics, the raw optical data rate will be 4.8 Gbps.
- Calculate trigger primitives giving the energy in each projective cell of the calorimeter for a given bunch-crossing and containing information about the longitudinal distribution of that energy. This calculation requires the application of calibration data, pulse analysis, and summing over multiple depths or readouts of the detector. The trigger primitives are used by the calorimeter trigger system for clustering jets and determining isolation conditions for electrons and muons.
- Transmit the trigger primitives over optical fiber to the calorimeter trigger system, with clear marking of the data such that the data from a given bunch is always handled coherently across the system.
- Pipeline the ADC, TDC, and trigger primitive data for the full Level 1 trigger latency period. If the global CMS trigger generates a Level 1 Accept (L1A), then the appropriate data must be collected and forwarded to the central DAQ system.
- Receive and process not only the L1A signals, but also the LHC clock, orbit synchronization, and fast control signals. These are currently distributed by the fast control system (TTC), but support for planned upgrades of the TTC system must be provided.
- Besides support for global DAQ and the global calorimeter, maintenance and commissioning of the HCAL system require support for local DAQ and local triggering.
 - The local DAQ must be capable of 1 kHz readout of data to support testbeam operation. The local DAQ must also be capable of readout for source calibration operations, which may require up to 10 MBps readout bandwidth.
 - The local trigger support should be capable of generating triggers based on a single cell over threshold or a coincidence of up to four such cells.
- The CMS Luminosity measurement system uses the occupancy of the forward calorimeter as a measure of the LHC luminosity. This data is collected in the form of a set of histograms as a function of LHC bunch-number using Ethernet. The back-end electronics must support the continued acquisition of this data.

- To support the efficient phased installation of the Upgrade, the upgraded back-end electronics must also support the existing 1.6 Gbps data links, operating in a mixed system – including mixing on a single receiver card.
- The back-end electronics system should use modern components and techniques to simplify the maintenance of the system over its long expected functional lifetime.

6.2 The MicroTCA Standard and IPBus Protocol

To meet these requirements, the back-end electronics will utilize modern FPGAs and the μ TCA crate architecture. The μ TCA or MicroTCA standard [62] was developed by the telecommunications industry and is based on the Advanced Mezzanine Card (AMC) standard [63] which was part of the Advanced Telecommunications Architecture (ATCA) [64]. The ATCA standard specifies a crate of large carrier cards hosting multiple AMC cards each. In the simpler μ TCA architecture, AMC cards are plugged directly into a backplane. The μ TCA standard allows for up to twelve standard AMC cards in a crate. The μ TCA standard also includes one or two special “hub” slots in each crate. At least one of these slots must be occupied by a “MicroTCA Carrier Hub” (MCH) card which is responsible for the control of the power to each slot and for general house-keeping of the crate.

The μ TCA standard has explicit support for the hot-swapping of AMCs. When an AMC is inserted into the μ TCA crate, the MCH communicates via the I₂C protocol with a sub-component of the AMC called the Mezzanine Management Controller (MMC). After a successful negotiation, including the information that sufficient electrical power will be available, the 12 V payload power to the AMC is turned on by the MCH. The communication between the MCH and MMC is also used for monitoring voltages, currents, and temperatures on the AMC card. Additionally, low-level configuration of the card can be performed over this link, including providing the card with its crate identifier.

Besides the slow-control I₂C link, each MCH site has multiple high-speed serial pairs connecting to the AMC slots. One of these is used for a Gigabit Ethernet (GbE) link which is the primary communication path for configuration and monitoring in a μ TCA crate. Several connections are used for the distribution of clock signals in the crate, and each MCH site has at least four bidirectional high-speed serial connections to each AMC slot. In the μ TCA standard, the protocol to be used on these additional ports is a user-specified condition.

Table 6.1: Port assignments under the CMS common μ TCA specification.

AMC Port	Fabric	MCH	Purpose
0	A	Primary	Gigabit ethernet
1	A	Secondary	Data acquisition
2	B	Primary	(Spare)
3	B	Secondary	Fast controls/TTC
TCLKA	CLK1/2	Primary	(Spare)
FCLKA	CLK1/2	Secondary	LHC Clock

The CMS Upgrade Working Group has defined a minimal set of connections to be used in CMS electronics to support the common functionalities needed in any CMS μ TCA crate. The Working Group specifies a μ TCA crate with two MCH sites and up to twelve AMC slots. The primary MCH site is to be used for a commercial MCH card responsible for crate management and the Ethernet network. The secondary site is to be used for a CMS-common card which will be responsible for clock and fast control distribution as well as local and global DAQ. To

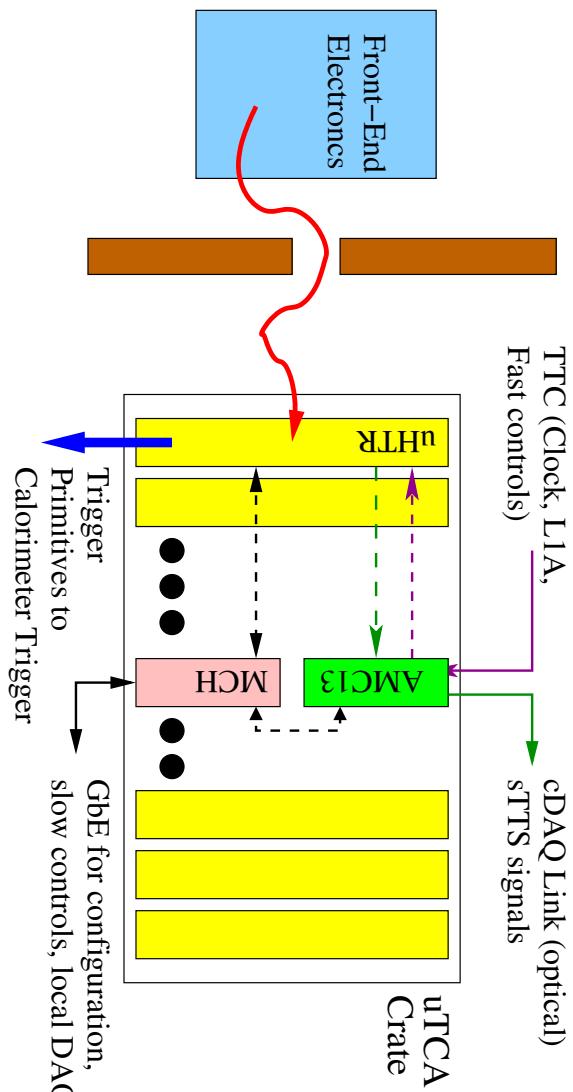


Figure 6.1: Crate layout structure of the μ TCA-based back-end electronics, showing the data links from the front-end electronics to the uHTRs, the connections from the uHTR cards to the calorimeter trigger, and the fast control and DAQ connections which connect to the AMC13 and use the μ TCA backplane.

support these functionalities, the CMS Upgrade Working Group defines the port usage for a standard CMS AMC given in Table 6.1.

The μ TCA standard does not specify any details of the communication between a control PC and an AMC beyond the low-level transport specification of gigabit Ethernet. The CMS Upgrade Working Group has adopted a standard protocol called “IPBus” to provide a uniform solution for communication across all CMS upgrades which will use μ TCA. The protocol defines a virtual A32/D32 bus on each Ethernet target and allows the programmer to pack multiple read, write, bit-set, and bit-clear operations into a single Ethernet packet. The base protocol uses the User Datagram Protocol (UDP) over the Internet Protocol (IP). The use of UDP rather than bare Ethernet allows development of control code with no specialized drivers or enhanced machine access – standard user accounts and interfaces can be used for all purposes. The use of UDP/IP instead of TCP/IP greatly reduces the complexity of the implementation in the FPGA firmware of the AMC. Reliable delivery is ensured by a software server layer which manages multiple parallel requests for the same resources across multiple clients. The IPBus protocol and firmware module are supported by the Bristol University group.

6.3 Back-end Architecture

The HCAL upgrade back-end electronics use the μ TCA standard as adopted by the CMS Upgrade Working Group, including the port usage specified in Table 6.1 and the IPBus communication protocol. The structure of a single crate is shown in Fig. 6.1. Each crate will typically include twelve μ TCA HCAL Trigger/Readout (uHTR) cards. These cards are responsible for receiving the data links from the front-ends, calculating and transmitting trigger primitives, and holding the Level 1 readout pipeline. Each crate will contain one AMC13 card which will occupy the secondary MCH site and which will be responsible for data acquisition as well as distribution of the LHC clock and fast control signals.

The HCAL Upgrade back-end electronics will use Vadatech crates which provide a backplane compatible with Table 6.1. These crates will include commercial power modules which convert the incoming bulk -48 V DC power into 12 V DC for each slot. The bulk -48 V DC power will be provided from the AC mains at a rack level by a CMS-standard solution. A commercial MCH which meets CMS DCS requirements will be included in each crate, potentially either the NATNAT-MCH-Base12-GbE or the Vadatech UTC002-210-000-300. Three μ TCA crates will be required for the HF upgrade and nine for the HB/HE upgrade, three for each of the three partitions which the HB/HE readout and electronics are divided into as listed in Table 6.2.

Table 6.2: HCAL partitions

Partition	BE crates	FE crates / RBXs	Notes
HBHEa	3	24	120-degree sector
HBHEb	3	24	120-degree sector
HBHEc	3	24	120-degree sector
HF	3	12	No upgrade of the electronics planned in this
HO	4	36	upgrade phase

6.4 Optical Splitters and Optical Receivers

For the commissioning of the calorimeter trigger, it is important to be able to operate the upgrade backend electronics for the HB and HE in parallel with the existing VME electronics for some time. This would occur before the installation of the HB/HE front-ends, and can be achieved by splitting the incoming 1.6 Gbps optical stream using 50:50 passive optical splitters. A prototype optical splitter was installed during the 2011/2012 YETS period to split a $\Delta\phi = 40^\circ$ region of HB-, HE-, and HF-, a total of 124 fibers carrying 372 channels of data. These splitter units can be installed in replacement of an existing optical patch panel which is located at the bottom of each rack of HCAL electronics. The optical splitting process typically reduces the optical power to a receiver by 5 to 7 dB compared to the arrangement without the optical splitter.

The optical components chosen to receive the links from the FE must be able to work reliably at 4.8 Gbps and 1.6 Gbps and to operate reliably with both the current Honeywell VCSEL laser diode and the laser diode identified by the Versatile Link project for the upgrade. Additionally, the link must work stably at 5 Gbps over the existing multimode 50/120 μ m graded-index optical fiber plant. The Avago AFBR-820BEPZ PPOD optical receiver has been tested by the Versatile Link project and has found to have excellent characteristics as shown in Fig. 6.3. The link behavior continues to be excellent even in the presence 100 meters of optical cable and multiple couplers. This optical sensitivity is sufficient for both the operation at 1.6 Gbps and 5 Gbps both with and without optical splitters.

The performance of these components has also been validated experimentally in tests performed with the 124 optical links at in-situ in USC which contains the CMS off-detector electronics. In these tests, described in more detail below, the optically-split signal from the detector was successfully received by a PPOD for all fibers in the test, giving a good confidence in the performance of the receiver including its performance when used with the optical splitter.

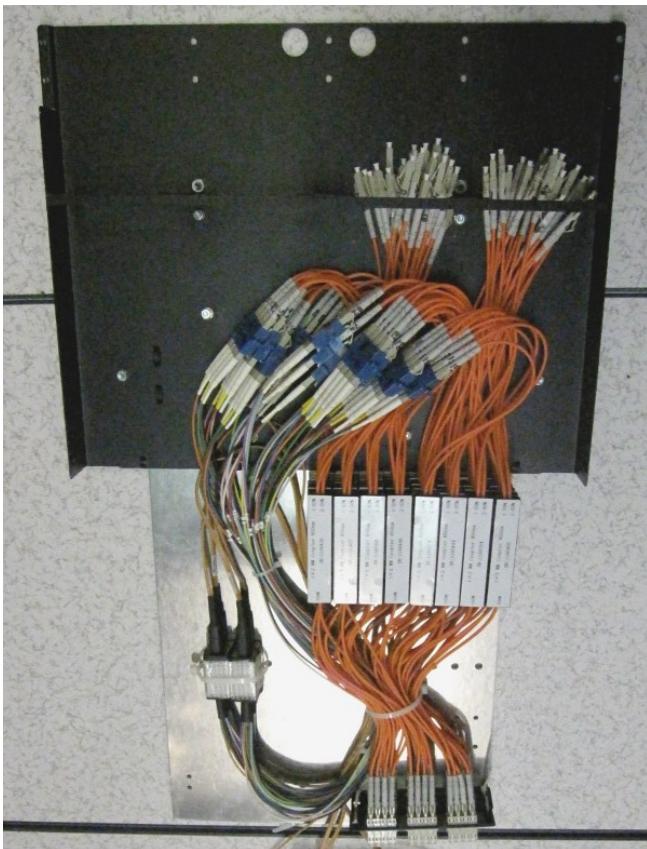


Figure 6.2: Passive optical splitter prototype which was installed in USC during YETS 2011/2012. The rectangular modules in the center of the image are the splitter units.

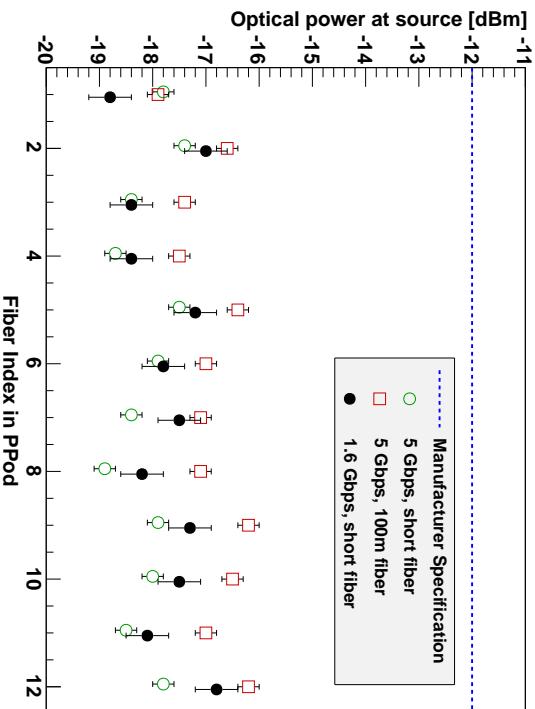


Figure 6.3: Optical power level at transmitter for error-free operation ($\text{BER} < 10^{-12}$) for PPOD parallel optical receivers at 5 Gbps and 1.6 Gbps and including the effect of 100 m of multimode optical fiber.

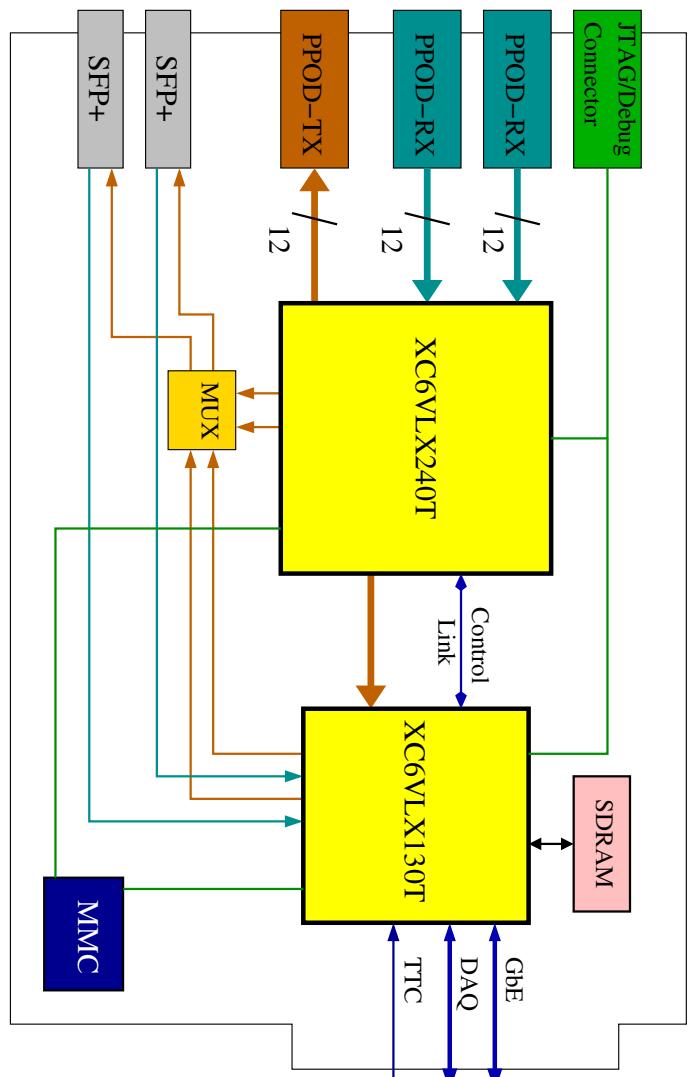


Figure 6.4: Block diagram for the structure of the uHTTR card showing the connectivity of the high speed links to the front and back FPGAs as well as the MMC and SDRAM.

6.5 uHTTR Design

The block diagram for the uHTTR card is shown in Fig. 6.4.

The uHTTR card will receive data from the front-end electronics using PPOD-type parallel optical receivers. These receivers accept twelve fibers each and are capable of operating up to 10 Gbps. The serial electrical signals from these receivers are de-serialized and processed using RocketIO logic in a Xilinx Virtex 6-series FPGA. The uHTTR contains two Virtex 6 FPGAs. The FPGA which connects directly to the front-end links is called the *front FPGA*, while the FPGA which connects directly to the DAQ and control links is called the *back FPGA*. Two FPGAs are used rather than a single larger FPGA as the cost increment for an FPGA with more than 24 RocketIO blocks is very large. The front FPGA also connects directly to a PPOD parallel optical transmitter for transmission of trigger primitives to the calorimeter trigger system. There are two SFP+ transceiver sites on the uHTTR. The transmitter on these sites can be driven by either the front or back FPGA, as determined by a multiplexer setting. The receiver connections come to the back FPGA only as the front FPGA has no available receivers.

The front FPGA is responsible for synchronizing the data from all links, calculating and transmitting the trigger primitives, and holding the data pipeline while waiting for the Level 1 decision. Once a Level 1 decision is issued, the front FPGA transmits all the samples associated with the event to the back FPGA. The data link from the front to the back FPGA is implemented using unidirectional RocketIO links, providing a large bandwidth. The back FPGA is responsible for buffering the data and performing zero-suppression. The zero-suppression may involve the use of selective readout masks produced using information from both the CMS ECAL and HCAL. The use of selective readout techniques would allow the optimization of the available DAQ bandwidth for focussing on regions of interest defined by the ECAL or HCAL or even by the muon system. To allow for the latency of a selective readout scheme, the back FPGA

is provided with an SDRAM buffer to store samples for a minimum of 100 milliseconds at full DAQ rate rate, which requires 64 MB.

The SFP+ inputs will be used to collect data from the calibration modules directly into the back FPGA. Each calibration module in the system will send a single fiber of data to the DAQ. This information is not used in the trigger calculations and thus is not needed to be connected to the front FPGA. The second SFP+ input will be available for other possible developments.

As shown in Fig.6.4, the Port 0 GbE is directly connected only to the back FPGA. The Ethernet is bridged into the front FPGA using the built-in ISERDES/OSERDES components. The bridging functions similarly to a classic Ethernet hub. This allows direct IPbus access to both front and back FPGAs.

The interconnection between the uHTTR and the AMC13 is defined by a set of firmware module interfaces. The implementation of the modules is provided by the AMC13 group for both ends of the interconnect. This design methodology has allowed for rapid development of relatively complex interconnects. The two main firmware blocks are the fast-controls interface and the local trigger/local DAQ interface. The fast-controls interface brings the orbit signal and other TTC fast control signals from the AMC13 to the uHTTR. The ports of this interface are given in Table 6.3. The local trigger /local DAQ interface encapsulates the Port 1 DAQ link and provides a path for bunch-synchronized local trigger data and the primary DAQ data to leave the uHTTR. The ports of this interface are given in Table 6.4. As can be seen from the interface, the local trigger path carries eight bits whose purpose can be defined by the firmwares in the uHTTR and AMC13. These local trigger bits are distinct from the full trigger primitive information sent to the calorimeter trigger and are useful for testbeam and teststand operation as well as allowing a technical trigger on anomalous conditions such as gathering events with very long pulses as measured by the TDC.

Table 6.3: Firmware interface ports for the fast-controls/TTC interface from the AMC13 to the uHTTRs.

Port	Direction	Width	Functionality
TTCdata	in	Differential	TTC data stream from Port 3
TTCready	out	1	Valid TTC data is being received
L1Accept	out	1	Level 1 Accept signal
BCntRes	out	1	Bunch-Count-Reset signal
EvCntrRes	out	1	Event-Count-Reset signal
SinErrStr	out	1	Single-Bit Hamming error identified/corrected
DbErrStr	out	1	Double-Bit Hamming error identified
BrcstStr	out	1	Broadcast message strobe
Brcst	out	6	Broadcast message (bits [7:2])

6.6 Trigger Primitive Generation

The trigger calculation is performed in the front FPGA. The calculation requires the application of a linearization and calibration lookup table which corrects for the non-linear scale of the QIE10 and the gain of an individual channel. Multiple channels may be summed and the amplitude from each channel may be passed through a filter, as discussed below in the case of HB/HE. The final amplitude measurement is then sent to the trigger along with feature bits which characterize the energy distribution among the summed channels and the TDC information. These steps are all performed in the front FPGA and the result is sent to the calorimeter

Table 6.4: Primary firmware interface ports for the local trigger and DAQ functionalities between the AMC13 and the uHTTR. The technical ports related to RocketIO management are not shown.

Port	Direction	Width	Functionality
reset	in	1	Reset the interface/link logic
TTCClk	in	1	Clock for the bunch-synchronized data
BC0	in	1	Signal which indicates when the trigger data associated with LHC bunch zero is at the input of the module
t_trig	in	8	Eight bits of local trigger data which is sent to the AMC13
TTS	in	4	Trigger-Throttling System inputs
dataClk	in	1	Clock for the DAQ data (not LHC clock)
data_valid	in	1	Data valid valid input signal
data_header	in	1	Marks the first data word of an event payload
data_trailer	in	1	Marks the last data word of an event payload
data	in	16	Sixteen-bit-wide data payload
AlmostFull	out	1	Output from the interface indicating that the link is nearly full and that the uHTTR should pause sending data
Ready	out	1	Output from the interface indicating that the link is up and ready for operation

trigger electronics via the PPOD and/or the SFP+ optical links. The trigger primitives are also retained in the Level 1 pipeline and included in the DAQ output if a Level 1 Accept is generated.

One of the main advantages of the combined HCAL and calorimeter trigger upgrades is the ability to allow clustering and jet finding over uniform-sized objects over the whole detector, as detailed in Table 6.5. The current trigger regions in the Regional Calorimeter Trigger (RCT), which are constructed from 4×4 trigger primitives in ECAL and HCAL in the central portion of the detector, are not uniformly sized outside the $|\eta| < 1.74$ central portion, which can lead to anomalous jet rates and challenges in jet finding. After the combined upgrades, the calorimeter trigger will be able to operate with uniform $\Delta\eta \times \Delta\phi = 0.174 \times 0.174$ cluster object inputs. Achieving uniform clustering inputs requires increasing the bandwidth for trigger primitives for HF and making small adjustments in HE which are discussed below.

Table 6.5: Calorimeter region/cluster size ($\Delta\eta \times \Delta\phi$) comparison between current HCAL+RCT and upgrade HCAL+calorimeter trigger showing the uniform cluster size in the upgraded trigger. In a small portion of the endcap, the geometry of the scintillator tiles means the cluster size will be slightly larger in $\Delta\eta$, which is expected to have negligible effect.

$ \eta $	Current HCAL+RCT	Upgrade HCAL+CT
0-1.74	$0.348 \times 0.348 (4 \times 4)$	$0.174 \times 0.174 (2 \times 2)$
1.74-2.17	$0.432 \times 0.348 (4 \times 2)$	$0.210 \times 0.174 (2 \times 2)$
2.17-3.00	$0.828 \times 0.348 (4 \times 2)$	$0.174 \times 0.174 (1 \times 2)$
3.00-5.00	$0.522 \times 0.348 (3 \times 2)$	$0.174 \times 0.174 (1 \times 1)$

Table 6.6: Trigger link data format for the upgraded HF trigger primitives.

Byte	7	6	5	4	3	2	1	0
0								8b10b K-Character/BC0
1								TP Tower 30
2								TP Tower 31
3								TP Tower 32
4								TP Tower 33
5								TP Tower 34
6								TP Tower 35
7								TP Tower 36
8								TP Tower 37
9								TP Tower 38
10								TP Tower 39
11								TP Tower 40/41
12	FB Tower 33		FB Tower 32		FB Tower 31			FB Tower 30
13	FB Tower 37		FB Tower 36		FB Tower 35			FB Tower 34
14	Reserved (0)		FB Tower 40/41		FB Tower 39			FB Tower 38
15						CRC-8-CCITT		

- TP – Compressed transverse energy for the tower
- FB – Feature bits for the tower (two bits / tower)
- 8b10b K-Character/BC0 – the K-character is either K28.3 (for the first bunch of an orbit) or K28.5 (for all other bunches)

6.6.1 HF Trigger Primitives

For HF, the μ TCA electronics is expected to operate with both the existing RCT trigger and the upgraded calorimeter trigger simultaneously. Each uHTTR will be connected to a single $\Delta\phi = 20^\circ$ wedge of either HF+ or HF-. For the existing RCT trigger, the uHTTR is responsible for calculating region energy sums which cover $\Delta\eta \times \Delta\phi = 0.52 \times 0.35$. With single-anode PMTs, this corresponds to a sum over twelve channels, six long-fiber channels and six short-fiber channel. The regions are indicated by colored areas in Fig. 6.5. These trigger primitives require only a single fiber link per uHTTR and would be transmitted over one of the SFP+ connectors. The link would carry four region sums and would use a format to be specified by the RCT group. The fast response of the HF means that no summing of signals over multiple crossings is appropriate – all calculations are based on the readings of a single bunch-crossing.

For the HF link to the upgraded trigger, the data will be transferred over two fibers per uHTTR at 6.4 Gbps using 8b10b encoding. The link will thus carry sixteen bytes from the uHTTR to the calorimeter trigger for every bunch crossing. The expected format for this data is shown in Table 6.6. The first byte of each 16-byte packet will be an 8b10b control character. For the packet associated with the first bunch of an orbit, the character K28.3 will be used. For all other bunches, the character K28.5 (the Ethernet ‘comma’ character) will be used. The comma character is required to be present in the data stream to align the optical link deserializer engine. The last byte of each packet will be an eight-bit CRC using the CCITT CRC generator which will validate the successful transmission of the data packet.

The fourteen bytes left in each link packet after the control character and CRC will carry the data for eleven physical towers. The response from tower $i\eta = 29$, which serves for shower containment, will be added to $i\eta = 30$. Each link will carry the trigger primitives from a single

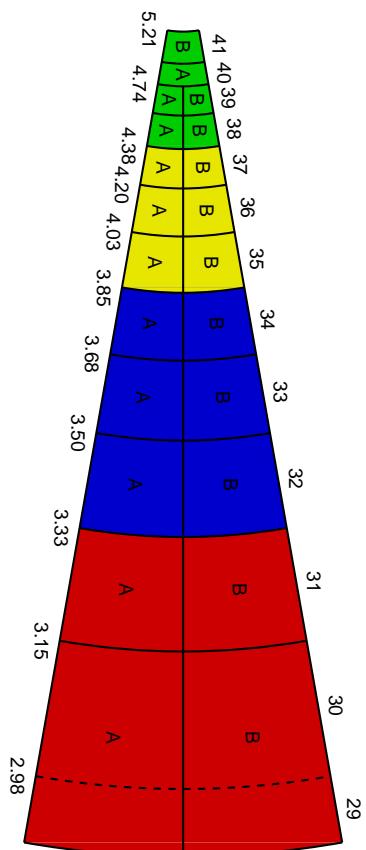


Figure 6.5: Trigger tower arrangement for a single 20° wedge of HF. Each wedge is connected to a single uHTR. The colored areas indicate the RCT trigger regions while the letters indicate the towers carried on each of the two links to future upgraded calorimeter.

$i\phi$ slice from $|i\eta| = 30$ through $|i\eta| = 39$ and one of the two double-width towers $i\eta = 40$ and $i\eta = 41$. This arrangement is shown in Fig.6.5 with ‘A’ and ‘B’ indicating the two fibers sent from each uHTR. Each trigger primitive will consist of an eight-bit E_T value determined from the combination of the long and short fiber energy for the tower and two feature bits. The E_T may be compressed to a non-linear scale by a lookup table which can be undone at the trigger to allow for a broader dynamic range while retaining the ability to distinguish small signals. One of the feature bits will indicate if the distribution of energy in the tower between the long and short fibers is consistent with an electron. The second feature bit will indicate energy deposits which are out-of-time with respect to the collision, as determined by the TDC measurements.

The EM feature bit and the full-granularity tower data will be available to an upgraded calorimeter trigger as soon as the HF back-end upgrade is complete – the installation of the upgraded front-end is not required. The upgrade of the front-end will bring in the TDC feature bit and new handles for identifying and recovering or suppressing anomalous noise signals at the trigger level. In particular, the TDC readings and the energy distributions between the various readouts will allow the identification of anomalous hits. If the anomalous hit affects only one of two anodes for a channel, the response from the ‘clean’ channel will be doubled and sent for the total energy response of the tower, with only a minimal loss of resolution. If the anomalous signal affects both anodes, as determined from the TDCs, the tower energy will be zeroed in the uHTR. If a trigger on out-of-time energy is defined, the uHTR can instead pass the energy and use the TDC-out-of-time feature bit to identify the situation.

As each uHTR has twelve fiber links available for transmitting trigger data, there is also significant scope for expansion if required in the future. The resources in the HF front FPGAs are sufficient for implementation of the full baseline functionality with less than 40% resource utilization.

6.6.2 HB/HE Trigger Primitives

In the case of the HB/HE, each trigger link is expected to carry data for eight trigger towers, which matches the number of channels carried on an RCT SLB cable. The current baseline for the trigger upgrade envisions operation at 4.8 Gbps using the format shown in Table 6.7. In this format, each trigger tower has a eight-bit energy field and two feature bits. If the trigger link is run at 6.4 Gbps, each trigger tower could have up to six feature bits or additional bits of

Table 6.7: Trigger link data format for 4.8 Gbps transmission of the HB/HE trigger primitives.

Byte	7	6	5	4	3	2	1	0
0								8b10b K-Character/BC0
1								TP Tower 1
2								TP Tower 2
3								TP Tower 3
4								TP Tower 4
5								TP Tower 5
6								TP Tower 6
7								TP Tower 7
8								TP Tower 8
9	FB Tower 4		FB Tower 3		FB Tower 2		FB Tower 1	
10	FB Tower 8		FB Tower 7		FB Tower 6		FB Tower 5	
11					CRC-8-CCITT			
15					CRC-8-CCITT			

- TP – Compressed transverse energy for the tower
- FB – Feature bits for the tower (two bits/tower)
- 8b10b K-Character/BC0 – the K-character is either K28.3 (for the first bunch of an orbit) or K28.5 (for all other bunches)

energy dynamic range.

In the case of HB/HE, the calorimeter pulse shape extends over multiple 25 ns bunch-crossings. To obtain a proper estimate of the signal amplitude for a given bunch-crossing, an FIR filter will be applied. The coefficients of the filter will be adjusted to maximize the accuracy of the energy reconstruction and minimize the effects of out-of-time pileup. These coefficients will be determined specifically and separately for the cases of operation with HPDs and the QIE8 and for SiPMs and the QIE10. The rising edge TDC will also be useful in identifying the appropriate bunch crossing for energy deposits and a peak-detection algorithm can be used when necessary to identify the appropriate bunch-crossing for the energy to be sent to the trigger.

There are several possible feature bit algorithms which could be of use. As pileup energy depositions are primarily in the first layer or two, as shown in Section 2.1, lepton isolation can potentially be most usefully defined using the deeper depths of the calorimeter. For electrons, one feature bit might mark cases where the energy is almost all in the first layer, allowing this energy to be ignored for isolation sums. For muon, an algorithm would identify situations where the energy in the deep depths of the calorimeter are compatible with a single isolated muon – such a feature bit would be useful within the muon trigger. For calibration of the detector, it would be useful to mark towers with a MIP energy deposit in the first layer to identify isolated tracks for calibration purposes. Feature bits could also be used for marking hits with early or late times as determined by the TDC. These hits could be ignored or focused on for triggers searching for slow particles or asynchronous decays.

The mapping of trigger data links to HB/HE cards is expected to match the mapping of RCT-SLB cables in the current system, so each HTR card will have either six or four fibers used for the trigger data – six in the case of uHTRs which receive data only from HB and four for uHTRs which receive data from HE only or the HB/HE overlap region. The number of trigger links per uHTR is smaller in the HE as the number of readout depths per tower is larger. Also in this region, the $\Delta\phi$ size of the towers increases from 5° to 10° . In the highest η region of the HE,

HCAL towers $i\eta = 28$ and $i\eta = 29$ are summed into a single $i\eta_{\text{trig}} = 28$ trigger tower. This tower is quite large ($\Delta\eta = 0.35$) and has a very atypical energy response, as seen very clearly in heavy ion collisions. In the upgrade, the $i\eta = 28$ and $i\eta = 29$ would be sent separately to the trigger, improving further the energy-density uniformity in this η region which is crucial for Higgs tagging jets.

As each PPOD has twelve output drivers, more information could be sent into the trigger system. For example, information relevant to the muon trigger could be packaged onto a single fiber per uHTR and sent directly into the muon trigger without requiring processing by the calorimeter trigger. This would preserve feature bits which are relevant for calorimeter trigger purposes.

6.7 HF Luminosity

The calculations for the HF luminosity determination will be split between the two FPGAs. The front FPGA will calculate the numbers of long-fiber cells over threshold and the total transverse energy observed during each bunch crossing. These calculations will be performed with a subset of HF towers, currently defined as $3.3 < |\eta| < 4.1$, to avoid any effects near the edges of the calorimeter. The front FPGA will transmit this information to the back FPGA via a unidirectional 3.6 gigabit copper link. The back FPGA then creates a set of histograms to collect the occupancy and total E_T as a function of LHC bunch number. At the end of each integration cycle, the histograms will be moved into a storage buffer from which the Lumi DAQ will read them via the IPBus.

The firmware and software for the uHTR will be designed to allow separate operation of the luminosity path and the trigger/DAQ path. The two data paths will be coupled only at the alignment of the data from the front-ends which will be reset only when required by clock changes or other effects. The luminosity system will have its own set of calibration lookup tables (LUTs) and the software stack will be designed to allow separate xDAQ applications and RCMs controllers to be responsible for the luminosity and trigger/DAQ activities of the uHTR. This separation will provide maximum flexibility for both systems, allowing the luminosity system to have the largest possible uptime while also granting operational simplicity for the trigger/DAQ operations.

6.8 AMC13 Design

The AMC13 provides TTC, TTS and DAQ functions for a MicroTCA crate in CMS. It mounts in the secondary MCH site of the MicroTCA crate (see Fig. 6.1) which provides point-to-point connections to each of the 12 AMC modules in the crate. The AMC13 is a module with the form factor of an MCH but is treated by the primary MCH as a “13th AMC”, thus the name AMC13.

A block diagram for the AMC13 card is shown in Fig. 6.6. The AMC13 is implemented as a 3-board PCB stack. The T1 (Tongue 1) board provides the high-speed serial links for GbE, backplane and front-panel DAQ interfaces. The T2 (Tongue 2) board contains the MMC, clock and TTC functions.

MMC: The AMC13 uses an MMC implemented in an AVR-32 microcontroller with custom firmware providing standard MMC functions plus enhancements. The MMC is directly connected via several GPIO lines as well as an SPI (Serial Peripheral Interface) bus to the FPGA on the T2 board.

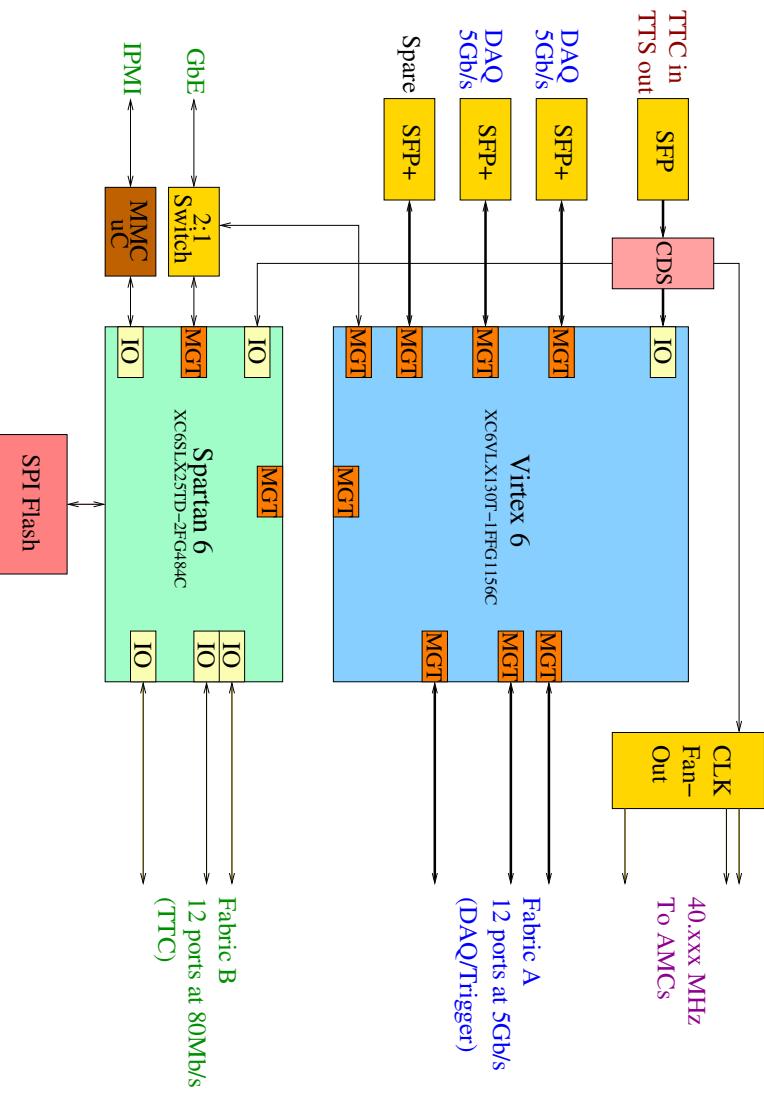


Figure 6.6: Block diagram for the structure of the AMC13 card showing the main data paths. Note that the circuitry shown is contained on two separate PC boards (T1 and T2).

Clock/TTC: The AMC13 is designed to receive TTC data on a fiber using the LHC standard 160 MHz biphase-mark encoding scheme used throughout the TTC system. The AMC13 does not use a TTCrx ASIC, but a novel design based on an ADN2814 clock/data recovery IC. This chip provides a 160 MHz recovered clock along with the 80 Mb/s encoded TTC data stream. A simple decoder implemented in the Spartan-6 FPGA acquires bit alignment of the data stream, and resets an SY89872 clock divider, which provides a 40 MHz low-jitter clock. The TTC data stream is re-timed to align with the clock, and delivered to the AMC modules in the crate over the MicroTCA Fabric B connections using DC-coupled LVDS signalling. A block diagram of the clock logic is shown in Fig. 6.8.

Trigger and DAQ

The AMC13 provides both a fixed-latency trigger path (level 1), and a pipelined readout path (level 2) multiplexed on the Fabric A MicroTCA backplane path. The VHDL ports provided in the reference design at the AMC end are outlined in Table 6.4.

The level 1 path delivers up to eight bits of fixed-latency data on each bunch crossing from each AMC to the AMC13. The AMC13 may perform local trigger processing on these data, and can provide a local trigger on the low-speed front panel fiber output for test purposes. This path is not intended for use in delivering trigger primitives to the standard CMS level 1 trigger system.

The TTS inputs are used to request a change of state in the TTS outputs from the AMC13 to

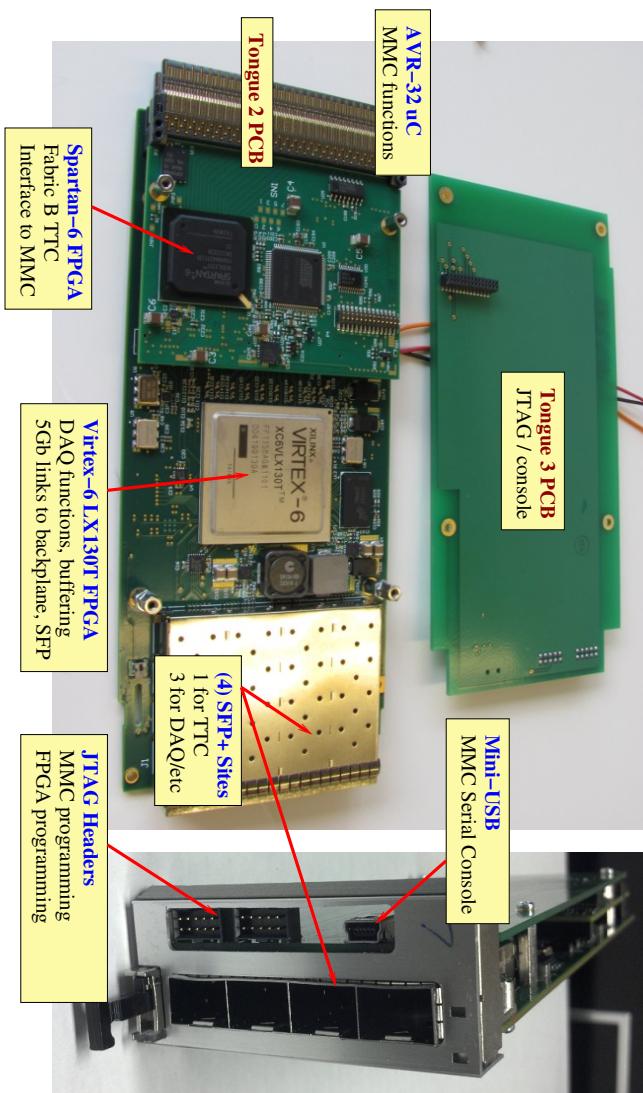


Figure 6.7: AMC13 Photograph

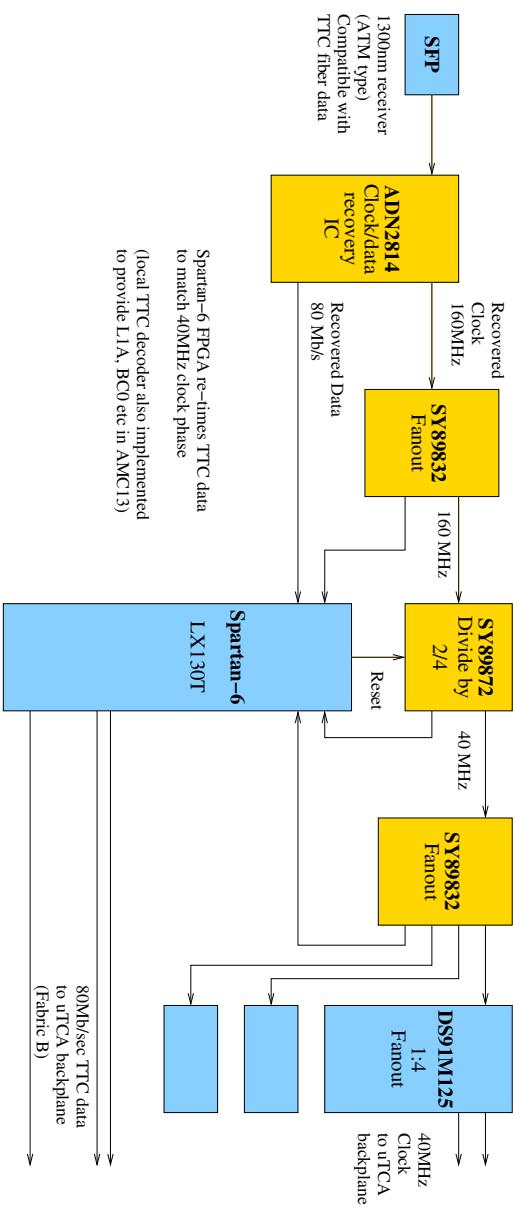


Figure 6.8: AMC13 TTC and Clock Logic

the CMS trigger throttling system. They would be used by the AMC13 to report *e.g.* overflow warning or synchronization error conditions. The AMC13 response to these inputs will be programmable.

The level 2 path provides for delivery of one event fragment per L1A from each AMC module to the CMS central DAQ via the AMC13. The event builder receives and queues L1A from the TTC system with event, bunch crossing and orbit numbers (EvN, OrN and BcN). Simultaneously, event fragments are retrieved from enabled uHTTR cards. The event builder proceeds when an event fragment is available from each uHTTR matching the next EvN in the L1A queue. Completed events¹ are sent to two destinations: the AMC13 spy buffer and the DAQ output

¹actually FED event fragments

link.

Spy Buffer: This is a large circular buffer stored in on-board SDRAM on the AMC13. It can hold perhaps 1000 maximum-size events. It can operate in several modes:

- **Prescaled-In**–In this mode every n^{th} L1A causes an event to be stored in the buffer. When the buffer is full, no more events are stored and a status bit is set.
- **Error Capture**–In this mode all L1A cause events to be stored in the buffer, and the buffer is overwritten in a circular fashion. When a particular condition occurs (i.e. a mis-matched BcN) a fixed number of additional events are captured, then the buffer is frozen for readout. This allows a user to study the event stream surrounding a particular type of event. If no condition is selected, the buffer simply contains the most recent events captured.
- **Filtered Capture**–In this mode a particular class of event only is captured (i.e. events occurring within a particular BcN range).

DAQ Output: This is a fiber-optic link to the CMS central DAQ. The details of the protocol on this link are being negotiated at the time of this writing, but the final link should have at least the following features:

- Transmit data at $>400 \text{ MB/sec}$ to CDAQ
- Provide an error-correcting scheme (i.e. packet retransmission) which operates reliably at essentially full throughput in the presence of link errors at the rate of up to 1 in 10^{12} bits and operates at reduced speed with much higher error rates.
- Support a return channel for back-pressure and testing.

Monitoring

The AMC13 will provide extensive monitoring. This will be implemented as a series of counters. The details will evolve as the firmware is developed, but at least the following quantities will be monitored:

- Total number of events and words transmitted through each link
- EvN, BcN, OrN mis-match errors
- Link errors (TTC, uHTTR-AMC13, AMC13-CDAQ)
- CRC errors on uHTTR payloads
- Occurrence of various specific error conditions within uHTTR payload (typically bits set in a header error word).

TTS Interface

Every CMS FED must provide buffer status information to the TTS subsystem. The current TTS interface uses four LVDS signals carried on a network-type RJ-45 cable. The TTS outputs convey the current state of the FED as one of the following: Ready, Overflow Warning, Busy, Out-of-Sync, Error and Disconnected. The AMC13 provides this information on an optical fiber at 160 Mb/s.

A simple translator module is being developed by HCAL which may be used to interface the AMC13 to the existing TTS subsystem, as well as providing required timing and control signals in a test stand. A block diagram of the module is shown in Fig. 6.9.

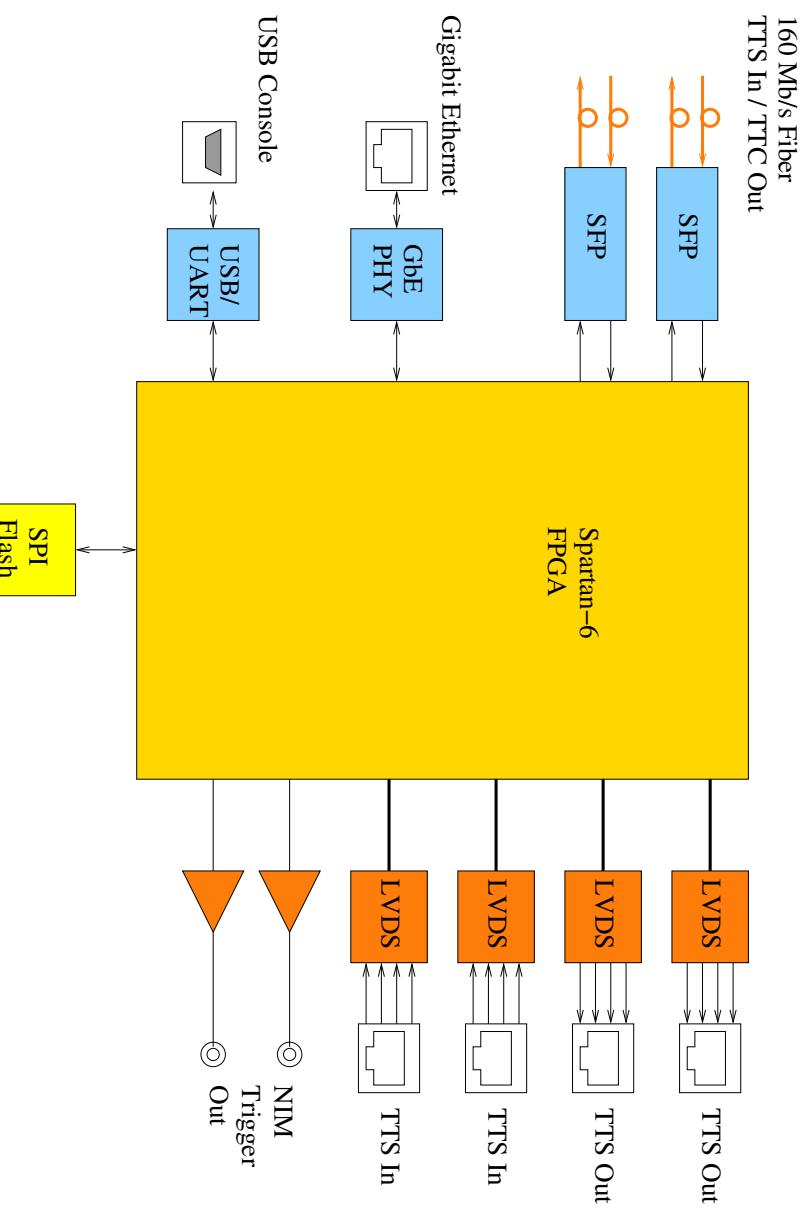


Figure 6.9: AMC13 TTS Adapter and Test Module

6.9 Control system

The control system in the counting room is responsible for slow control and fast control. In the HCAL upgrade, the system located in the counting room and responsible for the control (DCS and TTC) of the FE is the ngFEC (new generation FrontEnd Controller). There is also a system responsible for the control of the BE electronics, which is built out of more standard hardware components and is not described in this section. The HCAL acquisition system is divided in five partitions as shown on Table 6.2.

No changes have been planned to the partitioning in the HCAL upgrade. The fast control must be distributed identically (in units of LHC clock cycles) to all FE crates within each partition.

The requirements of the ngFEC are:

- ability to receive fast control (TTC) signals from the present system
- flexibility to accommodate future evolutions of the TTC system, like [65] as much as reasonably achievable
- ability to interface to DCS computers
- ability to merge fast control and slow control over the same bidirectional GBT link used to communicate with the ngCCM
- maintain a fixed latency of the fast control signals across power cycles and across identical ngFEC channels
- ability to make use of the ngCCM redundancy scheme

The baseline option to implement the FE control is shown in Fig. 6.10.

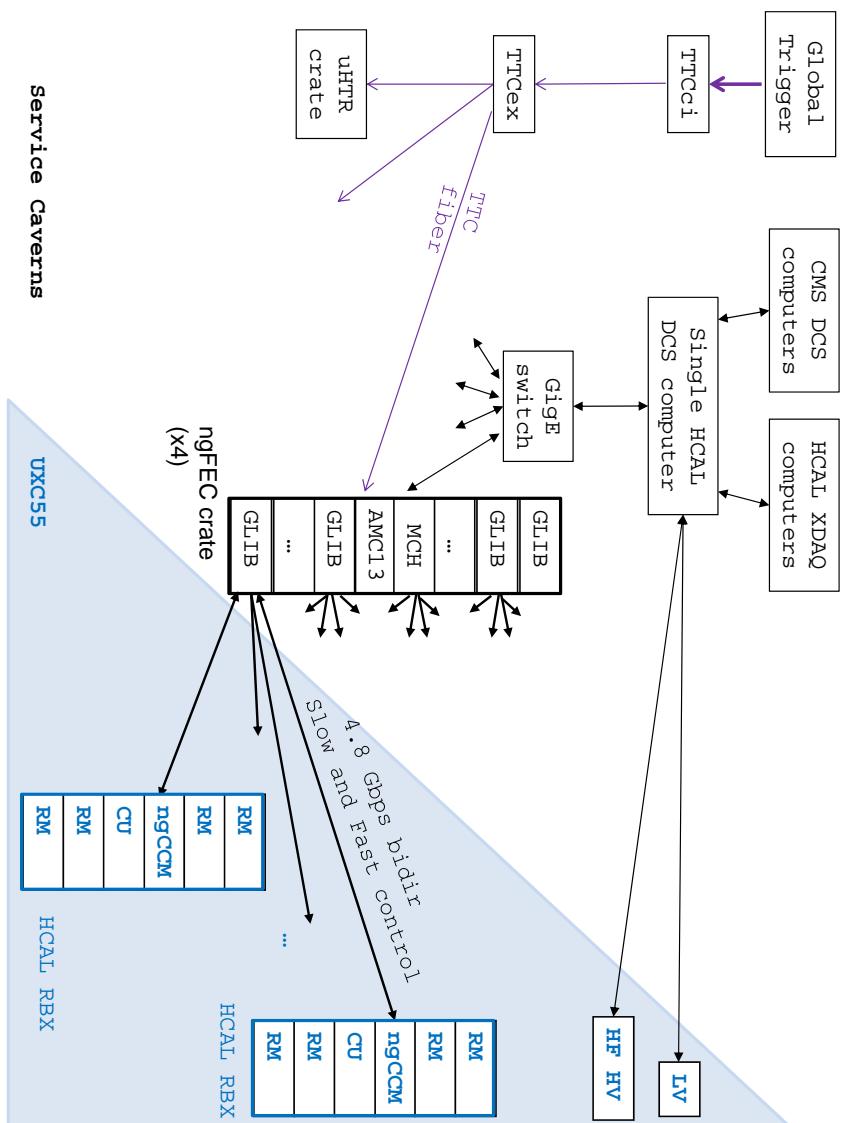


Figure 6.10: Block diagram of the baseline option for the HCAL control

This option makes use of the AMC13 card previously described and of the GLIB card presently developed at CERN [66]. It can meet the requirements and is compatible with the present TTC system without developing any new hardware. A limitation of this option is that one ngFEC crate can serve only one partition; this will require to use four crates (for the three HBHE partitions and for HF), even if only a few slots per crates will be used. The ngFEC crate could drive up to 72 ngCCM, which exceeds our requirements. In this option, the TTC transmission through the backplane is done through standard I/O buffers and not through SerDes, and this will ensure that no latency variations are added to the TTC in this part of the system. Regarding the need to accommodate future evolutions of the TTC system, this relies on the flexibility GLIB design (mostly via FMC mezzanines), and on the possibility to swap the AMC13 with a newly designed module.

6.10 Testing and Integration

Before production, the back-end electronics (uHTTR and AMC13) will be the subject of a specific electronics design review. This review will be separate from the EDRs for both the HF front-end and the HB/HE front-end, as the installation of the HF back-end is planned during LS1 and production must begin before final prototypes are available for the front-ends. The review will demonstrate that the designed electronics will meet the requirements detailed in Section 6.1.

This review is expected to be held approximately March 2013, with approval for production expected by June 2013.

The installation of the back-end electronics for HF will replace the existing VME electronics to provide sufficient USC rack space for the eventual installation of the HB/HE back-end electronics. As a result, it is particularly crucial that all requirements related to HF and operation with the legacy 1.6 Gbps data links be fully demonstrated at the EDR. These demonstrations will take advantage of the optical splitters installed in the data stream from the detector during the 2011/2012 YETS. These splitters allow a sophisticated set of tests to be carried out on the prototype backend electronics during 2012 LHC operations in parallel to the primary data-taking for the experiment. It has also facilitated the development of a full suite of firmware and software for the electronics so that the upgraded electronics chain can be fully ready for 1.6 Gbps operations and for integration in CMS. This parasitic slice testing will validate the following:

- Stable operation of the data links and stable link latency on the front-end/back-end data link. This has been successfully demonstrated over a series of multiple long LHC fills in June 2012.
- DAQ operation will first be validated with Ethernet readout. A special HLT path will be deployed to keep ≈ 0.1 Hz of triggers based on the Level-1 number and the μ TCA-based readout will keep the same subset of events as identified by Level-1 number. This will allow one-to-one validation.
- Full tests of the DAQ chain into central DAQ are planned to occur either during the LHC run or immediately after.
- The HF trigger path will be validated with tests in Building 904, as there is not an appropriate setup available at USC which would not affect primary data-taking.
- The luminosity DAQ process will also be demonstrated using LHC parasitic data-taking.

The operation with the 4.8 Gbps link has been demonstrated with front-end emulators and will be evaluated with pre-production GBT parts as soon as they are available. The more-sophisticated trigger algorithms discussed above will be implemented and tested after the initial 1.6 Gbps firmware has been fully deployed and is operating stably. The back-end electronics will be used extensively at the testbeam electronics evaluations discussed in Section 4.4 and Section 5.8, which will provide a further validation of the back-end electronics and its firmware. For the ngFEC, development has begun using R&D prototype uHTR cards to substitute for the GLIB card. GLIB cards will be available by Fall 2012, allowing the firmware and software development to proceed with the final hardware. The ngCCM is designed to be a very simple module, so the primary validation effort will focus on the ngFEC firmware and software. Development will take place at teststands at CERN and DESY and final validation will be performed at the testbeam evaluations discussed in Section 4.4 and Section 5.8.

6.11 Installation and Commissioning

The back-end electronics for the upgrades will be produced, installed, and commissioned in advance of the installation of the front-end electronics for both the HF and HB/HE upgrades. As discussed in the Introduction, this strategy is adopted to minimize the risk of the front-end installation to CMS operations and to greatly simplify the planning for the front-end installation, as the back-end will be available for testing of the front-end at all times.

The back-end for the HF upgrade will be installed during LS1, near the end of 2013. Before installation, full crates of uHTTRs and AMC13 cards will be operated for at least two months at Building 904 to verify that all components are functional and stable. All three HF back-end crates will be installed in rack S2F05, which currently houses one HF VME crate and the parasitic slice test μ TCA crate. The optical fibers for the other two HF crates will be re-arranged from racks S2F02 and S2F07 in advance of the installation of the μ TCA crates. Once installed, the back-end electronics will be connected to the 1.6 Gbps front-end electronics and validated in local Ethernet DAQ operation. The connections to the RCT and central DAQ will be made in late 2013 or early 2014 based on the schedules of these groups. The full system will be tested thoroughly to ensure that it is ready for operation by mid 2014, well in advance of the LHC restart.

The back-end for the HB/HE upgrade will be installed in a staged manner to support the deployment of the calorimeter trigger upgrade. The μ TCA crates will not replace the VME crates, but rather optical splitters will on the incoming 1.6 Gbps links will be used to operate both the VME and μ TCA in parallel. These splitters can be installed in a single year-end technical stop. The first partition will be split and made available for a trigger slice test in 2015 and the second two partitions can be installed for 2016 operation. The μ TCA crates will be installed using the space made available by the removal of the HF VME crates and the luminosity patch panels which were required with the VME electronics. The systems will operate in parallel until CMS decides to de-commission the existing RCT. At that point, it will be possible to de-commission the HCAL VME crate and some consolidation of rack layout may be possible.

The ngFEC crates will be installed in racks in row C of the S2 level of USC, as is the current VME-based CCM control system. The installation and commissioning of the ngFEC crates will be determined by the installation schedule of the front-end systems which they control. The first crate will be installed during LS1 and will allow final validation of the system with the LHC clock and operational constraints during 2015 before the HF front-end installation. Later installations for HB/HE will be fully validated by the HF ngFEC crate and the experience of operation in Building 904, for activities which are specific to the HB/HE front-end such as the Peltier control loop.

Chapter 7

Project Organization, Cost, and Schedule

7.1 Project Organization

The HCAL Upgrade Sub-project is organized as an activity of the existing CMS Hadron Calorimeter Project, which is organized according to the CMS constitution. The Project involves 57 institutions worldwide, with 297 physicists, PhD students, and engineers, working together to maintain and operate the present calorimeters and to design and build the upgrades. Major institutes involved are from Brazil, Germany, India, Russia-Dubna Member States (RDMS), Turkey and United States.

7.1.1 Participating Institutes

The declared interests of the institutes of the HCAL Project on portions of the HCAL Upgrade Sub-project are listed in Table 7.1. This list is neither final or complete, as institutes within the current HCAL project are still considering involvements on the Upgrade Sub-project and new institutions are joining the HCAL Project.

Table 7.1: List of current declared interests and participation for HCAL institutes and institute groups in the HCAL Upgrade Sub-project.

Institute/Institute Group	Participation and Current Interests
Centro Brasileiro de Pesquisas Fisicas (Brazil)	HF Front-end
Universidade do Estado do Rio de Janeiro (Brazil)	HF Front-end
Universidade Estadual de Campinas (Brazil)	HF Front-end
Deutsches Elektronen-Synchrotron (Germany)	Controls and Online Software, μ TCA
Panjab University (India)	HB / HE Front-end
Tata Institute of Fundamental Research - EHEP (India)	HB / HE Front-end
Saha Institute of Nuclear Physics (India)	μ TCA Back-end
Institute for Research in Fundamental Sciences (Iran)	Simulation Studies
RDMS	HE Front-end, μ TCA Back-end, Controls
Cukurova University (Turkey)	HF Front-end
Middle East Technical University (Turkey)	HF Front-end
Bogazici University (Turkey)	HF Front-end
Istanbul Technical University (Turkey)	HF Front-end
University of Alabama (USA)	Controls and Online Software
Baylor University (USA)	HF Front-end, Simulation Studies
Boston University (USA)	μ TCA Back-end
Brown University (USA)	μ TCA Back-end, Trigger Algorithms, Simulation Studies
State University of New York at Buffalo (USA)	Simulation Studies
California Institute of Technology (USA)	Trigger Algorithms, Simulation Studies

Institute/Institute Group	Participation and Current Interests
Fairfield University (USA)	HF Front-end
Fermi National Accelerator Laboratory (USA)	HF Front-end, HB/HE Front-end
Florida International University (USA)	Controls and Online Software
Florida State University (USA)	HF Front-end, HB/HE Front-end
Florida Institute of Technology (USA)	HF Front-end, HB/HE Front-end
University of Iowa (USA)	HF Front-end, HB/HE Front-end, μ TCA Back-end
Kansas University (USA)	HF Front-end
University of Maryland (USA)	ngCCM, Controls and Online Software
University of Minnesota (USA)	μ TCA Back-end, Online Software
University of Mississippi (USA)	HF Front-end, HB/HE Front-end, Simulation Studies
Massachusetts Institute of Technology (USA)	μ TCA Back-end, Online Software, Simulation Studies
Northwestern University (USA)	HB/HE Front-end
Notre Dame University (USA)	HB/HE Front-end, Simulation Studies
Princeton University (USA)	HB/HE Front-end, Simulation Studies
University of California - Riverside (USA)	HB/HE Front-end
University of Rochester (USA)	Controls and Online Software, μ TCA ngFEC
Rockefeller University (USA)	Simulation Studies
University of California - Santa Barbara (USA)	HB/HE Front-end, Online Software
Texas Tech University (USA)	HF Front-end
University of Virginia (USA)	ngCCM
Wayne State University (USA)	Simulation Studies

7.1.2 Institution Board

The Institution Board (IB) is the highest decision-making body in the Hadron Calorimeter Project. The IB must ratify all decisions of importance of the HCAL Project. In particular, the IB must assess the real costs of the project and the sources of funding and seek appropriate balance. Each institute involved in the HCAL Project has a member on the IB. In addition, Project Managers, Resource Managers and Technical Coordinators are *ex. officio* members of the IB.

7.1.3 Organization

The organization of HCAL Project is structured similarly to the CMS Collaboration. The organization is completely described by the Constitution of the CMS Hadron Calorimeter Institution Board, which was approved on December 4, 1995 and last amended on June 26, 2012.

Project Manager

The Project Manager of the HCAL system is appointed by the Spokesman of CMS. Sub-system coordinators of HCAL are nominated by the Project Manager and appointed jointly by the CMS Spokesman and the Project Manager.

The organization chart of the HCAL Project for 2013 is shown on Fig. 7.1. The organization covers operations and upgrade of the following Hadron Calorimeter sub-systems: HCAL Barrel (HB), HCAL Endcap (HE), HCAL Forward (HF) and HCAL Outer (HO). Two additional calorimeter groups are part of HCAL organization: the Zero Degree Calorimeter (ZDC) and CASTOR. HCAL Project is subdivided into three sub-projects: Detector Performance Group (DPG), Installation and Commissioning Group (ICG) and Upgrade Group (UpG).

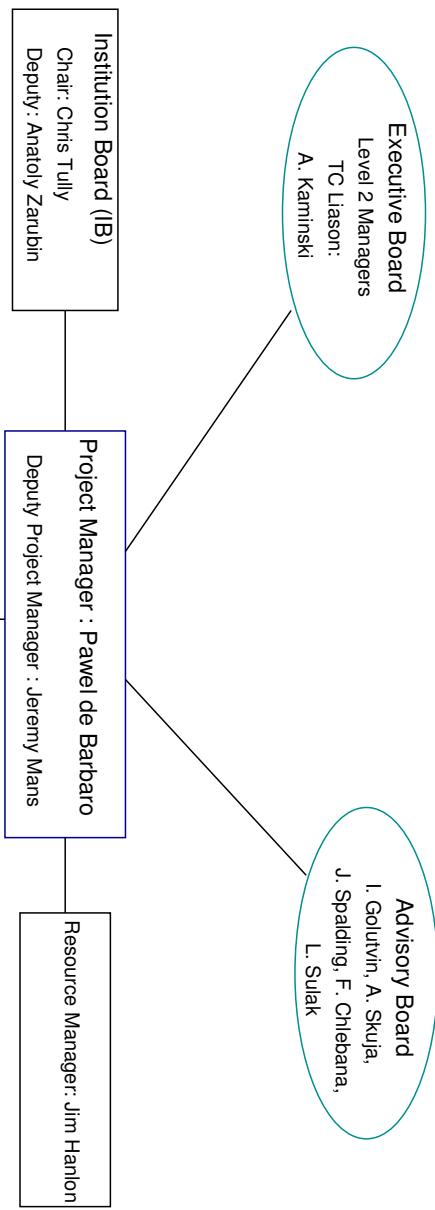


Figure 7.1: Organization chart of the HCAL Project for 2013.

HCAL Upgrade Sub-project

The HCAL Upgrade sub-project is organized under the HCAL Project, and overseen by the HCAL Institution Board. HCAL Upgrade sub-project co-leaders are appointed by HCAL Project Manager.

The HCAL Upgrades are fully integrated into the overall organization. The Upgrade Group is responsible for designing, prototyping and building all sub-systems of the HCAL upgrades. This group interfaces with the Installation and Commissioning group in system commissioning, installation and operational commissioning at the experiment. The scope of responsibility of Upgrade Group covers both Phase I, as well as Phase II projects. Co-leaders of HCAL Upgrade Group are at the same time HCAL Project liaisons to the CMS Upgrade Project Office.

Upgrade Simulation studies and code development are carried out within HCAL Detector Performance Group.

Finances of the HCAL Upgrade sub-project are incorporated into HCAL finances. In particular, HCAL Resource Manager helps HCAL PM to manage financial aspects of HCAL Upgrade project.

7.2 Project Schedule

7.2.1 Schedule Constraints and External Milestones

The schedule for the HCAL Upgrade Project is driven by the need for high detector performance as the LHC luminosity and event pile-up increase, by the LHC operating schedule, and by the availability of key custom components. On the side of the LHC schedule, the performance of the detector must match the luminosity which the LHC can deliver and sufficient time must be available for installation of the front-end electronics. The schedule inputs for ac-

cess to the CMS experimental hall as determined by the LHC operations schedule are taken to be:

- The first long shutdown of the LHC (LS1) will begin by March 2013 and end by September 2014.
- The second long shutdown of the LHC (LS2) will begin December 2017 and end in February 2019.
- Regular year-end technical stops (YETS) will occur between operational years of LHC, generally stretching from December to late February or early March.

For the long shutdowns, significant re-commissioning time is likely to be required for the detector, so any major work should be completed six months before the end of the shutdown.

The key custom components which drive the schedule, along with their expected availability/decision dates are:

- QIE10 chip – final version expected to be available by November 2013
- GBT chip and Versatile link components – final versions expected to be available by March 2013
- SiPM – final vendor decision expected to be possible by end of 2012, but additional time is allowed in the schedule for any final adjustments of parameters and for cost-competition between vendors

A final key input to the schedule comes from the calorimeter trigger upgrade. The operation of the upgraded calorimeter trigger depends on the availability of the HB/HE μ TCA back-end electronics. The μ TCA back-end electronics would be operated in parallel with the VME electronics using optical splitters on the digital data signal from the detector. To allow the trigger to be available midway between LS1 and LS2, the back-end must be fully installed in 2016.

This schedule has been determined by technical and operational considerations as discussed above. Project funding is currently under discussion with a number of funding sources. Appropriate levels and availability are assumed in the scheduling process presented here.

7.2.2 Schedule and Milestones

The HCAL Upgrade schedule is determined and tracked using the following milestones, grouped logically and chronologically. Schedule contingency is not included in these milestones. Additional milestones will be created in consultation with other projects and with Technical Coordination, which will include contingency. These will be used for overall CMS planning. The milestones identified as Level 1 (L1) milestones are critical milestones which are coordination points with other projects. Milestones identified as Level 2 (L2) are internal milestones for tracking project progress.

- HF Back-end Electronics
- CMS Electronics Design Review Approval (L2) : April 2013
- Production complete (L2) : June 2013
- Ready for installation (L2) : October 2013
 - Ready for operation (L1) : April 2014
- HF Front-end
- Cable and optical fiber installation complete (L2) : February 2014

- CMS Electronics Design Review Approval (L2) : July 2014
- Production complete (L2) : April 2015
- Ready for installation (L2) : October 2015
- Ready for operation (L1) : March 2016
- HB/HE Back-end Electronics
- CMS Electronics Design Review Approval (L2) : May 2014
- First partition (1 / 3) installation and commissioning start (L2) : August 2014
- Full optical splitter infrastructure installed (L2) : February 2016
- Second and third partition installation and commissioning start (L2) : April 2016
- Ready for operation (L1) : July 2016
- HB/HE Front-end Electronics
- CMS Electronics Design Review Approval (L2) : June 2016
- Production 1 / 3 complete (L2) : January 2017
- Production complete (L2) : July 2017
- Ready for installation (L2) : January 2018
- Ready for operation (L1) : July 2018

A detailed schedule, consisting of approximately 300 WBS lines, has been produced with input from the engineers and installation experts. This schedule is shown on the next three pages, with some detail rolled up to allow easier inspection of the overall planning.

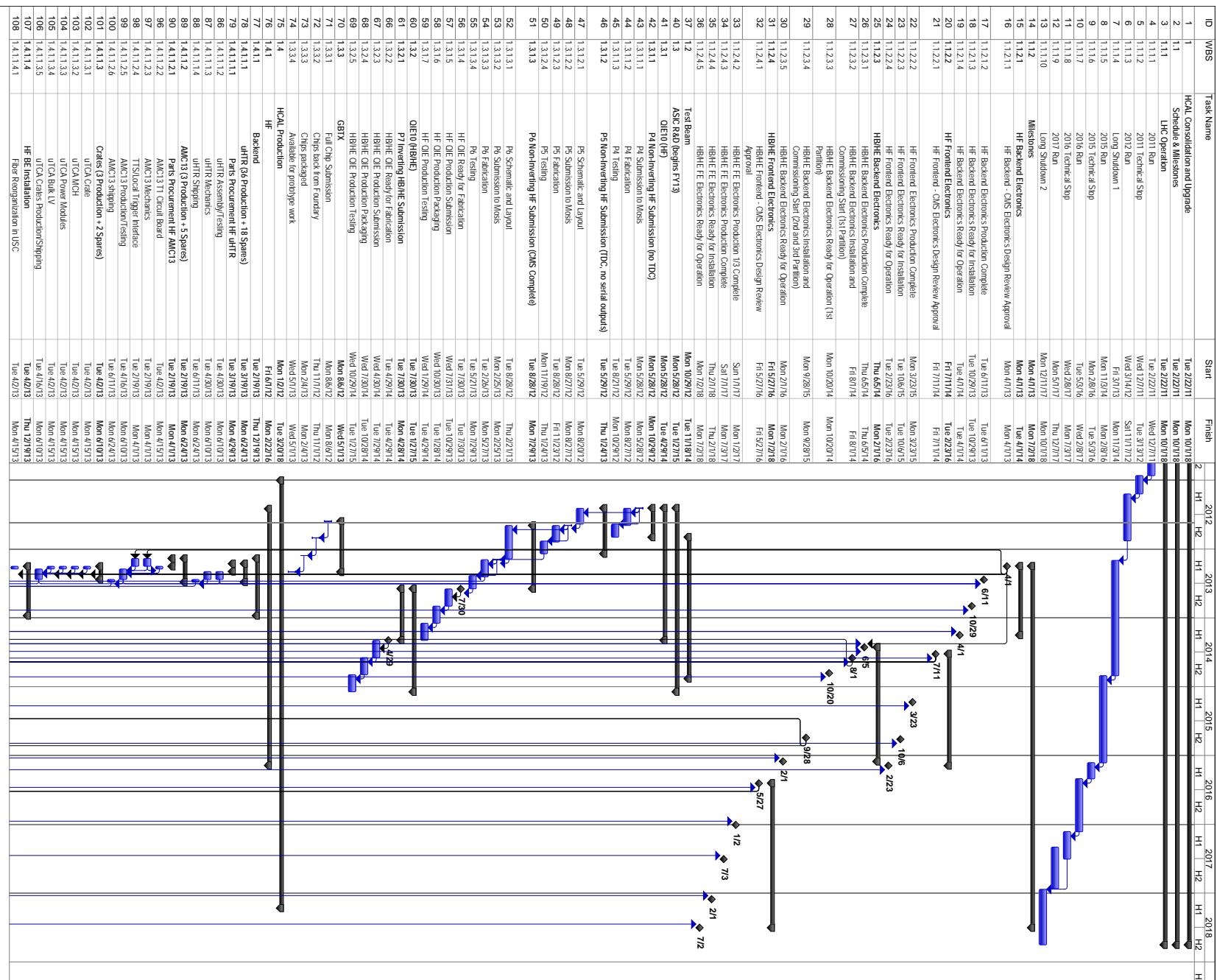
7.3 Cost Methodology

A detailed cost breakdown for the HF and HB/HE upgrades has been developed, with about 100 individual items in the Cost Book. These cost estimates are for materials and services (M&S) only and are those which fall into the allowed expense group 4.6.3 as defined by the CORE (LHCC Cost Review Committee) and recently reformulated by the CMS Resource Manager specifically for the CMS Upgrade project as follows:

1. Final prototype or pre-production fabrication required to validate a final design or product quality, prior to production
2. Engineering costs incurred during production at a vendor or contractor, not at a CMS member Institution
3. Production fabrication and construction costs, including QA and system testing during the assembly process
4. Transportation costs, integration and installation

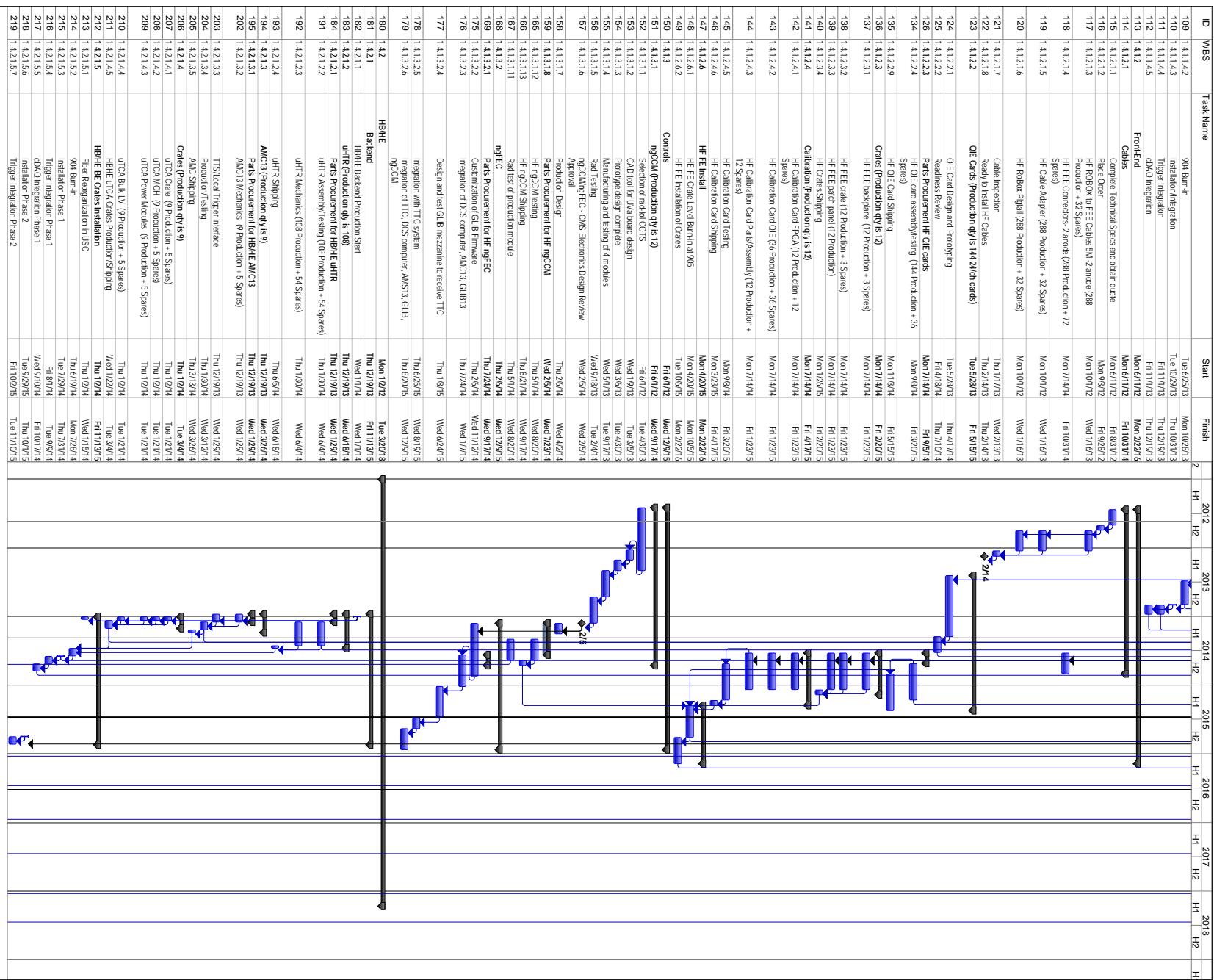
This cost definition does not include research and development or engineering costs incurred at member institutions.

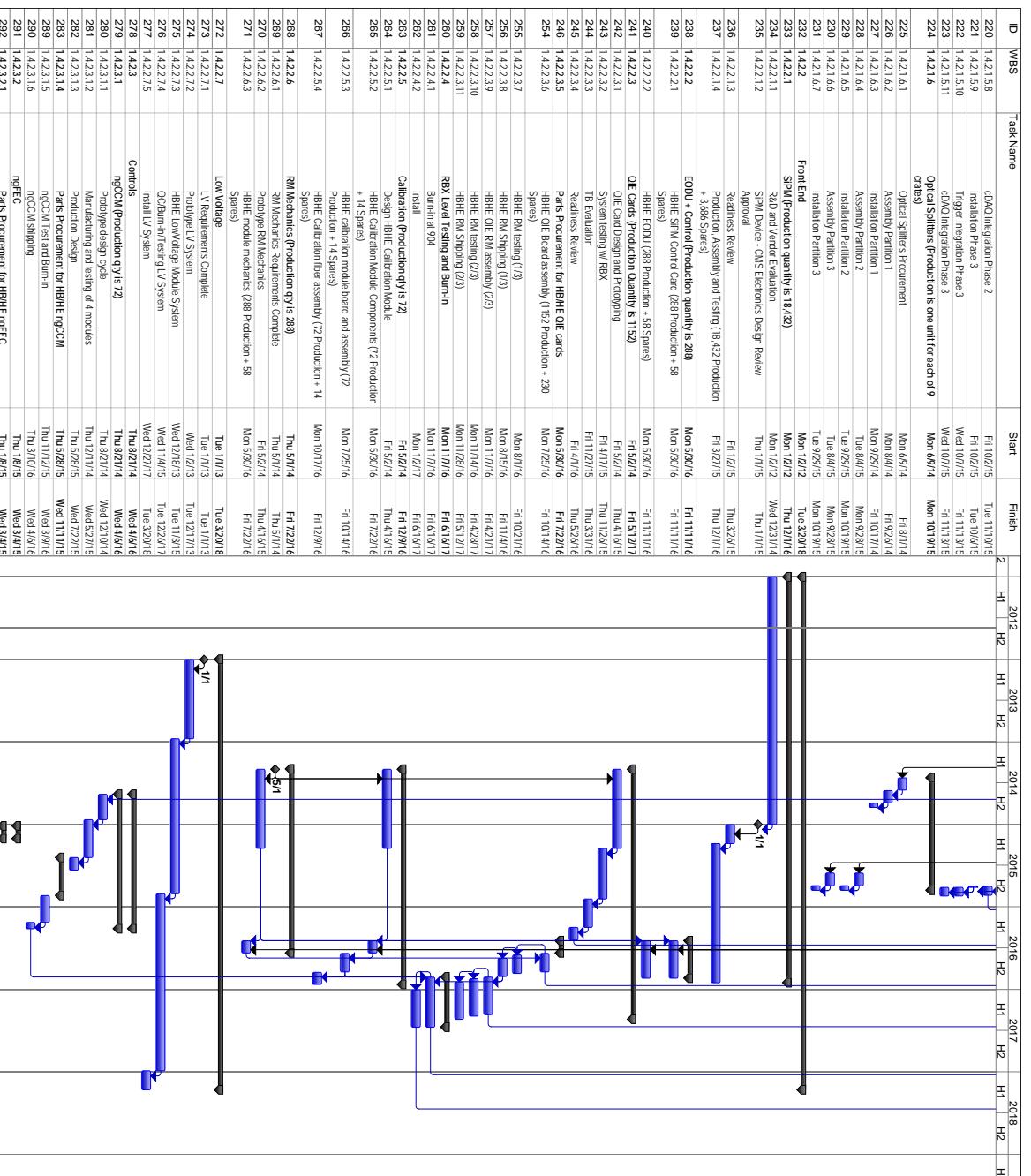
The quality of the cost estimates ranges from firm vendor quotes down to educated guesses. Whenever available, actual quotes already obtained from vendors and/or companies have been used. The cost estimates for portions of the system which have not been fully engineered



7.3. Cost Methodology

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are necessarily somewhat uncertain, however the lead engineers for each subsystem have provided detailed costs for the leading cost elements and estimates for the remaining costs. In some cases, careful extrapolations from similar parts of the existing detector were carried out by the experts, or groups thereof, who took care of the corresponding parts of the existing detectors.

All quotes and estimates have been collected in calendar years 2011 and 2012. Quotes and estimates have been provided in CHF, EUR, or USD, depending on the geographical location of institutes, companies, vendors, or suppliers. In this chapter, all monetary values are expressed in CHF. The following conventional exchange rates have been used to convert EUR and USD to CHF:

- 1 USD = 1.0 CHF
- 1 EUR = 1.2 CHF

As a general procedure, the cost of each individual item is estimated by using a unit cost and an estimate of the quantity needed. The latter parameter deserves some further illustration. For most items, e.g. the modular ones such as the module components, or electronic boards and units, the quantity is the sum of three numbers:

1. The actual quantity needed to build the detector.
2. The number of spares estimated as needed to safely overcome the assembly, integration, commissioning, and installation stages, when handling of parts may result into accidental damage of them, thus needing replacement. The spares requirement also includes replacements for installation during operation. In general, the spares requirement is estimated to be 20% of the bare quantity to be mounted in the detector.
3. A quantity of additional components, primarily in the back-end electronics, to support the simultaneous operation of the back-end with the upgraded trigger in USC55 and the burn-in of the front-end modules at B904. Support of this requirement mandates an additional 30% spares for the back-end components.

These remarks intend to show that a purely technical “contingency”, in the form of added quantities to compensate for operational losses and for ordinary accidents during handling is built into the final estimated cost of this project. More conventional general contingency, however, is not included, as CMS guidelines prevent us from doing so. The costs that we are about to quote, therefore, do not include neither general technical contingency for unexpected or unforeseen technical flaws or major accidents, nor financial contingency for inflation, exchange rate variations, or general evolution of economy or market conditions which may alter the cost of procured materials and components. For these issues, in case of cost increase, we will have no other choice than turning to CMS for help or, ultimately, to the FAs with additional, *ad-hoc* requests for further funding.

With this preliminary discussion complete, the costs for the HF and HB/HE upgrades are detailed in Table 7.2 and Table 7.3 respectively. The total cost for the HF upgrade is **1503 kCHF** while the cost for the HB/HE upgrades is **6541 kCHF**. The significantly-larger cost of the HB/HE upgrades represents the fact that the HB and HE subdetectors have a factor of three more electronics channels than the HF and that the SiPM costs are included in this upgrade while the PMT replacement in HF was funded earlier and is not included in this project cost. As the back-end and control systems use a large amount of common hardware, it is useful to consider these as common sub-projects, with the breakdown shown in Table 7.4.

Table 7.2: Cost breakdown for the HF upgrade by area

	Area	Cost (kCHF)
Front-end		1103
QIE Cards	639	
PMT-QIE cables	320	
Optical readout fibers	67	
Low-voltage supplies	33	
QIE Readout crates	28	
Calibration modules	17	
Controls		
ngCCM (Front-end component)	57	
ngFEC (Back-end component)	22	
	35	
Back-end		280
uHTR	186	
AMC13	41	
Crates	53	
Installation Labor		64
Total		1503

Table 7.3: Cost breakdown for the HB/HE upgrade by area

Area	HB Cost (kCHF)	HE Cost (kCHF)	Total Cost (kCHF)
Front-end	2482	2482	4964
SiPM Photodetectors	774	774	1548
QIE Cards	1009	1009	2018
ODU and SiPM Control	354.5	354.5	709
Calibration modules	45	45	90
RM mechanics	86.5	86.5	173
Low-voltage supplies	153	153	306
Burn-in station	60	60	120
Controls	151	151	302
ngCCM (Front-end component)	68	68	136
ngFEC (Back-end component)	83	83	166
Back-end	488	488	976
uHTR	279	279	558
AMC13	36	36	72
Crates	74	74	148
Optical-splitter modules	99	99	198
Installation Labor	150	150	300
Total	3271	3271	6542

Table 7.4: Cost breakdown for the HCAL controls and back-end combining HB, HE, and HF showing common costs. These costs are included in Tables 7.2 and 7.3, but are collected here for understanding the costs for the portions which are common across the project.

Controls	HF Cost (kCHF)	HB Cost (kCHF)	HE Cost (kCHF)	Total Cost (kCHF)
HF ngCCM (Front-end component)	57	151	151	359
HB/HE ngCCM (Front-end component)	22	-	-	22
ngFEC (Back-end component)	35	83	83	201
Back-end	280	488	488	1256
uHTR	186	279	279	744
AMC13	41	36	36	113
Crates	53	74	74	201
Optical-splitter modules	-	99	99	198

Chapter 8

Glossary of special terms and acronyms

- APD = Avalanche Photodiode
- AMC = Advanced Mezzanine Card (from the ATCA specification)
- ASIC = Application-Specific Integrated Circuit
- ATCA = Advanced TeleCommunications Architecture
- BE = Back-End
- BV = Bias Voltage
- CCITT-CRC = Standard cyclical redundancy check algorithm developed by the International Telecommunications Union
- CCM = Clock and Control Module
- cDAQ = central Data Aquistion
- CRC = Cyclical-redundency check, a widely-used family of algorithms for identifying data corruption
- DCC = Data Concentrator Card
- DCS = Detector Control System, in HCAL it indicates the slow control of the FE
- DDR = Double Data Rate, the transfer of data on a synchronous digital link at both the rising and falling edges of a clock
- FE = Front-End
- FEC = Forward Error Correction
- FEE = Front-End Electronics
- FIR = Finite-Input Response Filter
- FPGA = Field-Programmable Gate Array
- GbE = Gigabit Ethernet
- GBT = Gigabit Transceiver Project developed at CERN, source of the GBTx and associated chips
- GBTx = Gigabit Transceiver ASIC developed at CERN
- GLIB = μ TCA card developed by the CERN microelectronics group for testing and operating with the GBT link
- HCAL = Hadron Calorimeter
 - HB = HCAL Barrel
 - HE = HCAL Endcap
 - HF = HCAL Forward

- HLT = High Level Trigger, a collection of software trigger algorithms
- HO = HCAL Outer
- HTR = HCAL Trigger and Readout Card
- I2C = Inter-Integrated Circuit chip-to-chip communications protocol
- ieta = integer index for defining detector volumes as a function of pseudorapidity
- iphi = integer index for defining detector volumes as a function of azimuthal angle
- LC = Common optical fiber connector standard
- LVDS = Low-Voltage Differential Signaling
- MCH = μ TCA Control Hub
- minbias = Soft proton-proton collision
- MMC = Mezzanine Management Controller, part of the μ TCA specification
- MTP = Optical fiber connector standard allowing up to 12 fibers in a single connector
- MTP-LC = An optical cable with an MTP connector on one end and many LC connectors on the other
- ngCCM = new generation Clock and Control Module (part of the FEE)
- ngFEC = new generation Front-End Controller (part of the BE electronics)
- ODU = Optical Decoder Unit
- pileup = overlapping of multiple soft interactions during a single LHC beam crossing
- pseudorapidity (η) = $-\ln \tan \frac{\theta}{2}$, where θ is the angle of the particle momentum with respect to the anti-clockwise beam direction.
- PDE = Photon-detection efficiency defined as the product of geometrical acceptance of an SiPM and the silicon quantum efficiency
- PLL = Phase Locked Loop
- QA = Quality Assurance
- QIE = Charge (Q) Integrator and Encoder, a series of ASICs
- RCT = Regional Calorimeter Trigger
- RBX = Readout Box, housing the HB and HE FEE
- SEE = Single Event Effect, a generic effect of radiation on electronics
- SEL = Single Event Latchup
- SerDes = Serializer/Deserializer
- SET = Single Event Transient
- SEU = Single Event Upset
- SFP = Small Form-factor Pluggable standard for optical and other transceivers which connect to a standard-defined socket
- SFP+ = Extension of the SFP standard to support up to 10 Gbps data rates
- SiPM = Silicon Photomultiplier
- SLB = Serial Link Board of the CMS calorimeter trigger system
- SLVS = Scalable Low Voltage Signaling
- TDC = Time-to-Digital Converter
- TID = Total Ionizing Dose

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- TMR = Triple Modular Redundancy, a technique for avoiding errors in electronics circuits
 - TTC = Trigger Timing and Control
 - TTS = Trigger-Throttling System
 - uHTTR = μ TCA HCAL Trigger and Readout card
 - UDP/IP = User Datagram Protocol using the Internet Protocol
 - USC = Underground Service Cavern
 - UXC = Underground Experimental Cavern
 - VBF = Vector Boson Fusion
 - VTRX = Versatile Link Transmitter/Receiver, optical transceiver developed by the CERN Versatile Link project
 - VTTx = Versatile Link Dual Transmitter, optical transmitter developed by the CERN Versatile Link project which combines two transmission channels in a single SFP module
 - WLS = Wavelength shifter
 - WTE = Warning Test Enable
 - YETS = Year-End Technical Stop – a relatively brief stop of the LHC, typically less than three months in length, during the winter holidays

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