SN74AHC1G00 Single 2-Input Positive-NAND Gate

1 Features

- Operating Range: 2 V to 5.5 V
- Maximum t_{pd} of 6.5 ns at 5 V
- Low Power Consumption: Maximum I_{CC} of 10 µA
- ±8-mA Output Drive at 5 V
- Schmitt Trigger Action at All Inputs Makes the Circuit Tolerant for Slower Input Rise and Fall Time
- Latch-Up Performance Exceeds 250 mA Per JESD 17
- ESD Protection Exceeds JESD 22
  - 2000-V Human-Body Model (A114-A)
  - 1000-V Charged-Device Model (C101)

2 Applications

- IP Phones
- Notebook PCs
- Printers
- Access Control and Security
- Solar Inverters
- Personal Electronics

3 Description

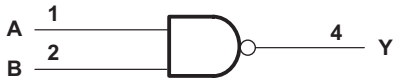
The SN74AHC1G00 performs the Boolean function $Y = \overline{A \bullet B}$ or $Y = \overline{A} + \overline{B}$ in positive logic.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
SN74AHC1G00DBV	SOT-23 (5)	2.90 mm × 1.60 mm
SN74AHC1G00DCK	SC70 (5)	2.00 mm × 1.25 mm
SN74AHC1G00DRL	SOT (5)	1.60 mm × 1.20 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Logic Diagram (Positive Logic)



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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision N (May 2013) to Revision O — **Page**

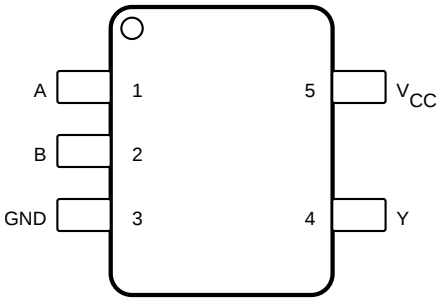
- Added *Device Information* table, *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section. ... 1

Changes from Original (March 1996) to Revision N — **Page**

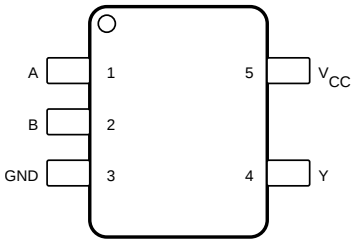
- Changed document format from Quicksilver to DocZone. ... 1

5 Pin Configuration and Functions

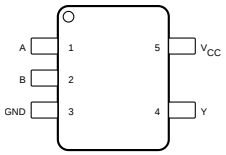
DBV Package
5-Pin SOT-23
Top View



DCK Package
5-Pin SC70
Top View



DRL Package
5-Pin SOT
Top View



Pin Functions

PIN		I/O	DESCRIPTION
NO.	NAME		
1	A	I	A input
2	B	I	B input
3	GND	—	Ground
4	Y	O	Output
5	V_{CC}	—	Power

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) (1)

			MIN	MAX	UNIT
V_{CC}	Supply voltage		–0.5	7	V
V_I	Input voltage(2)		–0.5	7	V
V_O	Output voltage(2)		–0.5	V_{CC} + 0.5	V
I_{IK}	Input clamp current	V_I < 0		–20	mA
I_{OK}	Output clamp current	V_O < 0 or V_O > V_{CC}		±20	mA
I_O	Continuous output current	V_O = 0 to V_{CC}		±25	mA
	Continuous current through V_{CC} or GND			±50	mA
T_J	Maximum junction temperature			150	°C
T_{stg}	Storage temperature		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

See (1)

			MIN	MAX	UNIT
V_{CC}	Supply voltage		2	5.5	V
V_{IH}	High-level input voltage	V_{CC} = 2 V	1.5		V
		V_{CC} = 3 V	2.1		
		V_{CC} = 5.5 V	3.85		
V_{IL}	Low-level input voltage	V_{CC} = 2 V		0.5	V
		V_{CC} = 3 V		0.9	
		V_{CC} = 5.5 V		1.65	
V_I	Input voltage		0	5.5	V
V_O	Output voltage		0	V_{CC}	V
I_{OH}	High-level output current	V_{CC} = 2 V		–50	µA
		V_{CC} = 3.3 V ± 0.3 V		–4	mA
		V_{CC} = 5 V ± 0.5 V		–8	
I_{OL}	Low-level output current	V_{CC} = 2 V		50	µA
		V_{CC} = 3.3 V ± 0.3 V		4	mA
		V_{CC} = 5 V ± 0.5 V		8	
Δt/Δv	Input transition rise or fall rate	V_{CC} = 3.3 V ± 0.3 V		100	ns/V
		V_{CC} = 5 V ± 0.5 V		20	
T_A	Operating free-air temperature		–40	125	°C

(1) All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. See the TI application report, *Implications of Slow or Floating CMOS Inputs*, SCBA004.

6.4 Thermal Information

THERMAL METRIC(1)		SN74AHC1G00			UNIT
		DBV (SOT-23)	DCK (SC70)	DRL (SOT)	
		5 PINS	5 PINS	5 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	240	276.53	256	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	174.5	118.5	130	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	73.7	62.8	152	°C/W
ψ_{JT}	Junction-to-top characterization parameter	54.9	6.7	9.9	°C/W
ψ_{JB}	Junction-to-board characterization parameter	72.9	62.1	152	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

6.5 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER(1)	TEST CONDITIONS		V_{CC}	MIN	TYP	MAX	UNIT
V_{OH}	I_{OH} = –50 µA	T_A = 25°C	2 V	1.9	2		V
		T_A = –40°C to +85°C		1.9			
		T_A = –40°C to +125°C		1.9			
		T_A = 25°C	3 V	2.9	3		
		T_A = –40°C to +85°C		2.9			
		T_A = –40°C to +125°C		2.9			
		T_A = 25°C	4.5 V	4.4	4.5		
		T_A = –40°C to +85°C		4.4			
		T_A = –40°C to +125°C		4.4			
	I_{OH} = –4 mA	T_A = 25°C	3 V	2.58			
		T_A = –40°C to +85°C		2.48			
		T_A = –40°C to +125°C		2.48			
	I_{OH} = –8 mA	T_A = 25°C	4.5 V	3.94			
		T_A = –40°C to +85°C		3.8			
		T_A = –40°C to +125°C		3.8			
V_{OL}	I_{OL} = 50 µA	T_A = 25°C	2 V			0.1	V
		T_A = –40°C to +85°C				0.1	
		T_A = –40°C to +125°C				0.1	
		T_A = 25°C	3 V			0.1	
		T_A = –40°C to +85°C				0.1	
		T_A = –40°C to +125°C				0.1	
		T_A = 25°C	4.5 V			0.1	
		T_A = –40°C to +85°C				0.1	
		T_A = –40°C to +125°C				0.1	
	I_{OL} = 4 mA	T_A = 25°C	3 V			0.36	
		T_A = –40°C to +85°C				0.44	
		T_A = –40°C to +125°C				0.44	
	I_{OL} = 8 mA	T_A = 25°C	4.5 V			0.36	
		T_A = –40°C to +85°C				0.44	
		T_A = –40°C to +125°C				0.44	
I_I	V_I = 5.5 V or GND	T_A = 25°C	0 V to 5.5 V			±0.1	µA
		T_A = –40°C to +85°C				±1	
		T_A = –40°C to +125°C				±1	

(1) Recommended T_A = –40°C to +125°C

Electrical Characteristics (continued)

over operating free-air temperature range (unless otherwise noted)

PARAMETER(1)	TEST CONDITIONS		V_{CC}	MIN	TYP	MAX	UNIT
I_{CC}	$V_I = V_{CC}$ or GND, $I_O = 0$	T_A = 25°C	5.5 V			1	µA
		T_A = –40°C to +85°C				10	
		T_A = –40°C to +125°C				10	
C_i	$V_I = V_{CC}$ or GND	T_A = 25°C	5 V		2	10	pF
		T_A = –40°C to +85°C				10	
		T_A = –40°C to +125°C				10	

6.6 Switching Characteristics: V_{CC} = 3.3 V ± 0.3 V

over recommended operating free-air temperature range, V_{CC} = 3.3 V ± 0.3 V (unless otherwise noted) (see Figure 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	OUTPUT CAPACITANCE	T_A(1)	MIN	TYP	MAX	UNIT
t_{PLH}	A or B	Y	C_L = 15 pF	25°C		5.5	7.9	ns
				–40°C to +85°C	1		9.5	
				–40°C to +125°C	1		10.5	
t_{PHL}				25°C		5.5	7.9	
				–40°C to +85°C	1		9.5	
				–40°C to +125°C	1		10.5	
t_{PLH}	A or B	Y	C_L = 50 pF	25°C		8	11.4	ns
				–40°C to +85°C	1		13	
				–40°C to +125°C	1		14	
t_{PHL}				25°C		8	11.4	
				–40°C to +85°C	1		13	
				–40°C to +125°C	1		14	

(1) Recommended T_A = –40°C to +125°C

6.7 Switching Characteristics: V_{CC} = 5 V ± 0.5 V

over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see Figure 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	OUTPUT CAPACITANCE	T_A(1)	MIN	TYP	MAX	UNIT
t_{PLH}	A or B	Y	C_L = 15 pF	25°C		3.7	5.5	ns
				–40°C to +85°C	1		6.5	
				–40°C to +125°C	1		7	
t_{PHL}				25°C		3.7	5.5	
				–40°C to +85°C	1		6.5	
				–40°C to +125°C	1		7	
t_{PLH}	A or B	Y	C_L = 50 pF	25°C		5.2	7.5	ns
				–40°C to +85°C	1		6.5	
				–40°C to +125°C	1		9	
t_{PHL}				25°C		5.2	7.5	
				–40°C to +85°C	1		6.5	
				–40°C to +125°C	1		9	

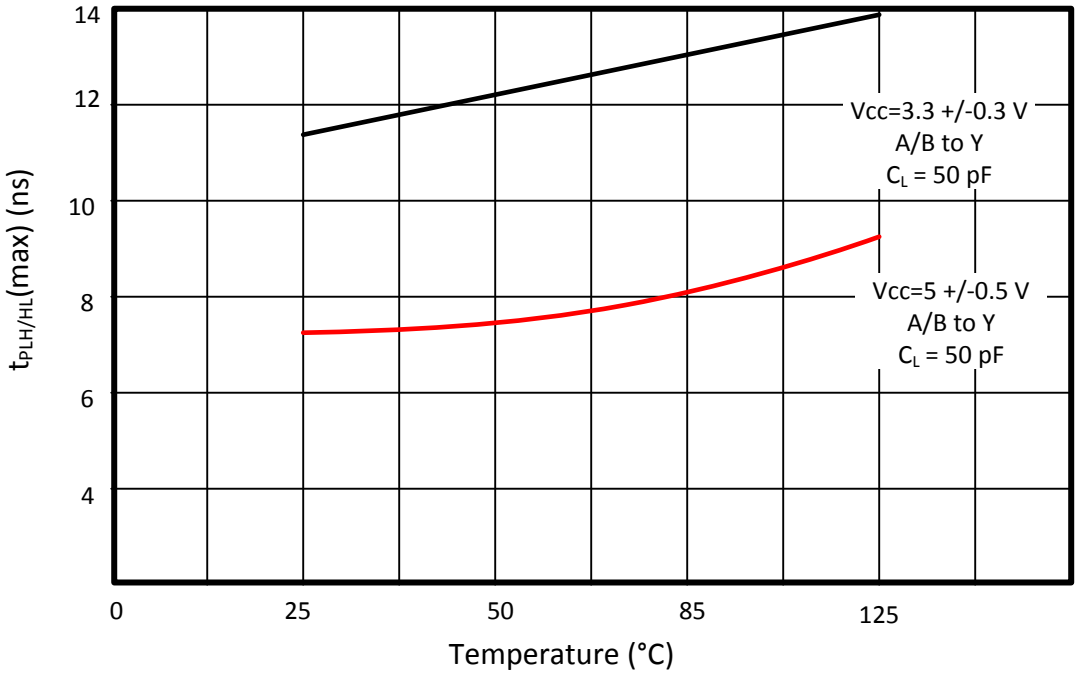
(1) Recommended T_A = –40°C to +125°C

6.8 Operating Characteristics

V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
C_{pd}	Power dissipation capacitance	No load, f = 1 MHz		9.5		pF

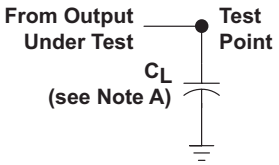
6.9 Typical Characteristics



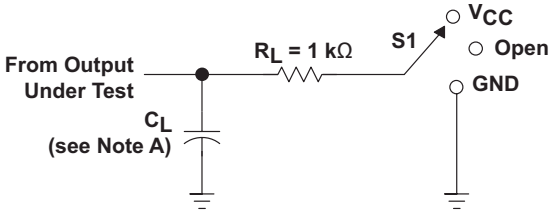
C_L = 50 pF

Figure 1. Propagation Delay vs Temperature

7 Parameter Measurement information

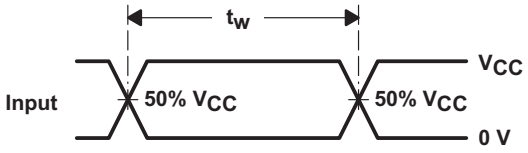


LOAD CIRCUIT FOR
TOTEM-POLE OUTPUTS

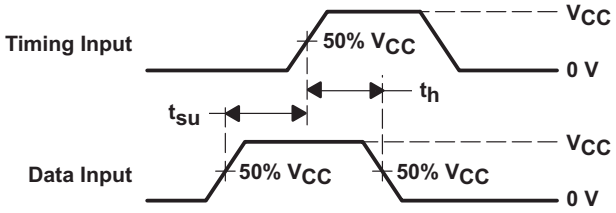


LOAD CIRCUIT FOR
3-STATE AND OPEN-DRAIN OUTPUTS

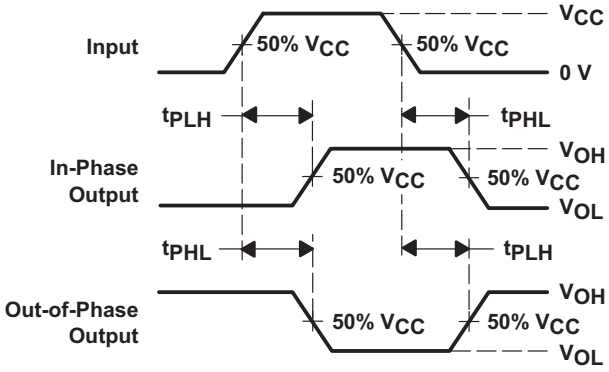
TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	V_{CC}
t_{PHZ}/t_{PZH}	GND
Open Drain	V_{CC}



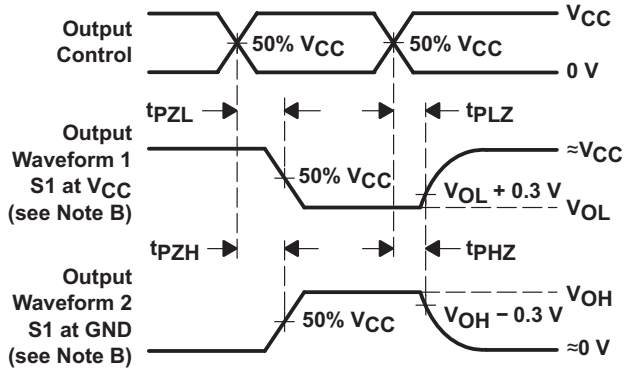
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

A. C_L includes probe and jig capacitance.

B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control.
Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.

C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O = 50 Ω, t_r ≤ 3 ns, t_f ≤ 3 ns.

D. The outputs are measured one at a time with one input transition per measurement.

E. All parameters and waveforms are not applicable to all devices.

Figure 2. Load Circuit and Voltage Waveforms

8 Detailed Description

8.1 Overview

The SN74AHC1G00 device performs the NAND Boolean function $Y = \overline{A \times B}$ or $Y = \overline{A} + \overline{B}$ in positive logic. The device has a wide operating range of V_{CC} from 2 V to 5 V.

8.2 Functional Block Diagram

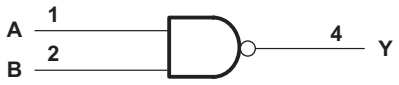


Figure 3. Logic Diagram (Positive Logic)

8.3 Feature Description

The SN74AHC1G00 device has wide operating voltage range for logic system from 2 V to 5 V. The low propagation delay allows fast switching and higher speeds of operation. In addition, the low power consumption of 10-uA (maximum) makes this device a good choice for portable and battery power-sensitive applications. The Schmitt trigger action on all inputs have noise rejection capabilities.

8.4 Device Functional Modes

Table 1 lists the functions of the SN74AHC1G00 device.

Table 1. Function Table

INPUTS		OUTPUT
A	B	Y
H	H	L
L	X	H
X	L	H

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The SN74AHC1G00 device is a low-drive CMOS device with 8-mA output drive at 5 V. It can be used for a multitude of bus interface type applications where output ringing is a concern. The low drive and slow edge rates minimizes overshoot and undershoot on the outputs. The NAND gates are used to build simple SR flip flop. They could be used in removing noise from a switch debounce circuit

9.2 Typical Application

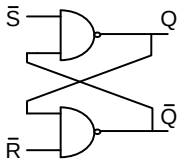


Figure 4. Typical Application

9.2.1 Design Requirements

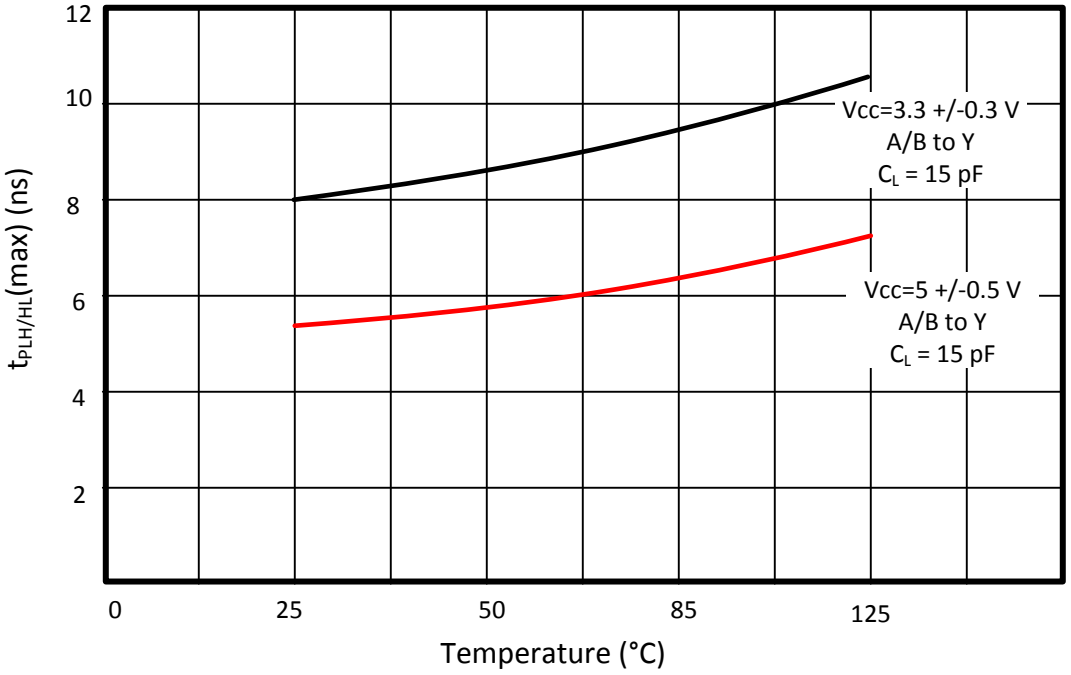
This SN74AHC1G00 device uses CMOS technology and has balanced output drive. Take care to avoid bus contention becuase it can drive currents that would exceed maximum limits. The high drive also creates fast edges into light loads. Routing and load conditions must be considered to prevent ringing.

9.2.2 Detailed Design Procedure

- Recommended input conditions:
  - Specified high and low levels. See V_{IH} and V_{IL} in *Recommended Operating Conditions*.
  - Inputs are overvoltage tolerant allowing them to go as high as 5.5 V at any valid V_{CC}.
- Recommended output conditions:
  - Load currents must not exceed 25 mA per output and 50 mA total for the part.
  - Outputs should not be pulled above V_{CC}.

Typical Application (continued)

9.2.3 Application Curve



C_L = 15 pF

Figure 5. Propagation Delay vs Temperature

10 Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating located in the *Recommended Operating Conditions*.

Each V_{CC} terminal should have a good bypass capacitor to prevent power disturbance. For devices with a single supply, TI recommends a 0.1-µF capacitor; if there are multiple V_{CC} terminals, then TI recommends a 0.01-µF or 0.022-µF capacitor for each power terminal. Multiple bypass capacitors can be paralleled to reject different frequencies of noise. Frequencies of 0.1 µF and 1 µF are commonly used in parallel. The bypass capacitor must be installed as close as possible to the power terminal for best results.

11 Layout

11.1 Layout Guidelines

When using multiple bit logic devices inputs must not ever float.

In many cases, functions or parts of functions of digital logic devices are unused. For example, when only two inputs of a triple-input AND gate are used or only three of the four buffer gates are used. Such input pins must not be left unconnected because the undefined voltages at the outside connections result in undefined operational states. The following are the rules must be observed under all circumstances.

All unused inputs of digital logic devices must be connected to a high or low bias to prevent them from floating. The logic level that should be applied to any particular unused input depends on the function of the device. Generally they will be tied to GND or V_{CC} whichever make more sense or is more convenient. Floating outputs is generally acceptable, unless the part is a transceiver. If the transceiver has an output enable pin, it disables the outputs section of the part when asserted. This does not disable the input section of the input and output, so they also cannot float when disabled.

11.2 Layout Example

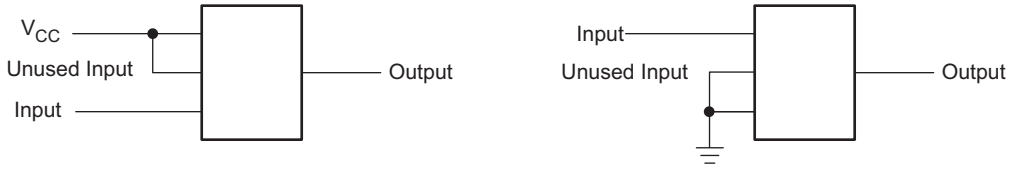


Figure 6. Layout Recommendation

12 Device and Documentation Support

12.1 Documentation Support

12.1.1 Related Documentation

For related documentation see the following:

- *Introduction to Logic*, SLVA700
- *Implications of Slow or Floating CMOS Inputs*, SCBA004

12.2 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.3 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

12.4 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

12.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN74AHC1G00DBVR	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	(A003 ~ A00G ~ A00L ~ A00S)	Samples
SN74AHC1G00DBVRE4	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	(A003 ~ A00G ~ A00L ~ A00S)	Samples
SN74AHC1G00DBVRG4	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	(A003 ~ A00G ~ A00L ~ A00S)	Samples
SN74AHC1G00DBVT	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	(A003 ~ A00G ~ A00L ~ A00S)	Samples
SN74AHC1G00DBVTG4	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	(A003 ~ A00G ~ A00L ~ A00S)	Samples
SN74AHC1G00DCKR	ACTIVE	SC70	DCK	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	(AA3 ~ AAG ~ AAL ~ AAS)	Samples
SN74AHC1G00DCKRE4	ACTIVE	SC70	DCK	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	(AA3 ~ AAG ~ AAL ~ AAS)	Samples
SN74AHC1G00DCKRG4	ACTIVE	SC70	DCK	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	(AA3 ~ AAG ~ AAL ~ AAS)	Samples
SN74AHC1G00DCKT	ACTIVE	SC70	DCK	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	(AA3 ~ AAG ~ AAL ~ AAS)	Samples
SN74AHC1G00DCKTG4	ACTIVE	SC70	DCK	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	(AA3 ~ AAG ~ AAL ~ AAS)	Samples
SN74AHC1G00DRLR	ACTIVE	SOT-OTHER	DRL	5	4000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	(AAB ~ AAS)	Samples
SN74AHC1G00HDCK3	OBSOLETE	SC70	DCK	5		TBD	Call TI	Call TI	-40 to 125		

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

OTHER QUALIFIED VERSIONS OF SN74AHC1G00 :

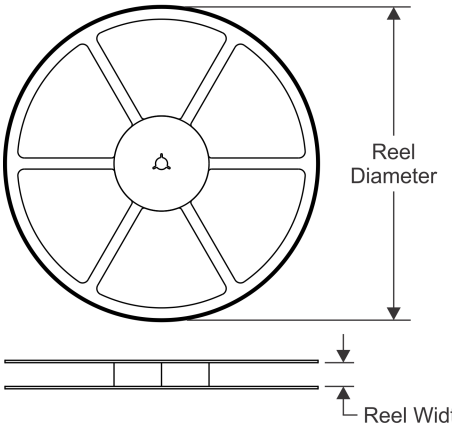
- Automotive: SN74AHC1G00-Q1

NOTE: Qualified Version Definitions:

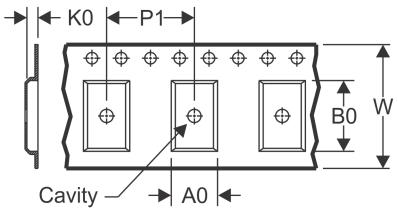
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION

REEL DIMENSIONS

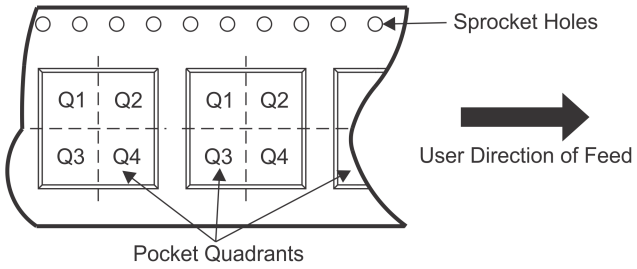


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

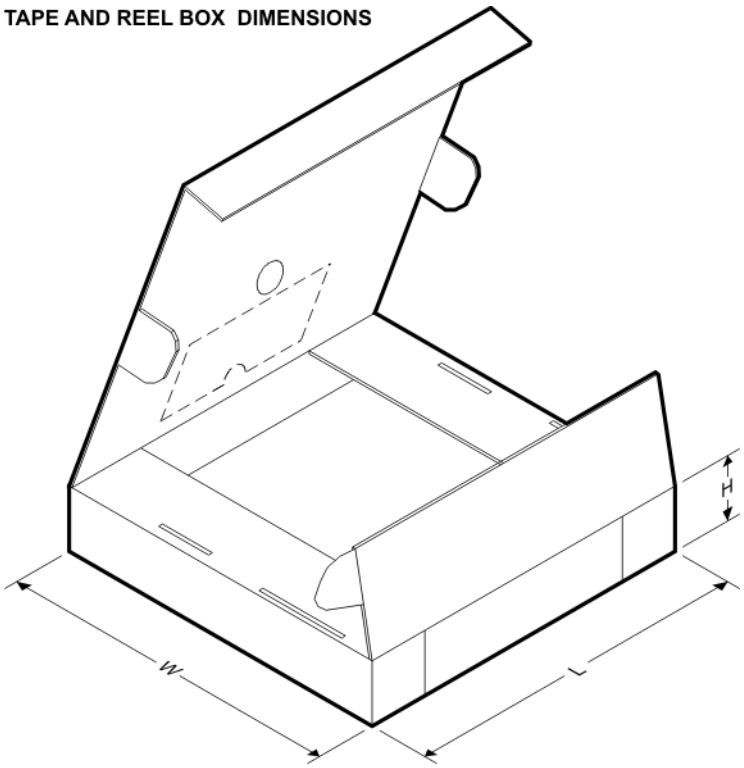
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

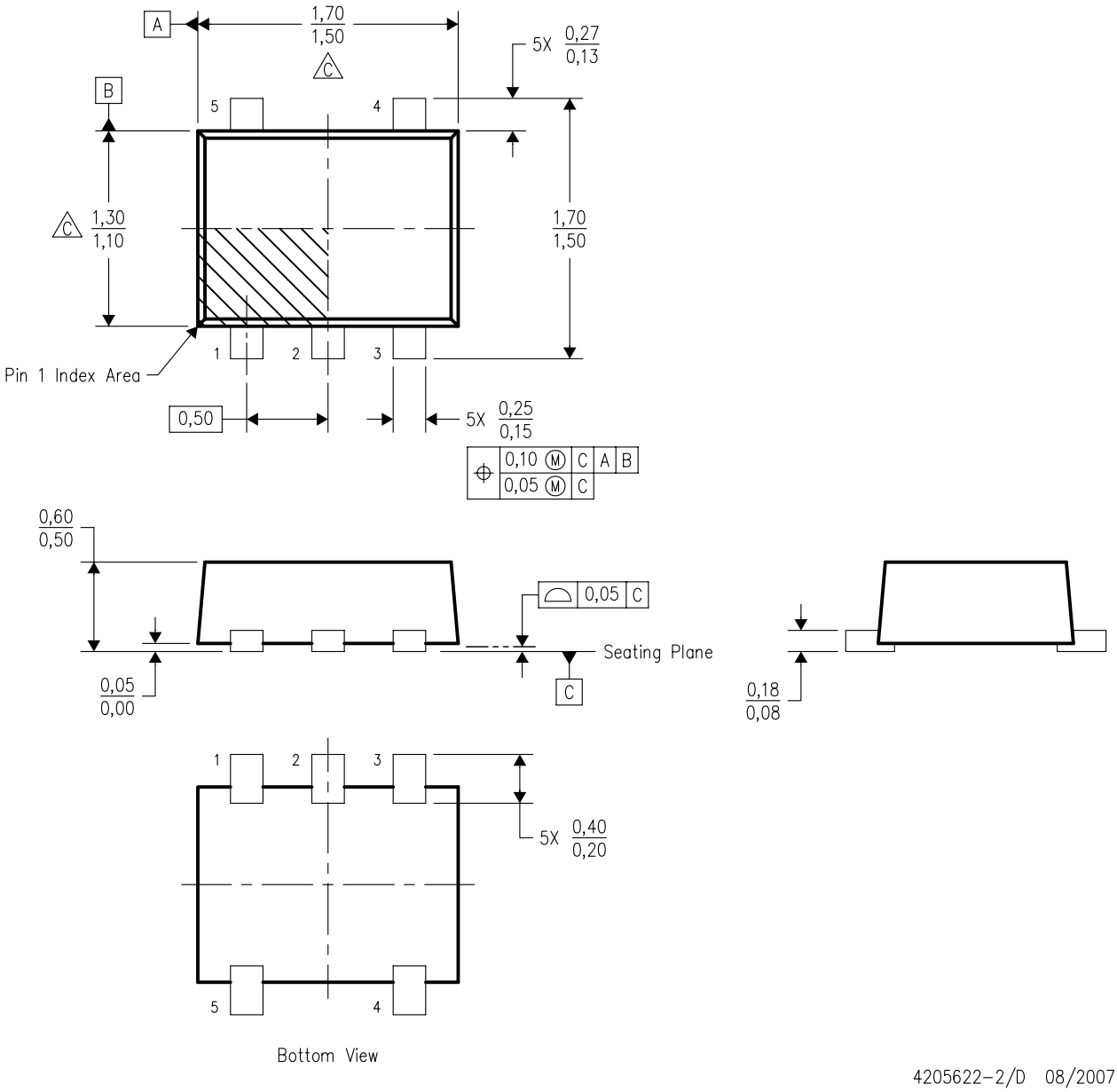
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74AHC1G00DBVR	SOT-23	DBV	5	3000	180.0	8.4	3.23	3.17	1.37	4.0	8.0	Q3
SN74AHC1G00DBVR	SOT-23	DBV	5	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
SN74AHC1G00DBVT	SOT-23	DBV	5	250	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
SN74AHC1G00DCKR	SC70	DCK	5	3000	180.0	8.4	2.47	2.3	1.25	4.0	8.0	Q3
SN74AHC1G00DCKR	SC70	DCK	5	3000	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3
SN74AHC1G00DCKR	SC70	DCK	5	3000	178.0	9.2	2.4	2.4	1.22	4.0	8.0	Q3
SN74AHC1G00DCKT	SC70	DCK	5	250	178.0	9.2	2.4	2.4	1.22	4.0	8.0	Q3
SN74AHC1G00DCKT	SC70	DCK	5	250	180.0	9.2	2.3	2.55	1.2	4.0	8.0	Q3
SN74AHC1G00DCKT	SC70	DCK	5	250	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3
SN74AHC1G00DRLR	SOT-OTHER	DRL	5	4000	180.0	9.5	1.78	1.78	0.69	4.0	8.0	Q3
SN74AHC1G00DRLR	SOT-OTHER	DRL	5	4000	180.0	8.4	1.98	1.78	0.69	4.0	8.0	Q3

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

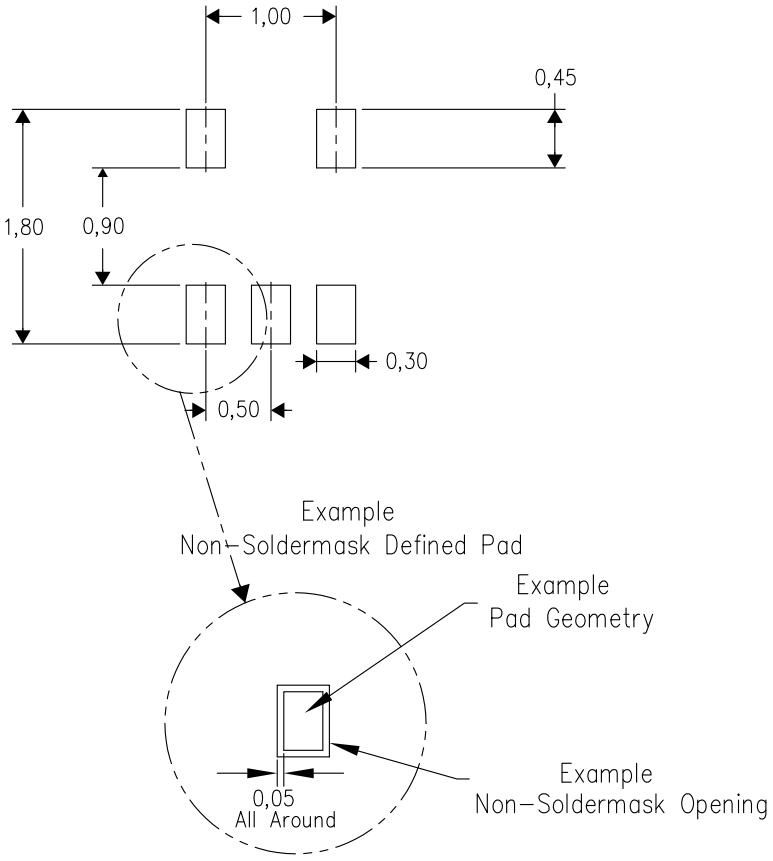
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74AHC1G00DBVR	SOT-23	DBV	5	3000	202.0	201.0	28.0
SN74AHC1G00DBVR	SOT-23	DBV	5	3000	180.0	180.0	18.0
SN74AHC1G00DBVT	SOT-23	DBV	5	250	180.0	180.0	18.0
SN74AHC1G00DCKR	SC70	DCK	5	3000	202.0	201.0	28.0
SN74AHC1G00DCKR	SC70	DCK	5	3000	180.0	180.0	18.0
SN74AHC1G00DCKR	SC70	DCK	5	3000	180.0	180.0	18.0
SN74AHC1G00DCKT	SC70	DCK	5	250	180.0	180.0	18.0
SN74AHC1G00DCKT	SC70	DCK	5	250	205.0	200.0	33.0
SN74AHC1G00DCKT	SC70	DCK	5	250	180.0	180.0	18.0
SN74AHC1G00DRLR	SOT-OTHER	DRL	5	4000	184.0	184.0	19.0
SN74AHC1G00DRLR	SOT-OTHER	DRL	5	4000	202.0	201.0	28.0



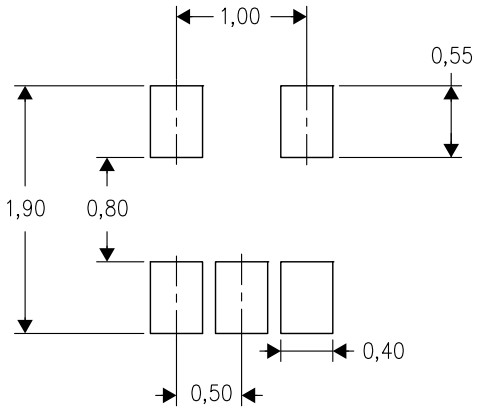
NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash, interlead flash, protrusions, or gate burrs. Mold flash, interlead flash, protrusions, or gate burrs shall not exceed 0,15 per end or side.
D. JEDEC package registration is pending.

DRL (R–PDSO–N5) PLASTIC SMALL OUTLINE

Example Board Layout



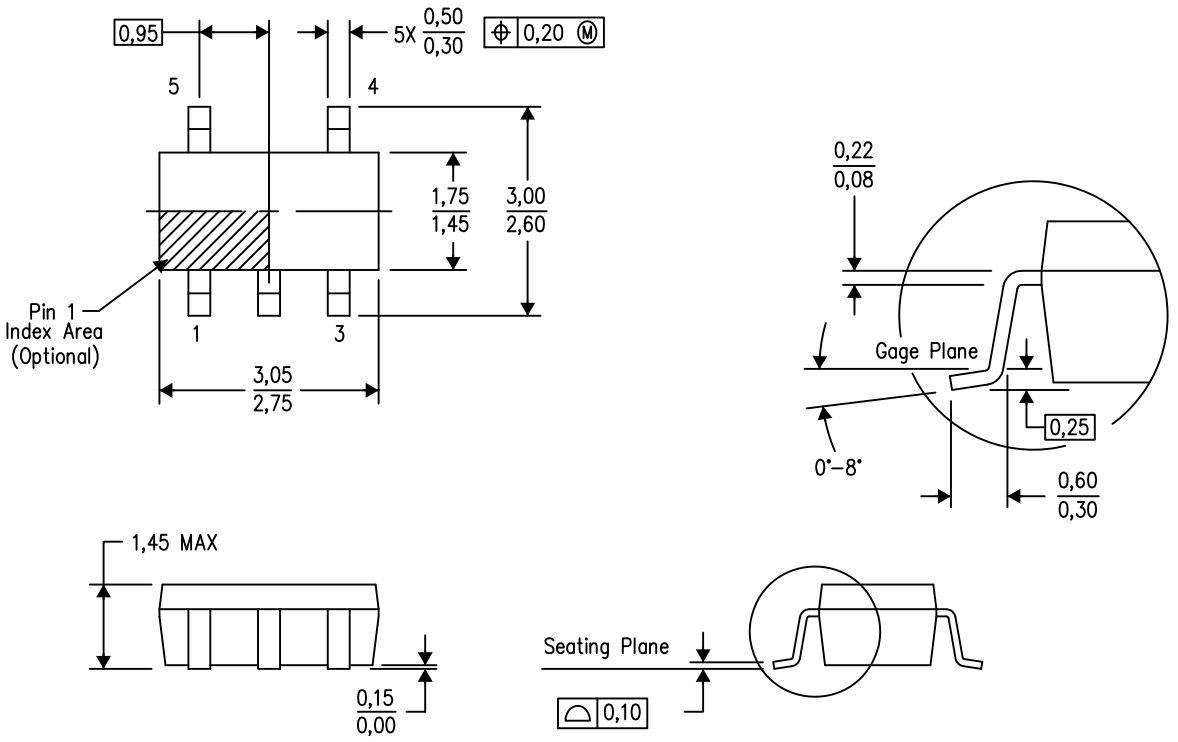
Example Stencil Design
(Note E)



4208207–2/E 06/12

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.
E. Maximum stencil thickness 0,127 mm (5 mils). All linear dimensions are in millimeters.
F. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
G. Side aperture dimensions over–print land for acceptable area ratio > 0.66. Customer may reduce side aperture dimensions if stencil manufacturing process allows for sufficient release at smaller opening.

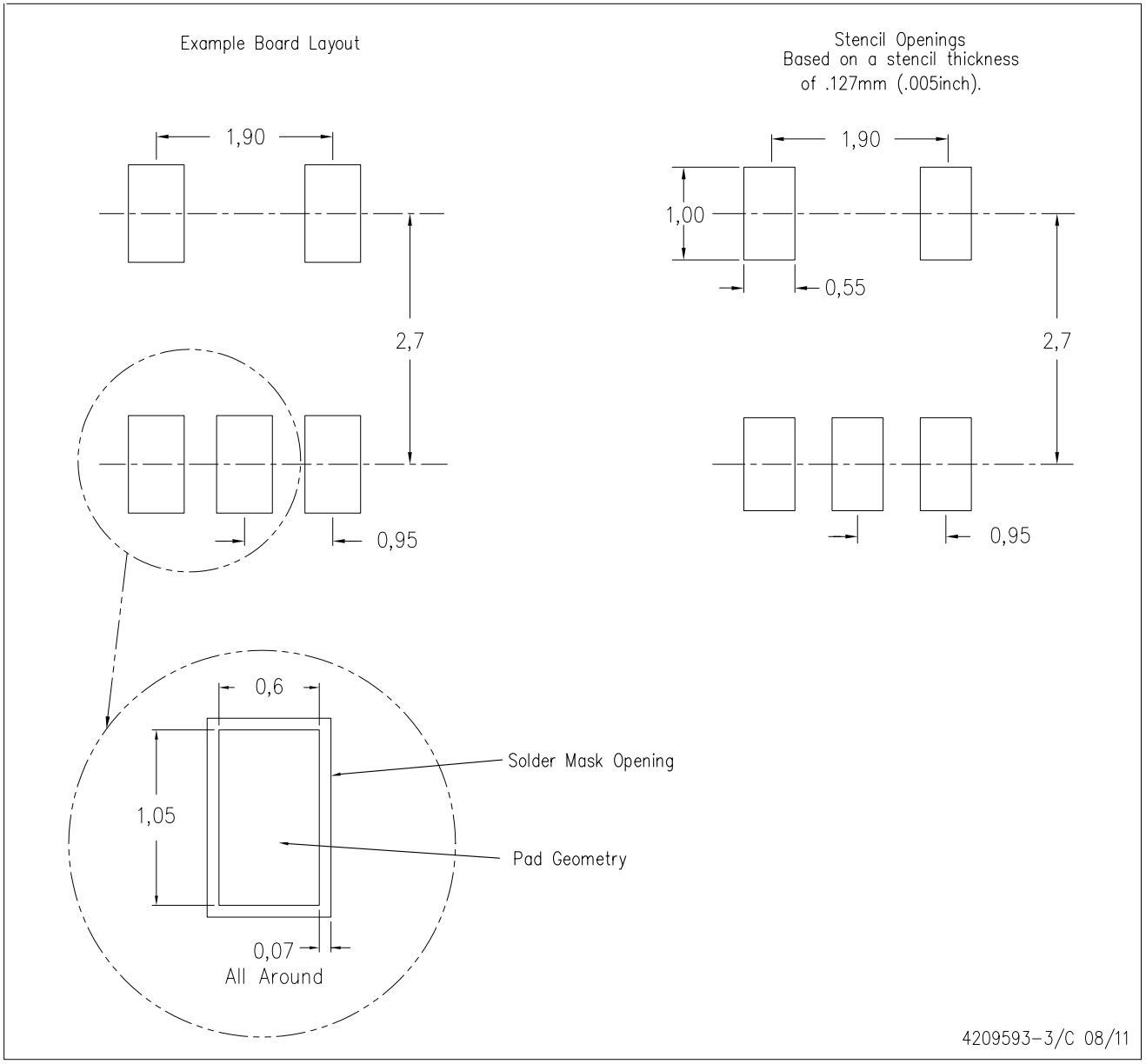
DBV (R–PDSO–G5) PLASTIC SMALL–OUTLINE PACKAGE



4073253–4/N 12/14

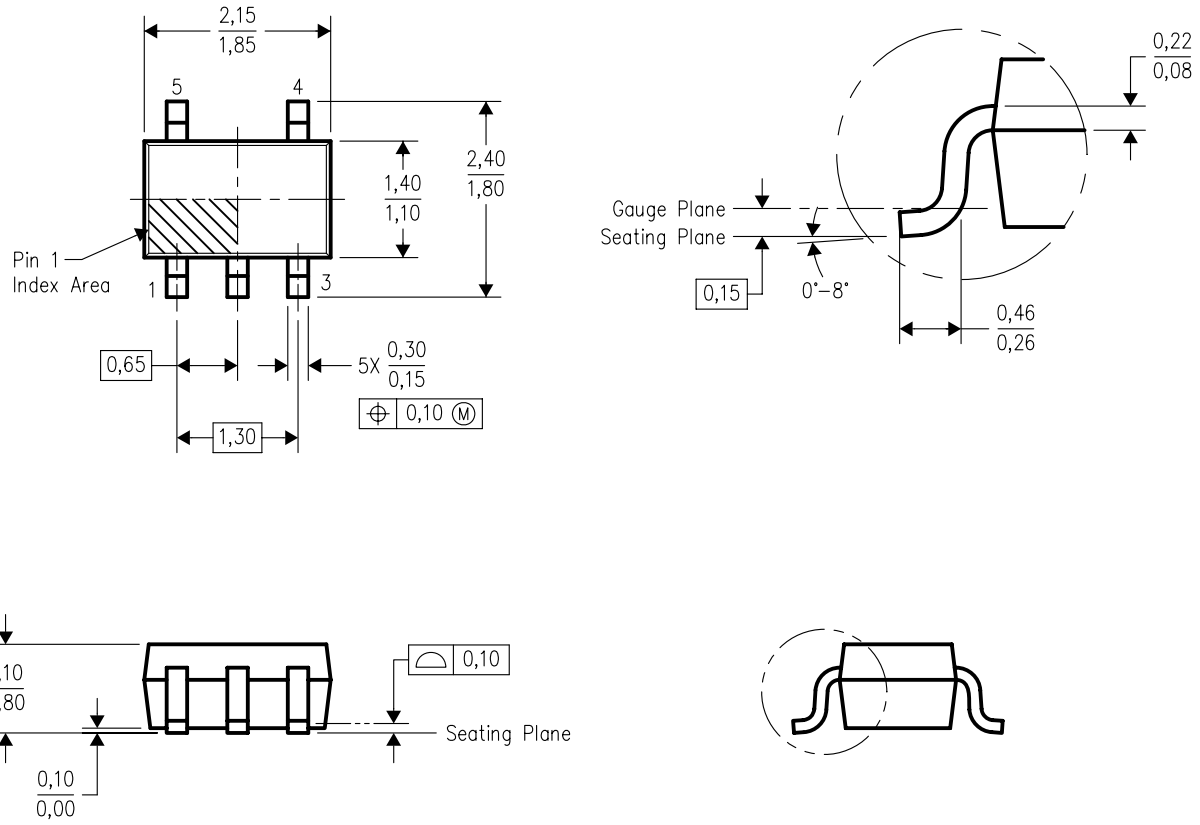
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
D. Falls within JEDEC MO–178 Variation AA.

DBV (R–PDSO–G5) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
D. Publication IPC–7351 is recommended for alternate designs.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.

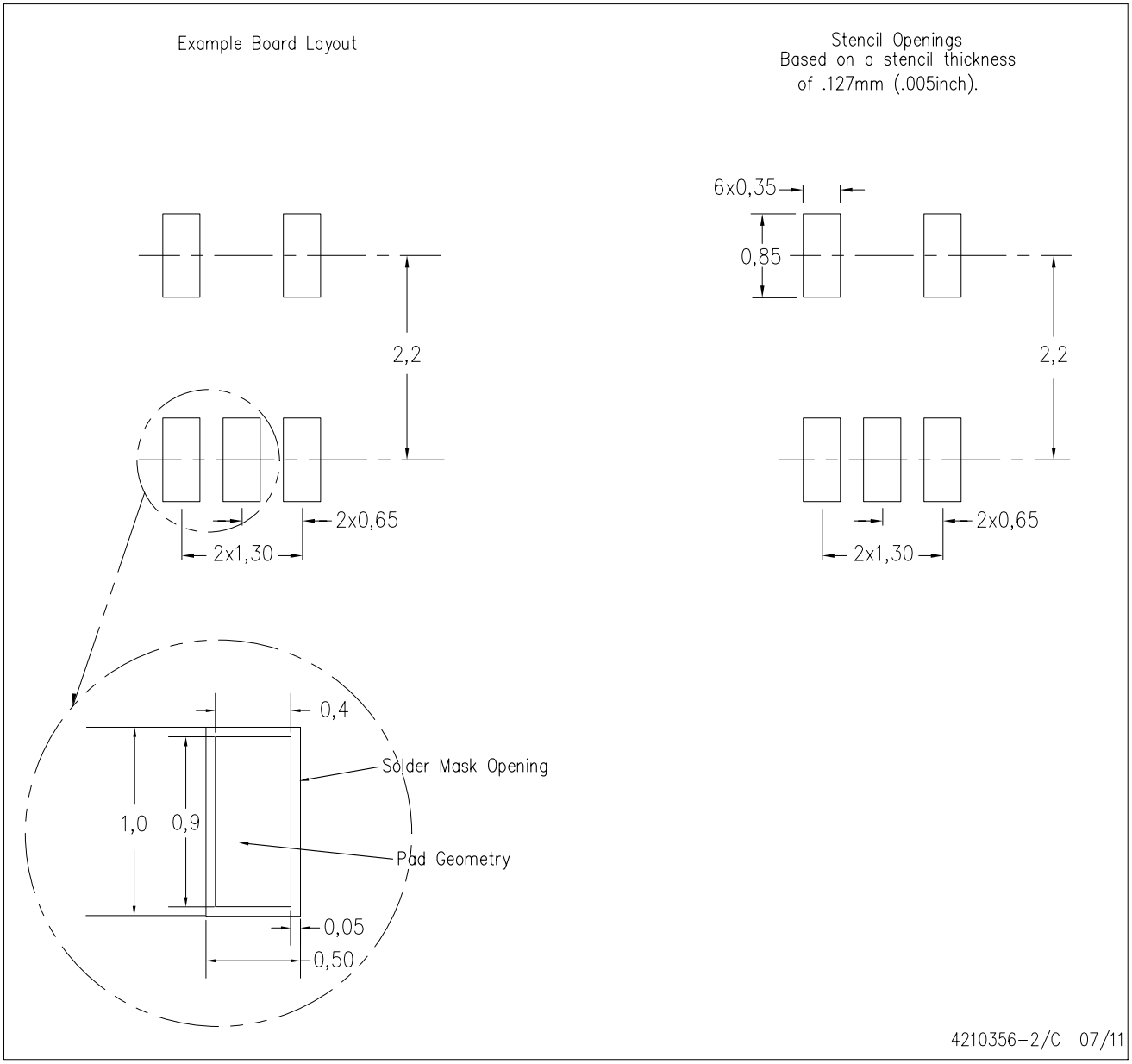
DCK (R–PDSO–G5) PLASTIC SMALL–OUTLINE PACKAGE



4093553–3/G 01/2007

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
D. Falls within JEDEC MO–203 variation AA.

DCK (R–PDSO–G5) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
D. Publication IPC–7351 is recommended for alternate designs.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.

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