

## Recommended Usage of Microchip SPI Serial EEPROM Devices

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### INTRODUCTION

The majority of embedded control systems require nonvolatile memory. Because of their small footprint, byte level flexibility, low I/O pin requirement, low-power consumption and low cost, serial EEPROMs are a popular choice for nonvolatile storage. Microchip Technology has addressed this need by offering a full line of serial EEPROMs covering industry standard serial communication protocols for two-wire ( $I^2C^{TM}$ ), three-wire (Microwire), and SPI communication. Serial EEPROM devices are available in a variety of densities, operational voltage ranges and packaging options.

In order to achieve a highly robust application when utilizing serial EEPROMs, the designer must consider more than just the data sheet specifications.

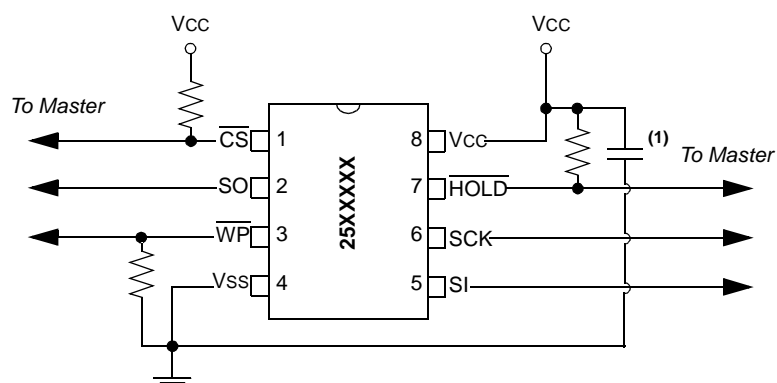
There are a number of conditions which could potentially result in nonstandard operation. The details of such conditions depend greatly upon the serial protocol being used.

This application note provides assistance and guidance with the use of Microchip SPI serial EEPROMs. These recommendations are not meant as requirements; however, their adoption will lead to a more robust overall design. The following topics are discussed:

- Input Considerations
- Write-Protection Features
- Power Supply
- Write Enable and Disable
- WIP Polling
- Increasing Data Throughput

Figure 1 shows the suggested connections for using Microchip SPI serial EEPROMs. The basis for these connections will be explained in the sections which follow.

**FIGURE 1: RECOMMENDED CONNECTIONS FOR 25XXXX SERIES DEVICES**



**Note 1:** A decoupling capacitor (typically 0.1  $\mu F$ ) should be used on VCC.

## INPUT CONSIDERATIONS

It is never good practice to leave an input pin floating. This can cause high standby current as well as undesired functionality. If a pin is left floating, it can either float low or high. Which direction the signal goes is dependant upon a number of factors, including noise in the system and capacitive coupling. Because of this, the level seen by the input circuitry is relatively random and likely to change during operation.

Such unpredictable input levels can have devastating effects on device operation. For example, Microchip's SPI serial EEPROMs feature a HOLD pin which allows the user to suspend the clock mid-stream. If this pin were to float low (active), the device would no longer react to any clock pulses received and communication would be disrupted.

Therefore, any unused input pins should always be tied to a proper level, such as high for an active-low input. Moreover, it is recommended that, if the microcontroller has extra, tri-state I/O pins available, connections be made to these unused inputs along with a pull-down/pull-up resistor, as shown in Figure 1. This will allow for the inputs to be used at a later date simply by modifying firmware.

Although the  $\overline{\text{CS}}$  pin should always be driven by the microcontroller during normal operation, it has potential for floating during power-down/power-up. As such, this pin should also have a pull-up resistor to avoid undesired commands due to noise during these conditions.

## WRITE PROTECTION FEATURES

There are two different write protection schemes featured in Microchip's SPI serial EEPROM family of devices. One for the 4 Kb and smaller devices, and one for 8 Kb and larger devices.

For the 25XX010A to 25XX040A, the  $\overline{\text{WP}}$  pin acts as a normal hardware write-protect pin. That is, if the  $\overline{\text{WP}}$  pin is low (active), the Write Enable Latch (WEL) is cleared and cannot be set until the pin is brought high (inactive). This means that any attempted writes to either the array or the STATUS register will be blocked. Note that bringing the  $\overline{\text{WP}}$  pin high does not set the WEL again. Another WREN instruction is required in order to do this.

For the 25XX080A/B and up, the  $\overline{\text{WP}}$  pin acts in conjunction with the Write-Protect Enable (WPEN) bit in the STATUS register. If the WPEN bit is cleared, the  $\overline{\text{WP}}$  pin is a don't care. If the WPEN bit is set, the  $\overline{\text{WP}}$  pin can be used to block attempted STATUS register writes. Note that for these devices, the  $\overline{\text{WP}}$  pin has no effect on array writes, regardless of the state of the WPEN bit. Only the Block Protect (BP) bits can block an attempted write to the array on these devices. Once the BP bits have been set, however, the  $\overline{\text{WP}}$  pin can be used with the WPEN bit to prevent them from being cleared, thus preventing writes to the array as well.

## POWER SUPPLY

Microchip serial EEPROMs feature a high amount of protection from unintentional writes and data corruption while power is within normal operating levels. But certain considerations should be made regarding power-up and power-down conditions to ensure the same level of protection during those times when power is not within normal operating levels.

As shown in Figure 1, a decoupling capacitor (typically 0.1  $\mu\text{F}$ ) should be used to help filter out small ripples on VCC.

### Power-Up

On power-up, VCC should always begin at 0V and rise straight to its normal operating level to ensure a proper Power-on Reset. VCC should not linger at an ambiguous level (i.e., below the minimum operating voltage).

### Brown-Out Conditions

For added protection, Microchip serial EEPROMs feature a Brown-out Reset circuit. However, if VCC happens to fall below the minimum operating voltage for the serial EEPROM, it is recommended that VCC be brought down fully to 0V before returning to normal operating level. This will help to ensure that the device is reset properly.

Furthermore, if the microcontroller features a Brown-out Reset with a threshold higher than that of the serial EEPROM, bringing VCC down to 0V will allow both devices to be reset together. Otherwise, the microcontroller may reset during communication while the EEPROM keeps its current state. In this case, a software Reset sequence would be required before beginning further communication.

### Power Failure During a Write Cycle

During a write cycle, VCC must remain above the minimum operating voltage for the entire duration of the cycle (typically 5 ms max. for most devices). If VCC falls below this minimum voltage at any point for any length of time, data integrity cannot be ensured. It will result in marginally programmed data that may or may not be correct. Furthermore, because the EEPROM cells were not able to be fully programmed, the device will have shorter data retention time than specified in the data sheet.

## WRITE ENABLE AND DISABLE

Microchip SPI serial EEPROMs feature a Write Enable Latch (WEL) as bit 1 of the STATUS register. This latch is used to allow write operations to occur to the array or STATUS register. When set to a '1', writes are enabled. When set to a '0', all writes are blocked. The WEL can only be set by issuing a valid Write Enable (WREN) instruction, but can be reset upon a number of conditions:

- Power-up
- Write Disable (WRDI) instruction successfully executed
- Write STATUS register (WRSR) instruction successfully executed
- Write instruction successfully executed

And on the 25XX010A-25XX040A only:

- $\overline{WP}$  pin is brought low (active)

Note that for the Write, WRSR, and WRDI instructions, the WEL is only reset if the instruction is executed successfully. This means that if, for some reason, the instruction is not valid, the WEL will not be reset. For example, if a write is attempted in an area of the array protected by the Block Protect (BP) bits, then the instruction will not succeed and the WEL will remain set.

For Write and WRSR instructions, the WEL is cleared at the end of the write cycle.

It is highly recommended that the WEL only be set immediately before issuing a Write or WRSR instruction in order to minimize the chance of an undesired write operation.

## WIP POLLING

Write operations on serial EEPROMs require that a write cycle time be observed after initiating the write, allowing the device time to store the data. During this time, normal device operation is disabled and any attempts by the master to access the memory array on the device will be ignored. Therefore, it is important that the master wait for the write cycle to end before attempting to access the EEPROM again.

Each device has a specified worst-case write cycle time, typically listed as TWC. A simple method for ensuring that the write cycle time is observed is to perform a delay for the amount of time specified before accessing the EEPROM again. However, it is not uncommon for a device to complete a write cycle in less than the maximum specified time. As such, using the previously shown delay method results in a period of time in which the EEPROM has finished writing, but the master is still waiting.

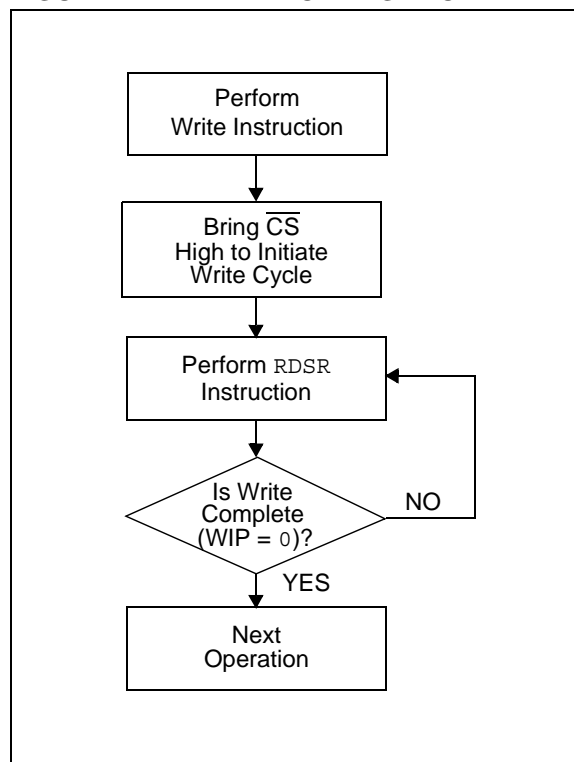
In order to eliminate this extra period of time, and therefore operate more efficiently, it is highly recommended to take advantage of the WIP Polling feature.

During both an array write and a STATUS register write, the STATUS register in Microchip's SPI serial EEPROMs can still be read. This allows the user to check the state of the Write-In-Progress (WIP) bit. This is a read-only bit, set only while a write operation is in progress. Once the operation completes, the WIP (and the WEL) are cleared. Therefore, the STATUS register can continue to be read in order to monitor the value of the WIP bit to determine when the write cycle completes.

## Procedure

Once  $\overline{CS}$  is brought high at the end of the Write instruction, the device initiates the internally timed write cycle, and WIP polling can begin immediately. This involves performing a Read STATUS register (RDSR) instruction and checking the value read for the WIP bit. If it is high, the device is still writing. If it is low, the write cycle is complete and the master can proceed with the next instruction. See Figure 2 for details.

**FIGURE 2: WIP POLLING FLOW**



## INCREASING DATA THROUGHPUT

### Page Writes

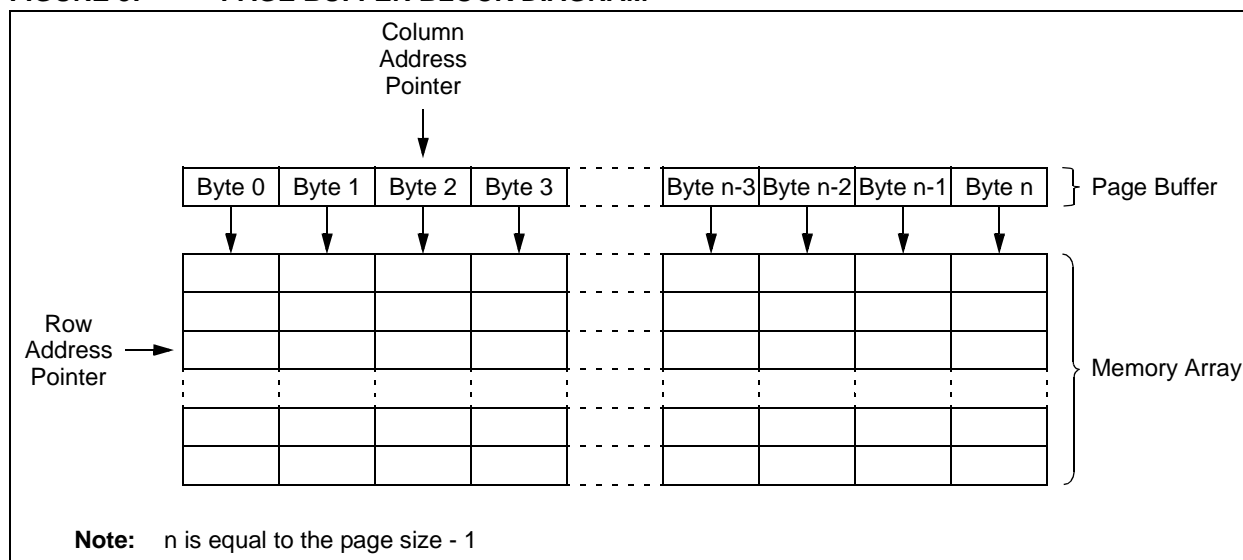
All Microchip SPI serial EEPROMs feature a page buffer for use during write operations. This allows the user to write any number of bytes from one to the maximum page size in a single operation. This can provide for a significant decrease in the total write time when writing a large number of bytes.

Page write operations are limited to writing within a single physical page, regardless of the number of bytes actually being written. This is because the memory array is physically stored as a two-dimensional array, as shown in Figure 3. When the word address is given at the beginning of a write operation, both the row and

column Address Pointers are set. The row Address Pointer selects which row, or page, is accessed, whereas the column Address Pointer selects which byte from the chosen page is accessed first. Upon transmission of each data byte, the column Address Pointer is automatically incremented. However, during a write operation, the page Address Pointer is not incremented, which means that attempting to cross a page boundary during a page write operation will result in the data being looped back to the beginning of the page.

Note that physical page boundaries start at addresses that are multiples of the page size. For example, the 25XX256 features a 64-byte page size, which means that physical pages on the device begin at addresses 0x0000, 0x0040, 0x0080, and so on.

**FIGURE 3: PAGE BUFFER BLOCK DIAGRAM**



### Procedure

After enabling writes by issuing a WREN command, the write instruction, word address, and the first data byte are transmitted to the device in the same way as in a byte write operation. But instead of toggling  $\overline{CS}$  high, the master continues transmitting additional data bytes, which are temporarily stored in the on-chip page buffer, up to the maximum page size of the device (with care being taken not to wrap around the page). As with the byte write operation, once  $\overline{CS}$  is toggled high, an internal write cycle will begin during which all bytes stored in the page buffer will be written.

### Write Time Comparisons

In order to accurately calculate the full period of time required to write a particular amount of data to a device, two things must be considered.

- **Load time** is the amount of time needed to complete all bus operations. This includes all  $\overline{CS}$ -related timings, issuing the necessary WREN instructions, as well as transmitting the Write instruction, address and data bytes. This amount of time is dependent on the bus clock speed, the number of data bytes to be written, and the addressing scheme of the particular device (some devices utilize a 1-byte address, whereas others use a 2-byte address).

- **Write cycle time** is the time during which the device is executing its internal write cycle. As described in the previous section ("WIP Polling"), there is a specified maximum write cycle time for each device. However, the internal write cycle typically completes in less time than specified. As such, both worst-case (5 ms) and typical (3 ms at T<sub>AMB</sub> = 25 °C) calculations are provided in Table 1.

The following equations were used to calculate the values for Table 1:

#### EQUATION 1: WRITE TIME EQUATIONS

$$T_{\text{LOAD}} = \frac{8 \cdot (2 + \# \text{ addr bytes} + \# \text{ data bytes})}{F_{\text{CLK}}} + 150 \text{ ns}$$

$$T_{\text{TOTAL}} = (T_{\text{LOAD}} + T_{\text{WC}}) \cdot \# \text{ write operations}$$

**TABLE 1: WRITE TIME COMPARISONS**

Device	Page Size (bytes)	# of Bytes to Write	Write Mode <sup>(1)</sup>	Clock Speed (MHz)	Load Time Per Operation (μs)	Total Time (ms) Worst-Case <sup>(2)</sup>	Total Time (ms) Typical <sup>(3)</sup>
25LC010A	16	1	Byte	1	32.15	5.03	3.03
		16	Byte	1	32.15	80.51	48.51
		16	Page	1	152.15	5.15	3.15
		1	Byte	10	3.35	5.00	3.00
		16	Byte	10	3.35	80.05	48.05
		16	Page	10	15.35	5.02	3.02
25LC160B	32	1	Byte	1	40.15	5.04	3.04
		32	Byte	1	40.15	161.28	97.28
		32	Page	1	288.15	5.29	3.29
		1	Byte	10	4.15	5.00	3.00
		32	Byte	10	4.15	160.13	96.13
		32	Page	10	28.95	5.03	3.03
25LC256	64	1	Byte	1	40.15	5.04	3.04
		64	Byte	1	40.15	322.57	194.57
		64	Page	1	544.15	5.54	3.54
		1	Byte	10	4.15	5.00	3.00
		64	Byte	10	4.15	320.27	192.27
		64	Page	10	54.55	5.05	3.05

**Note 1:** Byte Write mode signifies that only 1 byte is written during a single write operation.

Page Write mode signifies that a full page is written during a single write operation.

**2:** Worst-case calculations assume a 5 ms timed delay is used.

**3:** Typical calculations assume WIP polling is used, with typical T<sub>WC</sub> = 3 ms, T<sub>AMB</sub> = 25 °C.

From these examples, it is clear that both page writes and WIP polling can provide significant time savings. Writing 64 bytes to the 25LC256 via byte writes at 1 MHz requires roughly 320 ms worst-case. Switching to WIP polling brings that down to roughly 192 ms (assuming typical conditions), nearly a 40% decrease. Additionally, changing to page writes further lowers the time to an impressive 3.05 ms, a decrease of over 98%. Overall, the two techniques provide a combined time savings of over 317 ms, increasing the total data throughput a staggering 105 times over.

## SUMMARY

This application note illustrates recommended techniques for increasing design robustness when using Microchip SPI serial EEPROMs. These recommendations fall directly in line with how Microchip designs, manufactures, qualifies and tests its serial EEPROMs and will allow the devices to operate within the data sheet parameters. It is suggested that the concepts detailed in this application note be incorporated into any system which utilizes an SPI serial EEPROM.

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NOTES:

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**Note the following details of the code protection feature on Microchip devices:**

- Microchip products meet the specification contained in their particular Microchip Data Sheet.
- Microchip believes that its family of products is one of the most secure families of its kind on the market today, when used in the intended manner and under normal conditions.
- There are dishonest and possibly illegal methods used to breach the code protection feature. All of these methods, to our knowledge, require using the Microchip products in a manner outside the operating specifications contained in Microchip's Data Sheets. Most likely, the person doing so is engaged in theft of intellectual property.
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