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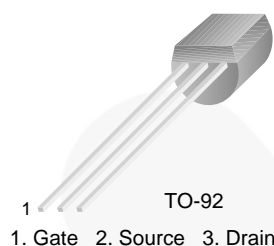
November 2014

BF256B

N-Channel RF Amplifiers

Features

- This device is designed for VHF / UHF amplifiers
- Sourced from process 50



Ordering Information

Part Number	Top Mark	Package	Packing Method
BF256B	BF256B	TO-92 3L	Bulk

Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only. Values are at $T_A = 25^\circ\text{C}$ unless otherwise noted.

Symbol	Parameter	Value	Unit
V_{DG}	Drain-Gate Voltage	30	V
V_{GS}	Gate-Source Voltage	-30	V
I_{GF}	Forward Gate Current	10	mA
T_J, T_{STG}	Operating and Storage Temperature Range	-55 to 150	$^\circ\text{C}$

Thermal Characteristics

Values are at $T_A = 25^\circ\text{C}$ unless otherwise noted.

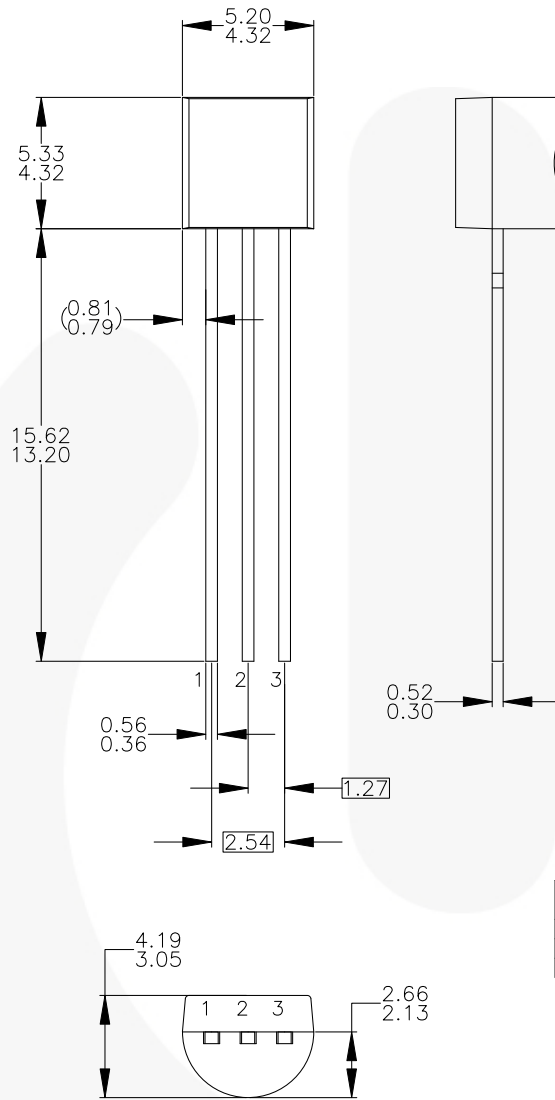
Symbol	Parameter	Value	Unit
P_D	Total Device Dissipation at $T_A = 25^\circ\text{C}$	350	mW
	Derate Above 25°C	2.8	mW/ $^\circ\text{C}$

Electrical Characteristics

Values are at $T_A = 25^\circ\text{C}$ unless otherwise noted.

Symbol	Parameter	Conditions	Min.	Max.	Unit
$V_{(BR)GSS}$	Gate-Source Breakdown Voltage	$V_{DS} = 0, I_G = 1\ \mu\text{A}$	-30		V
V_{GS}	Gate-Source Voltage	$V_{DS} = 15\ \text{V}, I_D = 200\ \mu\text{A}$	-0.5	-7.5	V
$V_{GS(off)}$	Gate-Source Cut-Off Voltage	$V_{DS} = 15\ \text{V}, I_D = 10\ \text{nA}$	-0.5	-8.0	V
I_{GSS}	Gate Reverse Current	$V_{GS} = -20\ \text{V}, V_{DS} = 0$		-5	nA
I_{DSS}	Zero-Gate Voltage Drain Current	$V_{DS} = 15\ \text{V}, V_{GS} = 0$	6	13	mA
gfs	Common Source Forward Transconductance	$V_{DS} = 15\ \text{V}, V_{GS} = 0, f = 1\ \text{kHz}$	4.5		mmhos

Physical Dimensions



NOTES: UNLESS OTHERWISE SPECIFIED

- A) DRAWING WITH REFERENCE TO JEDEC TO-92 RECOMMENDATIONS.
- B) ALL DIMENSIONS ARE IN MILLIMETERS.
- C) DRAWING CONFORMS TO ASME Y14.5M-1994.
- D) TO-92 (92,94,96,97,98) PIN CONFIGURATION:

PIN	92			94			96			97			98		
	P	F	M	P	F	M	P	F	M	P	F	M	P	F	M
1	E	S	S	E	S	S	B	D	G	C	G	D	C	G	D
2	B	D	G	C	G	D	E	S	S	B	D	G	E	S	S
3	C	G	D	B	D	G	C	G	D	E	S	S	B	D	G

LEGEND:

P - BIPOLAR E - EMITTER D - DRAIN
F - JFET B - BASE S - SOURCE
M - DMOS C - COLLECTOR G - GATE

- E) FOR PACKAGE 92, 94, 96, 97 AND 98: PIN CONFIGURATION DRAIN "D" AND SOURCE "S" ARE INTERCHANGEABLE AT JFET "F" OPTION.
- F) DRAWING FILENAME: MKT-ZAO3DREV3.

Figure 1. 3-Lead, TO-92, JEDEC TO-92 Compliant Straight Lead Configuration



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No Identification Needed	Full Production	Datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve the design.
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