MSP432P401R Device Erratasheet

1 Revision History

For information about migrating from the XMS rev B silicon to the MSP rev C silicon, visit the XMS432 Support wiki.

✓ The check mark indicates that the issue is present in the specified revision.

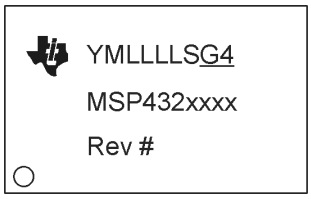
Errata Number	XMS Rev B	MSP Rev C
ADC44	✓	
ADC45	✓	
ADC46	✓	
ADC47	✓	
ADC48	✓	
ADC49	✓	
ADC51	✓	
ADC52	✓	
ADC53	✓	
ADC54	✓	
ADC55	✓	
ADC56	✓	
ADC57	✓	
ADC58	✓	
ADC59	✓	
ADC60	✓	
ADC61	✓	
ADC62	✓	
AES1	✓	
BSL13	✓	
BSL16	✓	✓
COMP8	✓	
COMP9	✓	
CS5	✓	
CS6	✓	
CS8	✓	
CS9	✓	
CS10	✓	
DMA12	✓	
FLASH38	✓	
FLASH39	✓	
FLASH40	✓	

Errata Number	XMS Rev B	MSP Rev C
FLASH41	✓	
PCM1	✓	
PCM2	✓	
PMAP2	✓	
PORT25	✓	
PORT27	✓	
PORT31	✓	✓
PORT32	✓	✓
PSS1	✓	
PSS2	✓	
PSS3	✓	
PSS4	✓	✓
REF3	✓	
REF4	✓	
REF7	✓	
REF8	✓	
REF9	✓	
RST1	✓	
RST2	✓	
RTC9	✓	
RTC11	✓	
RTC12	✓	
RTC13	✓	
SRAM1	✓	
SRAM2	✓	
SYS21	✓	
SYS26	✓	✓
SYSTICK1	✓	
USCI41	✓	
USCI42	✓	✓
WDG7	✓	

2 Package Markings

PZ100

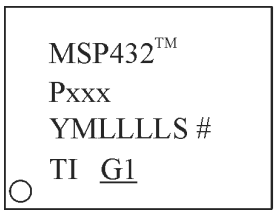
LQFP (PZ) 100 Pin



YM = Year and Month Date Code
S = Assembly Site Code
# = Die Revision
LLLL = Assembly Lot Code
○ = Pin 1

ZXH80

BGA, 80 Pin



YM = Year and Month Date Code
LLLL = Assembly Lot Code
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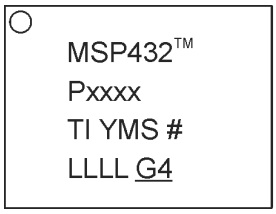
# = Die Revision
○ = Pin 1

RGC64

QFN (RGC), 64 pin



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3 Detailed Bug Description

ADC44 *ADC14 Module*

Function ADC stops converting during repeat-single-channel operation

Description The ADC module might hang if ADC14CTL0.ADC14ENC bit is reset during a repeat-single-channel operation. No subsequent triggers can start a conversion. Operation can only be restored after a module reset.

Workaround If a conversion needs to be stopped during a Repeat-Single-Channel conversion, reset both ADC14ENC & ADC14CONSEQ bits (ADC14CTL0.ADC14ENC = 0 & ADC14CTL0.ADC14CONSEQ =0) instead of just ADC14CTL0.ADC14ENC bit.

ADC45 *ADC14 Module*

Function Erroneous ADC busy bit value

Description ADC14CTL0.ADC14BUSY bit might not reflect true ADC busy state when the ADC is configured to use timer trigger source (ADC14CTL0.ADC14SHSx != 0) and the timer trigger arrives prior to ADC14CTL0.ADC14ENC bit being toggled.

Workaround 1. When timer is used as a trigger source, ensure to toggle the ADC14CTL0.ADC14ENC bit before the trigger arrives.

OR

2. Do not use ADC14CTL0.ADC14BUSY bit as completion indication. Instead use the conversion completion interrupt flag to service the interrupt upon conversion completion.

ADC46 *ADC14 Module*

Function Sequence of Channel conversion mode with temperature sensor and battery monitor

Description ADC Sequence & Repeat Sequence conversion modes generate wrong conversion results for all channels when either temperature sensor or battery monitor is selected as one of the channels in the sequence.

Workaround None.

ADC47 *ADC14 Module*

Function Byte write to ADC14MEMx registers

Description A byte write to ADC14MEMx register corrupts the entire 32-bit data content of the register.

Workaround None.

ADC48 *ADC14 Module*

Function Stopping sequence-of-channel conversion modes

Description In a sequence-of-channel or repeat-sequence-of-channel conversion mode, de-assertion of the ADC14CTL0.ADC14ENC bit stops ADC14 operation only at the end of a sequence of channels instead of at the end of the current channel conversion.

Workaround None.

ADC49 *ADC14 Module*

Function Switching reference in sequence-of-channel conversion modes

Description When an ADC sampling sequence (in either sequence-of-channel or repeated-sequence-of-channel mode) transitions from a channel using internal reference to a channel using external reference, ADC14RDYIFG is incorrectly set for the channel using external reference and the ADC conversion for this channel generates erroneous conversion result.

Workaround None.

ADC51 *ADC14 Module*

Function ADC operation with internal reference

Description When the ADC uses the internal reference buffer (ADC14MCTLx.ADC14VRSEL=1) in the buffer continuously on mode (ADC14CTL1.ADC14REFBURST=0), the reference buffer is unavailable for 5us after ADC14CTL0.ADC14ON and ADC14CTL0.ADC14ENC bits are set. ADC operation triggered before this 5us window will result in incorrect values.

Workaround Wait for 5us after ADC14CTL0.ADC14ON and ADC14CTL0.ADC14ENC bits are set before starting any ADC operation.

ADC52 *ADC14 Module*

Function ADC14IV register read

Description If ADC14IV register is read while another ADC14IFGx bit is being set, the ADC14IV read does not clear the ADC14IFGx bit.

Workaround Manually clear the ADC14IFGx bit in software.

ADC53 *ADC14 Module*

Function DMA request in repeat sequence of channel

Description ADC14 does not assert DMA request at the end of each sequence of conversions in a repeat sequence of channels mode of conversion, resulting in no DMA transfer triggered.

Workaround None.

ADC54 *ADC14 Module*

Function ADC window comparison incorrect result in signed binary data format

Description ADC14IFG1.ADC14LOIFG is erroneously set if:

1) When signed binary data format is selected (ADC14CTL1.ADC14DF=1)

AND

2) ADC14LOx threshold value and the ADC14 conversion result value are both negative

AND

3) Conversion result is greater than the ADC14LOx threshold value.

Similarly, ADC14IFG1.ADC14HIIFG is erroneously set if:

1) When signed binary data format is selected (ADC14CTL1.ADC14DF=1)

AND

2) ADC14HIx threshold value and conversion result are both negative

AND

3) Conversion result is lower than ADC14HIx threshold value.

Workaround None.

ADC55 *ADC14 Module*

Function REFOUT availability on pin during ADC operation

Description When the internal reference is output to a port pin (REFCTL0.REFOUT=1) and the ADC14 is converting an ADC channel using the AVCC reference, the ADC conversion results in incorrect values and the internal reference voltage is not available on the external REFOUT pin during ADC operation.

Workaround None.

ADC56 *ADC14 Module*

Function Extended sample pulse mode

Description In extended sample pulse mode (ADC14CTL0.ADC14SHP=0), ADC channel selection changes on the rising edge of the sample pulse. This may result in incorrect ADC conversion results. The issue occurs in single-conversion mode and only on the first conversion in a sequence or repeat mode of operations.

Workaround None.

ADC57 *ADC14 Module*

Function ADC operation in extended pulse sample mode

Description In low-speed ADC operation (ADC using 128-500kHz clock source) and extended pulse sample mode, conversion trigger might be missed during a time window consisting of the source oscillator starting up and two additional ADC cycles.

Workaround None.

ADC58 *ADC14 Module*

Function ADC14 ready flag not set in extended pulse mode in low-speed

Description ADC14 ready flag ADC14IFG1.ADC14RDYIFG does not get set after buffer is powered up when ADC is in buffered mode and extended pulse mode if the total time of (ADC clock start up time + 6 ADC clock cycles) exceeds 5us.

Workaround In extended pulse mode, delay 5us after sample time before de-asserting the trigger.

ADC59 *ADC14 Module*

Function ADC14MEMx registers writes with varying access sizes

Description Back-to-Back register writes to different ADC14MEMx registers with varying access sizes (any combinations of 32-bit, 16-bit, and 8-bit accesses) could corrupt the register data.

Workaround Always use the same access size when writing to ADC14MEMx registers back-to-back.

ADC60 *ADC14 Module*

Function Changing buffer mode in sequence-of-channel conversion modes

Description During a sequence of channel, the ADC conversion result for the second conversion of any consecutive pair will be erroneous if:

1) ADC14CTL0.ADC14SHP = 1 and ADC14CTL0.ADC14MSC = 1,

AND

2) The first channel in the consecutive pair uses non-buffered mode,

AND

3) The second channel in the consecutive pair uses buffered mode.

Workaround Add a dummy channel using buffered mode in between the two channels and disregard the conversion result for this dummy channel.

ADC61 *ADC14 Module*

Function Changing buffer mode in sequence-of-channel conversion modes

Description The ADC conversion results in a sequence or repeat sequence mode of operation will be erroneous if:

1) (ADC14CTL0.ADC14MSC = 0 and ADC14CTL1.ADC14REFBURST =0) or ADC14CTL0.ADC14MSC =1

AND

2) external reference buffered mode and internal reference modes used as consecutive channels

Workaround Add a dummy channel using buffered mode in between the two channels and disregard the conversion result for this dummy channel.

ADC62 *ADC14 Module*

Function Insufficient trigger width in extended sample mode

Description ADC can generate incorrect conversion results in extended sample mode, if the trigger width is less than:

1) 8 MODOSC cycles if MODOSC clock is already active (CSCLKEN.MODOSC_EN = 1).

OR

2) 8 MODOSC cyles + MODOSC startup time if MODOSC clock is not always on (CSCLKEN.MODOSC_EN = 0).

Workaround When using ADC in extended sample mode, ensure trigger width is equal or more than:

1) 8 MODOSC cycles if MODOSC clock is always on (CSCLKEN.MODOSC_EN = 1).

OR

2) MODOSC startup time + 8MODOSC cycles if MODOSC clock is not always on (CSCLKEN.MODOSC_EN = 0).

AES1 — *AES256 Module*

Function Ongoing AES operation cannot be aborted by writing to AESAXIN

Description Writing to AESAXIN register when AESASTAT.AESBUSY bit is set does abort the ongoing AES operation or set the AESACTL0.AESERRFG bit.

Workaround Always let AES operation run to completion (i.e. do not abort). Ignore the encryption/decryption output if AESAXIN is written when AESASTAT.AESBUSY is set.

BSL13 — *BSL Module*

Function BSL scans all three interfaces even when configured to use one

Description BSL re-configures the module register settings of all three serial interfaces and scans for serial communication on these three interfaces even when BSL is configured to use only one interface.

Workaround None.

BSL16 — *BSL Module*

Function On blank devices, debugger access over JTAG is disabled after the timeout window

Description On blank devices, the default device initialization sequence that resides in the boot strap loader (BSL) disables the JTAG pins after a 10 second timeout window if no activity has occurred. This causes debug and program access through JTAG to be disabled. JTAG access can be re-enabled through a device reset (either Class 0 or Class 1).

Workaround 1. Use Serial Wire Debug (SWD) as the debug/program interface instead of JTAG.

OR

2. If timeout occurs, reset device (either Class 0 or Class 1) and ensure JTAG is accessed within a 10 second window

COMP8 — *COMP_E Module*

Function Reference module enabled when comparator not used

Description The shared reference module is erroneously enabled in static mode operation if the comparator module is configured to use the shared reference (CECTL2.CERFLx=1 or 2 or 3) with or without the resistor ladder (CECTL2.CERSELx=2 or 3) even if the comparator module is disabled (CECTL1.CEON=0). This also override any reference sample mode request.

Workaround Disable the reference source for the comparator (CECTL2.CERSELx=0) when not using the comparator.

COMP9 — *COMP_E Module*

Function Comparator and reference ladder enable time specification

Description The parameter Comparator and reference ladder enable time (tEN_CMP_RL) CMPON = 0 to CMPON = 1, exceeds the spec value (1us) by 60us under the following conditions:

1) CMPPWRMD = 00

AND

2) CMPREFLx = 10

AND

3) CMPRSx = 10

AND

4) REFON = 1

AND

5) CMPREF0/1 = 0x0F

Workaround None.

CS5 *CS Module*

Function DCO failure in external resistor mode

Description The DCO might overshoot and get stuck at high frequency (>110MHz) if interference or disturbance occurs on the DCO external resistor pin.

Workaround None.

CS6 *CS Module*

Function DCO overshoot when switching to external resistor mode

Description The DCO might overshoot and get stuck at higher frequency (>110MHz) when switching from internal resistor (IR) mode to external resistor (ER) mode in RSEL=5 mode (CSCTL0.DCORSELx = 5) regardless of the frequency to which the DCO is tuned in RSEL=5 mode.

Workaround Switch from IR mode to ER mode at lower frequency range (CSCTL0.DCORSELx <= 4).

CS8 *CS Module*

Function Unreliable DCO operation during DCO external resistor short

Description Unreliable DCO operation can occur if the ROSC pin gets shorted to ground during run-time before DCO can switch to the internal resistor-based fail-safe mode. If MCLK is sourced by DCO, this could cause the device to hang.

Workaround None.

CS9 *CS Module*

Function DF/DV for DCO in ER mode (DCORES=1)

Description DCO clock output when programmed in external resistor mode (CSCTL0.DCORES = 1) will show higher frequency variation with AVDD/DVDD at up to 0.6%/V.

Workaround None.

CS10 *CS Module*

Function DCO calibration accuracy in RSEL5 mode

Description DCO frequency in RSEL5 mode (CSCTL0.DCORSEL=5) violates +/-0.5% calibration accuracy.

Workaround None.

DMA12 *DMA Module*

Function Multiple DMA interrrupts

Description When the DMA cycle for a channel is complete, the DMA internally disables that channel. If DMA receives another trigger on this disabled channel before the completion interrupt is serviced, additional interrupts might be observed.

Workaround 1. Set DMA trigger source as the last step in DMA configuration routine.

And

2. In DMA ISR, disable DMA trigger source first.

FLASH38 *FLASH Module*

Function Application Benchmarking Counter counts all non-flash access in Buffered Read Mode

Description When FLCTL_RDCTL_BNKx.BUFD or FLCTL_RDCTL_BNKx.BUFI bit is set, the application benchmark counter counts all data or instruction accesses made to the flash memory including the accesses accounted by the 128-bit flash buffer. Since the counter does not exclude the buffer accesses, it does not reflect the actual flash accesses, which will be lower than the amount reported.

Workaround None.

FLASH39 *FLASH Module*

Function Re-programming same memory fails with pre-verify enabled

Description The word programming is aborted for these conditions:

1)The pre-verify option is enabled (FCTL_PRG_CTLSTAT.VER_PRE = 1).

AND

2) The location is already programmed with parity = 0.

AND

3) The new word parity is also 0.

Workaround Disable the program pre-verify option (FCTL_PRG_CTLSTAT.VER_PRE = 0).

FLASH40 *FLASH Module*

Function Burst program across bank-boundaries

Description When pre-verify is enabled and a burst program is initiated across bank-boundaries, the memory locations in the first bank are not programmed.

Workaround Use DriverLib API for Flash programming, FlashCtl_programMemory. The API includes the workaround to ensure proper programming mode across all Flash memory addresses.

FLASH41 *FLASH Module*

Function Low-Frequency Mode entry during Flash Program/Erase operation causes future program/erase to hang

Description During erase or program burst operations, particularly during the verify operations, Low-

	Frequency Mode entry freezes the status of ERASE or PROGRAM_BURST to PEND. This prevents any further program/erase operations after the device returns from Low-Frequency Mode. This status can only be cleared with a device reset.
Workaround	Do not enter Low-Frequency Mode during Flash erase or program operations. If the application uses DriverLib APIs for Flash operations, wait until the application exits from the Flash API(s) before entering Low-Frequency Mode.

PCM1 *PCM Module*

Function	False interrupt when switching to DC-DC mode
Description	The DC-DC error interrupt flag (PCMIFG.DCDC_ERROR) might get erroneously triggered when the device switches from LDO regulator to DC-DC regulator.
Workaround	After DC-DC switching operation is complete, as indicated by PCMCTL0.PMR_BUSY bit being reset, clear the PCMIFG.DCDC_ERROR flag. Ensure VCC supply voltage meets the requirements for DC-DC operation per datasheet prior to switching from LDO to DC-DC regulator.

PCM2 *PCM Module*

Function	Incorrect SRAM and ROM access during VCORE changes
Description	Data accesses including reading from ROM and reading/writing to SRAM can be erroneous during VCORE change transition (from VCORE level 0 to 1 or vice versa).
Workaround	Avoid all SRAM/ROM access during all VCORE transitions.

PMAP2 *PMAP Module*

Function	Unlocked PMAP module prevents LPM3/4/3.5/4.5 entrance
Description	If the port mapper module is left unlocked after register configuration, the device is prevented from entering LPM3, LPM4, LPM3.5, and LPM4.5 modes in polite mode.
Workaround	None.

PORT25 *PORT Module*

Function	RSTnNMI pin in NMI mode
Description	When the RSTnNMI pin is configured with NMI functionality, the glitch filter is erroneously enabled. This prevents pulses with width<20ns from triggering an NMI in Active mode or waking up the device from low power modes (LPM0, LPM3).
Workaround	None.

PORT27 *PORT Module*

Function	Wakeup from LPM
Description	Interrupt wake-up from a port pin does not occur in low-power modes if the corresponding PxIFG flag is set prior to LPM entry.
Workaround	Clear PxIFGs prior to entry to low power mode.

PORT31 *PORT Module*

Function Fast transient noise on GPIOs may result in a constant high current

Description GPIOs subject to fast transient noise (for example, electromagnetic noise) may see a high constant current. The constant high current is a result of the fast transient noise triggering the internal ESD protection structure and it persists as long as the internal or external current driver sustains the current.

1. When using in Input mode (PxDIR = 0), all GPIOs are impacted by this issue. A fast transient noise on the pin configured as an input or on an adjacent pin could cause a constant high current that is sustained as long as the external driver is present.

2. When using in Output mode (PxDIR = 1), only the high drive GPIOs (P2.0,P2.1,P2.2 and P2.3) are impacted by this issue. If the affected GPIOs are configured in high drive mode (PxDS register) and they (or adjacent pins) are subject to fast transient noise, it could cause a constant high current. Note that this issue is not seen in GPIOs configured in the output direction with the regular drive strength setting since the high drive mode is required to sustain the high current.

If the GPIO configuration is reset by a power cycle, the constant high current is no longer sustained.

Workaround 1. For GPIOs configured as input, ensure that they are driven by a current-limited source < 30mA OR use a series resistance >100 ohm to limit the current.

2. For high drive GPIOs configured as output, ensure adequate protection from fast transients is provided to both the high drive IOs and any adjacent pins.

3. In general, it is recommended to terminate any unused GPIOs in the output direction, driving low to minimize the occurrence of this issue.

4. For guidelines on ESD considerations see, *MSP430 System-level ESD Considerations* .

PORT32 *PORT Module*

Function Sucessive writes to port registers may cause interrupt to pend incorrectly

Description Writing to the PxIES register sets the corresponding PxIFG bit. The PxIFG bit can be cleared by writing '0' to it (clearing the register).

However if the PxIFG bit is cleared immediately (next instruction cycle) after writing to the PxIES register, the interrupt flag does not clear and stays pending.

Workaround Insert a NOP or __no_operation(); instruction after writing to the PxIES register and before clearing the PxIFG register.

PSS1 *SVS Module*

Function Reset triggered by SVSMH/SVSL

Description Spurious reset may be triggered when SVSMH/SVSL is disabled and then enabled again in software, or if device enters LPM4.5 mode after SVSL is disabled in software.

Workaround 1. For SVSMH:

- Never disable SVSMH if the function is required in the application.

- Disable SVSMH permanently at the beginning of the application code if the functionality is not required.

2. For SVSL:

- Never disable SVSL if application requires LPM4.5 entry or SVSL functionality.

- Disable SVSL permanently at the beginning of the application code if application does not use SVSL and does not enter LPM4.5 mode.

PSS2 *PSS Module*

Function Power Supply System High-Side Reset

Description A PSS High-Side reset occurs if device enters LPM3/LPM3.5 mode with SVSM high-side reset voltage level (SVSMCTL.SVSMHTHx) is set to 0x6 or 0x7. The SVSH flag in the RSTCTL_PSSRSTSTAT register is set.

Workaround Use SVSMCTL.SVSMHTHx=[0-5] settings if application requires to enter LPM3/LPM3.5 mode.

PSS3 *PSS Module*

Function High-side POR generated after LPM4.5 wake-up

Description A high-side POR is generated, indicated with the high-side SVSM interrupt flag (PSSIFG.SVSMHIFG) set, upon LPM4.5 wake-up from a GPIO interrupt. In addition, the PCMCTL1.LOCKLPM5 bit is not cleared.

Need clarification:

- Does the text accurately convey the erroneous behavior?

- Does bug occur for all SVSMH threshold settings? Bug description above mentioned only 0x6/0x7 were used.

- VCC was also mentioned as constantly 3.3V. How is this significant to the bug? Is the point here being supply never drops below the SVS high-side setting? If so, that detail - can be safely removed from the text.

Workaround None.

PSS4 *PSS Module*

Function SVSMHLP has no impact in LPM4.5 mode

Description Upon entry into LPM4.5, the SVSMH is set to low power normal performance mode automatically regardless of the SVSMHLP setting.

Clearing the SVSMHLP bit (PSSCTL0.SVSMHLP = 0) has no impact in LPM4.5.

This bit works as expected in all other low power modes.

Workaround None

REF3 *REF Module*

Function Increased reference voltage temperature variation

Description The temperature variation for the reference voltage is higher than specification, with temperature co-efficient increased up to 30-40 ppm/degree Celsius.

Workaround None.

REF4 *REF Module*

Function REFGENBUSY status bit

Description The REFCTL0.REFGENBUSY bit is set when the ADC is configured to use the reference module in buffered mode (ADC14MCTLx.ADC14VRSEL= 1) even when the ADC is not actively converting.

Workaround None.

REF7 *REF Module*

Function REFOUT functionality not available on pin

Description The internal reference voltage is not available on VREF pin unless both ADC module is enabled (ADC14CTL0.ADC14ON=1) and the internal reference is selected (ADC14MCTLx.ADC14VRSEL=1). The erroneous behavior occurs even when the reference module is on (REFCTL0.REFON=1) and output to a pin (REFCTL.REFOUT=1).

Workaround 1) Turn on the reference module (REFCTL0.REFON=1)

AND

2) Enable the reference output pin (REFCTL0.REFOUT=1).

AND

3) Enable the ADC 14 module (ADC14CTL0.ADC14ON=1).

AND

4) Select the internal reference for one ADC channel (ADC14CTL1.ADC14CSTARTADD=x & ADC14MCTLx.ADC14VRSEL=1).

REF8 *REF Module*

Function Reference ready status prematurely enabled

Description The reference buffer ready status bit (REFCTL0.REFBGRDY or REFCTL0.REFGENRDY) might be triggered before the low-power buffer or reference buffer has settled.

Workaround Insert a 50us delay after REFCTL0.REFBGRDY or REFCTL0.REFGENRDY bit is set before using the reference buffer for comparator or ADC operation.

REF9 *REF Module*

Function REFON Feature

Description The Reference module does not not provide REF voltage to Comparator module when the REFON bit is set (REFCTL0.REFON=1).

Workaround 1. Use REFBGOT bit of the REFCTL0 regsiter instead of REFON bit to provide REF voltage to Comparator.

OR

2. Enable the Comparator module with internal REF setting (CEREFL + CERS bits of the CECTL2 register) to request the REF module.

RST1 *RSTCTL Module*

Function LPM3.5 and LPM4.5 status bits not reset on RSTNMI pin interrupt.

Description LPM3.5 and LPM4.5 status bits (RSTCTL_PCMRSTSTAT_REG.LPM35 and RSTCTL_PCMRSTSTAT_REG.LPM45) might not get reset after LPMx.5 wake-up triggered by an IO wake-up on RSTNMI pin interrupt.

Workaround Clear RSTCTL_PCMRSTSTAT_REG.LPM35 and RSTCTL_PCMRSTSTAT_REG.LPM45 status bits after RSTNMI pin wake-up from LPMx.5 power mode.

RST2 *RSTCTL Module*

Function LPM4.5 bit in RSTCTL_PCMRESET_STAT not cleared

Description The LPM4.5 bit in RSTCTL_PCMRESET_STAT (set after waking up from LPM4.5) cannot be cleared (by setting RSTCTL_PCMRESET_CLR.LPM45 bit) until after the PCMCTL0.LOCKLPM5 bit is cleared.

Workaround After LPM4.5 wake up, clear PCMCTL.LOCKLPM5 bit before clearing the LPM4.5 flag by setting RSTCTL_PCMRESET_CLR.LPM45 bit.

RTC9 *RTC_C Module*

Function RTCRDYIFG may cause unexpected wake-up from LPM3.5

Description RTCRDYIFG is not an LPM3.5 wake-up interrupt source. However due to the erratum, when the device is placed in LPM3.5 and RTCRDYIE is enabled, RTCRDYIFG being set can cause an inadvertent wake-up from LPM3.5.

Workaround Do not enable RTCRDYIE before the device is placed in LPM3.5

RTC11 *RTC_C Module*

Function RTC interrupt service after wake-up from LPM3.5

Description After device wakes up from LPM3.5 triggered by an RTC event, the device enters the RTC ISR when the NVIC is configured for RTC interrupt even when the RTC interrupt enable bits (RTCCTL0.RTCOFIE, RTCCTL0.RTCTEVIE, RTCCTL0.RTCAIE, RTCPS1CTL.RT1PSIE) are not set.

Workaround None.

RTC12 *RTC_C Module*

Function Real-time clock temperature compensation RTCTCOK bit not retained after LPM3.5 wake up

Description The RTC real-time clock temperature compensation write OK bit (RTCTCMP.RTCTCOK) is reset on wake up from LPM3.5 mode and does not get retained.

Workaround Store the RTCTCMP register content into Flash content or SRAM bank 0 for retention after wake up from LPM3.5

RTC13 *RTC_C Module*

Function Device enters LPM3 mode even when RTCCLK is output to a port pin

Description Device enters LPM3 mode even when RTCCLK is output to an external port pin of the device.

Workaround None.

SRAM1 *SRAM Module*

Function SRAM access stalled when core voltage level changed

Description When the core voltage level is changed from 0 to 1, SRAM access is stalled for ~600ns after the transition is complete.

Workaround Insert a 600ns delay after the core voltage transition is complete (PCMCTL1.PMR_BUSY bit is clear). 3 SYSOSC cycles can be used for the 600ns delay.

SRAM2 *SRAM Module*

Function SRAM bank enable and retention ready bits not set

Description The SRAM ready bits (SYS_SRAM_BANKEN.SRAM_RDY/SYS_SRAM_BANKRET.SRAM_RDY) are not set if both conditions apply:

1. The SRAM bank enable or retention bits are modified (SYS_SRAM_BANKEN/SYS_SRAM_BANKRET) .

2. A POR-class reset occurs prior to SRAM operation completion, which is indicated by the SRAM ready bits getting set.

Workaround None.

SYS21 *SYS Module*

Function Write access to SYSCTL registers in low power modes

Description Debugger write access to the SYSCTL registers is not possible when the device is in LPM0 or LPM3.

Workaround None.

SYS26 *SYS Module*

Function IP Protetcion Feature not available

Description The Regional IP Protection feature is not available up to Revision C for the MSP432P401R/M devices.

If your application only requires MSP432 full-chip security to protect your software IP from JTAG read-out, this limitation does not apply to you.

Regional IP Protection is used in (i) protecting a specific block of code/data from readout by the rest of the application code and (ii) multi-party firmware development, where each software IP owner delivers an executable IP that is protected from read-out by code from other IP owners using the device.

For more information on benefits and how to use Regional IP Protection, see Software IP Protection on MSP432P4xx Microcontrollers

Workaround None

SYSTICK1 *SYSTICK Module*

Function CLKSOURCE selection bit of Systick register-SCS_STCSR is read-writeable

Description The CLKSOURCE bit of SCS_STCSR (SYSTICK control and status register) is read/write-able instead of read-only. Do not write 0 to the SCS_STCSR.SCS_STCSR_CLKSOURCE bit since the device does not support external reference clock.

Workaround None.

USCI41 *eUSCI Module*

Function UCBUSY bit of eUSCIA module stuck to 1 when device is in SPI mode.

Description When eUSCIA is configured in SPI mode, and the last transfer bit changes from 0 to 1, the UCBUSY bit gets stuck to 1. This happens in all four combinations of Clock Phase and Clock Polarity options (UCAxCTLW0.UCCKPH & UCAxCTLW0.UCCKPL bits). There is no data loss or corruption.

Workaround Check on transmit or receive interrupt flag UCTXIFG/UCRXIFG instead of UCBUSY to know if the UCAxTXBUF buffer is empty or ready for the next complete character.

USCI42 *eUSCI Module*

Function UART asserts UCTXCPTIFG after each byte in multi-byte transmission

Description UCTXCPTIFG flag is triggered at the last stop bit of every UART byte transmission, independently of an empty buffer, when transmitting multiple byte sequences through UART. The erroneous UART behavior occurs with and without DMA transfer.

Workaround None.

WDG7 *WDT_A Module*

Function Watchdog function when switching clock source

Description The watchdog timer module stops working when switching clock source from VLOCLK/BCLK to any other clock source.

Workaround None.

4 Document Revision History

Changes from device specific erratasheet to document Revision A.

1. Errata ADC48 was added to the errata documentation.
2. Errata ADC46 was added to the errata documentation.
3. Errata ADC49 was added to the errata documentation.
4. Errata FLASH38 was added to the errata documentation.
5. Errata ADC47 was added to the errata documentation.
6. Errata DMA12 was added to the errata documentation.

Changes from document Revision A to Revision B.

1. PSS1 Description was updated.
2. Errata REF8 was added to the errata documentation.
3. SYS21 Description was updated.
4. Errata RTC11 was added to the errata documentation.
5. Errata RST2 was added to the errata documentation.
6. SYS22 Description was updated.
7. PSS1 Workaround was updated.
8. Errata PCM1 was added to the errata documentation.
9. Errata CS8 was added to the errata documentation.
10. Errata USCI36 was removed from the errata documentation.
11. SYS21 Function was updated.
12. Errata FLASH39 was added to the errata documentation.
13. Errata ADC58 was added to the errata documentation.
14. SYS24 Description was updated.
15. SYS22 Function was updated.
16. SYS24 Function was updated.
17. Errata PORT25 was added to the errata documentation.
18. Errata PSS2 was added to the errata documentation.
19. Errata REF7 was added to the errata documentation.
20. Errata COMP8 was added to the errata documentation.
21. Silicon Revision B was added to the errata documentation.
22. Errata RST1 was added to the errata documentation.

Changes from document Revision B to Revision C.

1. Errata ADC61 was added to the errata documentation.
2. Errata BSL13 was added to the errata documentation.
3. Errata RTC12 was added to the errata documentation.
4. Errata SRAM1 was added to the errata documentation.
5. Errata ADC51 was added to the errata documentation.
6. RST1 Description was updated.
7. Errata ADC57 was added to the errata documentation.
8. Errata PMAP2 was added to the errata documentation.
9. Errata ADC55 was added to the errata documentation.
10. Errata ADC56 was added to the errata documentation.
11. Errata ADC53 was added to the errata documentation.
12. Errata CS5 was added to the errata documentation.
13. Errata ADC52 was added to the errata documentation.

14. Errata PORT27 was added to the errata documentation.
15. Errata SYSTICK1 was added to the errata documentation.
16. Errata PCM2 was added to the errata documentation.
17. Package Markings section was updated.
18. Errata ADC54 was added to the errata documentation.
19. Errata CS6 was added to the errata documentation.
20. Errata FLASH40 was added to the errata documentation.
21. RST1 Workaround was updated.
22. Errata ADC59 was added to the errata documentation.
23. RST1 Function was updated.

Changes from document Revision C to Revision D.

1. Errata CS9 was added to the errata documentation.
2. Errata COMP9 was added to the errata documentation.
3. Errata REF9 was added to the errata documentation.
4. Errata USCI42 was added to the errata documentation.
5. Errata USCI41 was added to the errata documentation.
6. Silicon Revision C was added to the errata documentation.
7. Errata AES1 was added to the errata documentation.
8. Errata FLASH41 was added to the errata documentation.
9. Errata PSS3 was added to the errata documentation.
10. Errata COMP10 was added to the errata documentation.
11. Errata CS10 was added to the errata documentation.

Changes from document Revision D to Revision E.

1. Errata PORT27 was removed from the errata documentation.
2. Errata ADC58 was removed from the errata documentation.
3. Errata REF8 was removed from the errata documentation.
4. Errata CS10 was removed from the errata documentation.
5. Errata FLASH38 was removed from the errata documentation.
6. Errata ADC59 was removed from the errata documentation.
7. Errata REF9 was removed from the errata documentation.
8. Errata CS6 was removed from the errata documentation.
9. Errata ADC57 was removed from the errata documentation.
10. Errata RTC13 was removed from the errata documentation.
11. Errata SYS21 was removed from the errata documentation.
12. Errata CS5 was removed from the errata documentation.
13. Errata PCM1 was removed from the errata documentation.
14. Errata RTC9 was removed from the errata documentation.
15. Errata SRAM1 was removed from the errata documentation.
16. Errata RTC12 was removed from the errata documentation.
17. Errata PSS2 was removed from the errata documentation.
18. Errata ADC47 was removed from the errata documentation.
19. Errata ADC49 was removed from the errata documentation.
20. Errata COMP10 was removed from the errata documentation.
21. Errata REF7 was removed from the errata documentation.
22. Errata PMAP2 was removed from the errata documentation.

23. Errata CS8 was removed from the errata documentation.
24. Errata COMP9 was removed from the errata documentation.
25. Errata FLASH40 was removed from the errata documentation.
26. Errata AES1 was removed from the errata documentation.
27. Errata ADC55 was removed from the errata documentation.
28. Errata FLASH39 was removed from the errata documentation.
29. Errata PSS3 was removed from the errata documentation.
30. Package Markings section was updated.
31. Errata ADC61 was removed from the errata documentation.
32. Errata ADC53 was removed from the errata documentation.
33. Errata DMA12 was removed from the errata documentation.
34. Errata REF3 was removed from the errata documentation.
35. Errata CS9 was removed from the errata documentation.
36. Errata ADC54 was removed from the errata documentation.
37. Errata RST2 was removed from the errata documentation.
38. Errata ADC52 was removed from the errata documentation.
39. Errata ADC60 was removed from the errata documentation.
40. Errata REF4 was removed from the errata documentation.
41. Errata ADC51 was removed from the errata documentation.
42. Errata BSL13 was removed from the errata documentation.
43. Errata USCI41 was removed from the errata documentation.
44. Errata ADC56 was removed from the errata documentation.
45. Errata PORT25 was removed from the errata documentation.
46. Errata WDG7 was removed from the errata documentation.
47. Errata SYSTICK1 was removed from the errata documentation.
48. Errata COMP8 was removed from the errata documentation.
49. Errata PSS1 was removed from the errata documentation.
50. Errata PCM2 was removed from the errata documentation.
51. Errata RST1 was removed from the errata documentation.
52. Errata FLASH41 was removed from the errata documentation.
53. Errata SRAM2 was removed from the errata documentation.
54. Errata ADC62 was removed from the errata documentation.
55. Errata RTC11 was removed from the errata documentation.
56. Errata ADC48 was removed from the errata documentation.

Changes from document Revision E to Revision F.

1. Added all XMS silicon rev B information (from the previously released revision of this document, SLAZ610C)
2. Added BSL16.

Changes from document Revision F to Revision G.

1. Added SYS26.

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