TEXAS INSTRUMENTS

OPA330, OPA2330, OPA4330

SBOS432G – AUGUST 2008 – REVISED AUGUST 2016

OPAx330 50-µV V_{OS}, 0.25-µV/°C, 35-µA CMOS Operational Amplifiers Zero-Drift Series

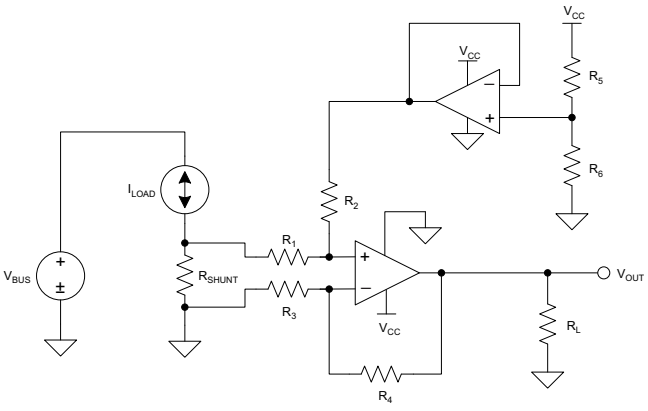
1 Features

- Unmatched Price Performance
- Low Offset Voltage: 50 µV (Maximum)
- Zero Drift: 0.25 µV/°C (Maximum)
- Low Noise: 1.1 μV_{PP}, 0.1 Hz to 10 Hz
- Quiescent Current: 35 µA (Maximum)
- Supply Voltage: 1.8 V to 5.5 V
- Rail-to-Rail Input and Output
- Internal EMI Filtering
- *micro*Size Packages: DSBGA, SC70, VQFN

2 Applications

- Battery-Powered Instruments
- Temperature Measurements
- Transducer Applications
- Electronic Scales
- Medical Instrumentation
- Handheld Test Equipment
- Current Sense

Bidirectional, Low-Side Current Sense



3 Description

The OPA330 series of CMOS operational amplifiers offer precision performance at a very competitive price. These devices are members of the Zero-Drift family of amplifiers which use a proprietary auto-calibration technique to simultaneously provide low offset voltage (50-µV maximum) and near-zero drift over time and temperature at only 35 µA (maximum) of quiescent current. The OPA330 family features rail-to-rail input and output in addition to near-flat 1/f noise, making this amplifier ideal for many applications and much easier to design into a system. These devices are optimized for low-voltage operation as low as 1.8 V (±0.9 V) and up to 5.5 V (±2.75 V).

The OPA330 (single version) is available in the 5-pin DSBGA, 5-pin SC70, 5-pin SOT-23, and 8-pin SOIC packages. The OPA2330 (dual version) is offered in 3 mm × 3 mm, 8-pin SON, 8-pin VSSOP, and 8-pin SOIC packages. The OPA4330 is offered in the standard 14-pin SOIC and 14-pin TSSOP packages, as well as in the space-saving 14-pin VQFN package. All versions are specified for operation from –40°C to 125°C.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
OPA330	SOIC (8)	4.90 mm × 3.91 mm
	SOT (5)	2.90 mm × 1.60 mm
	SC70 (5)	2.00 mm × 1.25 mm
	DSBGA (5)	0.00 mm × 0.00 mm
OPA2330	SOIC (8)	4.90 mm × 3.91 mm
	VSSOP (8)	3.00 mm × 3.00 mm
	SON (8)	3.00 mm × 3.00 mm
OPA4330	SOIC (14)	8.65 mm × 3.91 mm
	TSSOP (14)	5.00 mm × 4.40 mm
	VQFN (14)	3.50 mm × 3.50 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision F (June 2016) to Revision G **Page**

- Changed *Pin Functions: OPA330* so each pin has a separate row ... 4
- Changed position of Input Voltage Range, *CMRR* parameter specification values in *Electrical Characteristics* table ... 9
- Changed position of Open-Loop Gain, A_{OL} parameter specification values in *Electrical Characteristics* table ... 9

Changes from Revision E (February 2011) to Revision F **Page**

- Added *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section ... 1
- Added current package designators to second paragraph of *Description* section ... 1
- Removed *Package Information* table, see POA at the end of the datasheet ... 1
- Changed *Product Family Package Comparison* table to *Device Comparison* table; moved from page 1 of document ... 4

Changes from Revision D (June 2010) to Revision E **Page**

- Changed document status from Mixed Status to Production Data ... 1
- Deleted footnote 2 from the Package Information table ... 1
- Added remaining thermal information data ... 8

Changes from Revision C (October 2009) to Revision D **Page**

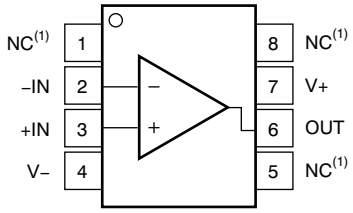
- Added last *Applications* bullet ... 1
- Deleted footnote 2 and shading from all packages except QFN-14; moved WCSP-5, SOIC-14, and TSSOP-14 packages to Production Data status; and added package marking information to Package Information table ... 1
- Deleted footnote 1 from Product Family Package Comparison table ... 4
- Moved TSSOP-14 thermal resistance to MSOP-8, SOIC-8 thermal resistance parameter in Electrical Characteristics table ... 9
- Deleted SOIC-14 and QFN-14 rows from Temperature Range section in Electrical Characteristics table ... 9
- Added *OPA330YFF, OPA4330* Input Bias Current parameter to Electrical Characteristics table ... 9
- Added Input Voltage Range, *OPA330YFF, OPA4330 Common-Mode Rejection Ratio* parameter to Electrical Characteristics table ... 9

5 Device Comparison Table

DEVICE	NO OF CHANNELS	PACKAGE-LEADS							
		DSBGA	SOIC	SOT	SC70	VSSOP	SON	VQFN	TSSOP
OPA330	1	5	8	5	5	—	—	—	—
OPA2330	2	—	8	—	—	8	8	—	—
OPA4330	4	—	14	—	—	—	—	14	14

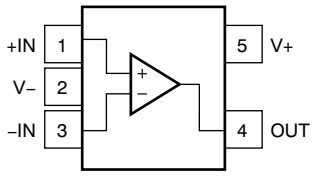
6 Pin Configurations and Functions

OPA330: D Package
8-Pin SOIC
Top View

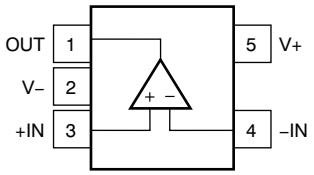


(1) NC denotes no internal connection.

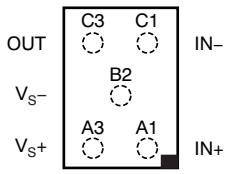
OPA330: DCK Package
5-Pin SC70
Top View



OPA330: DBV Package
5-Pin SOT-23
Top View



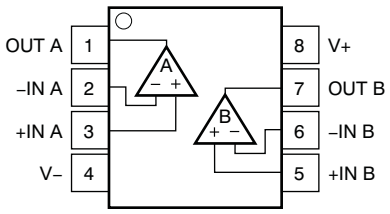
OPA330: YFF Package
5-Pin DSBGA
Top View



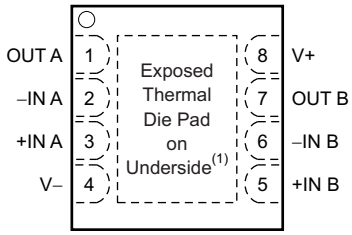
Pin Functions: OPA330

PIN					I/O	DESCRIPTION
NAME	SOIC	SOT-23	SC70	DSBGA		
–IN	2	4	3	C1	I	Negative (inverting) input
+IN	3	3	1	A1	I	Positive (noninverting) input
NC	1, 5, 8	—	—	—	—	No internal connection (can be left floating)
OUT	6	1	4	C3	O	Output
V–	4	2	2	—	—	Negative (lowest) power supply
V+	7	5	5	—	—	Positive (highest) power supply
$V_{S–}$	—	—	—	B2	—	Negative (lowest) power supply
V_{S+}	—	—	—	A3	—	Positive (highest) power supply

OPA2330: D and DGK Packages
8-Pin SOIC and 8-Pin VSSOP
Top View



OPA2330: DRB Package
8-Pin SON
Top View

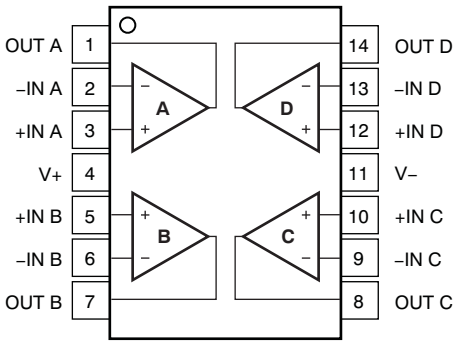


(1) Connect thermal die pad to V–.

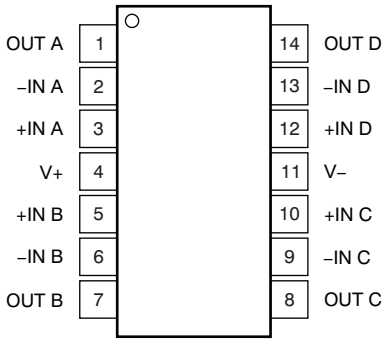
Pin Functions: OPA2330

PIN			I/O	DESCRIPTION
NAME	SOIC, VSSOP	SON		
–IN A	2	2	I	Negative (inverting) input signal, channel A
+IN A	3	3	I	Positive (noninverting) input signal, channel A
–IN B	6	6	I	Negative (inverting) input signal, channel B
+IN B	5	5	I	Positive (noninverting) input signal, channel B
OUT A	1	1	O	Output channel A
OUT B	7	7	O	Output channel B
V–	4	4	—	Negative (lowest) power supply
V+	8	8	—	Positive (highest) power supply

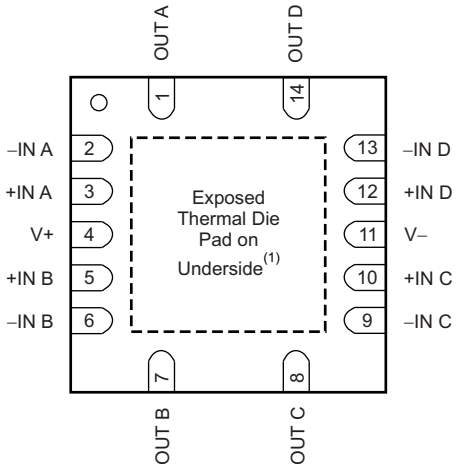
OPA4330: D Package
14-Pin SOIC
Top View



OPA4330: PW Package
14-Pin TSSOP
Top View



OPA4330: RGY Package
14-Pin VQFN
Top View



(1) Connect thermal die pad to V–.

Pin Functions: OPA4330

PIN				I/O	DESCRIPTION
NAME	SOIC	TSSOP	VQFN		
–IN A	2	2	2	I	Negative (inverting) input signal, channel A
+IN A	3	3	3	I	Positive (noninverting) input signal, channel A
–IN B	6	6	6	I	Negative (inverting) input signal, channel B
+IN B	5	5	5	I	Positive (noninverting) input signal, channel B
–IN C	9	9	9	I	Negative (inverting) input signal, channel C
+IN C	10	10	10	I	Positive (noninverting) input signal, channel C
–IN D	13	13	13	I	Negative (inverting) input signal, channel D
+IN D	12	12	12	I	Positive (noninverting) input signal, channel D
OUT A	1	1	1	O	Output channel A
OUT B	7	7	7	O	Output channel B
OUT C	8	8	8	O	Output channel C
OUT D	14	14	14	O	Output channel D
V–	11	11	11	—	Negative (lowest) power supply
V+	4	4	4	—	Positive (highest) power supply

7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Voltage	Supply, V_S = (V+) – (V–)		7	V
	Signal input terminals(2) (TBD should terminal be pin?)	(V–) –0.3	(V+) + 0.3	V
Current	Signal input terminals(2)	–10	10	mA
	Output short-circuit(3)	Continuous		
Temperature	Operating range, T_A	–40	150	°C
	Junction, T_J		150	°C
	Storage, T_{stg}	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) Input terminals are diode-clamped to the power-supply rails. Input signals that can swing more than 0.3 V beyond the supply rails should be current limited to 10 mA or less.
(3) Short-circuit to ground, one amplifier per package.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±4000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±1000	
		Machine model (MM)	±400	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
(V+) – (V–)	Supply voltage	±0.9 (1.8)	±2.5 (5)	±2.75 (5.5)	V
T_A	Specified temperature	–40	25	125	°C

7.4 Thermal Information: OPA330

THERMAL METRIC(1)		OPA330				UNIT
		D (SOIC)	DBV (SOT-23)	DCK (SC70)	YFF (DSBGA)	
		8 PINS	5 PINS	5 PINS	5 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	140.1	220.8	298.4	130	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	89.8	97.5	65.4	54	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	80.6	61.7	97.1	51	°C/W
ψ_{JT}	Junction-to-top characterization parameter	28.7	7.6	0.8	1	°C/W
ψ_{JB}	Junction-to-board characterization parameter	80.1	61.1	95.5	50	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

7.5 Thermal Information: OPA2330

THERMAL METRIC(1)		OPA2330			UNIT
		D (SOIC)	DGK (VSSOP)	DRB (SON)	
		8 PINS	8 PINS	8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	124	180.3	46.7	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	73.7	48.1	26.3	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	64.4	100.9	22.2	°C/W
ψ_{JT}	Junction-to-top characterization parameter	18	2.4	1.6	°C/W
ψ_{JB}	Junction-to-board characterization parameter	63.9	99.3	22.3	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	—	—	10.1	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

7.6 Thermal Information: OPA4330

THERMAL METRIC(1)		OPA4330			UNIT
		D (SOIC)	PW (TSSOP)	RGY (VQFN)	
		14 PINS	14 PINS	14 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	83.8	120.8	49.2	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	70.7	34.3	75.3	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	59.5	62.8	61.9	°C/W
ψ_{JT}	Junction-to-top characterization parameter	11.6	1	1.2	°C/W
ψ_{JB}	Junction-to-board characterization parameter	37.7	56.5	19.3	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	—	—	4.6	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

7.7 Electrical Characteristics

at T_A = 25°C, R_L = 10 kΩ connected to midsupply, V_S = 1.8 V to 5.5 V, and V_{CM} = V_{OUT} = midsupply (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
OFFSET VOLTAGE							
V_{OS}	Input offset voltage	V_S = 5 V			8	50	µV
dV_{OS}/dT	Input offset voltage versus temperature	At T_A = –40°C to +125°C			0.02	0.25	µV/°C
PSRR	Input offset voltage versus power supply	At T_A = –40°C to +125°C			1	10	µV/V
	Long-term stability(1)	V_S = 1.8 V to 5.5 V			See (1)		
	Channel separation, dc				0.1		µV/V
INPUT BIAS CURRENT							
I_B	Input bias current	At 25°C			±200	±500	pA
			OPA330YFF, OPA4330		±70	±300	pA
		At T_A = –40°C to +125°C			±300		pA
I_{OS}	Input offset current	At 25°C			±400	±1000	pA
			OPA330YFF, OPA4330		±140	±600	pA
NOISE							
e_n	Input voltage noise density	f = 1 kHz			55		nV/√Hz
	Input voltage noise	f = 0.01 Hz to 1 Hz			0.3		$µV_{PP}$
		f = 0.1 Hz to 10 Hz			1.1		$µV_{PP}$
i_n	Input current noise	f = 10 Hz			100		fA/√Hz
INPUT VOLTAGE RANGE							
V_{CM}	Common-mode voltage range			(V–) – 0.1		(V+) + 0.1	V
CMRR	Common-mode rejection ratio	At T_A = –40°C to +125°C, (V–) – 0.1 V < V_{CM} < (V+) + 0.1 V		100	115		dB
		At T_A = –40°C to +125°C, (V–) – 0.1 V < V_{CM} < (V+) + 0.1 V, V_S = 5.5 V		100	115		dB
			OPA330YFF, OPA4330	100	115		dB
INPUT CAPACITANCE							
	Differential				2		pF
	Common-mode				4		pF
OPEN-LOOP GAIN							
A_{OL}	Open-loop voltage gain	At T_A = –40°C to +125°C, (V–) + 100 mV < V_O < (V+) – 100 mV, R_L = 10 kΩ		100	115		dB
FREQUENCY RESPONSE							
GBW	Gain-bandwidth product	C_L = 100 pF			350		kHz
SR	Slew rate	G = +1			0.16		V/µs
OUTPUT							
	Voltage output swing from rail	At T_A = –40°C to +125°C			30	100	mV
I_{SC}	Short-circuit current				±5		mA
C_L	Capacitive load drive			See *Typical Characteristics*			
	Open-loop output impedance	f = 350 kHz, I_O = 0 mA			2		kΩ
POWER SUPPLY							
V_S	Specified voltage range			1.8		5.5	V
I_Q	Quiescent current per amplifier	At T_A = –40°C to +125°C, I_O = 0 mA			21	35	µA
	Turnon time	V_S = 5 V			100		µs

(1) 300-hour life test at 150°C demonstrated randomly distributed variation of approximately 1 µV.

7.8 Typical Characteristics

At T_A = 25°C, C_L = 0 pF, R_L = 10 kΩ connected to midsupply, and V_{CM} = V_{OUT} = midsupply, unless otherwise noted.

Table 1. Table of Graphs

DESCRIPTION	FIGURE NO.
Offset Voltage Production Distribution	Figure 1
Open-Loop Gain vs Frequency	Figure 2
Common-Mode Rejection Ratio vs Frequency	Figure 3
Power-Supply Rejection Ratio vs Frequency	Figure 4
Output Voltage Swing vs Output Current	Figure 5
Input Bias Current vs Common-Mode Voltage	Figure 6
Input Bias Current vs Temperature	Figure 7
Quiescent Current vs Temperature	Figure 8
Large-Signal Step Response	Figure 9
Small-Signal Step Response	Figure 10
Positive Overvoltage Recovery	Figure 11
Negative Overvoltage Recovery	Figure 12
Settling Time vs Closed-Loop Gain	Figure 13
Small-Signal Overshoot vs Load Capacitance	Figure 14
0.1-Hz to 10-Hz Noise	Figure 15
Current and Voltage Noise Spectral Density vs Frequency	Figure 16
Input Bias Current vs Input Differential Voltage	Figure 17

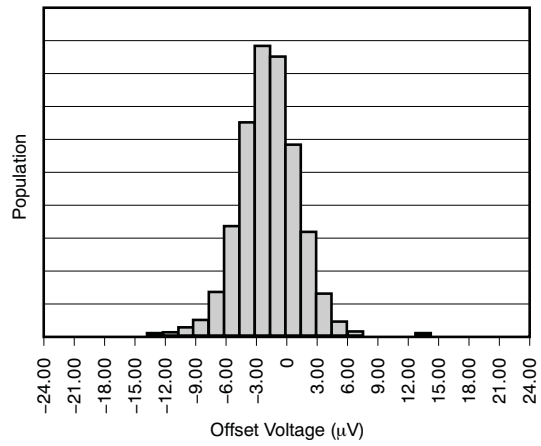


Figure 1. Offset Voltage Production Distribution

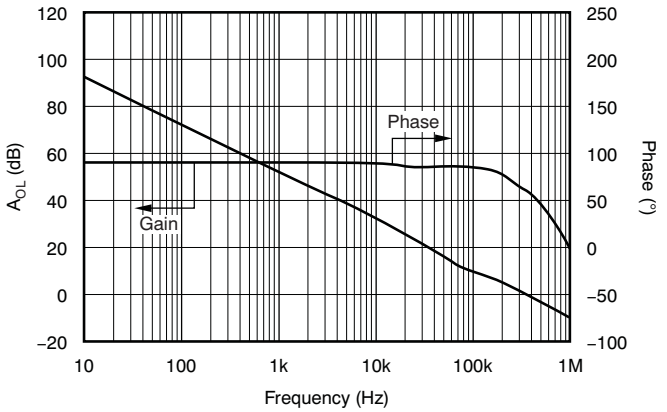


Figure 2. Open-Loop Gain vs Frequency

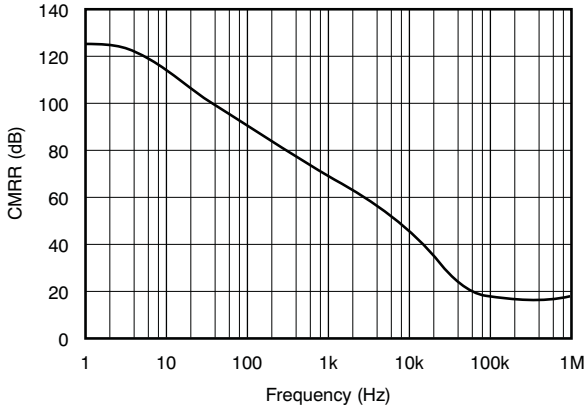


Figure 3. Common-Mode Rejection Ratio vs Frequency

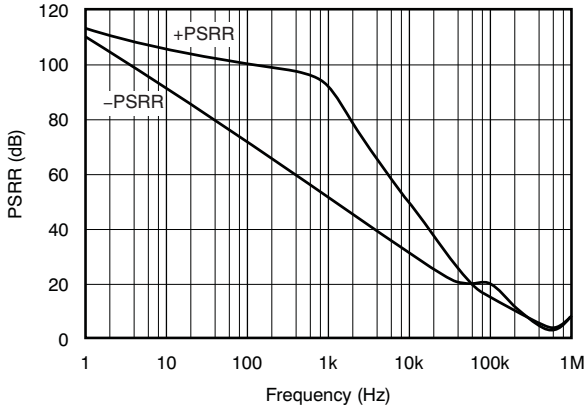


Figure 4. Power-Supply Rejection Ratio vs Frequency

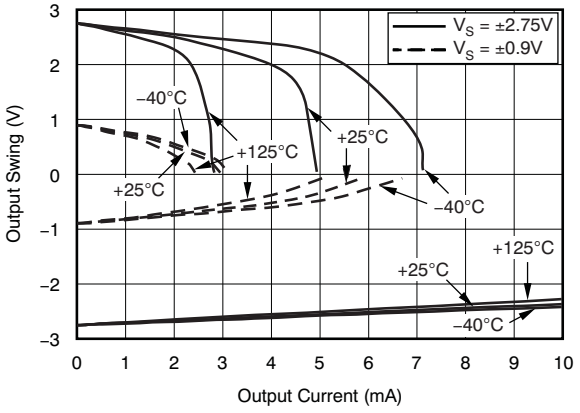


Figure 5. Output Voltage Swing vs Output Current

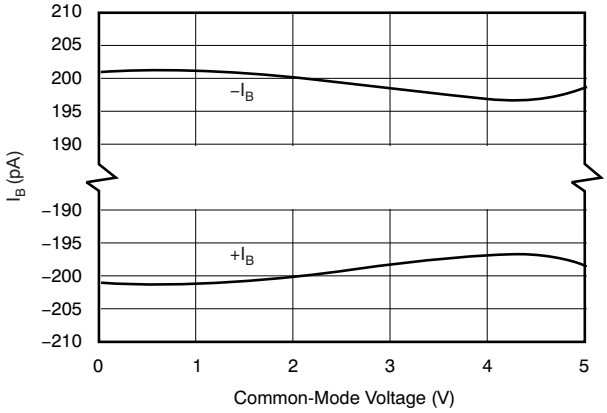


Figure 6. Input Bias Current vs Common-Mode Voltage

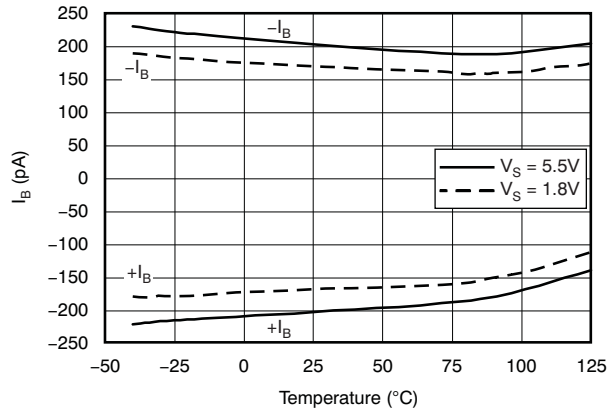


Figure 7. Input Bias Current vs Temperature

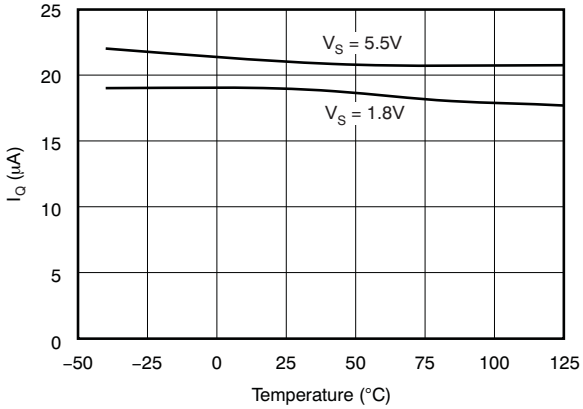


Figure 8. Quiescent Current vs Temperature

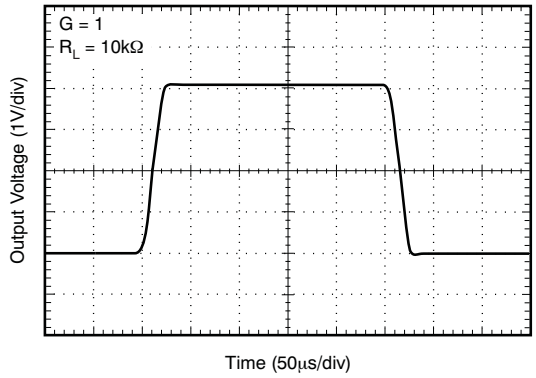


Figure 9. Large-Signal Step Response

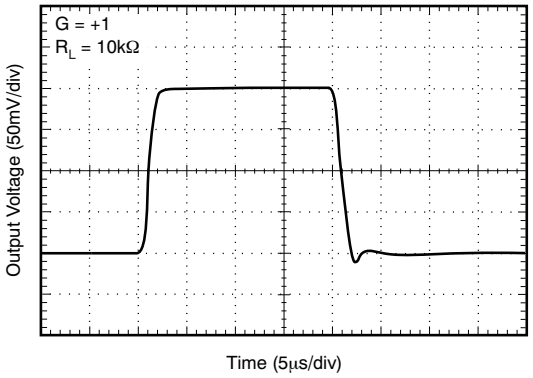


Figure 10. Small-Signal Step Response

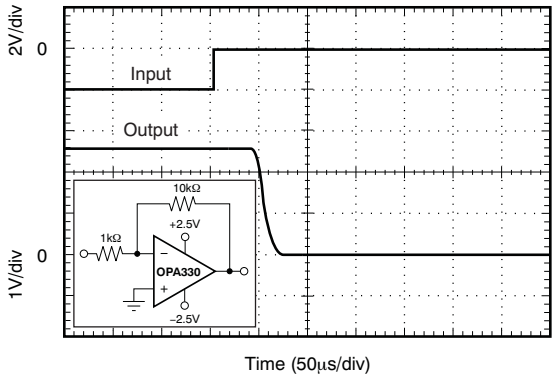


Figure 11. Positive Overvoltage Recovery

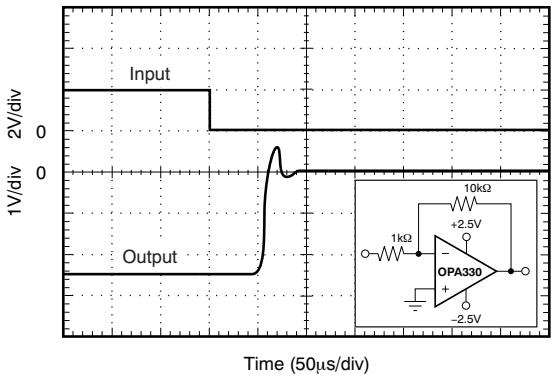


Figure 12. Negative Overvoltage Recovery

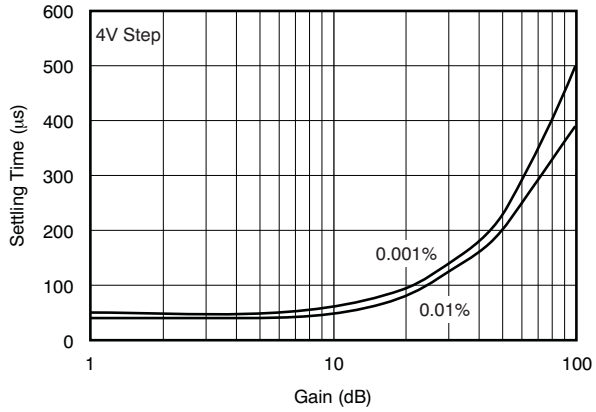


Figure 13. Settling Time vs Closed-Loop Gain

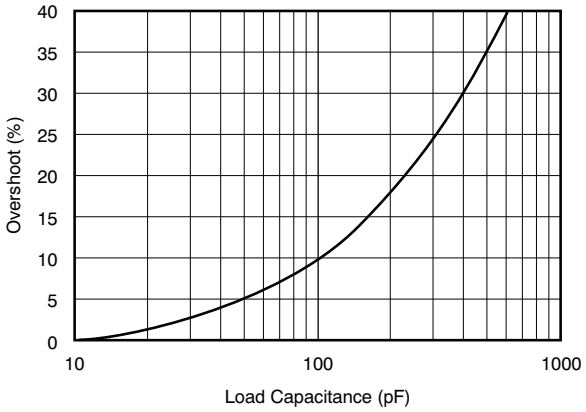


Figure 14. Small-Signal Overshoot vs Load Capacitance

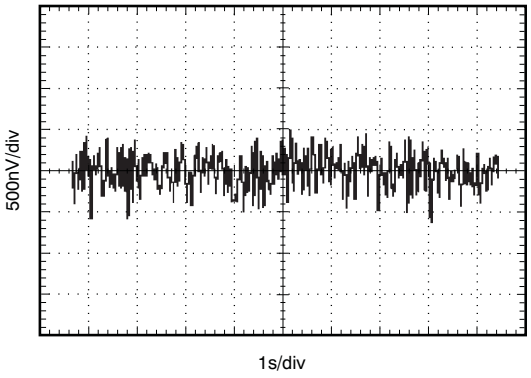


Figure 15. 0.1-Hz to 10-Hz Noise

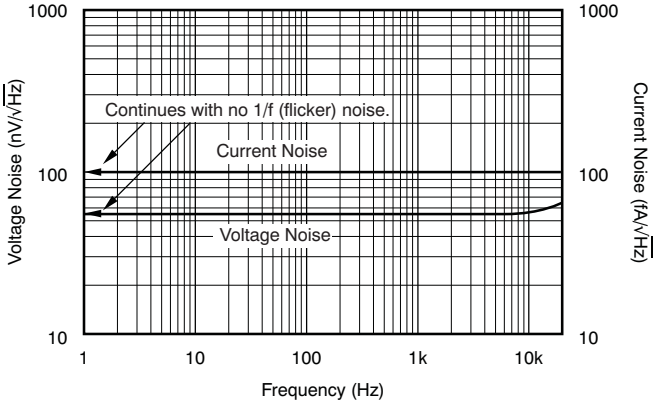


Figure 16. Current and Voltage Noise Spectral Density vs Frequency

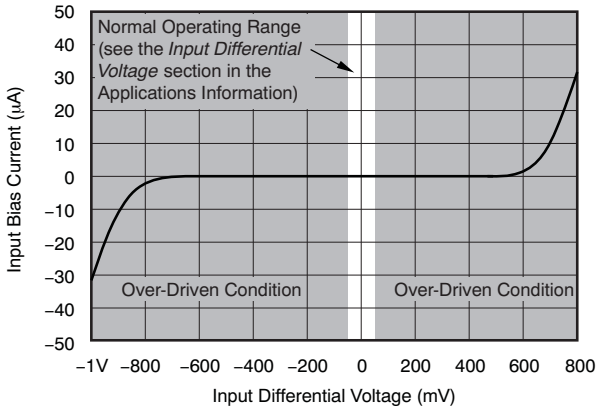


Figure 17. Input Bias Current vs Input Differential Voltage

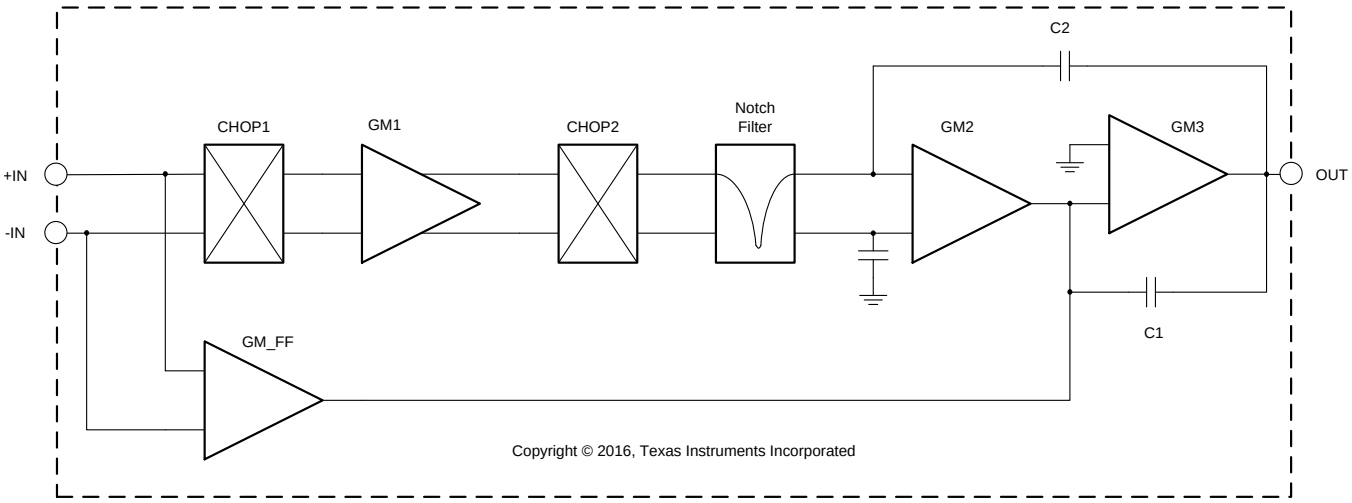
8 Detailed Description

8.1 Overview

The OPA330 family of Zerø-Drift amplifiers feature a proprietary auto-calibration technique to simultaneously achieve near-zero drift over time and temperature at only 35 µA (maximum) of quiescent current while also providing low offset voltage (50 µV maximum). These devices are unity-gain stable, precision operational amplifiers free from unexpected output and phase reversal. The OPA330 series are also optimized for low-voltage, single-supply operation: as low as 1.8 V (±0.9 V) and up to 5.5 V (±2.75 V).

The proprietary Zerø-Drift circuitry lowers the 1/f noise component as well as offers the advantage of low input offset voltage over time and temperature. The OPA330 series of operational amplifiers are ideal for cost-sensitive applications and applications that operate without regulation directly from battery power.

8.2 Functional Block Diagram



8.3 Feature Description

The OPA33x family is unity-gain stable and free from unexpected output phase reversal. These devices use a proprietary auto-calibration technique to provide low offset voltage and very low drift over time and temperature. For lowest offset voltage and precision performance, optimize circuit layout, and mechanical conditions. Avoid temperature gradients that create thermoelectric (Seebeck) effects in the thermocouple junctions formed from connecting dissimilar conductors. Cancel these thermally-generated potentials by assuring they are equal on both input terminals. Other layout and design considerations include:

- Use low thermoelectric-coefficient conditions (avoid dissimilar metals).
- Thermally isolate components from power supplies or other heat sources.
- Shield operational amplifier and input circuitry from air currents, such as cooling fans.

Following these guidelines reduces the likelihood of junctions being at different temperatures, which can cause thermoelectric voltage drift of 0.1 µV/°C or higher, depending on materials used.

8.4 Device Functional Modes

The OPAx330 has a single functional mode and is operational when the power-supply voltage is greater than 1.8 V (±0.9 V). The maximum power-supply voltage for the OPAx330 is 5.5 V (±2.75 V).

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The OPA330, OPA2330, and OPA4330 are unity-gain stable, precision operational amplifiers free from unexpected output and phase reversal. The use of proprietary Zerø-Drift circuitry gives the benefit of low input offset voltage over time and temperature, as well as lowering the 1/f noise component. As a result of the high PSRR, these devices work well in applications that run directly from battery power without regulation. The OPA330 family is optimized for low-voltage, single-supply operation. These miniature, high-precision, low quiescent current amplifiers offer high-impedance inputs that have a common-mode range 100 mV beyond the supplies and a rail-to-rail output that swings within 100 mV of the supplies under normal test conditions. The OPA330 series are precision amplifiers for cost-sensitive applications.

9.1.1 Operating Voltage

The OPA330 series operational amplifiers can be used with single or dual supplies from an operating range of V_S = 1.8 V (±0.9 V) up to 5.5 V (±2.75 V). Supply voltages greater than 7 V can permanently damage the device (see *Absolute Maximum Ratings*). Key parameters that vary over the supply voltage or temperature range are shown in *Typical Characteristics*.

9.1.2 Input Voltage

The OPA330, OPA2330, and OPA4330 input common-mode voltage range extends 0.1 V beyond the supply rails. The OPA330 is designed to cover the full range without the troublesome transition region found in some other rail-to-rail amplifiers.

Typically, input bias current is approximately 200 pA. Input voltages exceeding the power supplies however, can cause excessive current to flow into or out of the input pins. Momentary voltages greater than the power supply can be tolerated if the input current is limited to 10 mA. This limitation is easily accomplished with an input resistor, as shown in Figure 18.

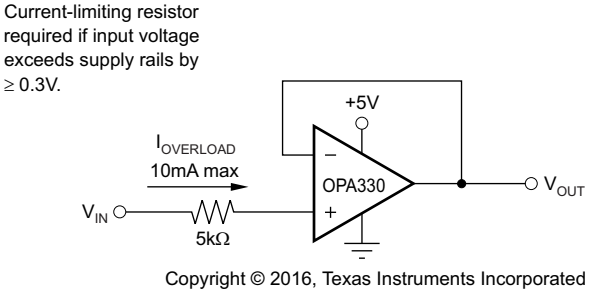


Figure 18. Input Current Protection

9.1.3 Input Differential Voltage

The typical input bias current of the OPA330 during normal operation is approximately 200 pA. In over-driven conditions, the bias current can increase significantly (see Figure 17). The most common cause of an over-driven condition occurs when the operational amplifier is outside of the linear range of operation. When the output of the operational amplifier is driven to one of the supply rails the feedback loop requirements cannot be satisfied and a differential input voltage develops across the input pins. This differential input voltage results in activation of parasitic diodes inside the front end input chopping switches that combine with 10-kΩ electromagnetic interference (EMI) filter resistors to create the equivalent circuit illustrated in Figure 19. Notice that the input bias current remains within specification within the linear region.

Application Information (continued)

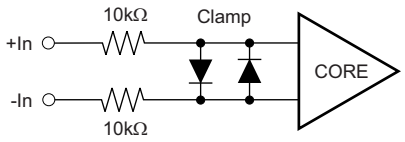


Figure 19. Equivalent Input Circuit

9.1.4 Internal Offset Correction

The OPA330, OPA2330, and OPA4330 operational amplifiers use an auto-calibration technique with a time-continuous, 125-kHz operational amplifier in the signal path. This amplifier is zero-corrected every 8 µs using a proprietary technique. Upon power up, the amplifier requires approximately 100 µs to achieve specified V_{OS} accuracy. This design has no aliasing or flicker noise.

9.1.5 EMI Susceptibility and Input Filtering

Operational amplifiers vary in their susceptibility to EMI. If conducted EMI enters the operational amplifier, the DC offset observed at the amplifier output may shift from its nominal value while the EMI is present. This shift is a result of signal rectification associated with the internal semiconductor junctions. While all operational amplifier pin functions can be affected by EMI, the input pins are likely to be the most susceptible. The OPA330 operational amplifier family incorporates an internal input low-pass filter that reduces the amplifier response to EMI. Both common-mode and differential mode filtering are provided by the input filter. The filter is designed for a cutoff frequency of approximately 8 MHz (–3 dB), with a rolloff of 20 dB per decade.

9.1.6 Achieving Output Swing to the Operational Amplifier Negative Rail

Some applications require output voltage swings from 0 V to a positive full-scale voltage (such as 2.5 V) with excellent accuracy. With most single-supply operational amplifiers, problems arise when the output signal approaches 0 V, near the lower output swing limit of a single-supply operational amplifier. A good single-supply operational amplifier may swing close to single-supply ground, but does not reach ground. The output of the OPA330, OPA2330, and OPA4330 can be made to swing to ground, or slightly below, on a single-supply power source. To do so requires the use of another resistor and an additional, more negative, power supply than the operational amplifier negative supply. A pulldown resistor may be connected between the output and the additional negative supply to pull the output down below the value that the output would otherwise achieve, as shown in Figure 20.

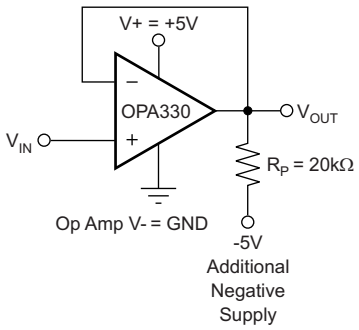


Figure 20. For V_{OUT} Range to Ground

Application Information (continued)

The OPA330, OPA2330, and OPA4330 have an output stage that allows the output voltage to be pulled to its negative supply rail, or slightly below, using the technique previously described. This technique only works with some types of output stages. The OPA330, OPA2330, and OPA4330 have been characterized to perform with this technique; the recommended resistor value is approximately 20 kΩ. This configuration increases the current consumption by several hundreds of microamps. Accuracy is excellent down to 0 V and as low as –2 mV. Limiting and nonlinearity occur below –2 mV, but excellent accuracy returns as the output is again driven above –2 mV. Lowering the resistance of the pulldown resistor allows the operational amplifier to swing even further below the negative rail. Resistances as low as 10 kΩ can be used to achieve excellent accuracy down to –10 mV.

9.1.7 Photosensitivity

Although the OPA330 YFF package has a protective backside coating that reduces the amount of light exposure on the die, unless fully shielded, ambient light can reach the active region of the device. Input bias current for the package is specified in the absence of light. Depending on the amount of light exposure in a given application, an increase in bias current, and possible increases in offset voltage should be expected. Fluorescent lighting may introduce noise or hum because of the time-varying light output. Best layout practices include end-product packaging that provides shielding from possible light sources during operation.

9.2 Typical Application

9.2.1 Bidirectional Current-Sensing

This single-supply, low-side, bidirectional current-sensing solution detects load currents from –1 A to 1 A. The single-ended output spans from 110 mV to 3.19 V. This design uses the OPA2330 because of its low offset voltage and rail-to-rail input and output. One of the amplifiers is configured as a difference amplifier and the other provides the reference voltage.

Figure 21 shows the solution.

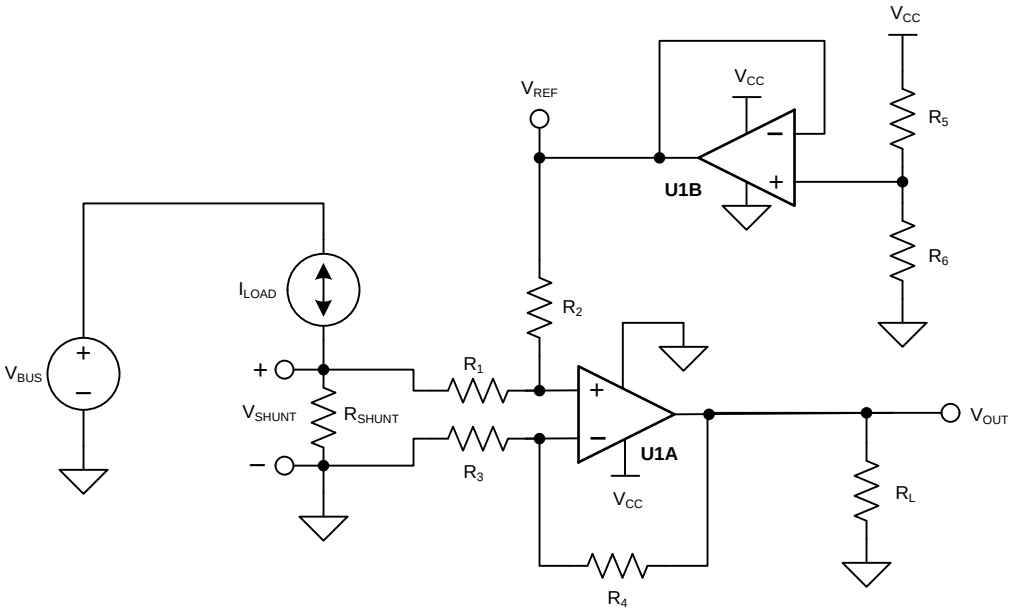


Figure 21. Bidirectional Current-Sensing Schematic

Typical Application (continued)

9.2.1.1 Design Requirements

This solution has the following requirements:

- Supply voltage: 3.3 V
- Input: –1 A to 1 A
- Output: 1.65 V ±1.54 V (110 mV to 3.19 V)

9.2.1.2 Detailed Design Procedure

The load current, I_{LOAD}, flows through the shunt resistor (R_{SHUNT}) to develop the shunt voltage, V_{SHUNT}. The shunt voltage is then amplified by the difference amplifier, which consists of U1A and R_1 through R_4. The gain of the difference amplifier is set by the ratio of R_4 to R_3. To minimize errors, set $R_2 = R_4$ and $R_1 = R_3$. The reference voltage, V_{REF}, is supplied by buffering a resistor divider using U1B. The transfer function is given by Equation 1.

$$V_{OUT} = V_{SHUNT} \times Gain_{Diff\_Amp} + V_{REF}$$

where

- $V_{SHUNT} = I_{LOAD} \times R_{SHUNT}$
- $Gain_{Diff\_Amp} = \frac{R_4}{R_3}$
- $V_{REF} = V_{CC} \times \left(\frac{R_6}{R_5 + R_6} \right)$

(1)

There are two types of errors in this design: offset and gain. Gain errors are introduced by the tolerance of the shunt resistor and the ratios of R_4 to R_3 and, similarly, R_2 to R_1. Offset errors are introduced by the voltage divider (R_5 and R_6) and how closely the ratio of R_4/R_3 matches R_2/R_1. The latter value impacts the CMRR of the difference amplifier, which ultimately translates to an offset error.

Because this is a low-side measurement, the value of V_{SHUNT} is the ground potential for the system load. Therefore, it is important to place a maximum value on V_{SHUNT}. In this design, the maximum value for V_{SHUNT} is set to 100 mV. Equation 2 calculates the maximum value of the shunt resistor given a maximum shunt voltage of 100 mV and maximum load current of 1 A.

$$R_{SHUNT(Max)} = \frac{V_{SHUNT(Max)}}{I_{LOAD(Max)}} = \frac{100\ mV}{1\ A} = 100\ m\Omega \quad (2)$$

The tolerance of R_{SHUNT} is directly proportional to cost. For this design, a shunt resistor with a tolerance of 0.5% was selected. If greater accuracy is required, select a 0.1% resistor or better.

The load current is bidirectional; therefore, the shunt voltage range is –100 mV to 100 mV. This voltage is divided down by R_1 and R_2 before reaching the operational amplifier, U1A. Take care to ensure that the voltage present at the noninverting node of U1A is within the common-mode range of the device. Therefore, it is important to use an operational amplifier, such as the OPA330, that has a common-mode range that extends below the negative supply voltage. Finally, to minimize offset error, note that the OPA330 has a typical offset voltage of merely ±8 µV (±50 µV maximum).

Given a symmetric load current of –1 A to 1 A, the voltage divider resistors (R_5 and R_6) must be equal. To be consistent with the shunt resistor, a tolerance of 0.5% was selected. To minimize power consumption, 10-kΩ resistors were used.

To set the gain of the difference amplifier, the common-mode range and output swing of the OPA330 must be considered. Equation 3 and Equation 4 depict the typical common-mode range and maximum output swing, respectively, of the OPA330 given a 3.3-V supply.

$$-100\ mV < V_{CM} < 3.4\ V \quad (3)$$

$$100\ mV < V_{OUT} < 3.2\ V \quad (4)$$

The gain of the difference amplifier can now be calculated as shown in Equation 5.

$$Gain_{Diff\_Amp} = \frac{V_{OUT\_Max} - V_{OUT\_Min}}{R_{SHUNT} \times (I_{MAX} - I_{MIN})} = \frac{3.2\ V - 100\ mV}{100\ m\Omega \times [1\ A - (-1A)]} = 15.5\ \frac{V}{V} \quad (5)$$

Typical Application (continued)

The resistor value selected for R_1 and R_3 was 1 kΩ. 15.4 kΩ was selected for R_2 and R_4 because it is the nearest standard value. Therefore, the ideal gain of the difference amplifier is 15.4 V/V.

The gain error of the circuit primarily depends on R_1 through R_4. As a result of this dependence, 0.1% resistors were selected. This configuration reduces the likelihood that the design requires a two-point calibration. A simple one-point calibration, if desired, removes the offset errors introduced by the 0.5% resistors.

9.2.1.3 Application Curve

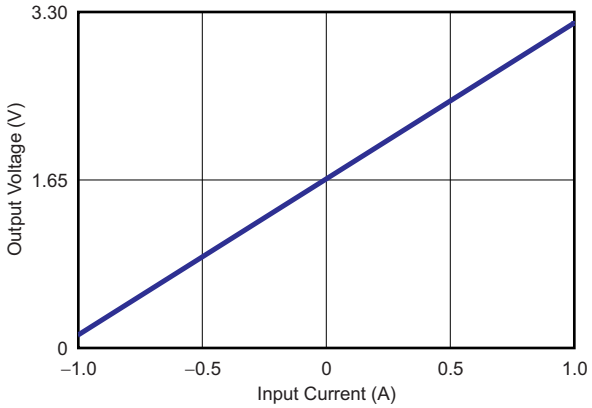


Figure 22. Bidirectional Current-Sensing Circuit Performance: Output Voltage vs Input Current

9.3 System Examples

9.3.1 Single Operational Amplifier Bridge Amplifier

Figure 23 shows the basic configuration for a bridge amplifier.

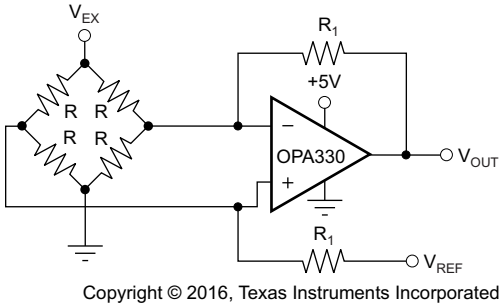


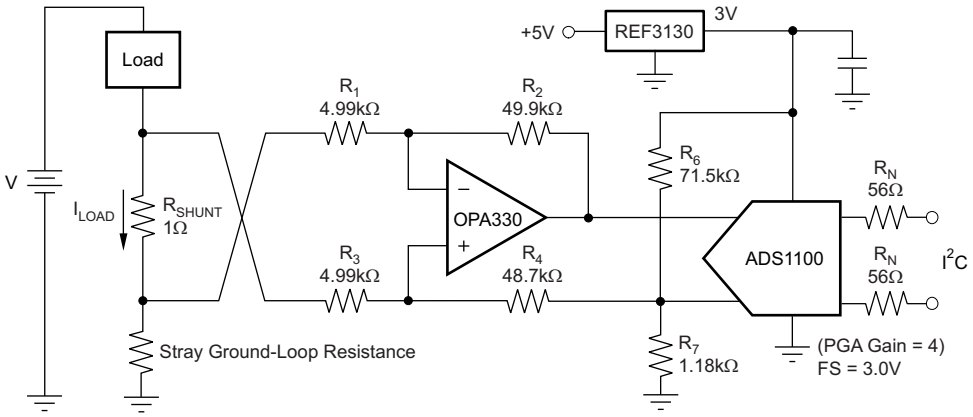
Figure 23. Single Operational Amplifier Bridge Amplifier Schematic

System Examples (continued)

9.3.2 Low-Side Current Monitor

A low-side current shunt monitor is shown in Figure 24.

R_N are operational resistors used to isolate the ADS1100 from the noise of the digital I^2C bus. Because the ADS1100 is a 16-bit converter, a precise reference is essential for maximum accuracy. If absolute accuracy is not required, and the 5-V power supply is sufficiently stable, the REF3130 may be omitted.



NOTE: 1% resistors provide adequate common-mode rejection at small ground-loop errors.

Figure 24. Low-Side Current Monitor

9.3.3 Thermistor Measurement

Figure 25 shows the OPA330 in a typical thermistor circuit.

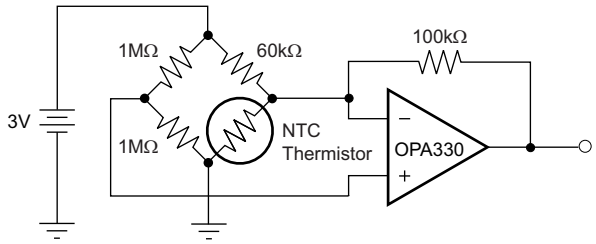


Figure 25. Thermistor Measurement Schematic

10 Power Supply Recommendations

The OPAx330 family of devices is specified for operation from 1.8 V to 5.5 V (±0.9 V to ±2.75 V). Parameters that can exhibit significant variance with regard to operating voltage are presented in *Typical Characteristics*.

11 Layout

11.1 Layout Guidelines

TI always recommends paying attention to good layout practice. Keep traces short and, when possible, use a printed-circuit board (PCB) ground plane with surface-mount components placed as close to the device pins as possible. Place a 0.1-µF capacitor closely across the supply pins. These guidelines must be applied throughout the analog circuit to improve performance and provide benefits such as reducing the electromagnetic interference (EMI) susceptibility.

For lowest offset voltage and precision performance, circuit layout, and mechanical conditions must be optimized. Avoid temperature gradients that create thermoelectric (Seebeck) effects in the thermocouple junctions formed from connecting dissimilar conductors. These thermally-generated potentials can be made to cancel by assuring they are equal on both input terminals. Other layout and design considerations include:

- Use low thermoelectric-coefficient conditions (avoid dissimilar metals).
- Thermally isolate components from power supplies or other heat sources.
- Shield operational amplifier and input circuitry from air currents, such as cooling fans.

Following these guidelines reduces the likelihood of junctions being at different temperatures, which can cause thermoelectric voltage drift of 0.1 µV/°C or higher, depending on materials used.

11.1.1 VQFN and SON Packages

The OPA4330 is offered in a VQFN package. The OPA2330 is available in a 8-pin SON package, which is a VQFN package with lead contacts on only two sides of the bottom of the package. These leadless, near-chip-scale packages maximize board space and enhance thermal and electrical characteristics through an exposed pad. VQFN and SON packages are physically small, have a smaller routing area, improved thermal performance, and improved electrical parasitics, with a pinout scheme that is consistent with other commonly-used packages, such as SOIC and VSSOP. Additionally, the absence of external leads eliminates bent-lead issues.

The VQFN and SON package can be easily mounted using standard PCB assembly techniques. See the application note, *QFN/SON PCB Attachment* (SLUA271), and the application report, *Quad Flatpack No-Lead Logic Packages* (SCBA017), both available for download at www.ti.com.

NOTE

The exposed leadframe die pad on the bottom of the package should be connected to V–.

11.1.2 VQFN and SON Layout Guidelines

The leadframe die pad must be soldered to a thermal pad on the PCB. A mechanical data sheet showing an example layout is attached at the end of this data sheet. Refinements to this layout may be required based on assembly process requirements. Mechanical drawings located at the end of this data sheet list the physical dimensions for the package and pad. The five holes in the landing pattern are optional, and are intended for use with thermal vias that connect the leadframe die pad to the heat sink area on the PCB.

Soldering the exposed pad significantly improves board-level reliability during temperature cycling, key push, package shear, and similar board-level tests. Even with applications that have low-power dissipation, the exposed pad must be soldered to the PCB to provide structural integrity and long-term reliability.

Layout Guidelines (continued)

11.1.3 OPA330 DSBGA

The OPA330 YFF package is a lead- (Pb-) free, die-level, wafer chip-scale package. Unlike devices that are in plastic packages, these devices have no molding compound, lead frame, wire bonds, or leads. Using standard surface-mount assembly procedures, the OPA330 YFF can be mounted to a printed-circuit board (PCB) without additional underfill. Figure 26 and Figure 27 detail the pinout and package marking, respectively. See the application note, *NanoStar™ and NanoFree™ 300μm Solder Bump WCSP* (SBVA017) for more detailed information on package characteristics and PCB design.

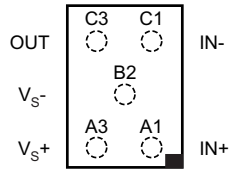


Figure 26. DSBGA Pin Description

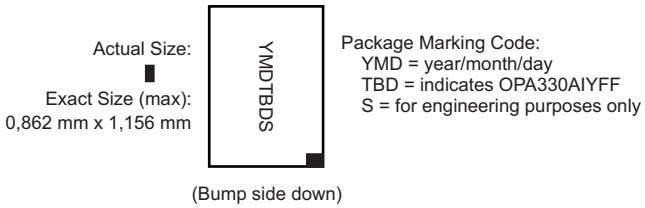


Figure 27. YFF Package Marking

11.2 Layout Example

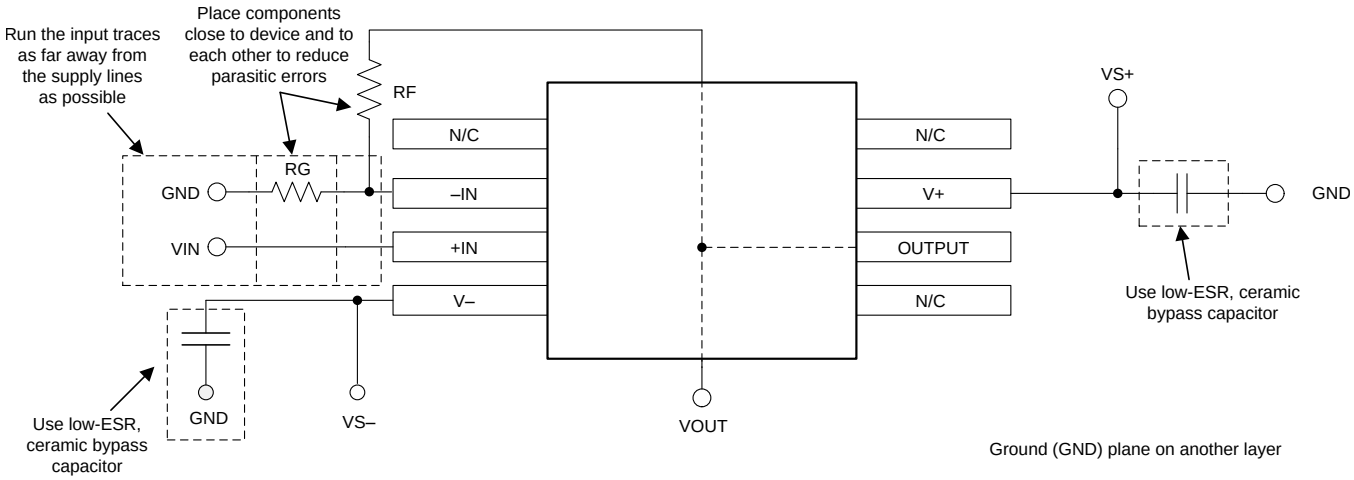


Figure 28. OPAx330 Layout Example

12 Device and Documentation Support

12.1 Device Support

12.1.1 Development Support

12.1.1.1 TINA-TI™ (Free Software Download)

TINA™ is a simple, powerful, and easy-to-use circuit simulation program based on a SPICE engine. TINA-TI™ is a free, fully-functional version of the TINA software, preloaded with a library of macro models in addition to a range of both passive and active models. TINA-TI provides all the conventional DC, transient, and frequency domain analysis of SPICE, as well as additional design capabilities.

Available as a free download from the Analog eLab Design Center, TINA-TI offers extensive post-processing capability that allows users to format results in a variety of ways. Virtual instruments offer the ability to select input waveforms and probe circuit nodes, voltages, and waveforms, creating a dynamic quick-start tool.

NOTE

These files require that either the TINA software (from DesignSoft™) or TINA-TI software be installed. Download the free TINA-TI software from the TINA-TI folder.

12.1.1.2 DIP Adapter EVM

The DIP Adapter EVM tool provides an easy, low-cost way to prototype small surface mount ICs. The evaluation tool these TI packages: D or U (SOIC-8), PW (TSSOP-8), DGK (VSSOP-8), DBV (SOT23-6, SOT23-5 and SOT23-3), DCK (SC70-6 and SC70-5), and DRL (SOT563-6). The DIP Adapter EVM may also be used with terminal strips or may be wired directly to existing circuits.

12.1.1.3 Universal Operational Amplifier EVM

The Universal Op Amp EVM is a series of general-purpose, blank circuit boards that simplify prototyping circuits for a variety of IC package types. The evaluation module board design allows many different circuits to be constructed easily and quickly. Five models are offered, with each model intended for a specific package type. PDIP, SOIC, VSSOP, TSSOP and SOT-23 packages are all supported.

NOTE

These boards are unpopulated, so users must provide their own ICs. TI recommends requesting several op amp device samples when ordering the Universal Op Amp EVM.

12.1.1.4 TI Precision Designs

TI Precision Designs are analog solutions created by TI's precision analog applications experts and offer the theory of operation, component selection, simulation, complete PCB schematic and layout, bill of materials, and measured performance of many useful circuits. TI Precision Designs are available online at http://www.ti.com/ww/en/analog/precision-designs/.

12.1.1.5 WEBENCH® Filter Designer

WEBENCH® Filter Designer is a simple, powerful, and easy-to-use active filter design program. The WEBENCH Filter Designer lets you create optimized filter designs using a selection of TI operational amplifiers and passive components from TI's vendor partners.

Available as a web-based tool from the WEBENCH® Design Center, WEBENCH® Filter Designer allows you to design, optimize, and simulate complete multistage active filter solutions within minutes.

12.1.1.6 Related Parts

For parts used in System Examples, see the following:

- *Self-Calibrating, 16-Bit Analog-to-Digital Converter*, ADS1100
- *20ppm/Degrees C Max, 100uA, SOT23-3 Series Voltage Reference*, REF3130

12.2 Documentation Support

12.2.1 Related Documentation

For additional information, see the following documents (available for download at www.ti.com):

- *QFN/SON PCB Attachment* (SLUA271)
- *Quad Flatpack No-Lead Logic Packages* (SCBA017)
- *NanoStar™ and NanoFree™ 300μm Solder Bump WCSP* (SBVA017)

12.3 Related Links

Table 2 lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 2. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
OPA330	Click here	Click here	Click here	Click here	Click here
OPA2330	Click here	Click here	Click here	Click here	Click here
OPA4330	Click here	Click here	Click here	Click here	Click here

12.4 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

12.5 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.6 Trademarks

NanoStar, NanoFree, TINA-TI, E2E are trademarks of Texas Instruments.
WEBENCH is a registered trademark of Texas Instruments.
TINA, DesignSoft are trademarks of DesignSoft, Inc.
All other trademarks are the property of their respective owners.

12.7 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

12.8 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
OPA2330AID	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	O2330A	Samples
OPA2330AIDGKR	ACTIVE	VSSOP	DGK	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	OCGQ	Samples
OPA2330AIDGKRG4	ACTIVE	VSSOP	DGK	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	OCGQ	Samples
OPA2330AIDGKT	ACTIVE	VSSOP	DGK	8	250	Green (RoHS & no Sb/Br)	CU NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	OCGQ	Samples
OPA2330AIDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	O2330A	Samples
OPA2330AIDRBR	ACTIVE	SON	DRB	8	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	OCGQ	Samples
OPA2330AIDRBRG4	ACTIVE	SON	DRB	8	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	OCGQ	Samples
OPA2330AIDRBT	ACTIVE	SON	DRB	8	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	OCGQ	Samples
OPA2330AIDRBTG4	ACTIVE	SON	DRB	8	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	OCGQ	Samples
OPA2330AIDRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	O2330A	Samples
OPA330AID	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	O330A	Samples
OPA330AIDBVR	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	OCFQ	Samples
OPA330AIDBVRG4	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	OCFQ	Samples
OPA330AIDBVT	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	OCFQ	Samples
OPA330AIDBVTG4	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	OCFQ	Samples
OPA330AIDCKR	ACTIVE	SC70	DCK	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	CHL	Samples
OPA330AIDCKRG4	ACTIVE	SC70	DCK	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	CHL	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
OPA330AIDCKT	ACTIVE	SC70	DCK	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	CHL	Samples
OPA330AIDCKTG4	ACTIVE	SC70	DCK	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	CHL	Samples
OPA330AIDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	O330A	Samples
OPA330AIDRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	O330A	Samples
OPA330AIYFFR	ACTIVE	DSBGA	YFF	5	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 125	OEH	Samples
OPA330AIYFFT	ACTIVE	DSBGA	YFF	5	250	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 125	OEH	Samples
OPA4330AID	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	O4330A	Samples
OPA4330AIDR	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	O4330A	Samples
OPA4330AIPW	ACTIVE	TSSOP	PW	14	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	O4330A	Samples
OPA4330AIPWR	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	O4330A	Samples
OPA4330AIRGYR	ACTIVE	VQFN	RGY	14	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	4330A	Samples
OPA4330AIRGYT	ACTIVE	VQFN	RGY	14	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	4330A	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

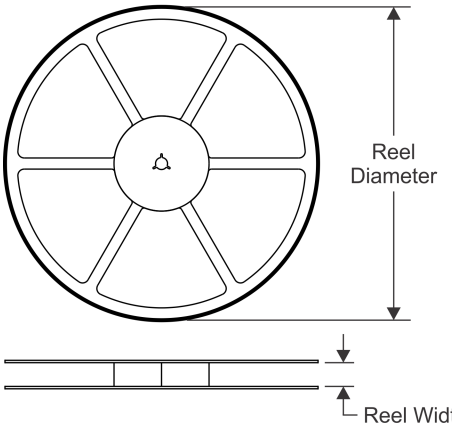
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

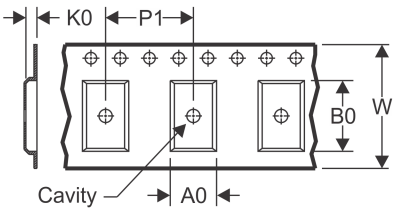
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

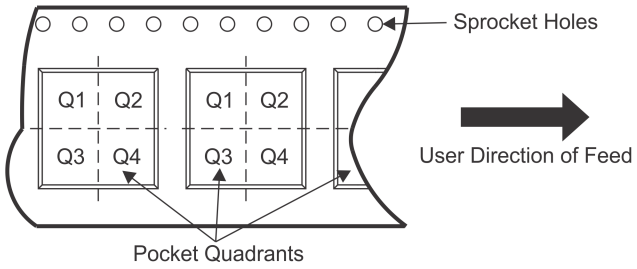


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

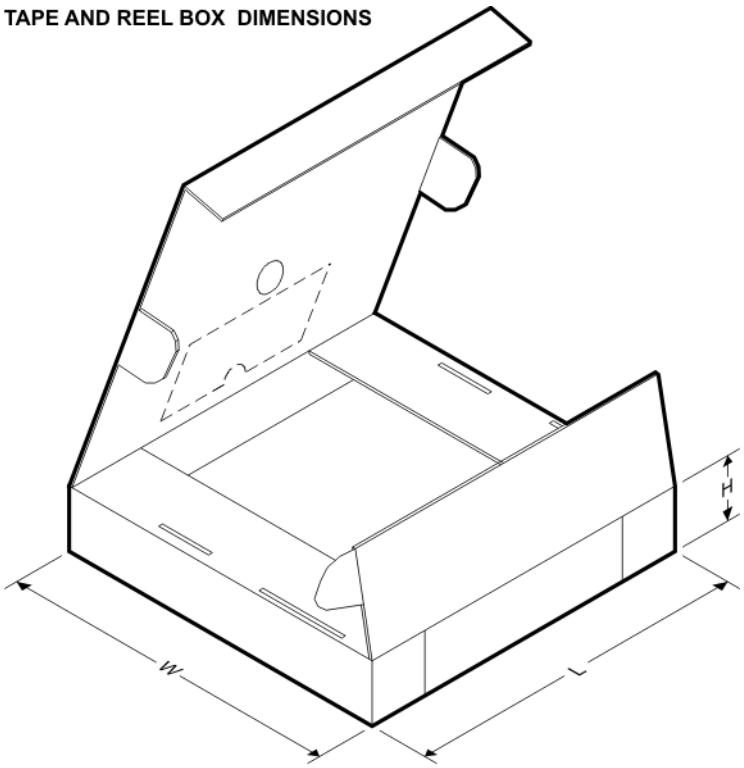
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
OPA2330AIDGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
OPA2330AIDGKT	VSSOP	DGK	8	250	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
OPA2330AIDRBR	SON	DRB	8	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
OPA2330AIDRBT	SON	DRB	8	250	180.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
OPA330AIDBVR	SOT-23	DBV	5	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
OPA330AIDBVR	SOT-23	DBV	5	3000	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
OPA330AIDBVT	SOT-23	DBV	5	250	178.0	9.0	3.3	3.2	1.4	4.0	8.0	Q3
OPA330AIDCKR	SC70	DCK	5	3000	179.0	8.4	2.2	2.5	1.2	4.0	8.0	Q3
OPA330AIDCKT	SC70	DCK	5	250	179.0	8.4	2.2	2.5	1.2	4.0	8.0	Q3
OPA330AIDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
OPA330AIYFFR	DSBGA	YFF	5	3000	180.0	8.4	0.97	1.27	0.73	4.0	8.0	Q1
OPA330AIYFFT	DSBGA	YFF	5	250	180.0	8.4	0.97	1.27	0.73	4.0	8.0	Q1
OPA4330AIDR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
OPA4330AIPWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
OPA4330AIRGYR	VQFN	RGY	14	3000	330.0	12.4	3.75	3.75	1.15	8.0	12.0	Q1
OPA4330AIRGYT	VQFN	RGY	14	250	180.0	12.4	3.75	3.75	1.15	8.0	12.0	Q1

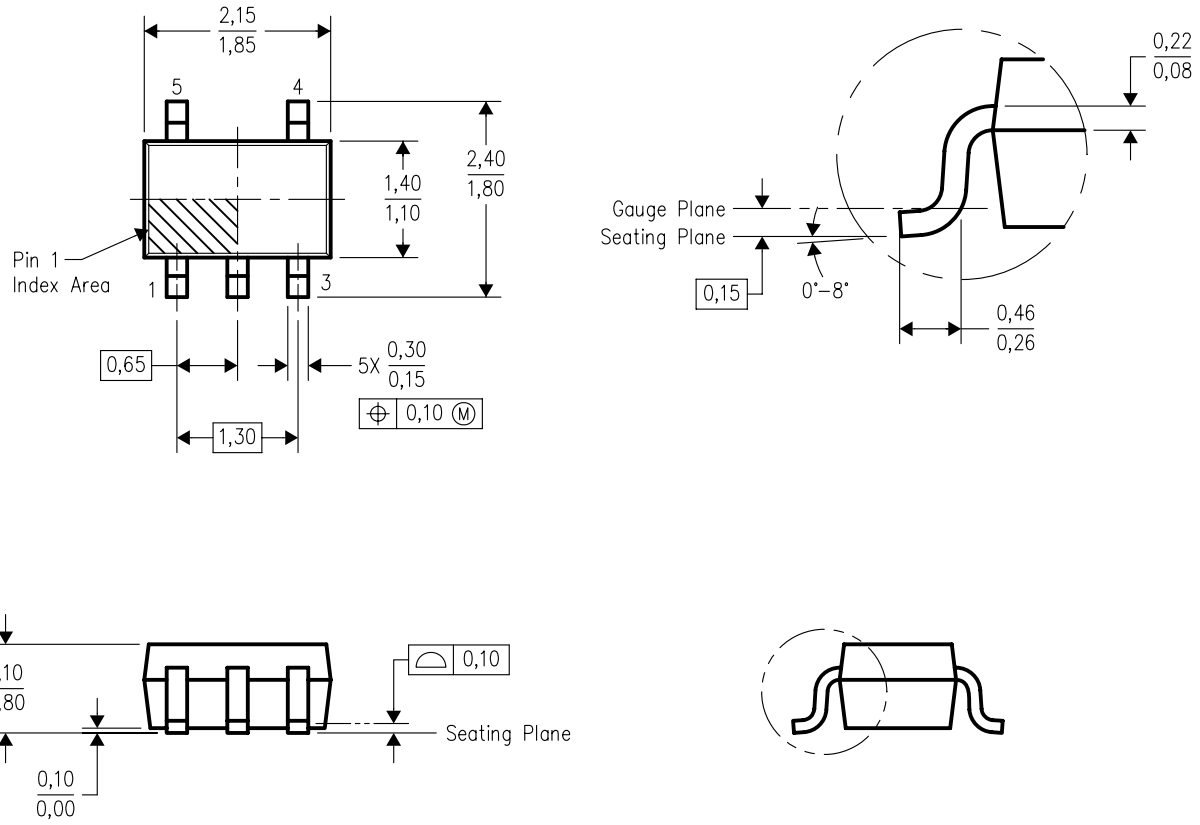
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
OPA2330AIDGKR	VSSOP	DGK	8	2500	364.0	364.0	27.0
OPA2330AIDGKT	VSSOP	DGK	8	250	364.0	364.0	27.0
OPA2330AIDRBR	SON	DRB	8	3000	367.0	367.0	35.0
OPA2330AIDRBT	SON	DRB	8	250	210.0	185.0	35.0
OPA330AIDBVR	SOT-23	DBV	5	3000	180.0	180.0	18.0
OPA330AIDBVR	SOT-23	DBV	5	3000	203.0	203.0	35.0
OPA330AIDBVT	SOT-23	DBV	5	250	180.0	180.0	18.0
OPA330AIDCKR	SC70	DCK	5	3000	203.0	203.0	35.0
OPA330AIDCKT	SC70	DCK	5	250	203.0	203.0	35.0
OPA330AIDR	SOIC	D	8	2500	367.0	367.0	35.0
OPA330AIYFFR	DSBGA	YFF	5	3000	210.0	185.0	35.0
OPA330AIYFFT	DSBGA	YFF	5	250	210.0	185.0	35.0
OPA4330AIDR	SOIC	D	14	2500	367.0	367.0	38.0
OPA4330AIPWR	TSSOP	PW	14	2000	367.0	367.0	35.0
OPA4330AIRGYR	VQFN	RGY	14	3000	367.0	367.0	35.0
OPA4330AIRGYT	VQFN	RGY	14	250	210.0	185.0	35.0

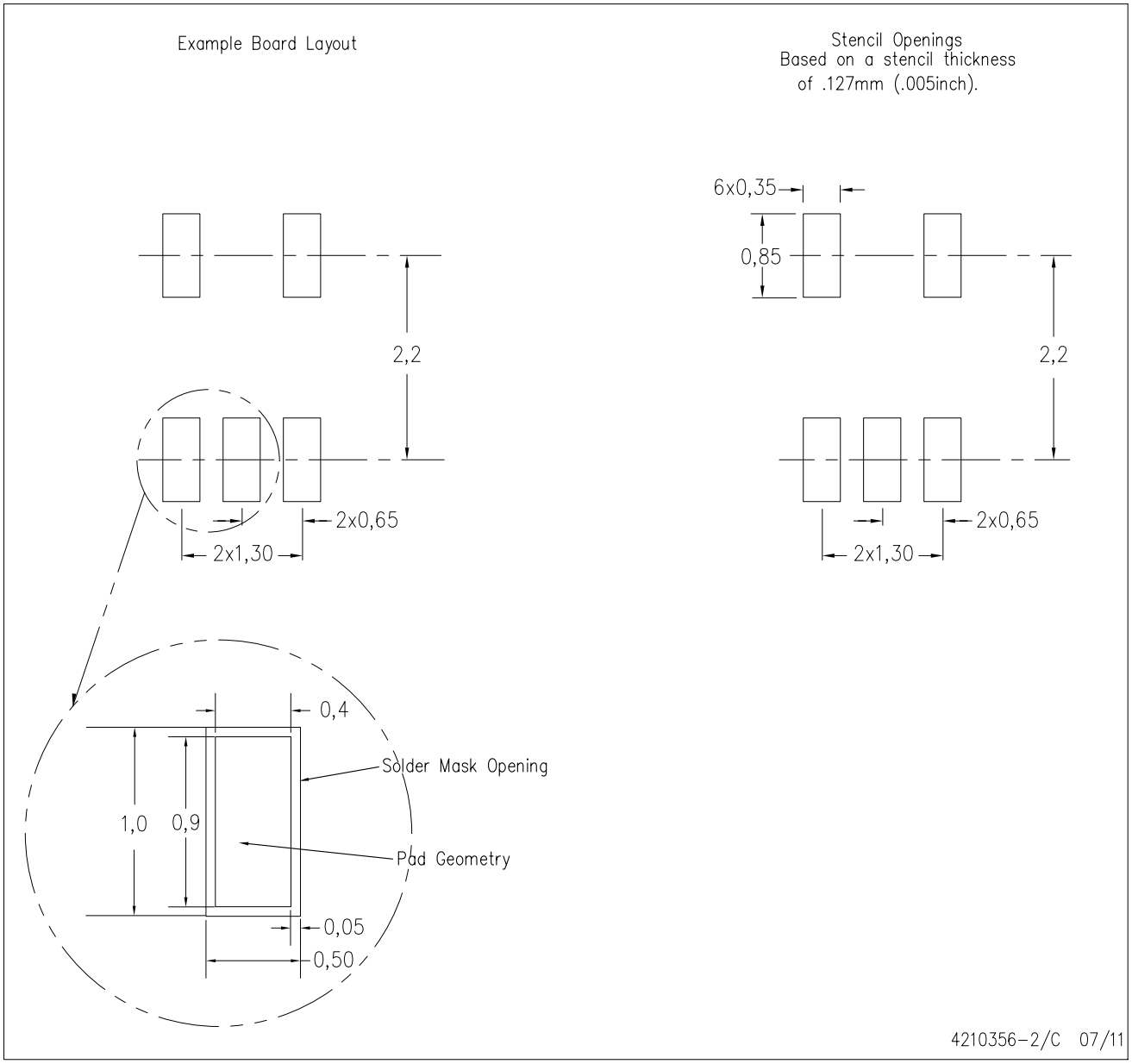
DCK (R–PDSO–G5) PLASTIC SMALL–OUTLINE PACKAGE



4093553–3/G 01/2007

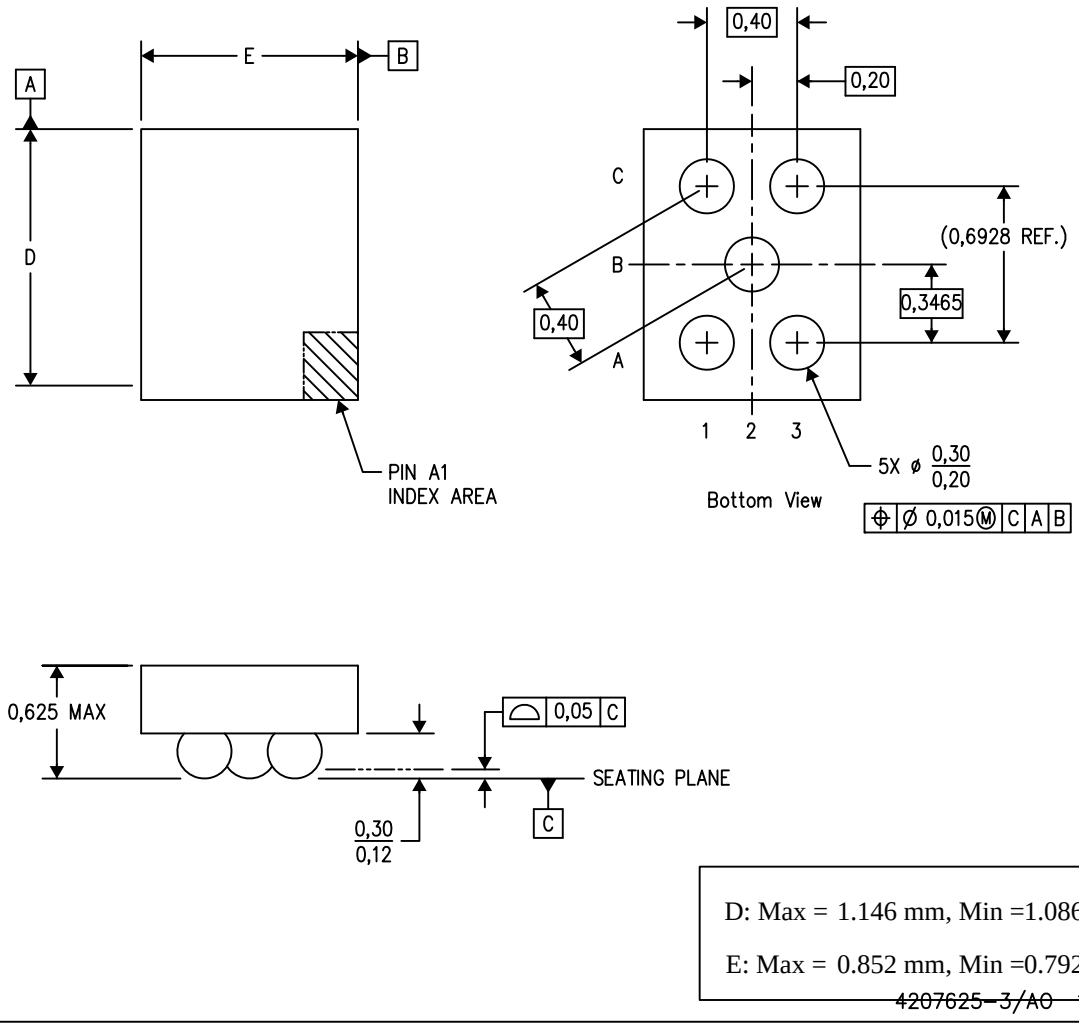
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
D. Falls within JEDEC MO–203 variation AA.

DCK (R–PDSO–G5) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
D. Publication IPC–7351 is recommended for alternate designs.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.

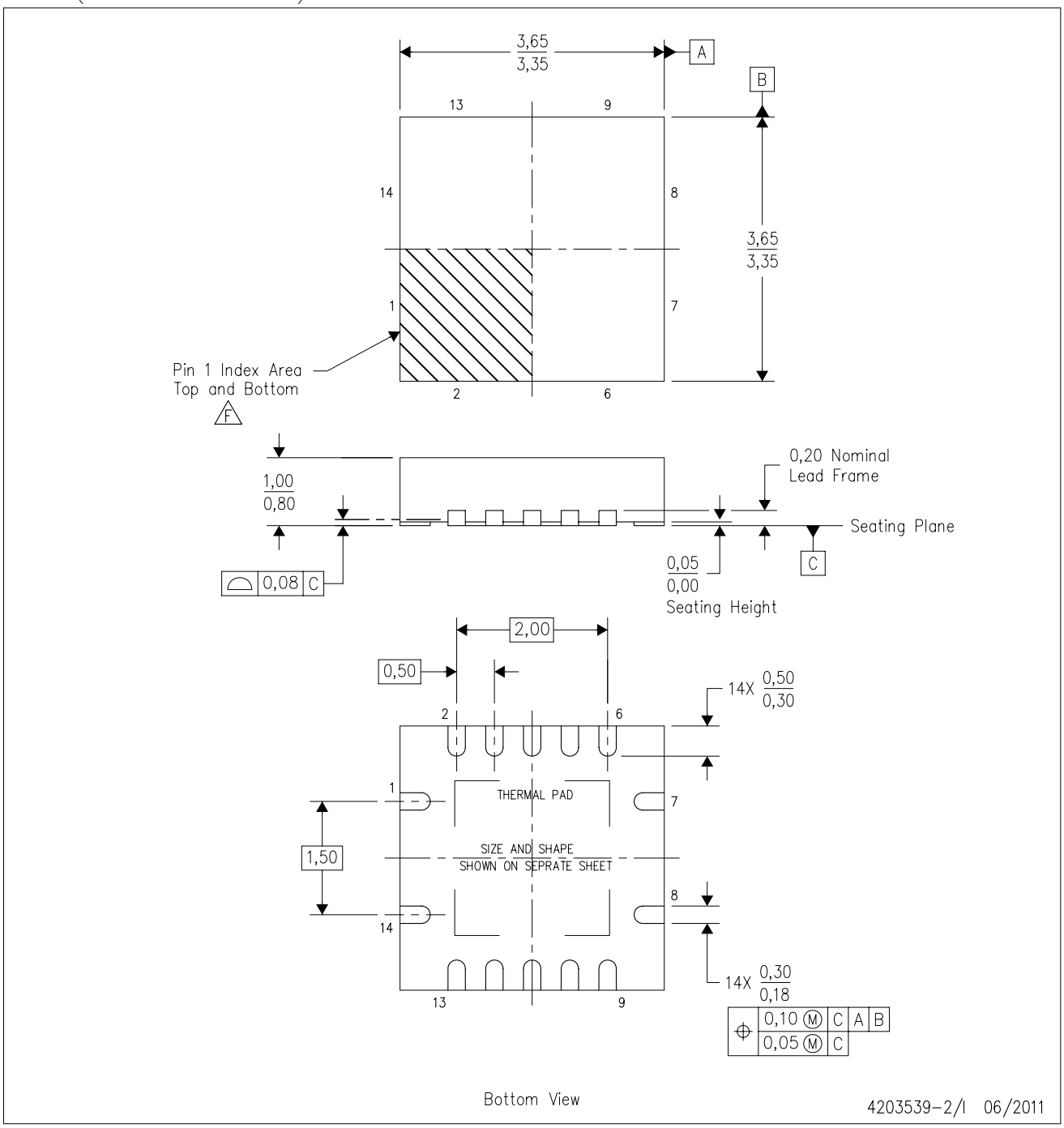
YFF (S–XBGA–N5) DIE–SIZE BALL GRID ARRAY



NOTES: A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. NanoFree™ package configuration.

NanoFree is a trademark of Texas Instruments.

RGY (S–PVQFN–N14) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. QFN (Quad Flatpack No–Lead) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
F. Pin 1 identifiers are located on both top and bottom of the package and within the zone indicated. The Pin 1 identifiers are either a molded, marked, or metal feature.
G. Package complies to JEDEC MO–241 variation BA.

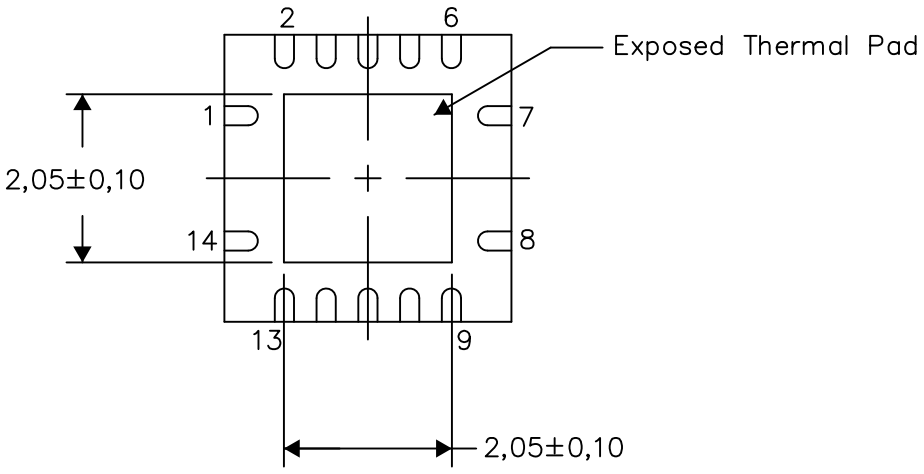
RGY (S–PVQFN–N14) PLASTIC QUAD FLATPACK NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



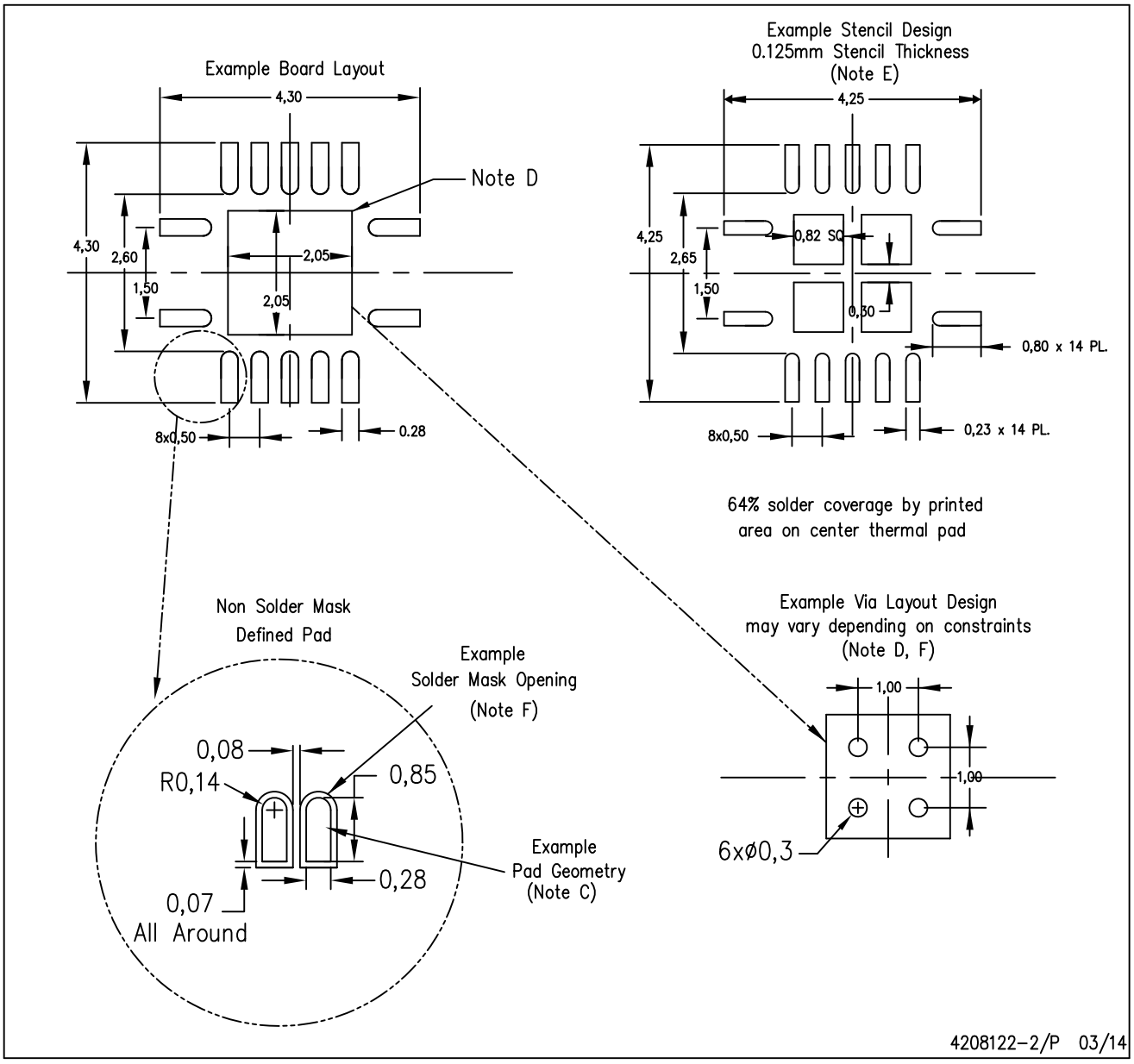
Bottom View

Exposed Thermal Pad Dimensions

4206353–2/P 03/14

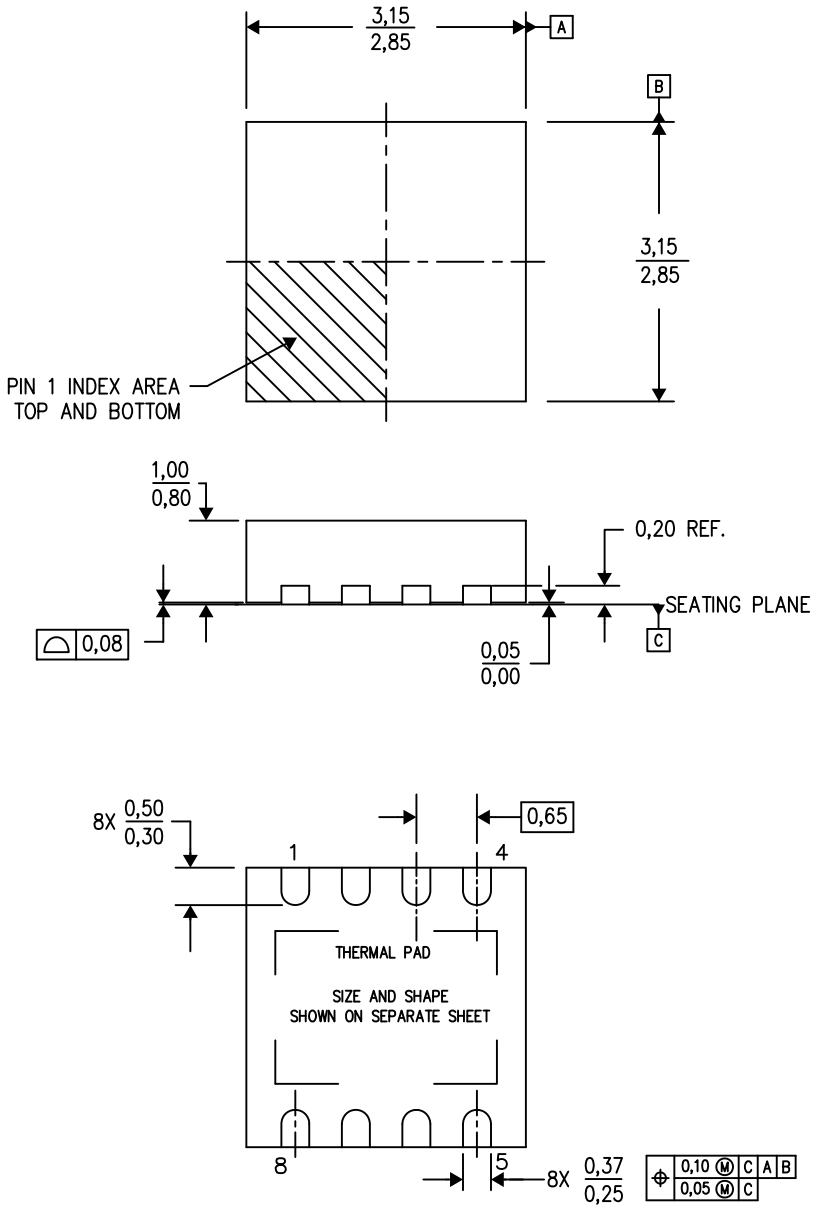
NOTE: All linear dimensions are in millimeters

RGY (S–PVQFN–N14) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat–Pack QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http: //www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.

DRB (S–PVSON–N8) PLASTIC SMALL OUTLINE NO–LEAD



4203482–2/K 06/12

NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Small Outline No–Lead (SON) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.

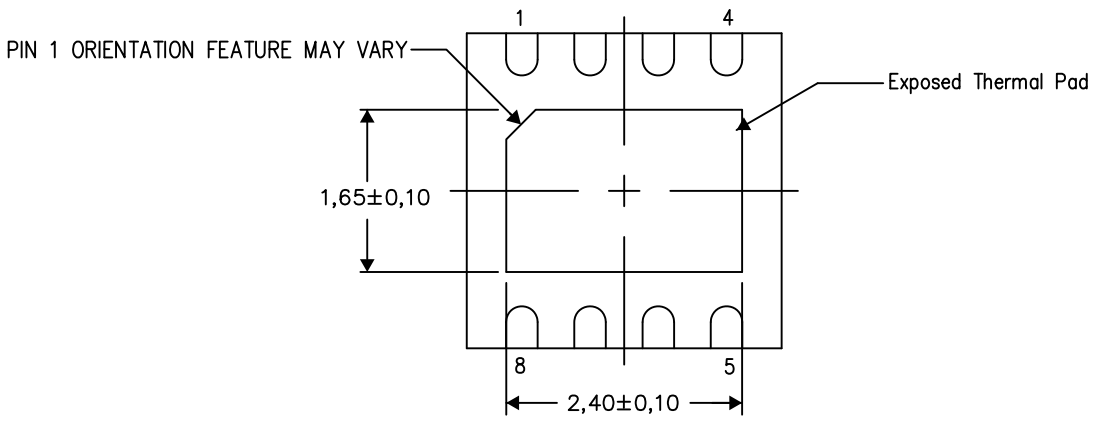
DRB (S–PVSON–N8) PLASTIC SMALL OUTLINE NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Bottom View

Exposed Thermal Pad Dimensions

4206340–3/T 08/15

NOTE: All linear dimensions are in millimeters

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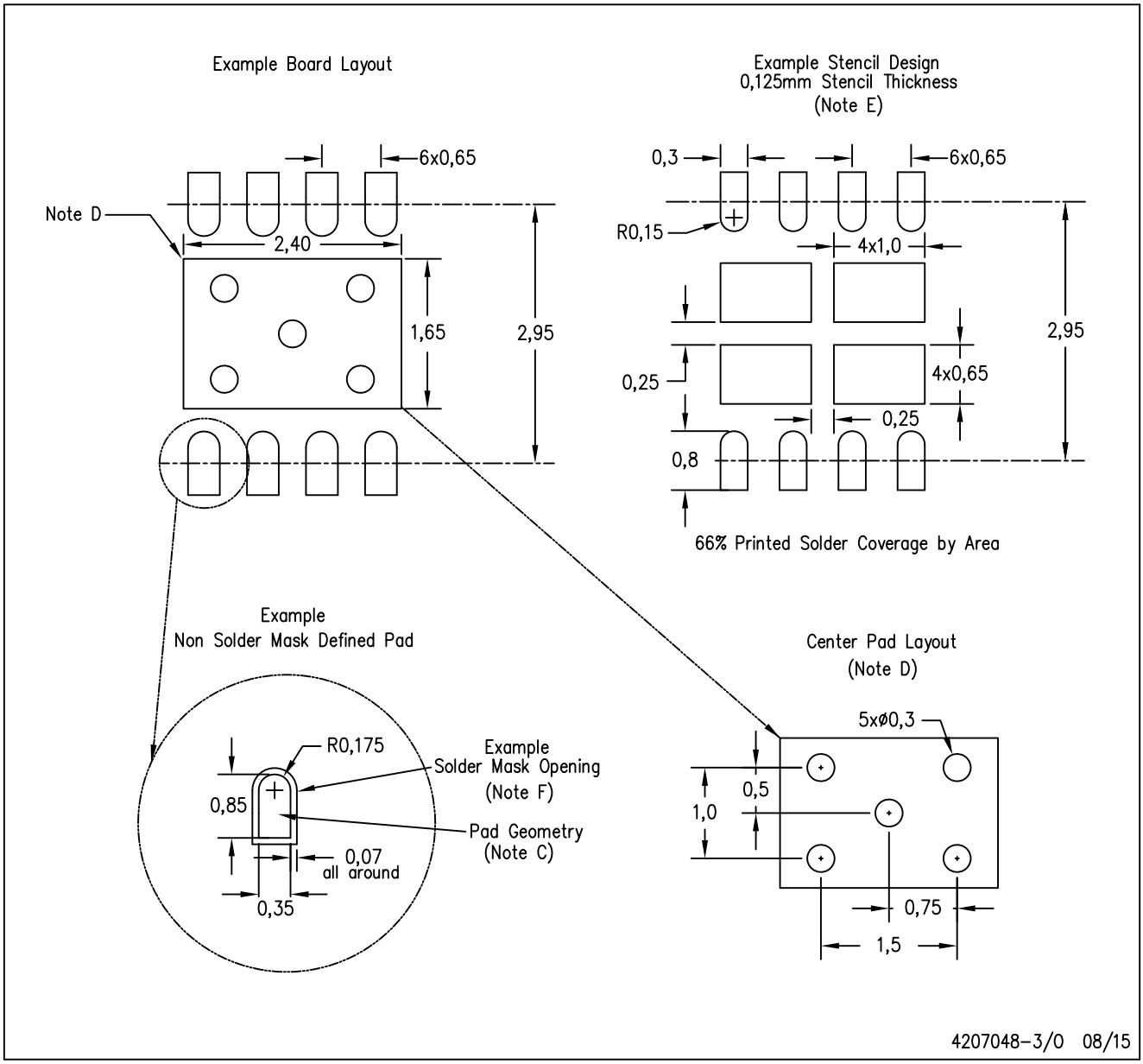
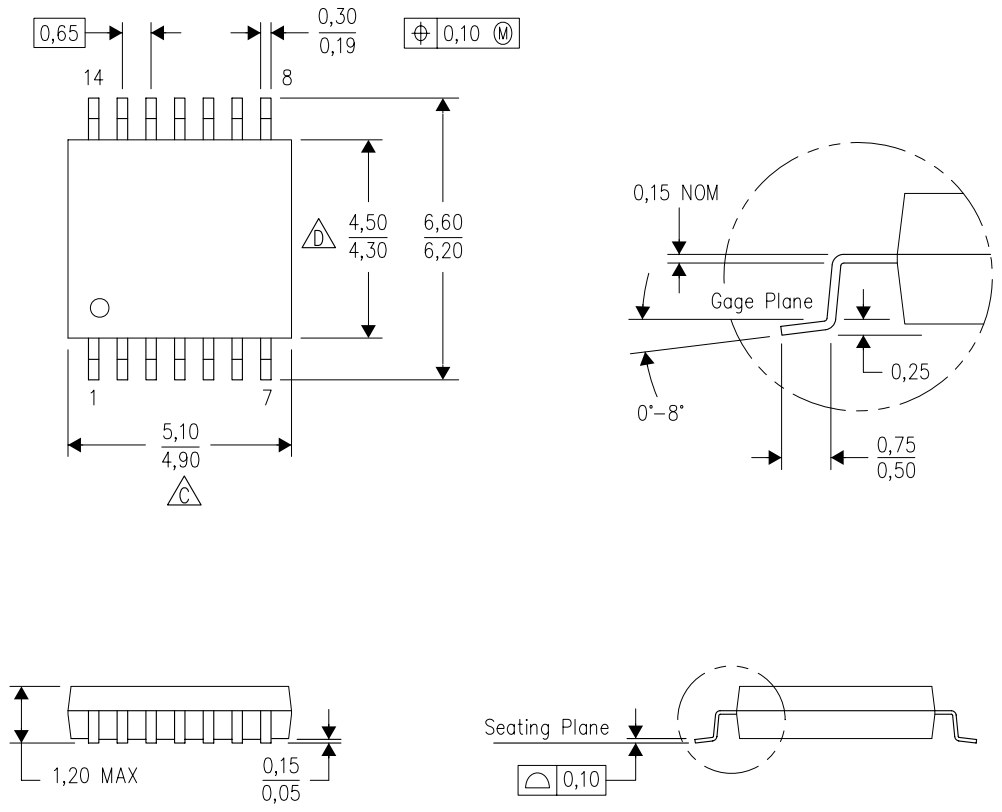


NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, QFN Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for solder mask tolerances.

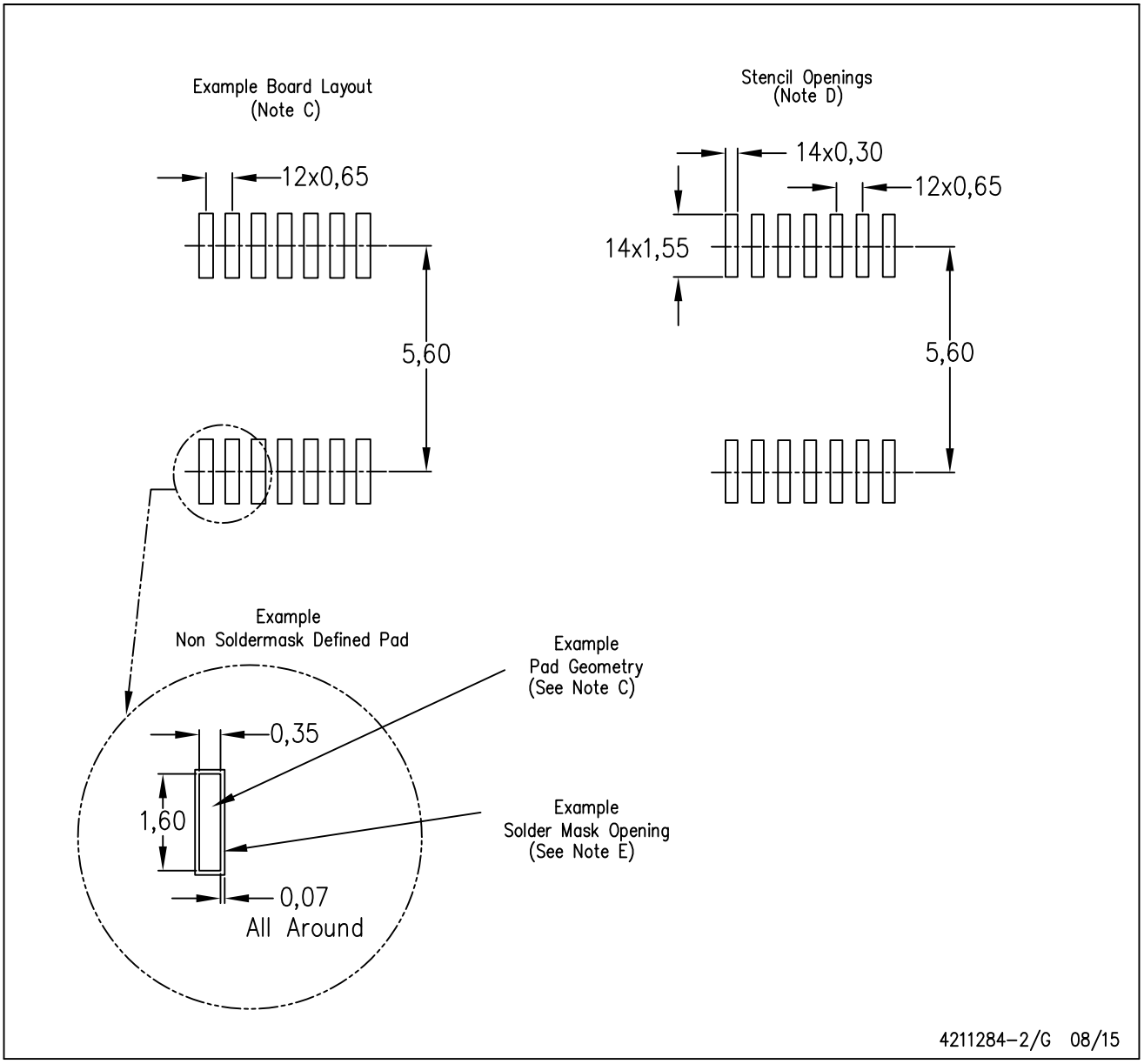
PW (R–PDSO–G14) PLASTIC SMALL OUTLINE



4040064–3/G 02/11

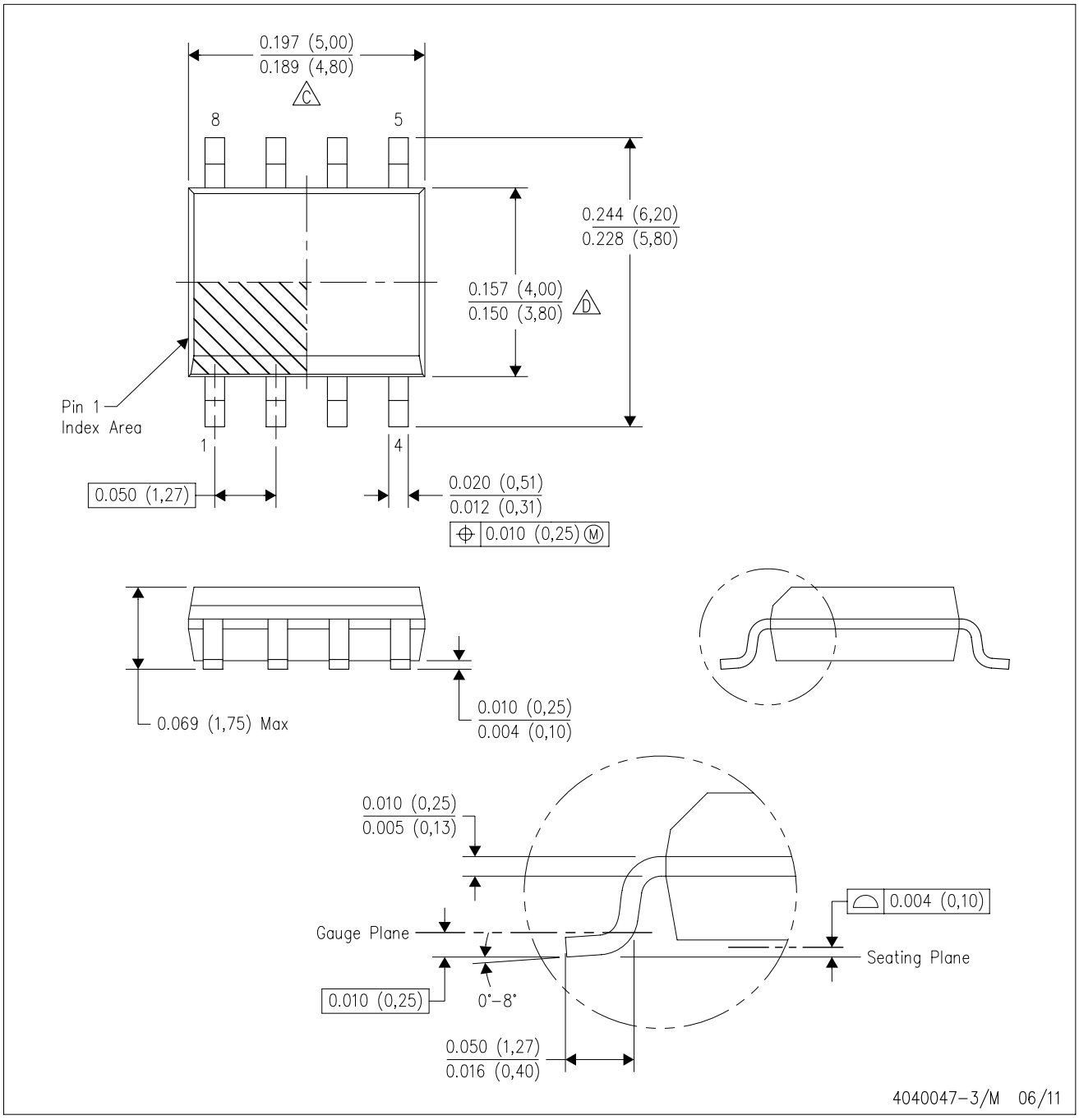
NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
E. Falls within JEDEC MO–153

PW (R–PDSO–G14) PLASTIC SMALL OUTLINE



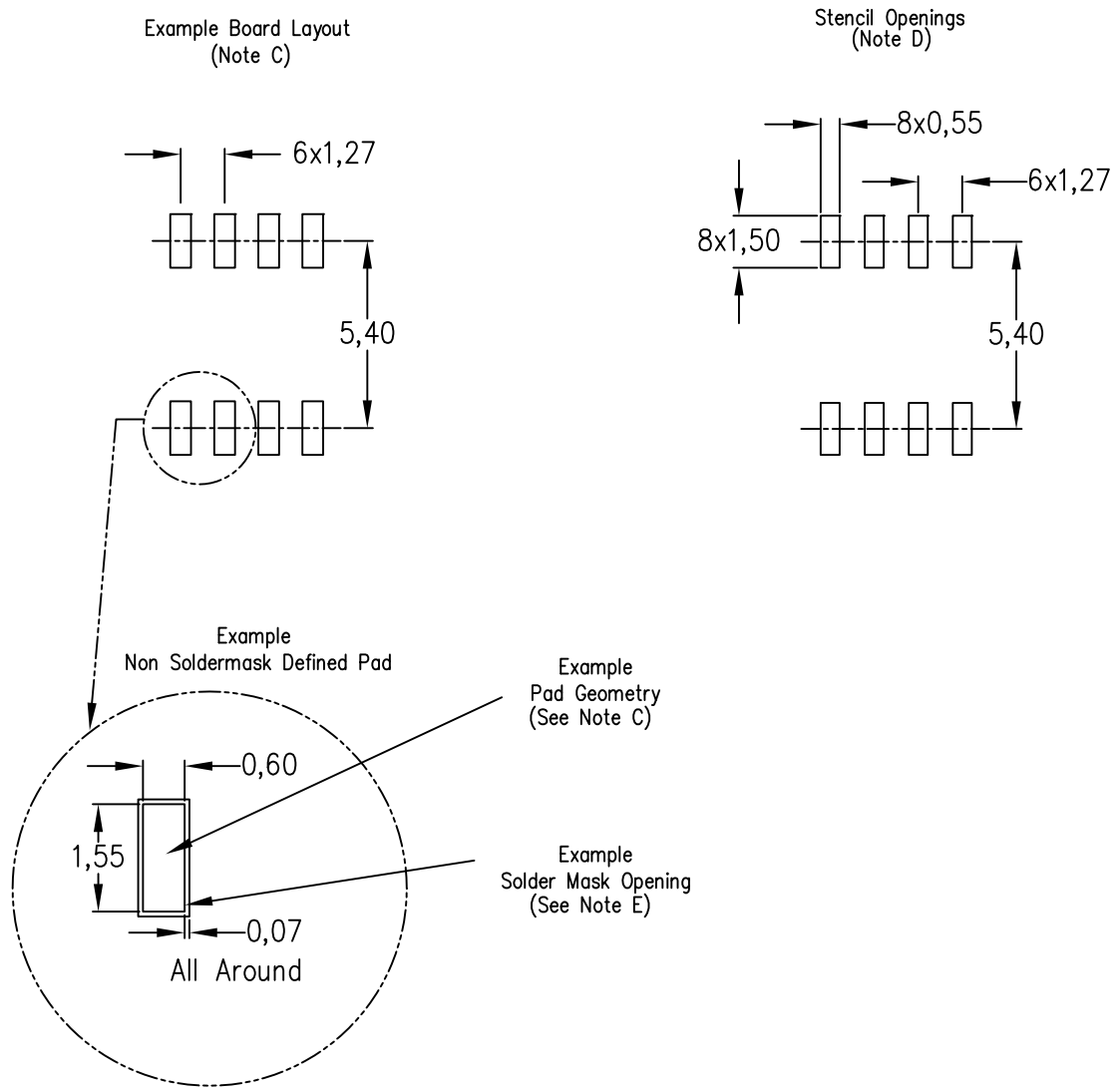
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

D (R–PDSO–G8) PLASTIC SMALL OUTLINE



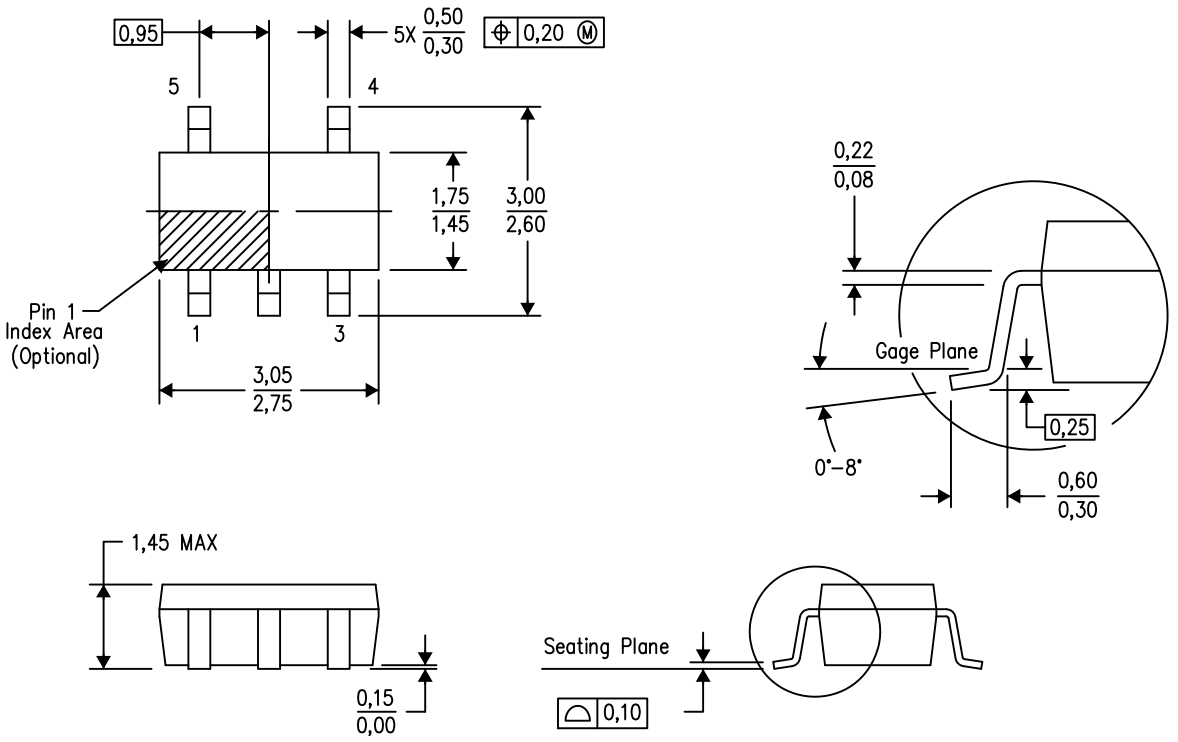
NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AA.

D (R–PDSO–G8) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

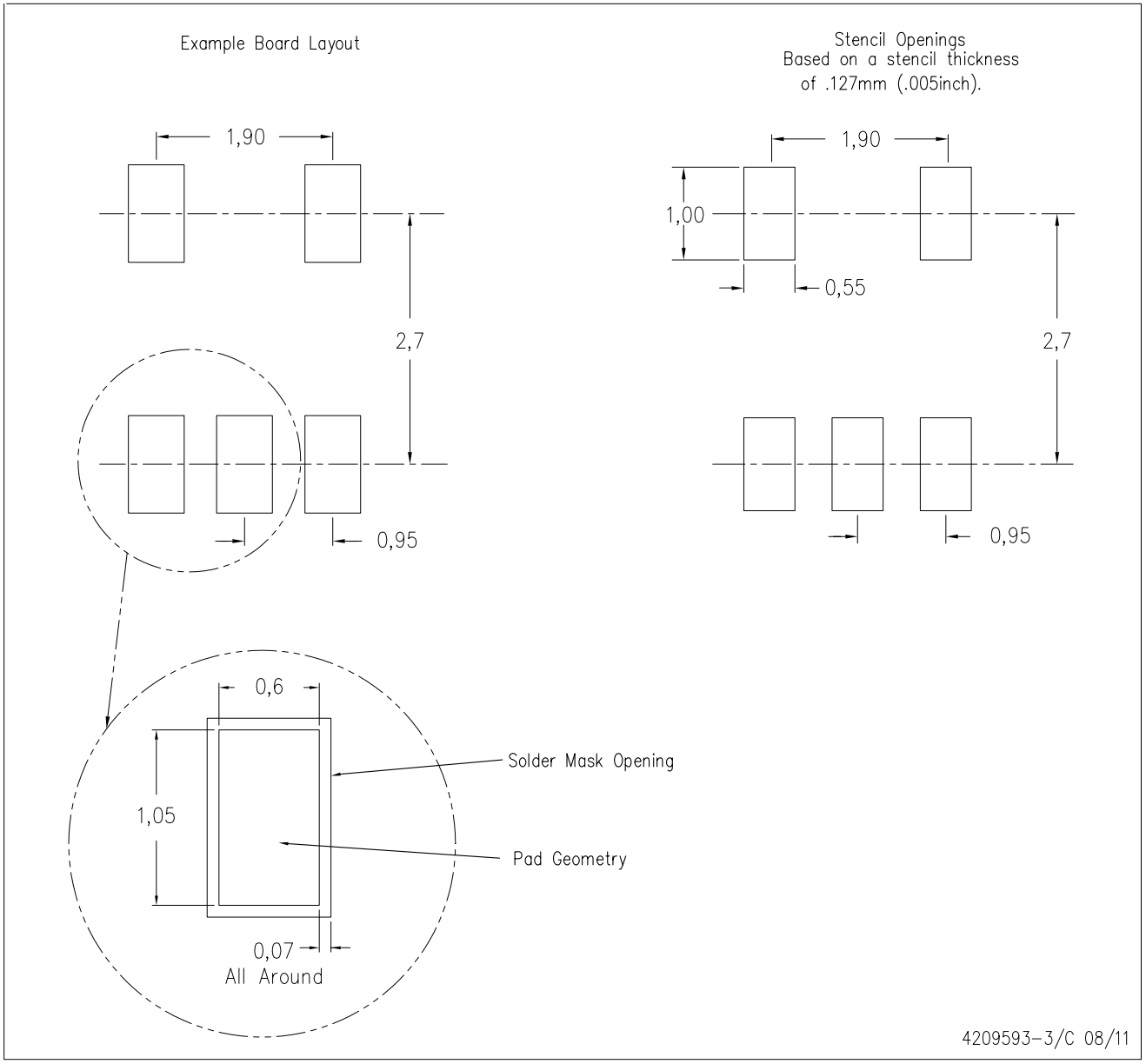
DBV (R–PDSO–G5) PLASTIC SMALL–OUTLINE PACKAGE



4073253–4/N 12/14

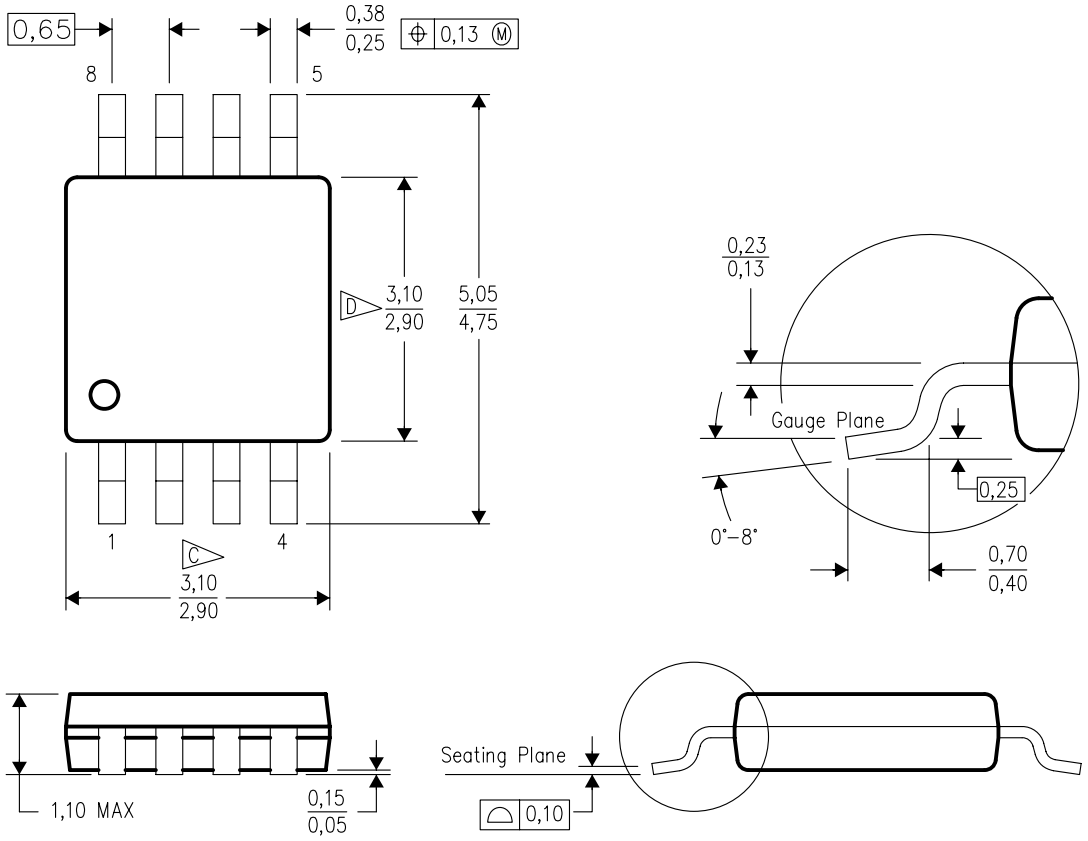
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
D. Falls within JEDEC MO–178 Variation AA.

DBV (R–PDSO–G5) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
D. Publication IPC–7351 is recommended for alternate designs.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.

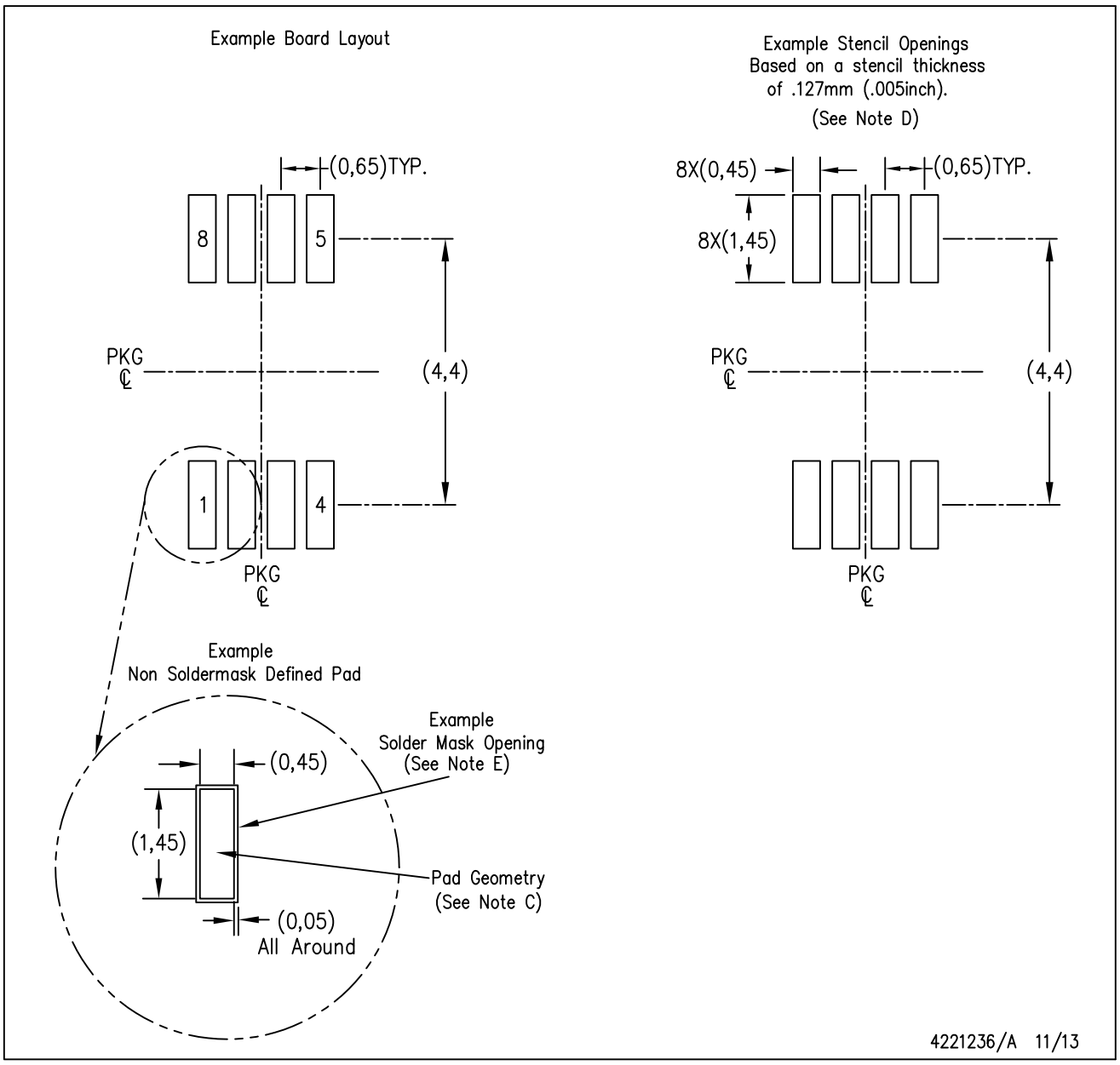
DGK (S–PDSO–G8) PLASTIC SMALL–OUTLINE PACKAGE



4073329/E 05/06

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per end.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.50 per side.
E. Falls within JEDEC MO–187 variation AA, except interlead flash.

DGK (S–PDSO–G8) PLASTIC SMALL OUTLINE PACKAGE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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