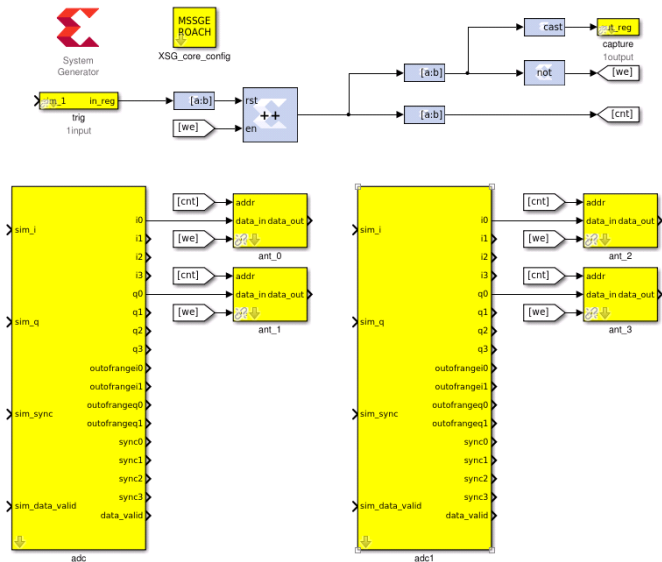


Creating a simple ADC capture on a ROACH

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Overview



Getting started...



System
Generator



XSG_core_config

Block Parameters: XSG core config

xsg core config (mask) (link)

The XSG Core Config block is used to configure the System Generator design for the casper_xps toolflow. Settings here are used to configure the Xilinx System Generator block parameters automatically, and control toolflow script execution. It needs to be at the top level of all designs being compiled with the casper_xps toolflow.

Parameters

Hardware Platform: **ROACH:sx95t**

User IP Clock Source: **adc0_clk**

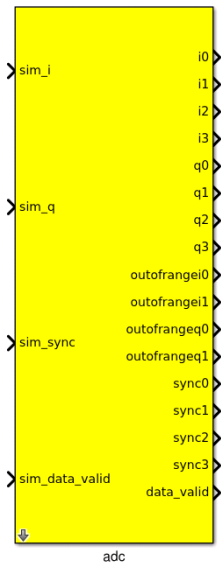
User IP Clock Rate (MHz): **200**

Sample Period: **1**

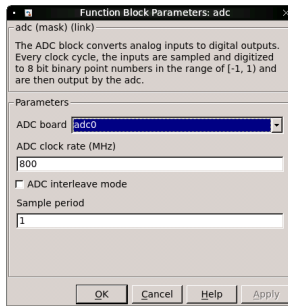
Synthesis Tool: **XST**

OK Cancel Help Apply

The iADC

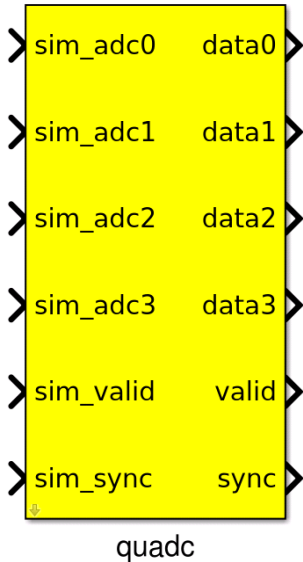


The iADC sample rate is four times the FPGA sampling rate.

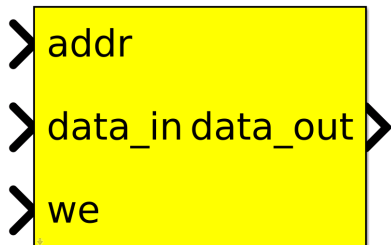


The QuadADC

- ADC card that can take up to four signal inputs.
- The QuadADC sampling rate is the same as the FPGA.



Shared BRAM



Shared BRAM

Function Block Parameters: ant 0

Subsystem (mask)

Parameters

Output Data Type: **Unsigned**

Address width: 11

Data Width: 32

☐ Register Primitive Output

☐ Register Core Output

Optimization: **Minimum_Area**

Data Binary Point: 0

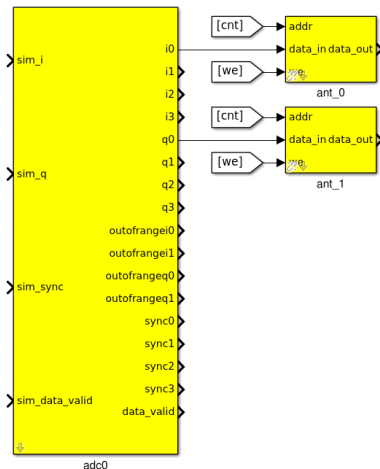
Initial values (simulation only): [0:2^10-1]

Sample rate: 1

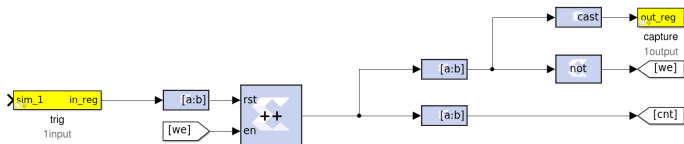
OK Cancel Help Apply

Putting it together...

- This reads out one sample per channel every FPGA clock cycle and stores it in BRAM.
- Data can be read out of the BRAM using KATCP in Python with the `FpgaClient.read()` function.
- Integers are stored in big-endian format and are read out as a sequence of hex strings.



Capturing a sample



- This system generates addresses to store each sample in BRAM and stops writing when all samples are read.
- A sample is captured by successively writing 1 and then 0 to the trig software register.
- The counter has one more bit than the BRAM address so that the counter's MSB acts as a write-enable.

The full design

