Performance Evaluation of a Novel Ternary CNTFET SRAM Cell

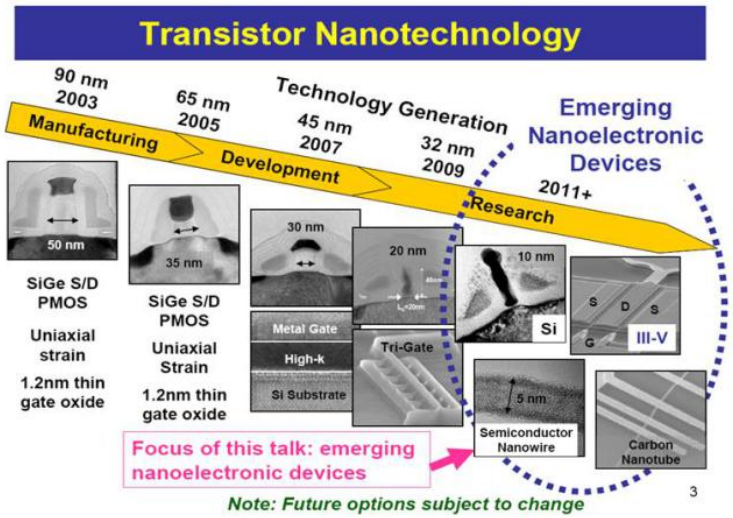
Pramod Srinivasan

BITS-Pilani

29 January 2015
Shillong

Overview

Emerging Nanotechnologies - Post-CMOS Alternatives



Critical Challenges in nanoscale

- Variations in I-V characteristics
- Reduced gate control
- Larger process variations

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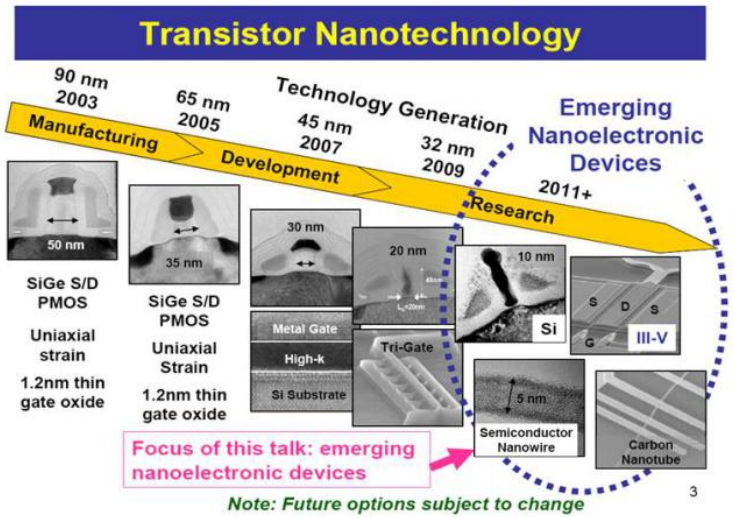

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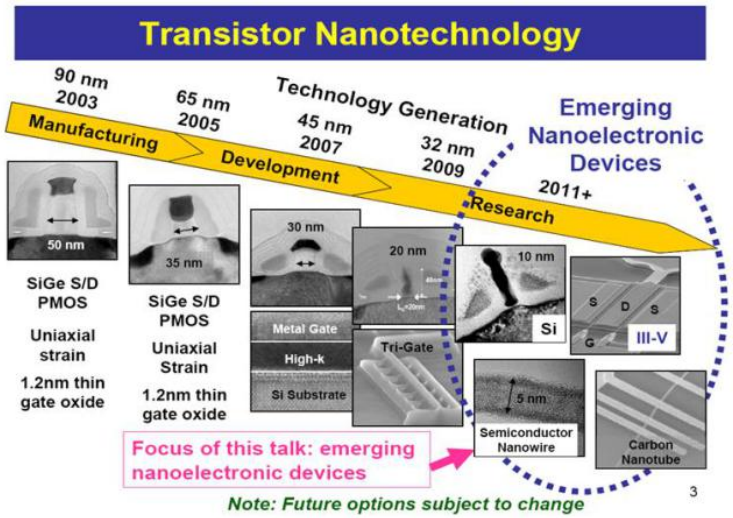

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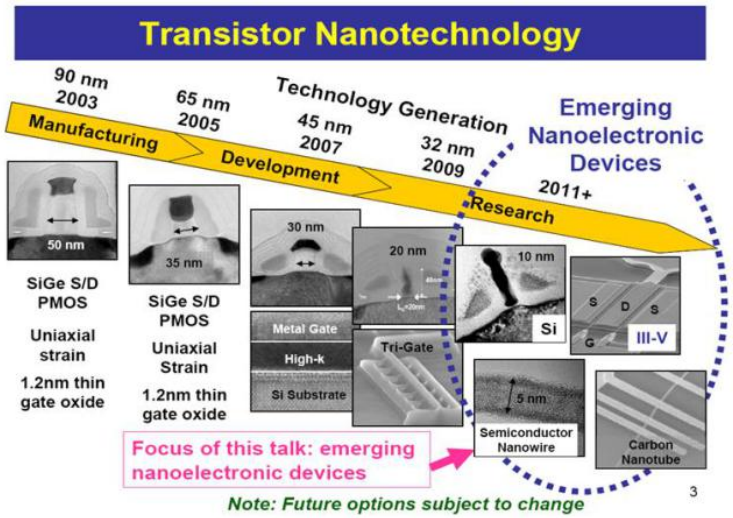

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CNTFET as the best alternative to CMOS

- Faster switching speeds and low power
- Bistability gives well defined on and off states
- P and N type CNTFETs of same size having same mobility
- Ballistic Nature suitable for high frequency operations -**100GHz**

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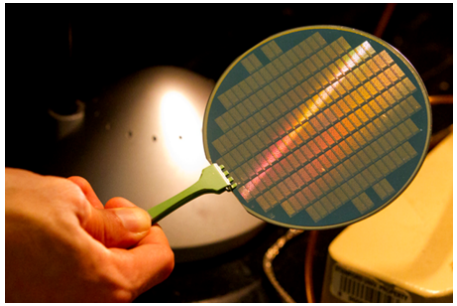
Heralding the Post-CMOS Era

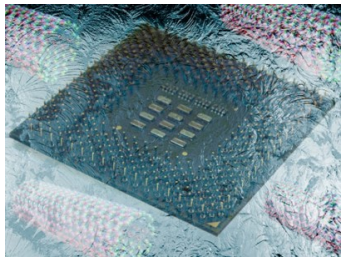
BBC Science,September 2013

First computer made of carbon nanotubes is unveiled at Stanford



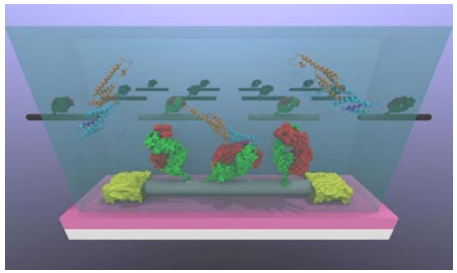
IEEE Spectrum,Jan 2014

Nanotubes Could Solve Overheating Problem for Next-Gen Computer Chips



PhysicsWorld,Mar 2013

Nanotube transistors detect cancer biomarkers



Ternary Logic with CNTFETs

- Reduces chip area
- Reduces complexity of interconnect with enhancing their information content
- Attains simplicity and energy efficiency in designing of digital circuits

Best way of designing is **multiple-threshold method** which can be achieved by utilizing **different diameters of Nanotubes**

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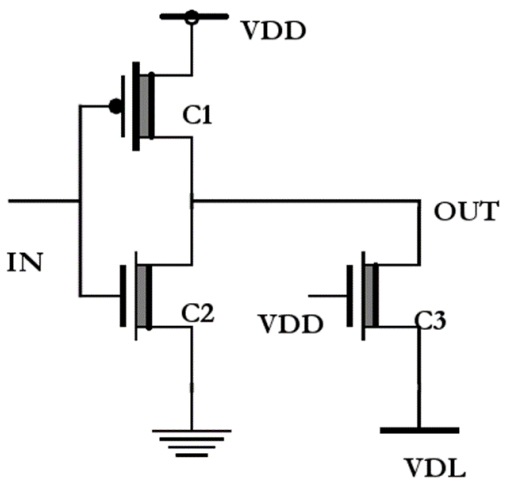
Standard Ternary Inverter

Key Statement

Improved performance of the inverter of a memory cell leads to **increased performance** of the whole ternary system



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- Multiple power supplies
- VDD = 0.9 V and VDD = 0.45 V
- Transistor C3 is always ON
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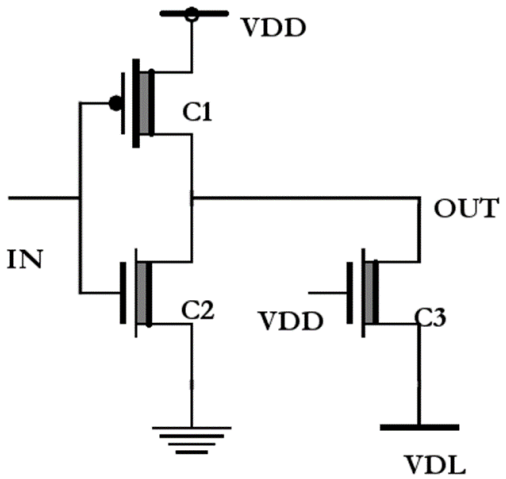

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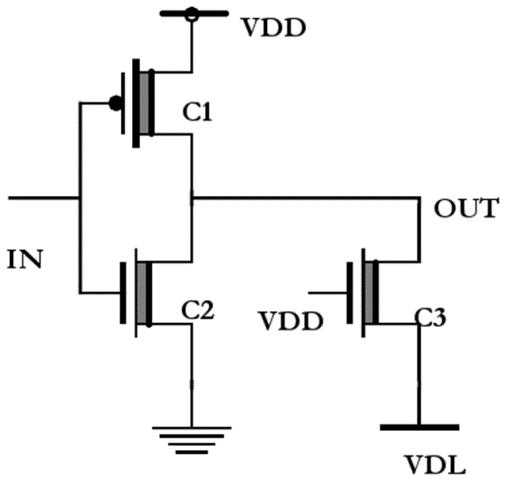

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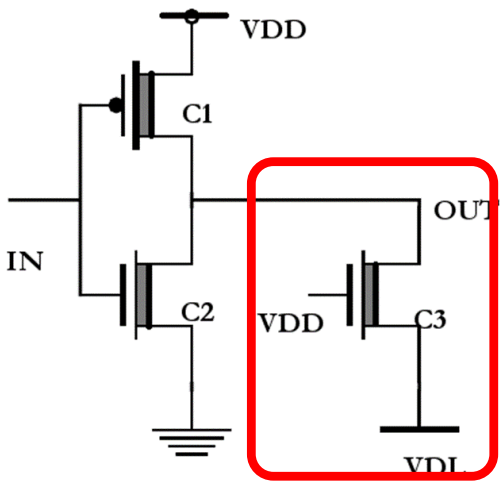

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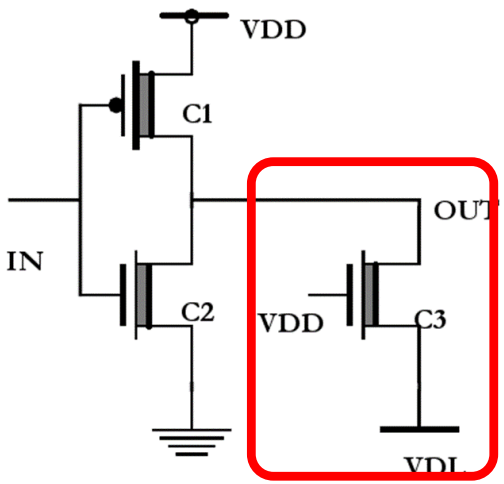

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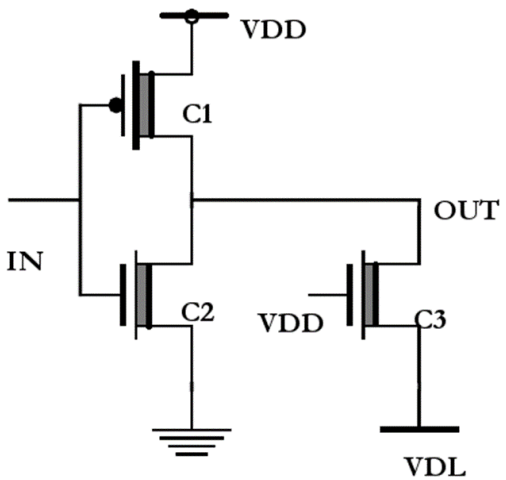

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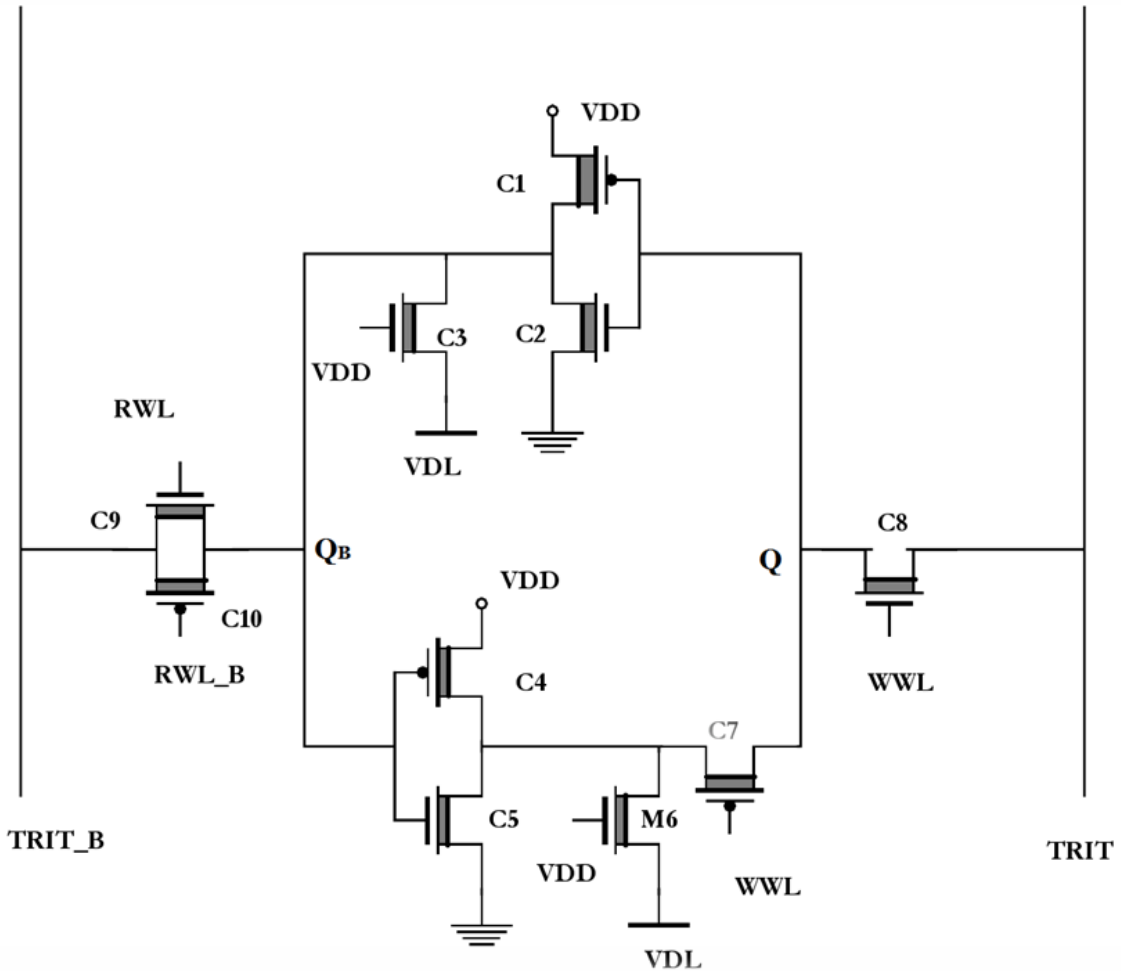

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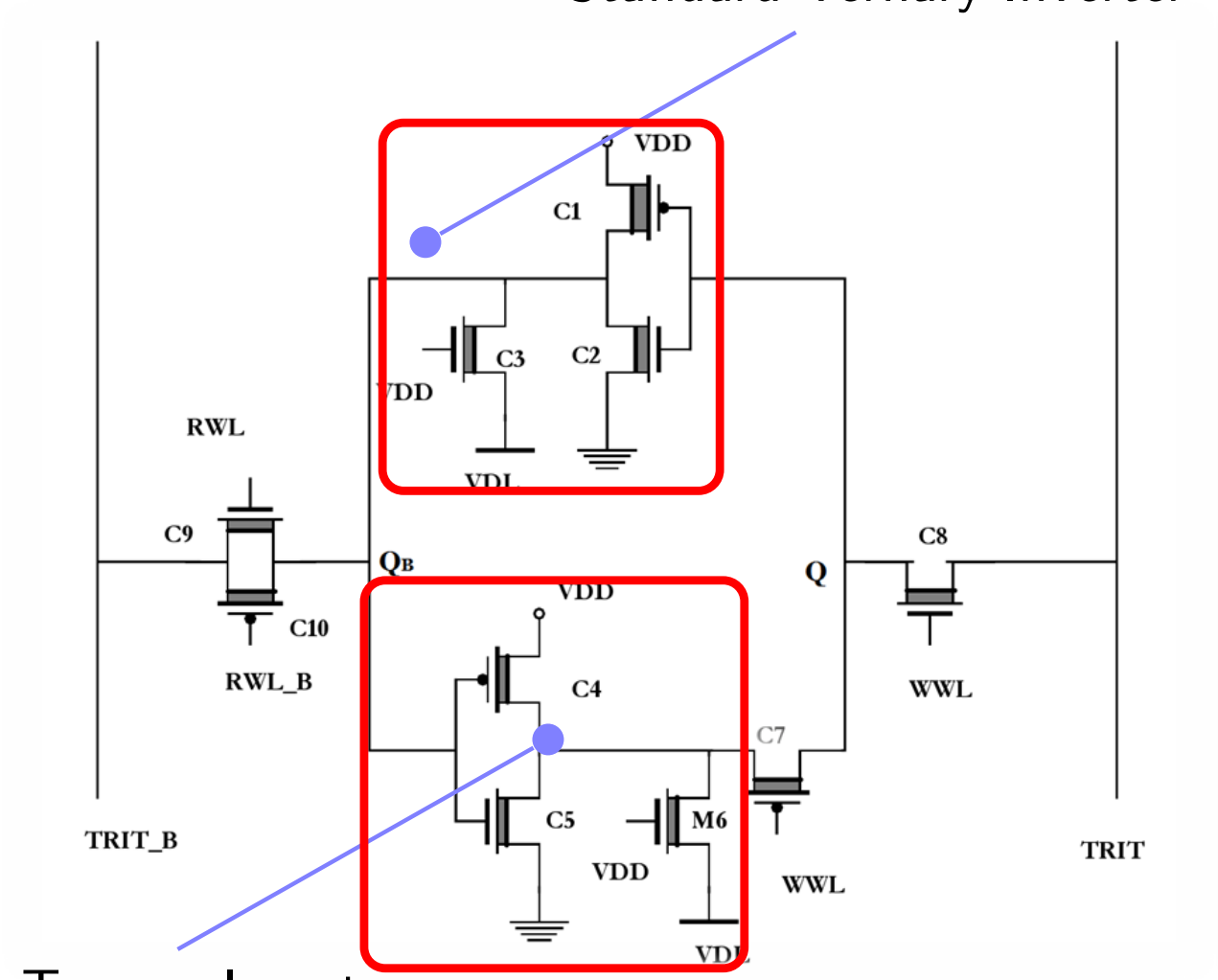

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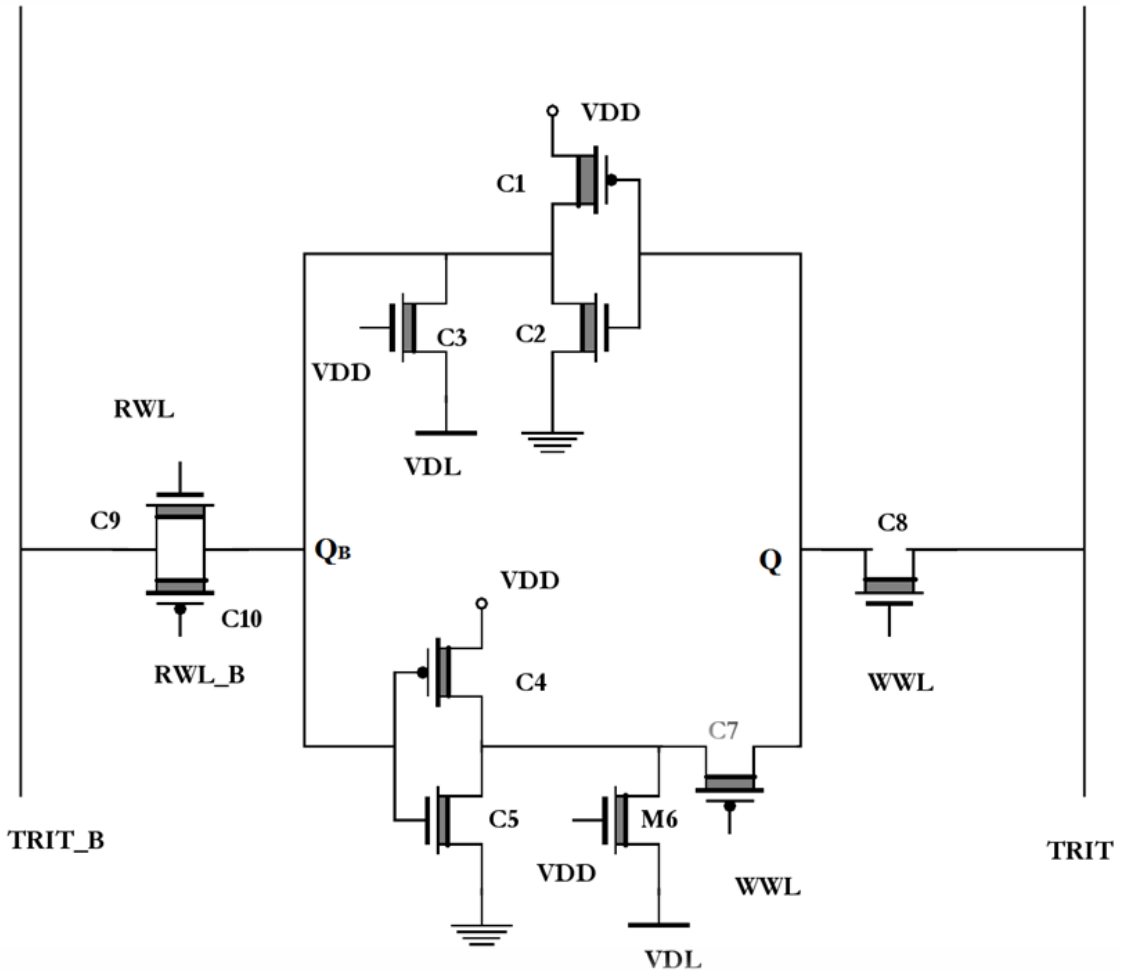

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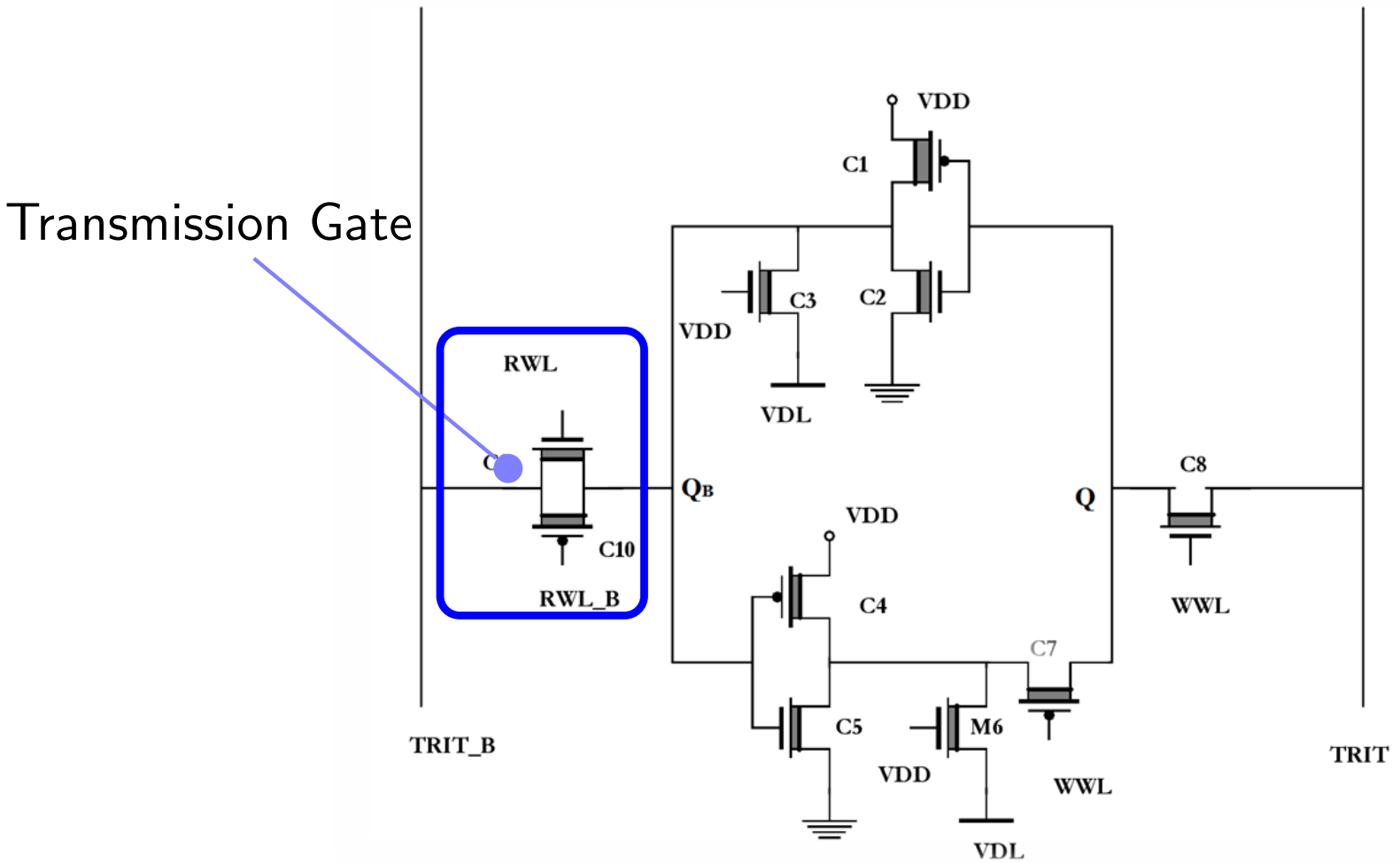

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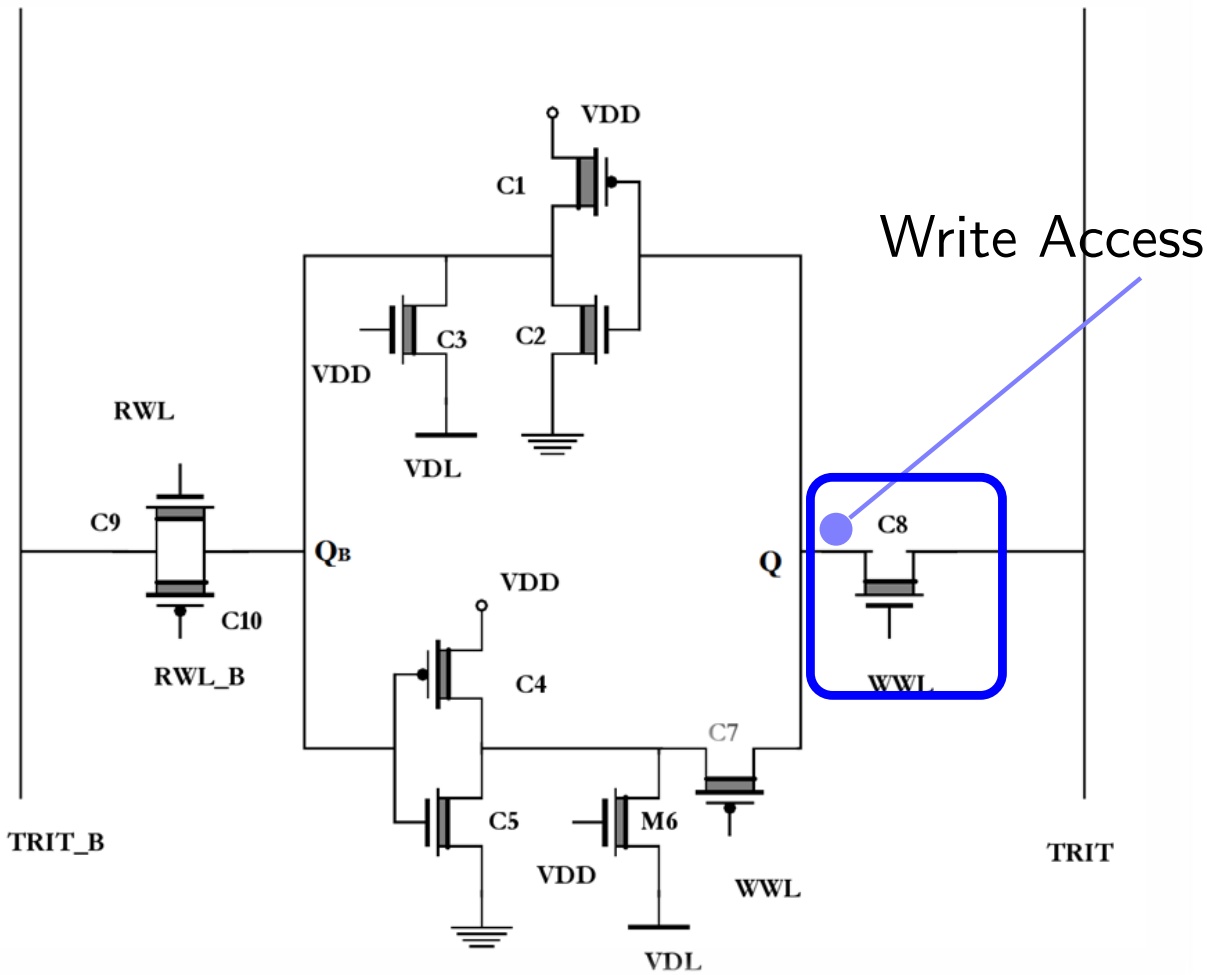

Write Access Transistor

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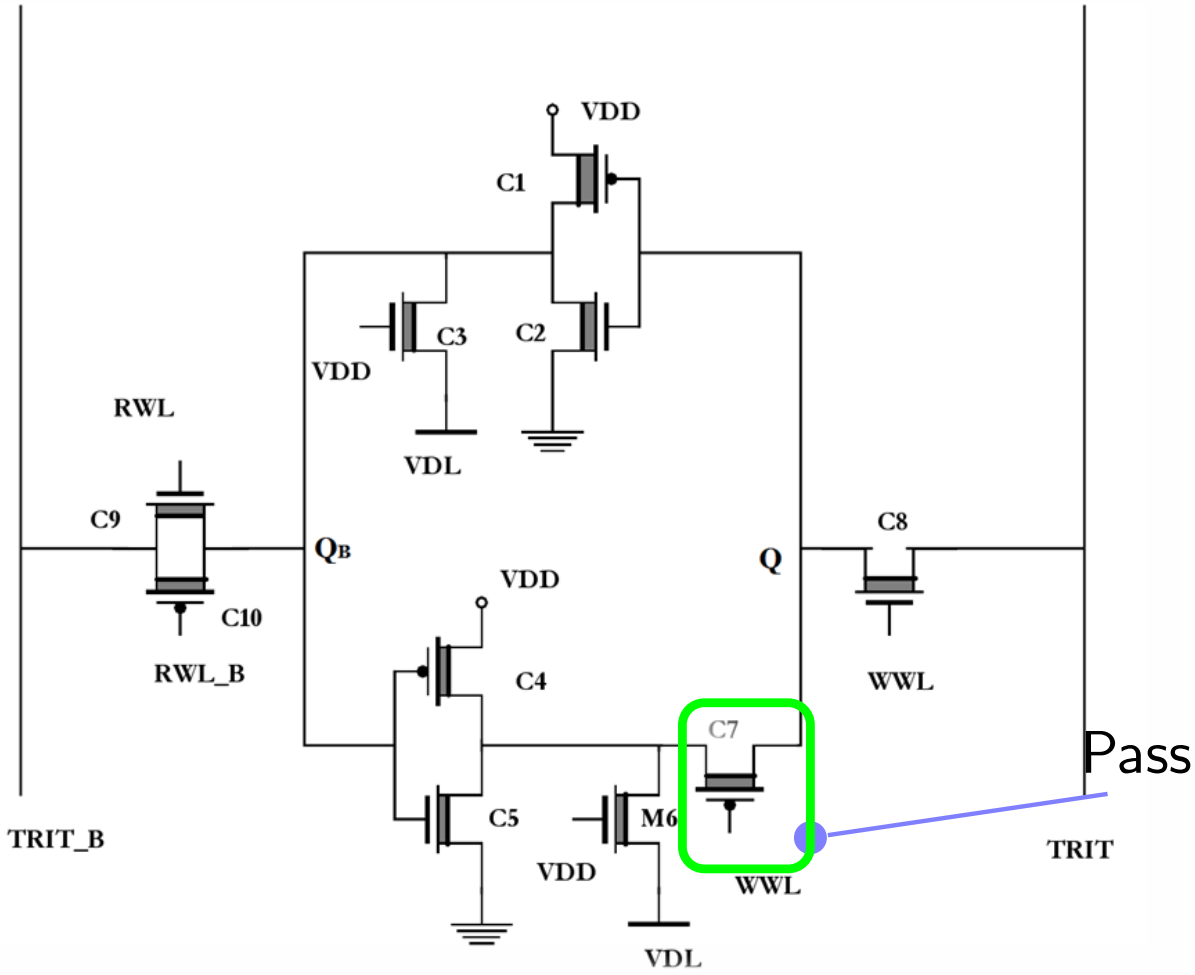
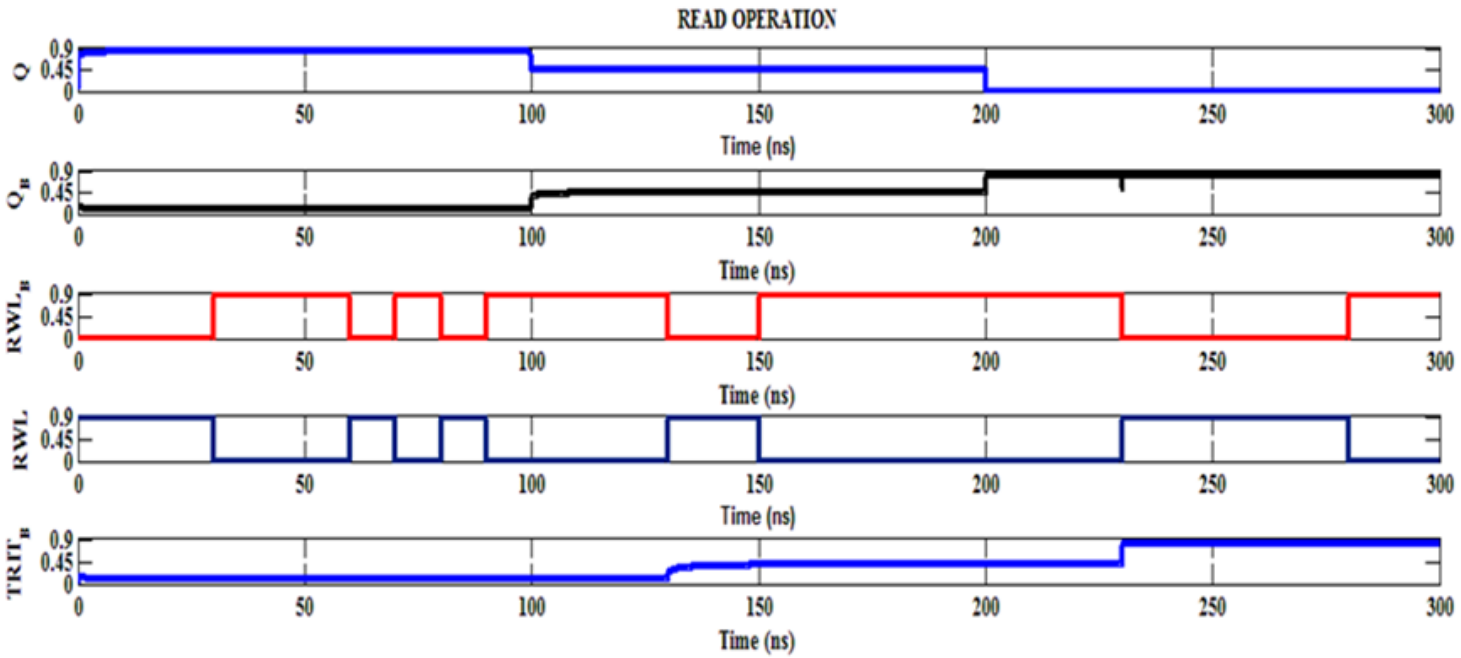


Simulation Environment Setup

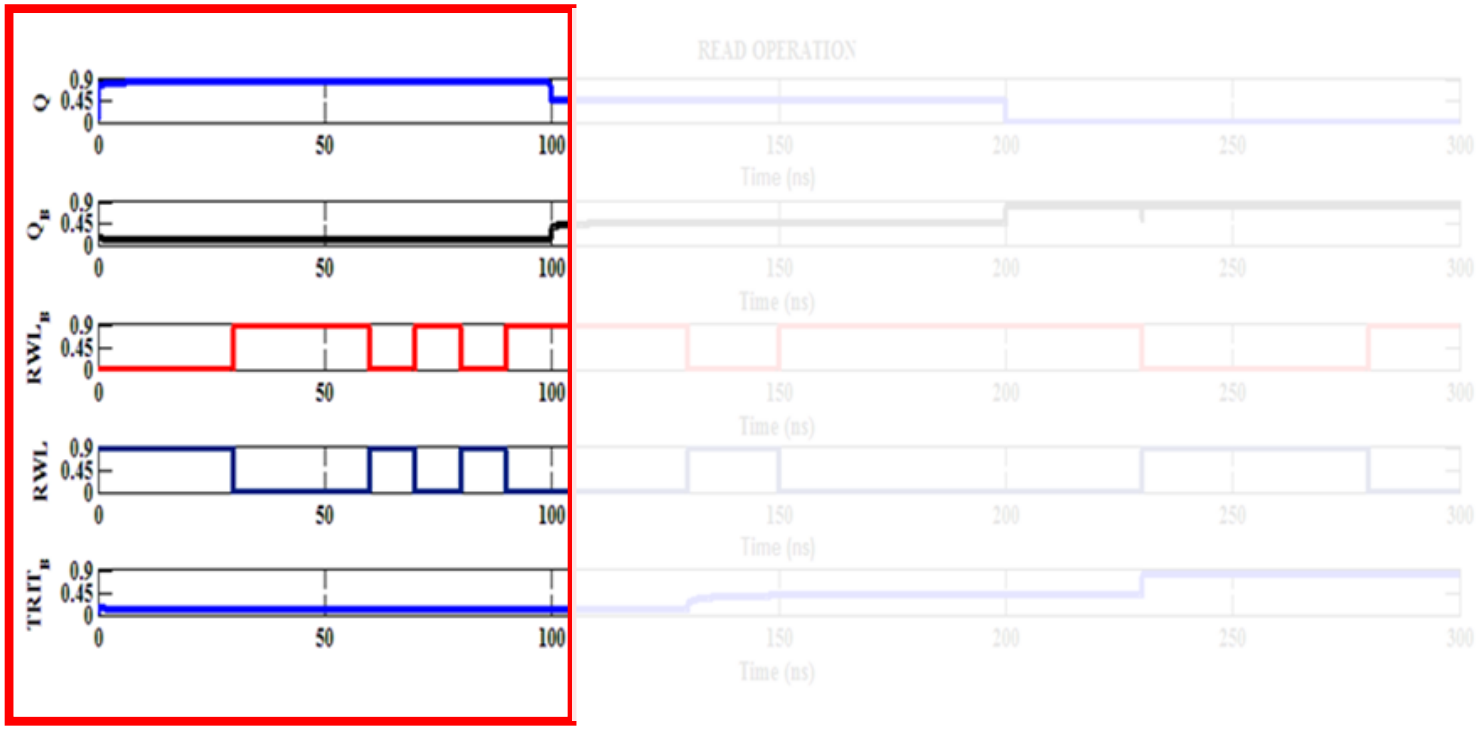
- Evaluation is done using Synopsis's HSPICE simulator with 32nm Stanford CNTFET model which includes a number of practical non idealities
- All the designs are simulated at room temperature, 250 MHz operating frequency, 0.9V power supply voltage with output load capacitor of 2.1fF

Read and Write Operations



Figur: Read Transient Simulation Result

Read and Write Operations



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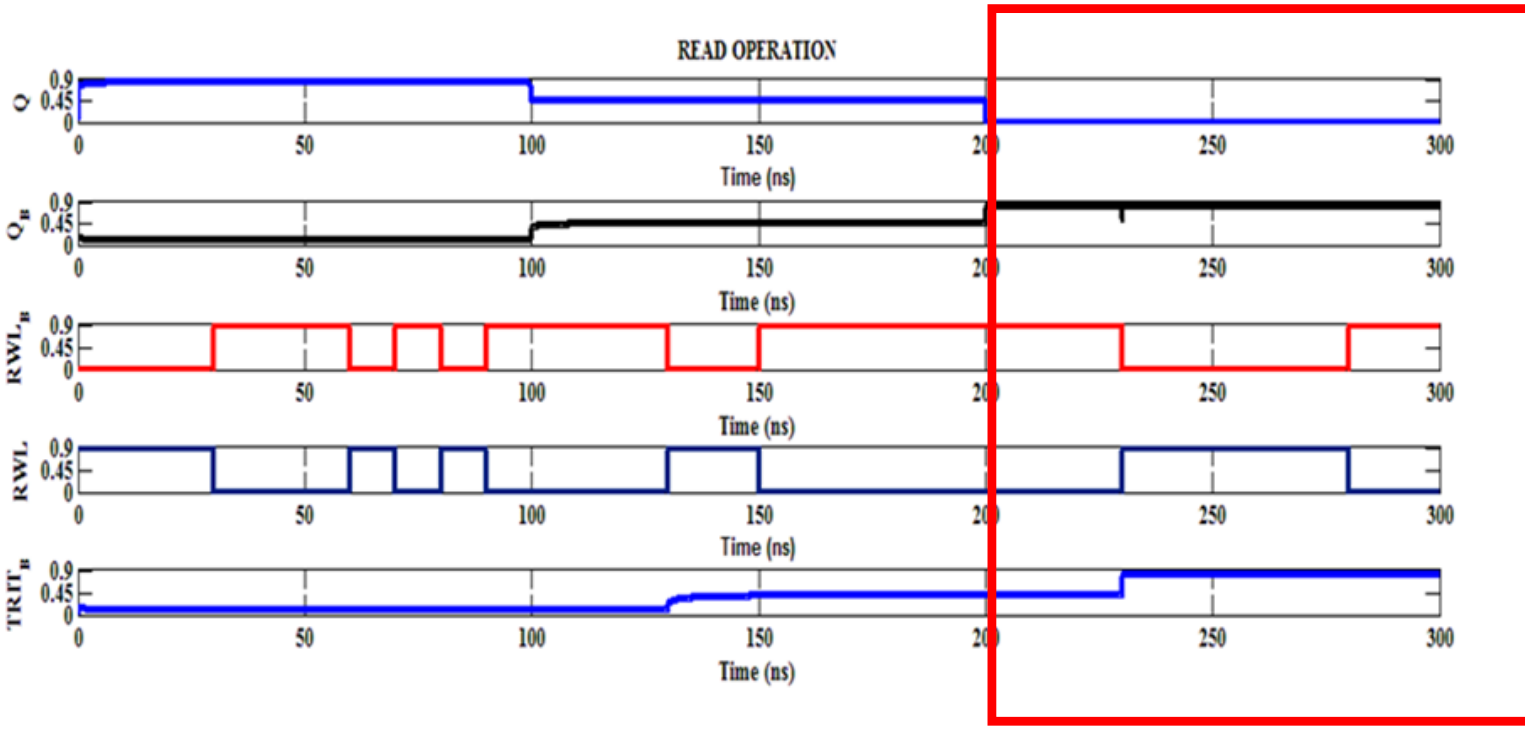

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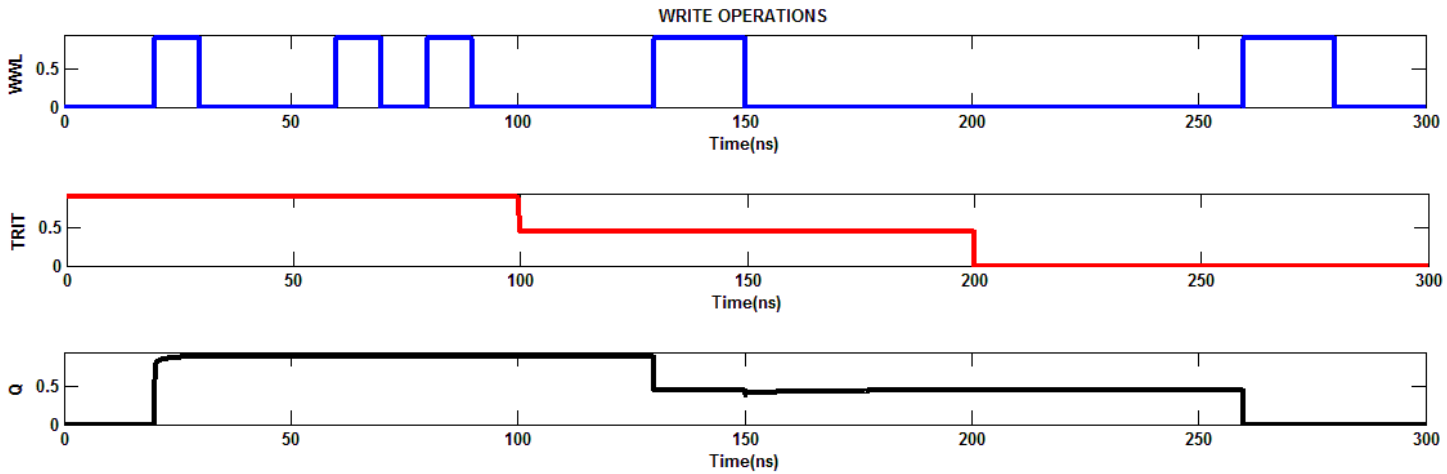

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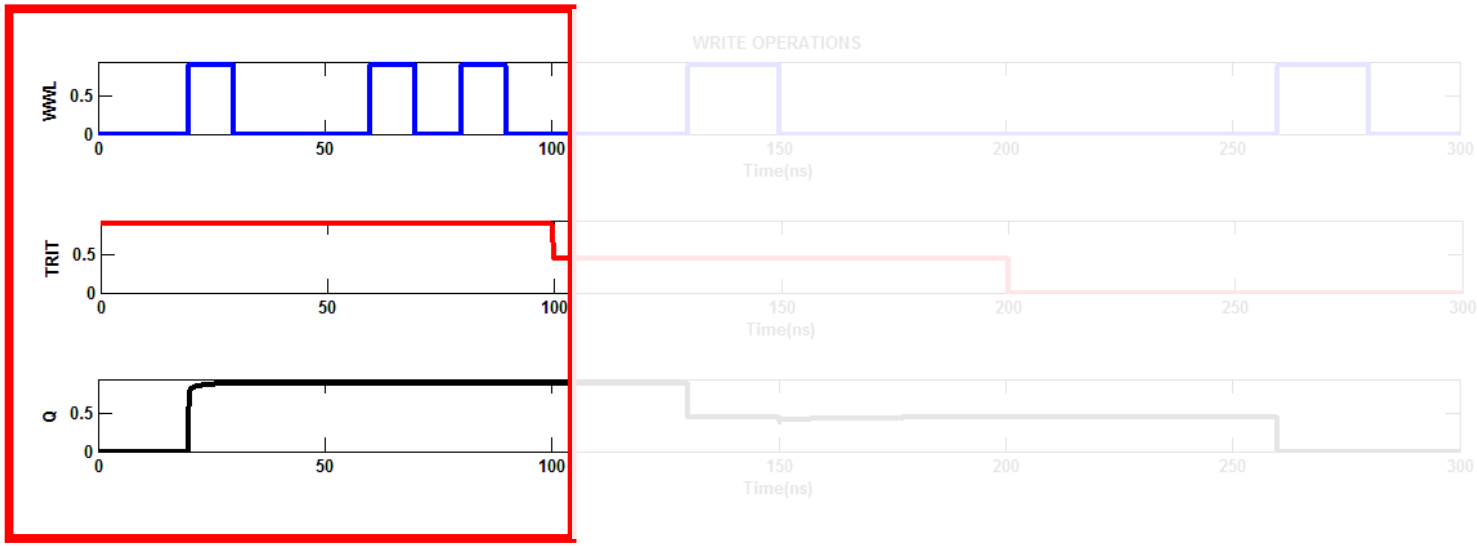

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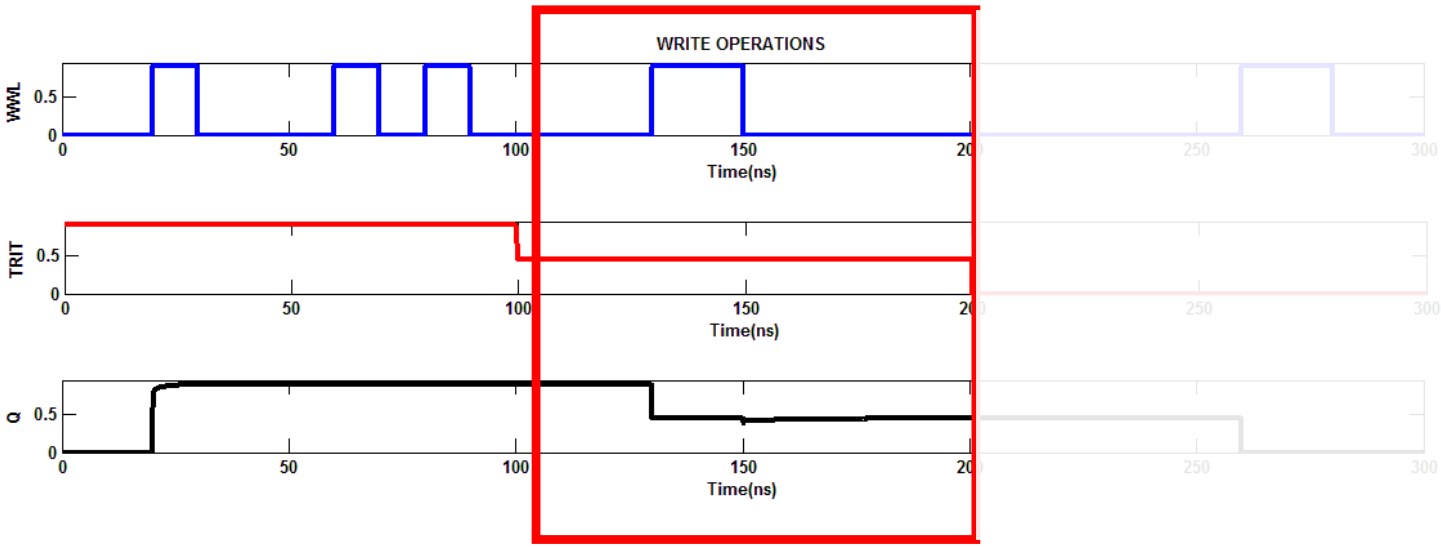

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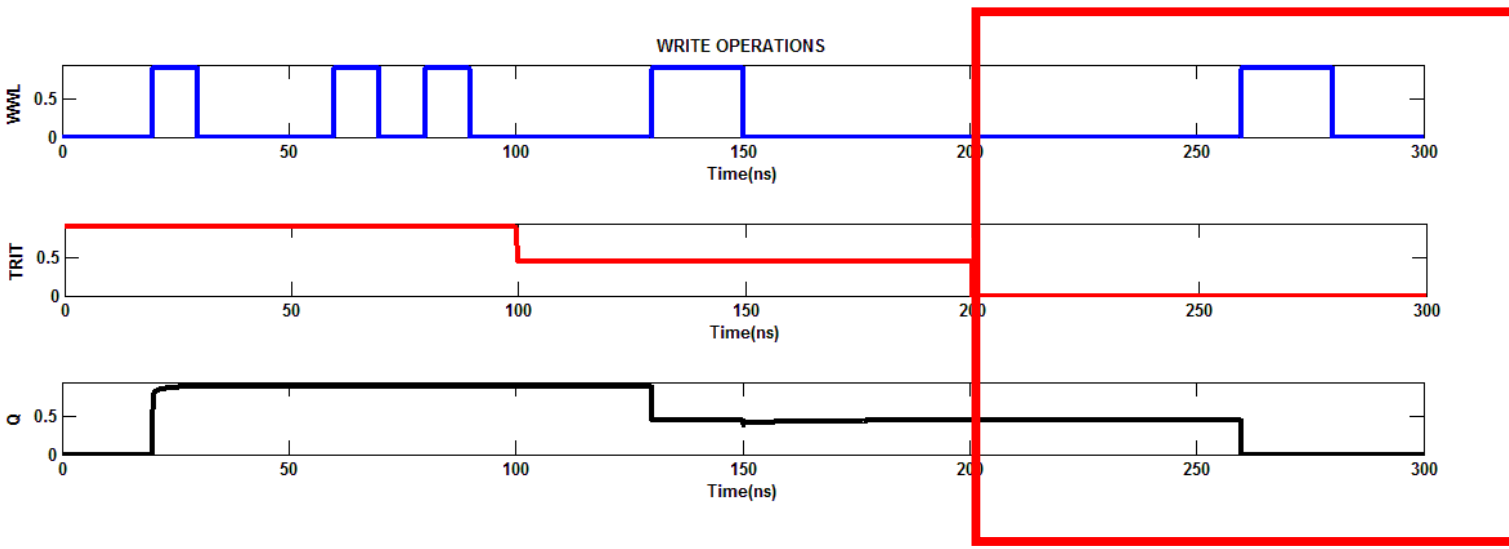

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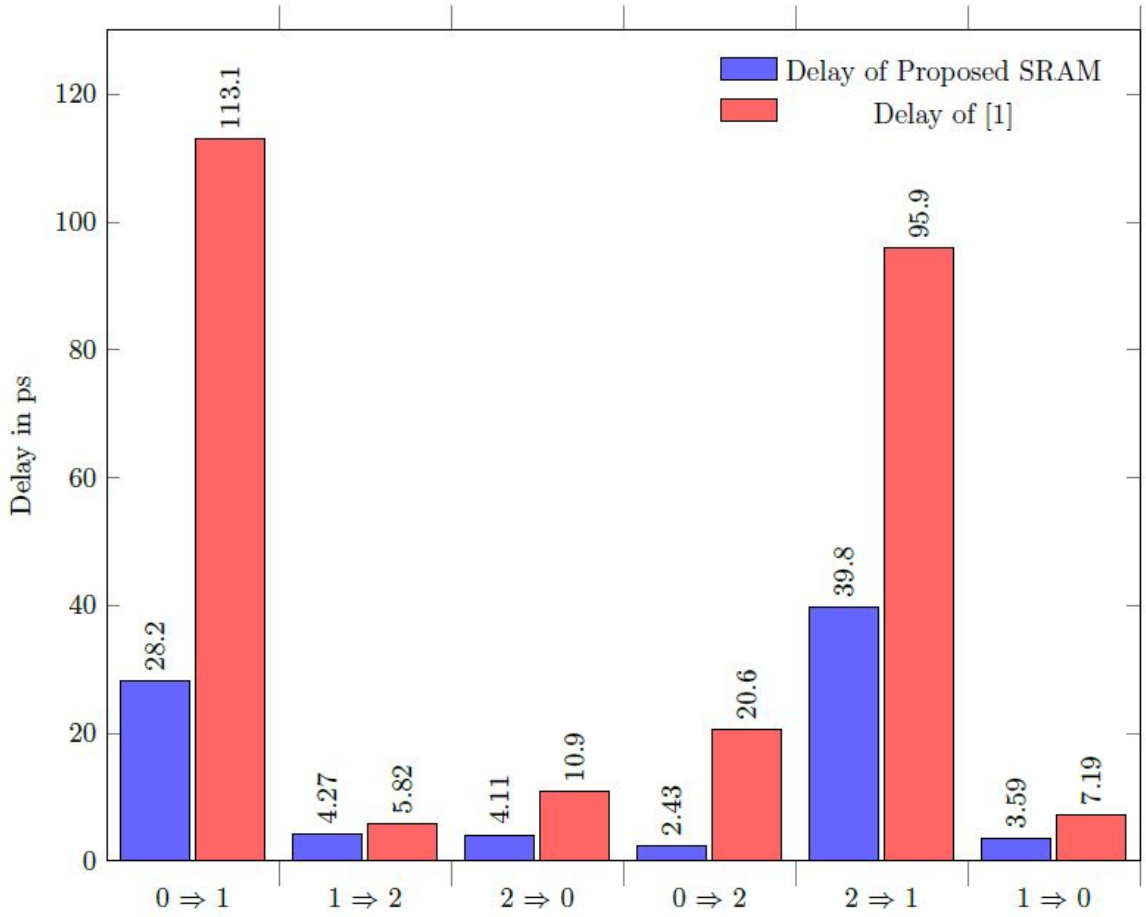
Simulation Results(contd)



Figur: Comparison of Write Simulation Results

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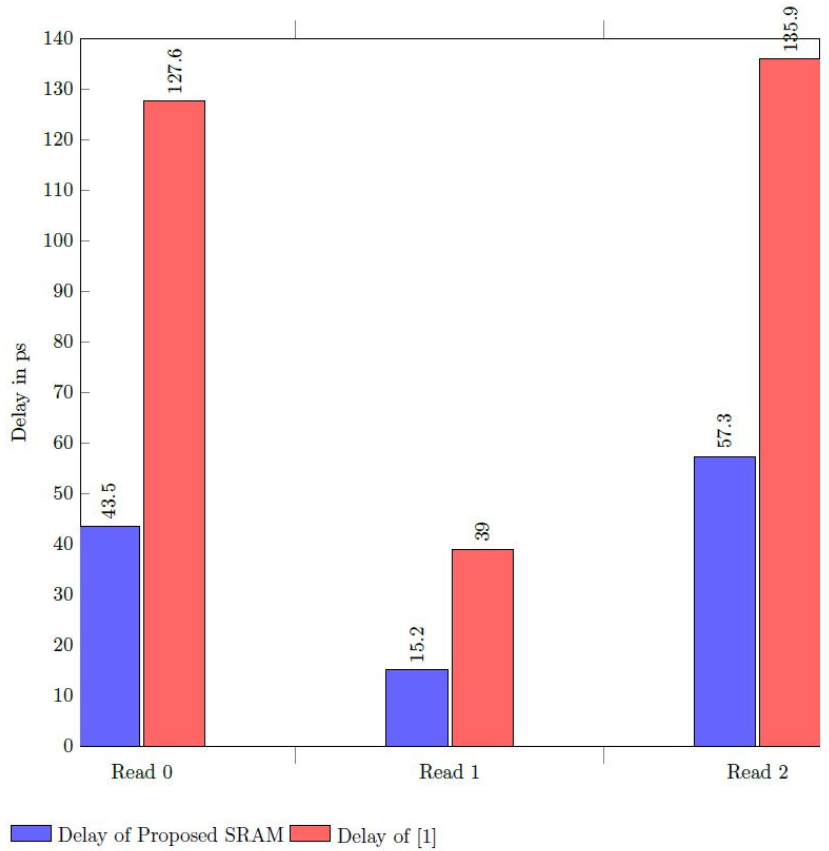

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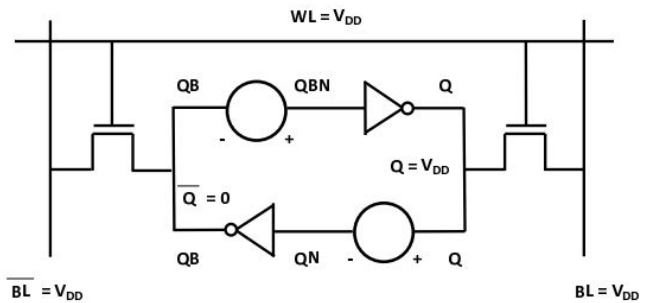
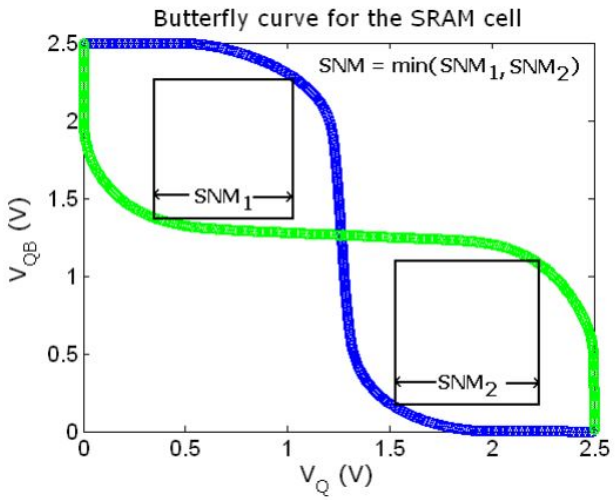
Static Noise Margin

- CNT Diameter has strongest impact.
- Monte Carlo simulations to assess the process variations





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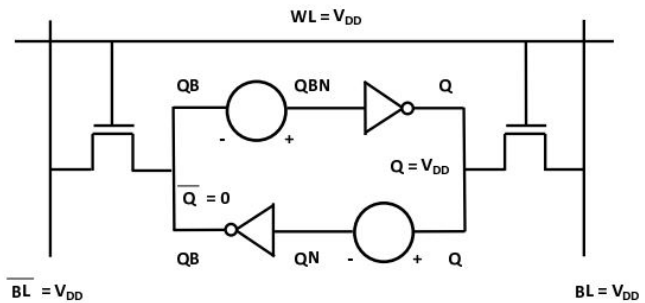

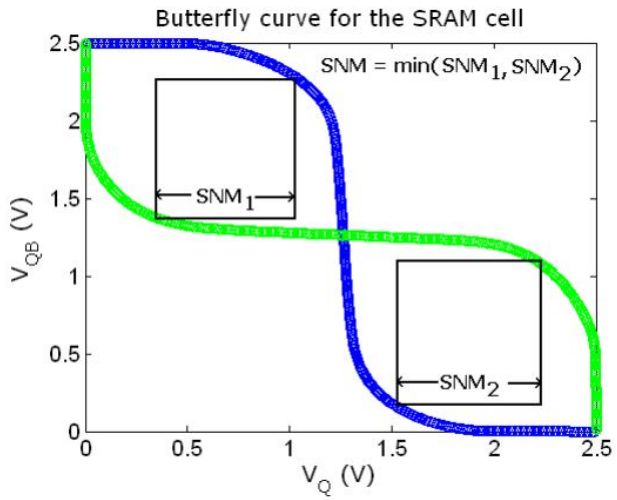

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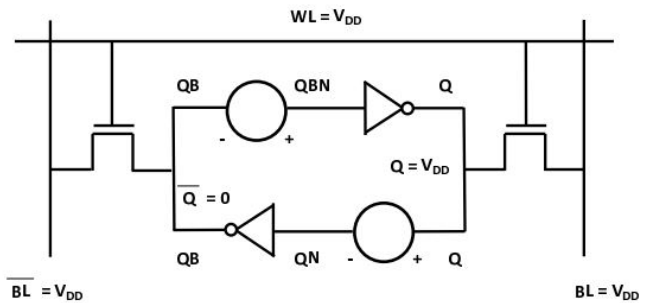

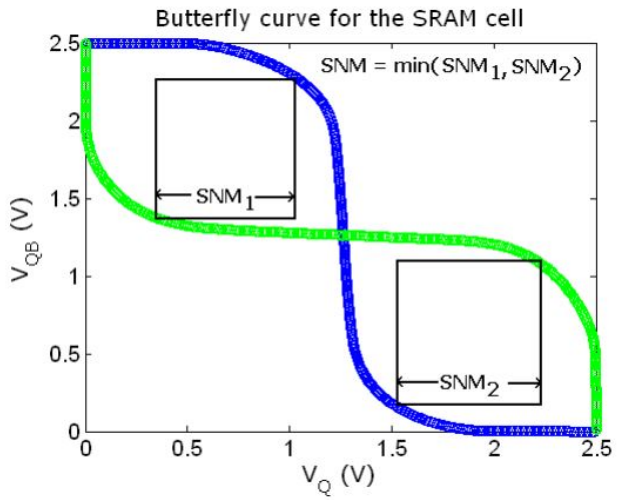

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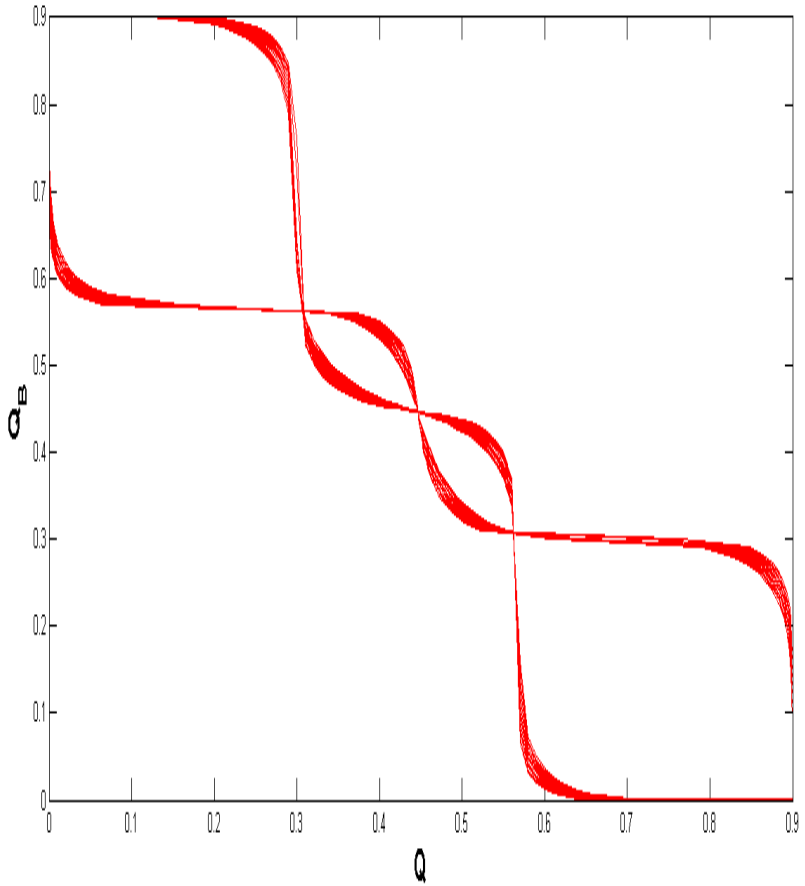

Figur: Static Noise Margin Butterfly Curve under various process variations

Performance Evaluation Parameters

- Cell design using multi-threshold method leveraging the unique characteristics of the CNTFET.
- Proposed memory cell design has one of the lowest number of transistors
- HSPICE simulations have demonstrated the correct functionality with **less area** and **high speed**.
- The SRAM cell outperforms the design proposed in [1] in write and read operations

Thank you

References

1. Lin S., Kim Y.B., Lombardi F. : 'Design of a CNTFET based SRAM cell by dual-chirality selection',*IEEE Trans. Nanotechnology*, 2010, 9,(1), pp. 30-37.
2. K. You, K. Nepal, Design of a ternary static memory cell using carbon nanotube-based transistors, *Published in Micro & Nano Letters*; 4th April 2011.