## Introduction

## Thesis Contribution

In this thesis, our aim is to provide an analysis of the available IP protection mechanisms, and to contribute with new solutions exploiting PUFs properties with SoPC and FPGA technologies.

Some of the work done during the thesis development has been published in academic conferences. In the following we list the papers developed during the thesis work:

- Paper IEJS
- KES
- Transaction IEEE

## Manuscript Remainder