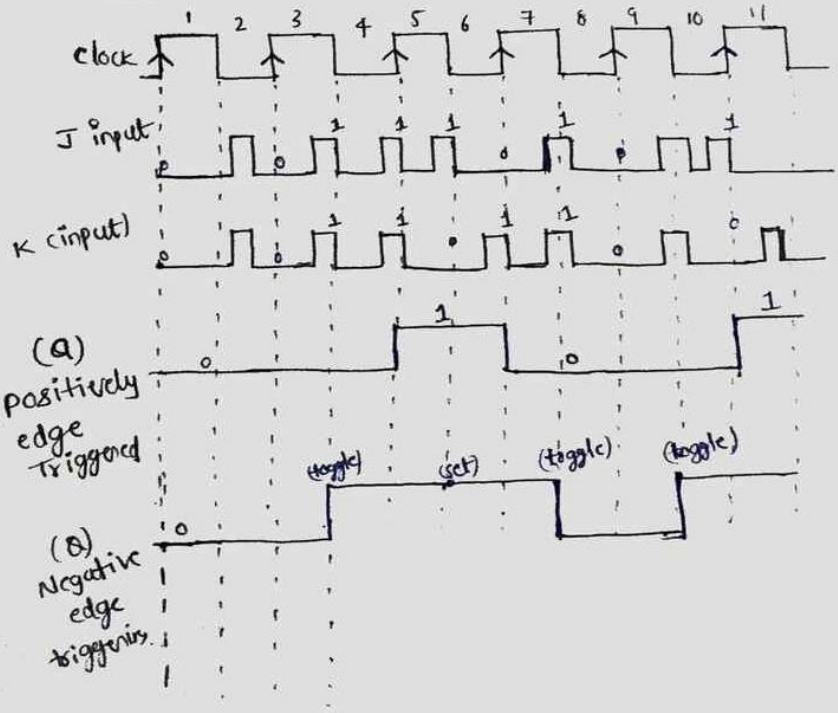
1)

Solution

Step 1: Truth table of JK FF

J	K	Q
0	0	Q (hold)
0	1	0 (reset)
1	0	1 (set)
1	1	$\bar{Q}$ (toggling)

Step 2:



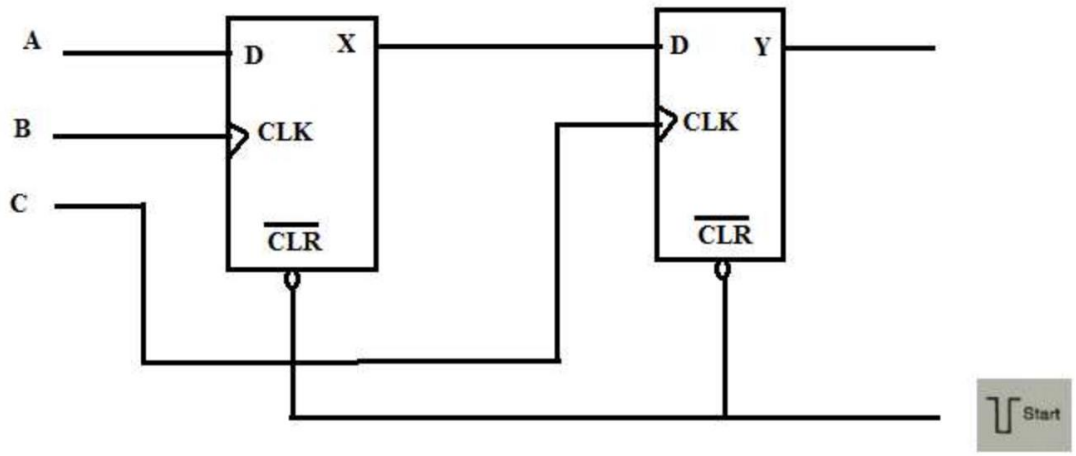
2)

a)after making A=1 , b=1 and making c=1 we'll get Y=1 or 100110111

b)To Initialize(reset) the flipflops to zero START pulse is needed

c.

USING D FLIPFLOP



3)

a)

⑨ The given circuit is (mod 8) Counter.

Input start by clk pulse.

Initial output state is 000 => binary "0"

As clk pulses negative edge arrives, the output state increments by 1 ~~and~~ untill binary "7" or 111. and starts again from 000 i.e, binary "0"

→ So after 13 clk pulses the output state is given as $13 \% 8 = 5$ (101).

The count is 5.

→ After 99 clocks pulses the count is 99%8

i.e, 8)99(12
8
19
16
(3) → answer

=> 99%8 = 3. => Count = 3 (011)

→ After 256 pulses the count is 256%8 i.e,

8)256(32
250
(0) → answ

the count is '0' (000)

---

⑥ The output stats at 100 i.e, binary value "4"

The output after 13 pulses is (13-4)%8

=> 9%8 = 1 (001)

b)

⑥ The output stats at 100 i.e, binary value "4"

The output after 13 pulses is $(13-4)\%8$

$\Rightarrow 9\%8 = 1\ (001)$

Count = 1 after 13 pulses

→ after 99 pulses $\Rightarrow (99-4)\%8$

$\Rightarrow 95\%8$

$8)95\ (11$

8

15

8

7 → answer (111)

Count = 7 after 99 pulses

→ after 256 pulses $\Rightarrow (256-4)\%8$

$8)252\ (31$

24

12

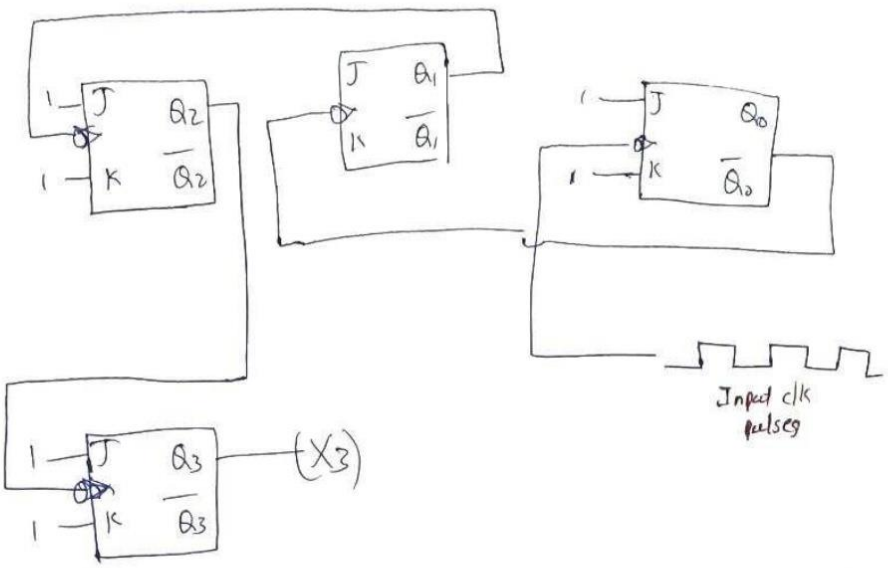
8

4 → answer (100)

Count = 4 after 256 pulses

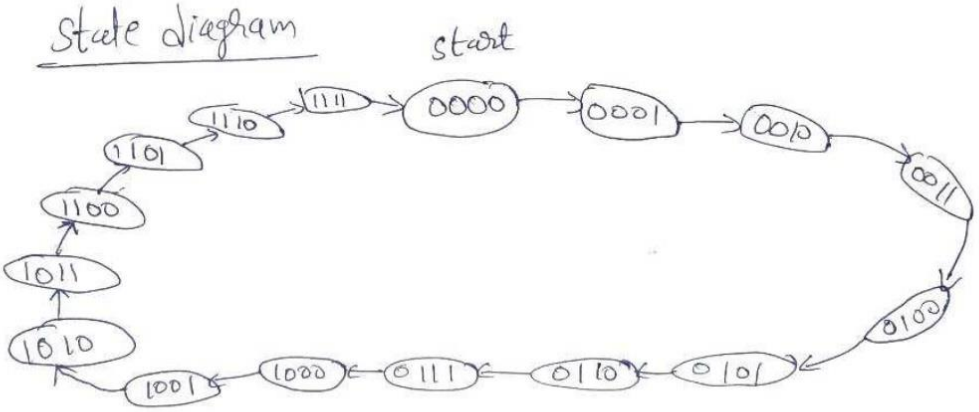
c)

(c)



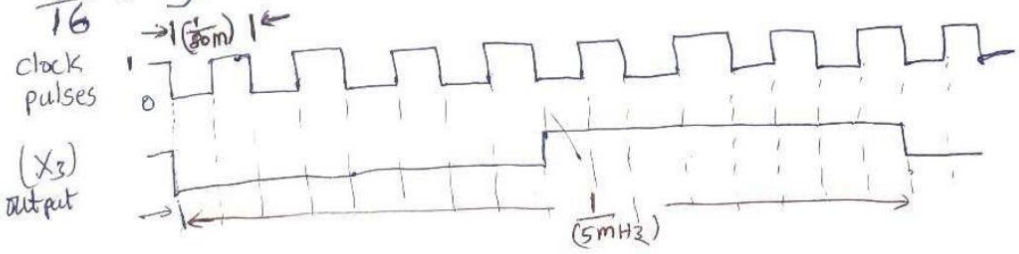
After connecting 4th JK flipflop the circuit becomes MOD 2^4 counter ⇒ MOD 16 Counter.

State diagram

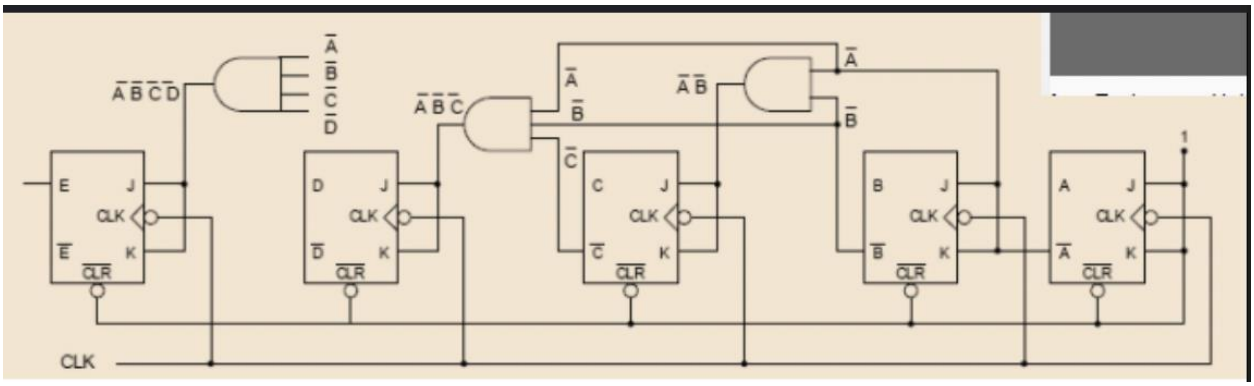


If input frequecy is 80mHz the (X_3) frequency is

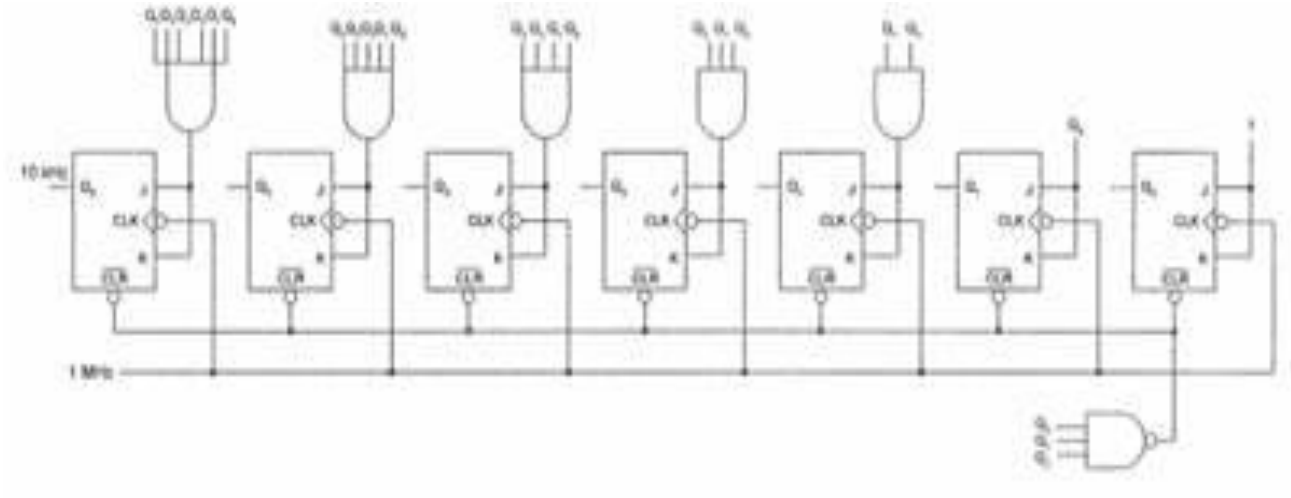
$\frac{80}{16} = 5$ mHz.



4)


$\overline{A}\,\overline{B}\,\overline{C}\,\overline{D}$
$\overline{A}\,\overline{B}\,\overline{C}$
$\overline{A}\,\overline{B}$
$\overline{A}$
$\overline{B}$
$\overline{C}$
$\overline{D}$
E
D
C
B
A
J
K
CLK
CLR
1
CLK

5)


10 MHz
1 MHz
CLK
CLR