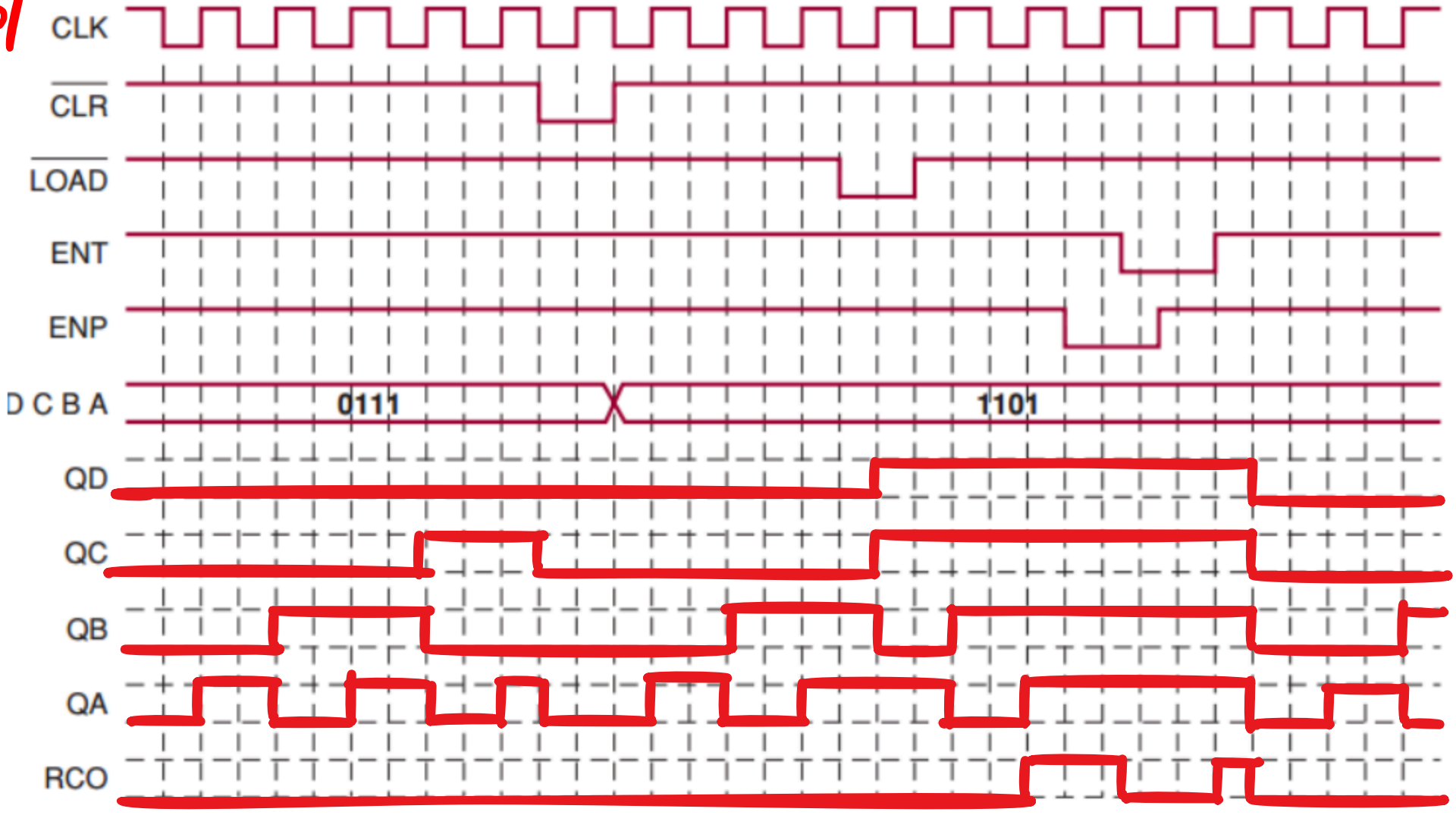
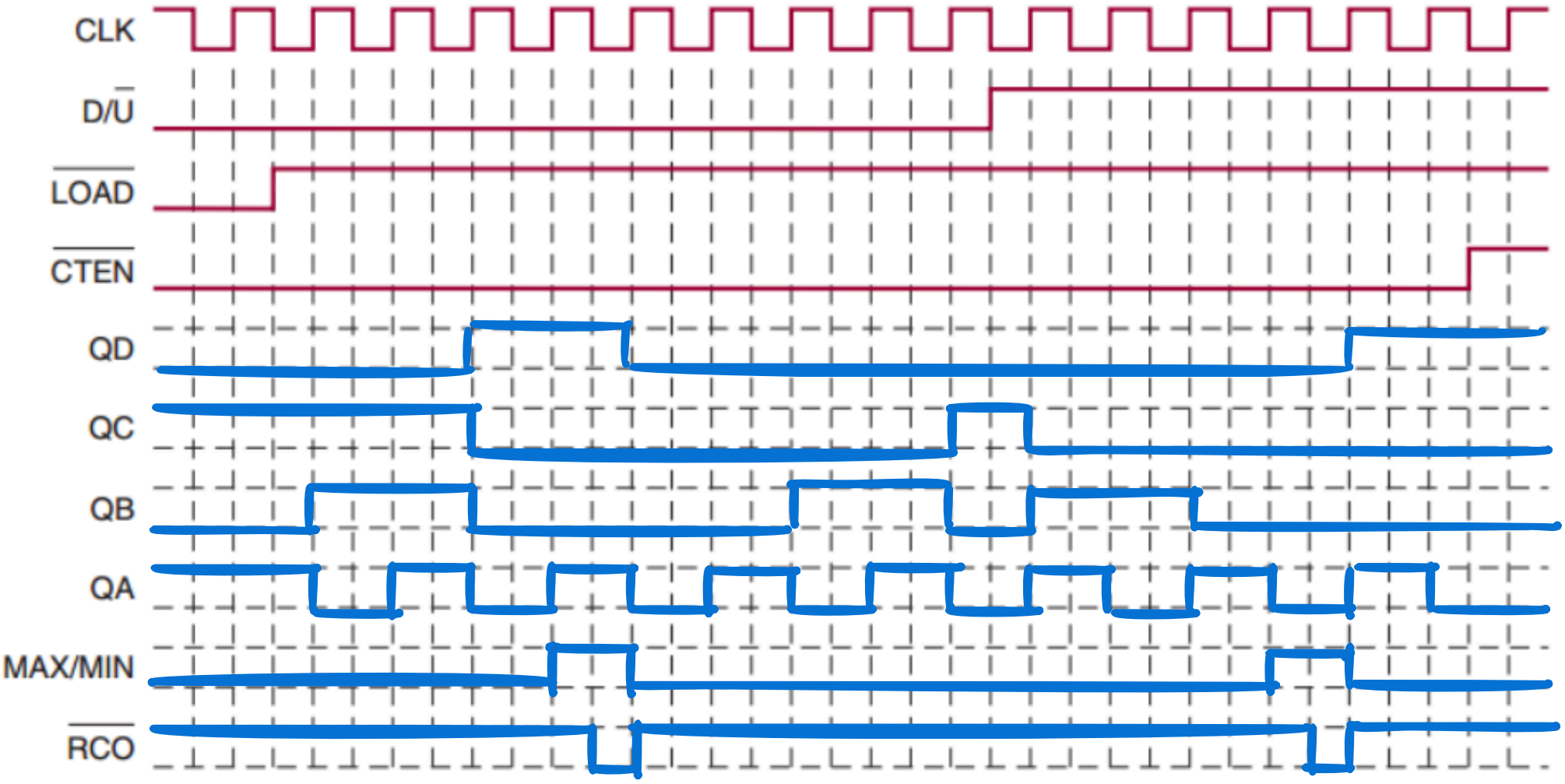
6/

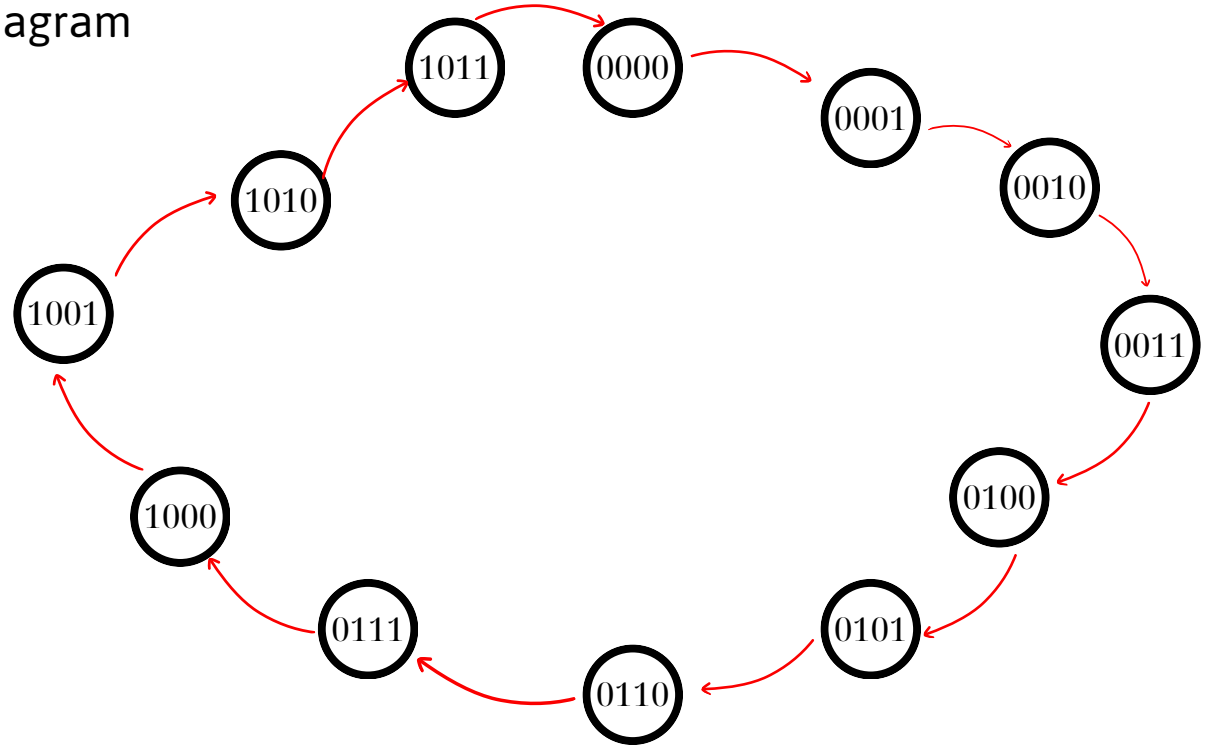


7. Complete the timing diagram in the following figure for a 74ALS190 with the indicated input waveforms applied. The DCBA input is 0101



8.

a) State Transition diagram



b)

From the STD, the counter gate goes through 12 distinct states

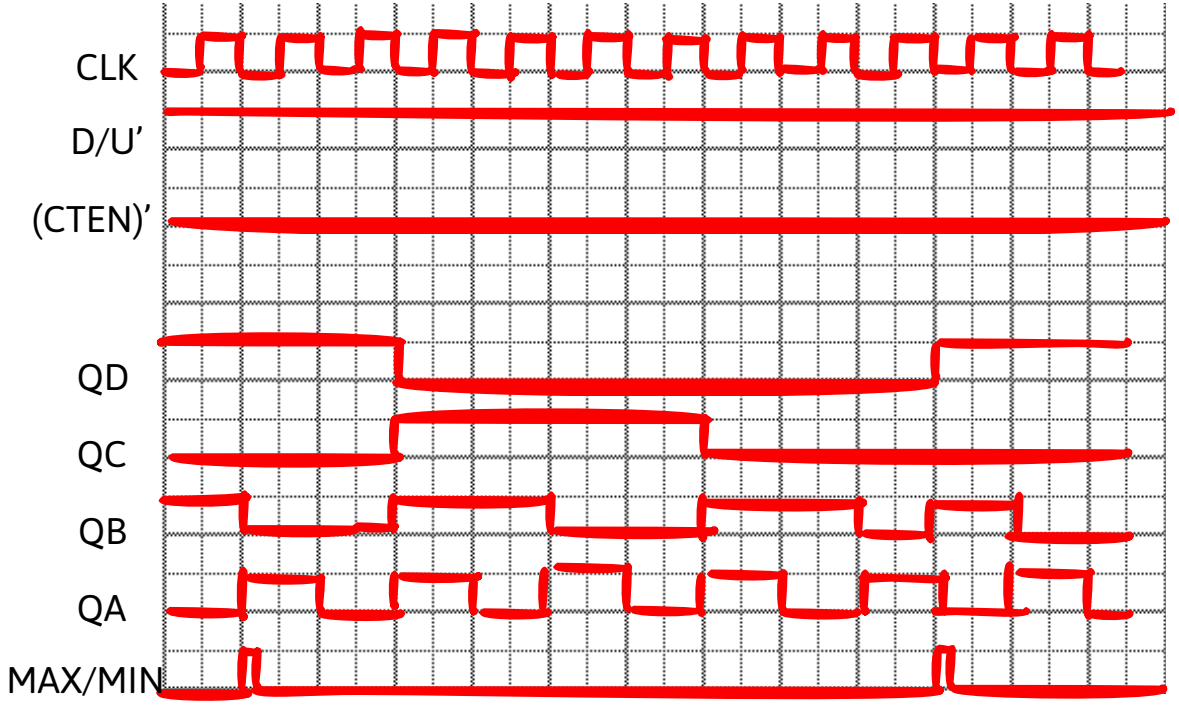
the IC counter circuit works as MOD-12

c)

frequency at QD (MSB) is 1/12 of CLK frequency

9.

a) Timing diagram for outputs QD QC QB QA



b)

the counter gate goes through 10 distinct states (1010 to 0001). It does not go to 0000 because LOAD goes LOW after few nanoseconds. So, the IC counter circuit works as MOD-10

c)

1010 --> 1001--> 1000 --> 0111-->0110 --> 0101 -->0100 --> 0011--> 0010 --> 0001 (10 to 1)

So, DOWN counter

d)

Can produce same modulus counters (MOD-10) but cannot produce the same counting sequence (while the 74HC190 counting upward, the 74HC191 counting downward)