Digital Logic Design Laboratory

Lab 7

Flip Flops and Counters

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GRADING GUIDELINE FOR LAB REPORT

Number	Content		Score	Comment
1	**Format (max 9%)**			
	- Font type	Yes No		
	- Font size	Yes No		
	- Lab title	Yes No		
	- Page number	Yes No		
	- Table of contents	Yes No		
	- Header/Footer	Yes No		
	- List of figures (if exists)	Yes No		
	- List of tables (if exists)	Yes No		
	- Lab report structure	Yes No		
2	**English Grammar and Spelling (max 6%)**			
	- Grammar	Yes No		
	- Spelling	Yes No		
3	**Data and Result Analysis (max 85%)**			
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I. Objectives

In this laboratory, students will study:

- Understand the operation of Flip Flops.
- Use a Flip Flops and design/implement a circuit based on a function definition.
- Design a counter based on Flip Flops

II. Procedure

1. Analyze and design synchronous counters

a. Analyze the counter given schematic circuit

Implement the below circuit in Figure 7. Control (SW1) and (SW2) to make the circuit operate.

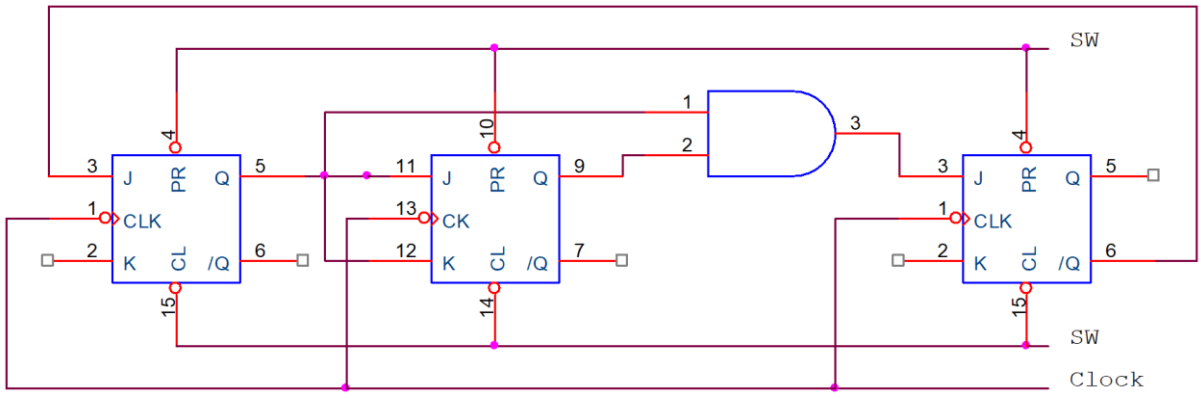


Figure 7. Logic diagram

When the clock is active:

When the clock signal is engaged, the state transitions. As the state undergoes changes, the inputs to the flip-flops adjust accordingly. These alterations in input, following the inherent behavior of the flip-flops, guide the system towards the subsequent state.

Write the excitation (trigger) input equations of all flip-flops:

$J_0 = \boldsymbol{Q_2}'$; $K_0 = 1$

$J_1 = \boldsymbol{Q_0}$; $K_1 = \boldsymbol{Q_0}$

$J_2 = \boldsymbol{Q_0} * \boldsymbol{Q_1}$; $K_2 = 1$

Transition Table

Present State									Next State		
Q2	**Q1**	**Q0**	**J2**	**K2**	**J1**	**K1**	**J0**	**K0**	**Q2**	**Q1**	**Q0**
0	0	0	0	x	0	x	1	x	0	0	1
0	0	1	0	x	1	x	x	1	0	1	0
0	1	0	0	x	x	0	1	x	0	1	1
0	1	1	1	x	x	1	x	1	1	0	0
1	0	0	x	1	0	x	0	x	0	0	0

J0

Q0 / Q2Q1	0	1
00	1	x
01	1	x
11	x	x
10	0	x

K0

Q0 / Q2Q1	0	1
00	x	1
01	x	1
11	x	x
10	x	x

J1

Q0 / Q2Q1	0	1
00	0	1
01	X	X
11	X	X
10	0	X

K1

Q0 / Q2Q1	0	1
00	X	X
01	0	1
11	X	X
10	X	X

J2

Q0 / Q2Q1	0	1
00	0	0
01	0	1
11	X	X
10	X	X

K2

Q0 / Q2Q1	0	1
00	X	X
01	X	X
11	X	X
10	1	X

J0=$\overline{Q2}$; K0=1

J1=K1=Q0

K2=1 ; J2=Q1.Q0

Implement the circuit via simulation software and paste the result in here

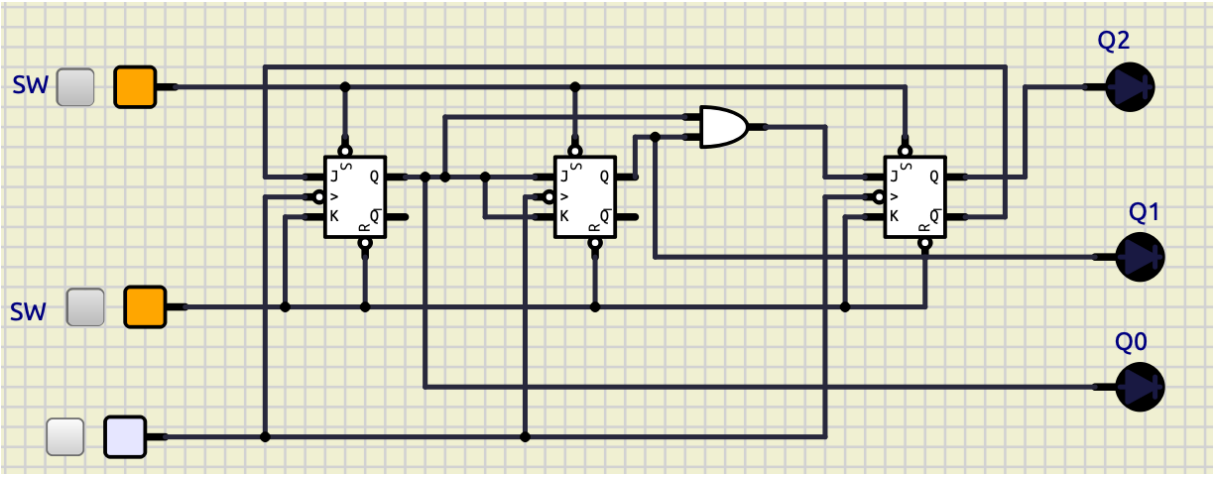


Figure 8. MOD-5 Counter

Draw the state diagram of the counter:

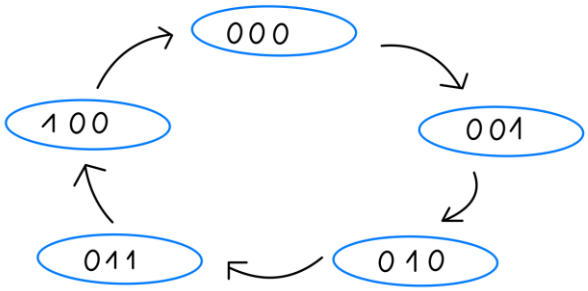


Figure 9. State diagram of the counter

Make comment on the results

This 3-bit synchronous counter perfectly demonstrates standard binary counting from 1 to 4. The chosen flip-flop excitation equations precisely govern this sequence, highlighting the direct influence of flip-flop configurations on counter behavior. This design underscores the essence of digital design - the ability to control outcomes through carefully chosen configurations.

b. Design and implement a synchronous counter by the given state diagram

Design and implement a synchronous 2-bit counter shown in the given diagram as shown in Figure 8 using J-K Flip Flops

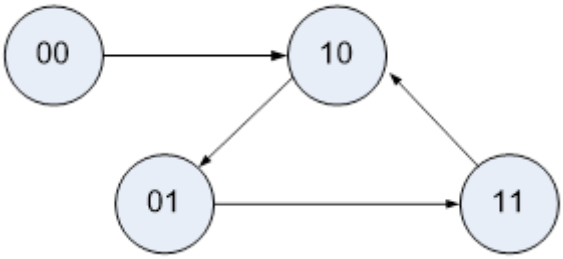


Figure 9. State diagram

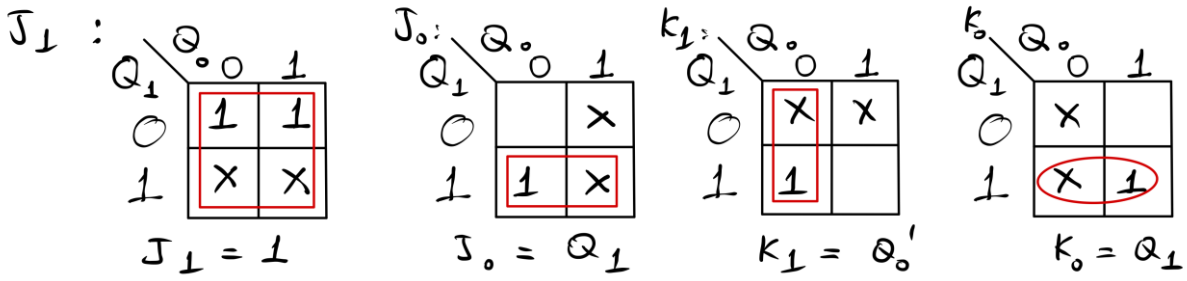
Transition Table

Present State						**Next State**	
Q1	**Q0**	**J1**	**K1**	**J0**	**K0**	**Q1**	**Q0**
0	0	1	X	0	X	1	0
1	0	X	1	1	X	0	1
0	1	1	X	X	0	1	1
1	1	X	0	X	1	1	0

Write the excitation (trigger) input equations of all flip-flops:

$J_0 = \boldsymbol{Q_1}$; $K_0 = \boldsymbol{Q_1}$

$J_1 = 1$; $K_1 = \boldsymbol{Q_0}$



Implement the circuit via simulation software and paste the result in here

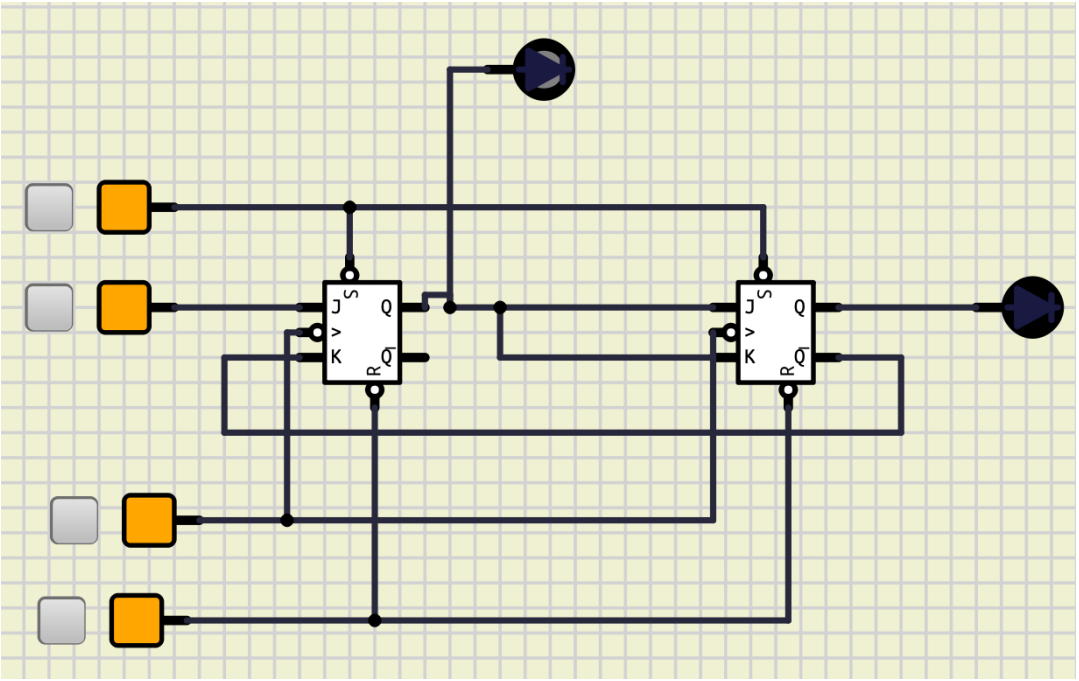


Figure 9. Circuit for the counter

Make comment on the results

Steps to design a synchronous 2-bit counter:

- First, we connect both of reset and set of two j-k flip flop to the fixed volt
- Second, we can see J0 and K0 equal to Q1, so we combine J0 and K0 together and connect to Q1
- Third, we connect J1 to fixed volt
- Final step, because the karaugh map of show that k1 equal to Q0', we connect k1 to Q0'

In conclusion, the 2-bit synchronous counter, with its unique 0-2-1-3-2 sequence, demonstrates how altering flip-flop configurations can yield varying counting patterns. The specific excitation equations (J0 = Q1, K0 = Q1, J1 = 1, K1 = Q0) drive the transitions, resulting in this unique sequence. This emphasizes that the design of synchronous counters isn't limited to standard binary counting, and they can be tailored for specific applications.