Name:
Student ID:

Analog Electronics

Homework # 1

Due date: March 23, 2020

Problem 1: BJT current steering circuit

For the circuit in Figure 1, every transistor is the same and has $|V_{BE}| = 0.7\ \text{V}$ and $\beta = \infty$. Find I, V_1, V_2, V_3, V_4, and V_5 for $R = 50k\Omega$. State briefly what will happen to I if β is finite

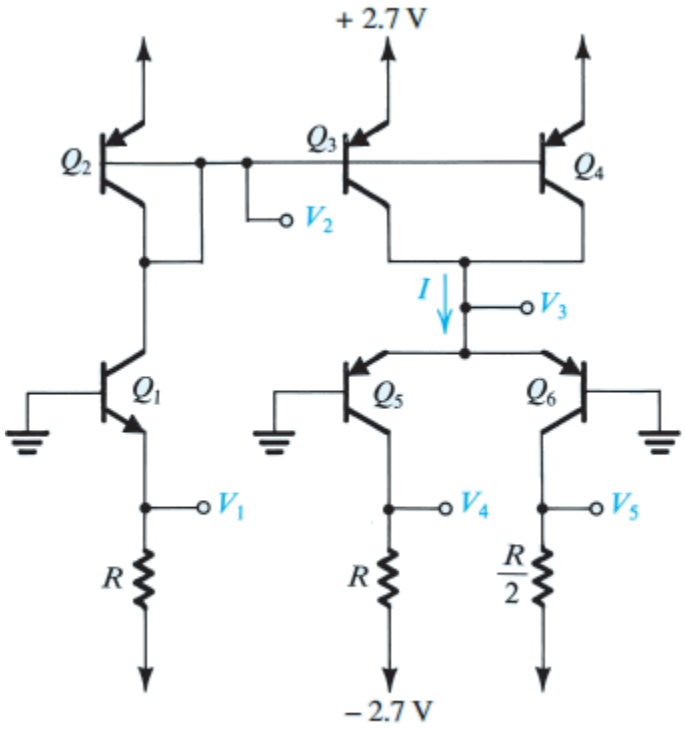

Figure 1

Problem 2: MOS current-steering circuit

The current-steering circuit of Figure 2 is fabricated in a CMOS technology for which $\mu_n C_{ox} = 400\,\mu A/V^2, \mu_p C_{ox} = 100\,\mu A/V^2, V_{tn} = 0.5V,\ V_{tp} = -0.5V, V'_{An} = 5\,V/\mu m$, and $|V'_{Ap}| = 5V/\mu m$. If all devices have $L = 0.5\mu m$, design the circuit so that $I_{REF} = 20\mu A, I_2 = 100\mu A, I_3 = I_4 = 40\mu A, and\ I_5 = 80\mu A$. Use the minimum possible device widths needed to achieve proper operation of the current source Q_2 for voltages at its drain as high as $+0.8V (V_{D2,max} = 0.8V)$ and proper operation of the current sink Q_5 with voltages at its drain as low as $-0.8V (V_{D5,min} = -0.8V)$.

a) Specify the widths of all devices and the value of R.

b) Find the output resistance of the current source Q_2 and the output resistance of the current sink Q_5.

Tip: *Assume* the transistors are in saturation mode. Remember the effect of channel length modulation when calculating i_D. From the given information of $V_{D2,max} = 0.8V$ and $V_{D5,min} = -0.8V$, you can calculate the corresponding overdrive voltage V_{OV}

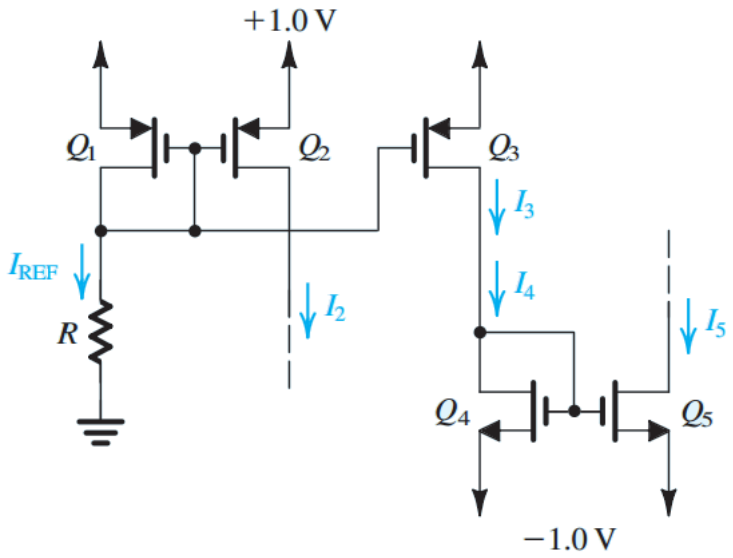

Figure 2

Problem 3: Basic Gain Cell

Figure 3 shows an IC MOS amplifier formed by cascading two common-source stages. Assuming that $V_{An} = |V_{Ap}|$ and that the biasing current sources have output resistances equal to those of Q_1 and Q_2.

a) Express the overall voltage gain v_0/v_i in terms of g_m and r_o of Q_1 and Q_2.

b) If Q_1 and Q_2 are to be operated at equal overdrive voltages, $|V_{OV}|$, find $|V_{OV}|$ if $|V_A| = 4V$ and $A_{vo} = 500\ V/V$

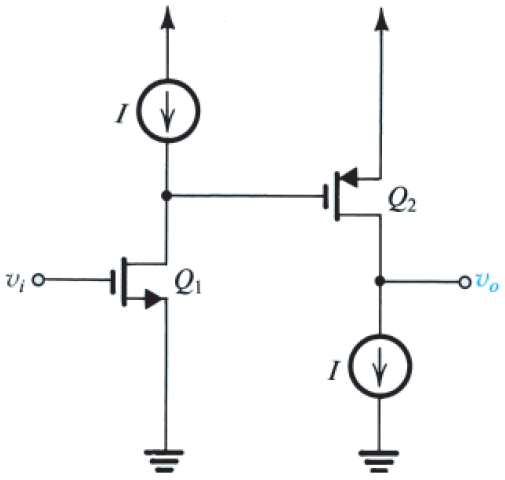

Figure 3

Problem 4: The MOS Cascode

Design the CMOS cascode amplifier in Figure 4 for the following specifications: $g_{m1} = 1.5\ mA/V$ and $A_v = -300\ V/V$. Assume that for the available fabrication process, $|V_A'| = 5\ V/\mu m$ for both NMOS and PMOS devices and that $\mu_n C_{ox} = 500\ \mu A/V^2$, $\mu_p C_{ox} = 200\ \mu A/V^2$. Use the same channel length L for all devices and operate all of them at $|V_{OV}| = 0.5\ V$. Determine L, the bias current I (I_{D1}), and the W/L ratio for each transistor. Assume that suitable bias voltages have been chosen, and neglect the Early effect in determining the W/L ratios

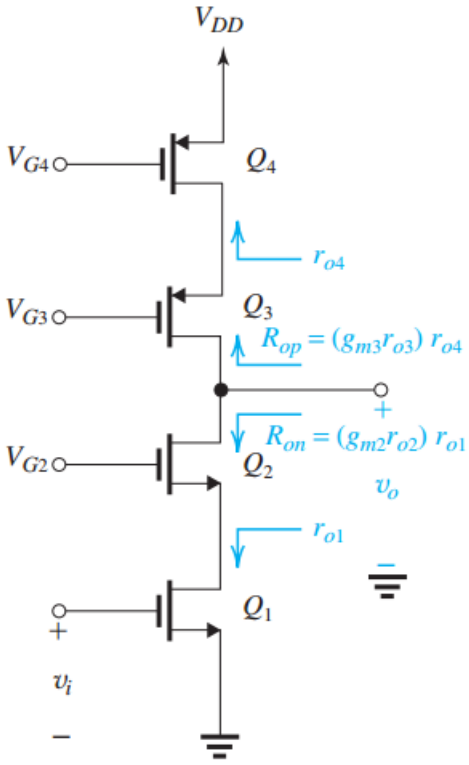

Figure 4