THE INTERNATINONAL UNIVERSITY (IU) – VIETNAM NATIONAL UNIVERSITY – HCMC

MIDTERM EXAMINATION

Date: 18 April 2019

Duration: 90 minutes

Subject: Digital Logic Design (EE053IU)	
Approved by Dean of School of Electrical Engineering **Mai Linh, Ph.D.**	Lecturer **Do Ngoc Hung**

READ CAREFULLY THE INSTRUCTIONS:

1. This is a semi-closed exam. Students are allowed to bring a handwritten A4 note.
2. Students are not allowed to leave the room before the exam ends. If you really want to do so, you MUST submit your paper before leaving the room at any time.
3. If there is any point in those questions that is not clear, please make assumptions and state clearly those assumptions in your work.
4. The usage of any electronic devices (electronic calculator, laptop, electronic dictionary, cell phones…) is strictly PROHIBITED.

Question 1. [20 marks]

a) Do the following conversions

i) $(2D.A)_{16}$ to decimal number

ii) $(261)_{10}$ to hexadecimal number

iii) $(1011101.101)_2$ to decimal number

iv) $(526)_8$ to BCD code

v) $(-102)_{10}$ to signed binary number using 1's complement format with minimum number of bits.

[15 marks]

b) Find $(35)_{10}$ - $(72)_{10}$ using two's complement format with 8-bit numbers. Then convert the result back to decimal number.

[5 marks]

Question 2. [20 marks]

Given the following logic diagram

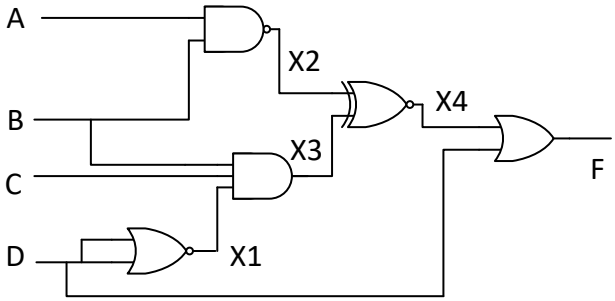

Figure 1. Logic diagram

a) Determine the output expressions of each logic gates X1, X2, X3, X4, and F

[10 marks]

b) Fill the following truth table

D	C	B	A	X1	X2	X3	X4	F
0	0	0	0					
0	0	0	1					
0	0	1	0					
.				.	.	.	.	.
.				.	.	.	.	.
.				.	.	.	.	.
1	1	1	0					
1	1	1	1					

[10 marks]

Question 3. [20 marks]

Given the 3 lines to 8 lines 74138 decoder IC as in figure 2:

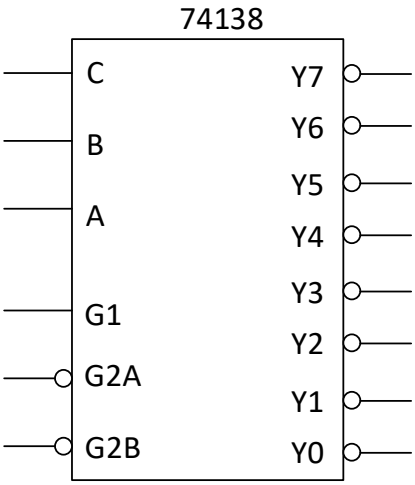

Figure 2. 74138 Decoder IC

a) Fill the following truth table

G1	G2A	G2B	C	B	A	Y7	Y6	Y5	Y4	Y3	Y2	Y1	Y0
0	X	X	X	X	X								
1	1	X	X	X	X								
1	X	1	X	X	X								
1	0	0	0	0	0								
1	0	0	0	0	1								
1	0	0	0	1	0								
1	0	0	0	1	1								
1	0	0	1	0	0								
1	0	0	1	0	1								
1	0	0	1	1	0								
1	0	0	1	1	1								

[5 marks]

b) Write the expressions of outputs $Y_7,...,Y_0$ as functions of the inputs C, B, A

[5 marks]

c) Use this decoder and logic gates to implement function $f(C,B,A)=\sum(0,1,2,5,6)$

[5 marks]

d) Use this decoder and NAND gates to implement function $f(C,B,A)=\bar{C}BA+\bar{B}A+CA$

[5 marks]

Question 4. [15 marks]

Design a circuit that counts the number of 1's present in 3 inputs A, B and C. Its output is a two-bit number X_1X_0, representing that count in binary number.

a) Draw the truth table for this circuit.

[5 marks]

b) Find the minimized logic equations for outputs.

[5 marks]

c) Draw the corresponding logic diagram for this circuit. Label all inputs and outputs.

[5 marks]

Question 5. [25 marks]

Given the following timing diagram

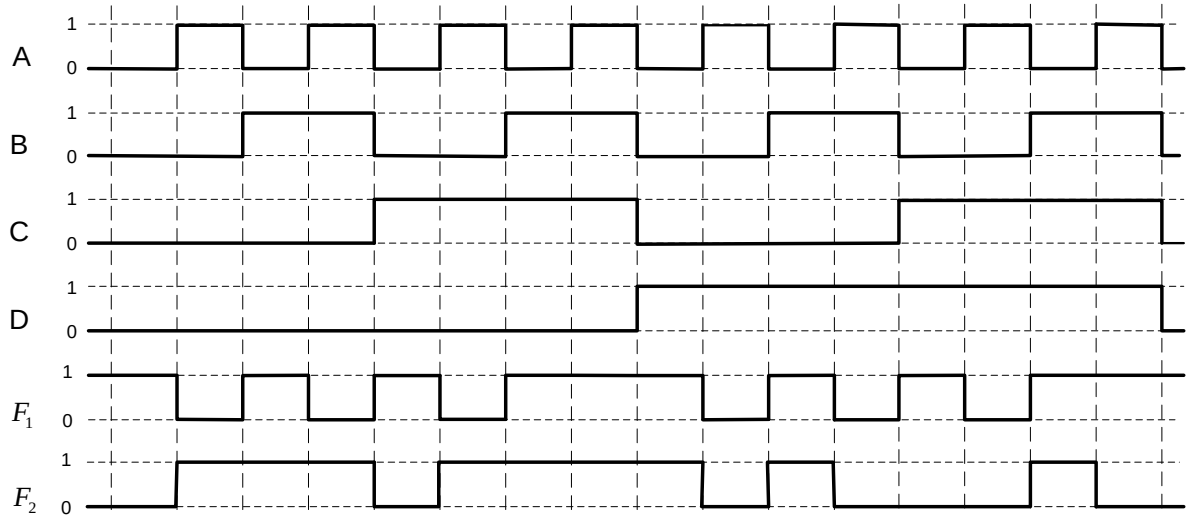

Figure 3. Timing Diagram

a) Draw the truth tables of $F_1(C,B,A), F_2(D,C,B,A)$

[5 marks]

b) Using K-map method, simplify the functions F_1, F_2

[8 marks]

c) Sketch the circuit diagrams by using logic gates

[4 marks]

d) Sketch the circuit diagrams by using only NAND gates

[8 marks]