THE INTERNATINONAL UNIVERSITY (IU) – VIETNAM NATIONAL UNIVERSITY – HCMC

FINAL EXAMINATION

Date: 24 Jan 2019

Duration: 120 minutes

Subject: Digital Logic Design (EE053IU)	
Approved by Dean of School of Electrical Engineering **Mai Linh, Ph.D.**	Lecturer **Do Ngoc Hung**

READ CAREFULLY THE INSTRUCTIONS:

1. This is a semi-closed exam. Students are allowed to bring a handwritten A4 note.
2. Students are not allowed to leave the room before the exam ends. If you really want to do so, you MUST submit your paper before leaving the room at any time.
3. If there is any point in those questions that is not clear, please make assumptions and state clearly those assumptions in your work.
4. The usage of any electronic devices (electronic calculator, laptop, electronic dictionary, cell phones…) is strictly PROHIBITED.

Question 1. [25 marks]

a) Do the following conversions

i) $(AF2)_{16}$ to decimal number

ii) $(36.5)_{10}$ to hexadecimal number

iii) $(10111.101)_2$ to decimal number

iv) $(-98)_{10}$ to signed binary number using 2's complement form

v) $(352.3)_8$ to decimal number

[15 marks]

b) Simplify the following Boolean function by using K-map method

$$f(D,C,B,A) = \sum(0,2,4,11,14,15) + d(6,7)\ ,$$

where d denotes 'don't care'.

Plot the simplified function using logic gates.

[10 marks]

Question 2. [20 marks]

a) Given the following Boolean function

$$f_1(w,x,y,z) = xy'z + x'y'z + w'xy + wx'y + wxy$$

Draw a corresponding Karnaugh map of the function f_1 .

[5 marks]

Simplify the function and implement it by using NAND gates only.

[5 marks]

b) Using MUX $8 \rightarrow 1$ (IC 74151 in Figure 1) to implement the function

$$f_2(w,x,y,z) = \sum(0,1,5,6,8,9,10,13,14,15)$$

[10 marks]

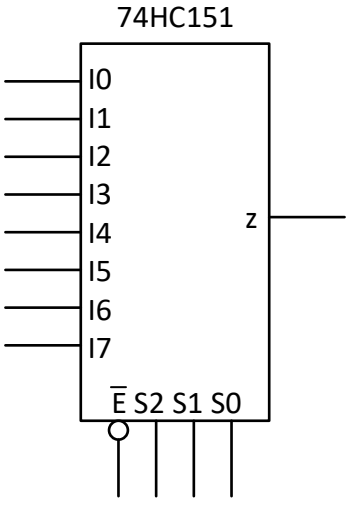

Figure 1. IC 74HC151

Question 3. [20 marks]

a) Convert a JK - Flip Flop into a D - Flip Flop

[10 marks]

b) Given the following JK - Flip Flop

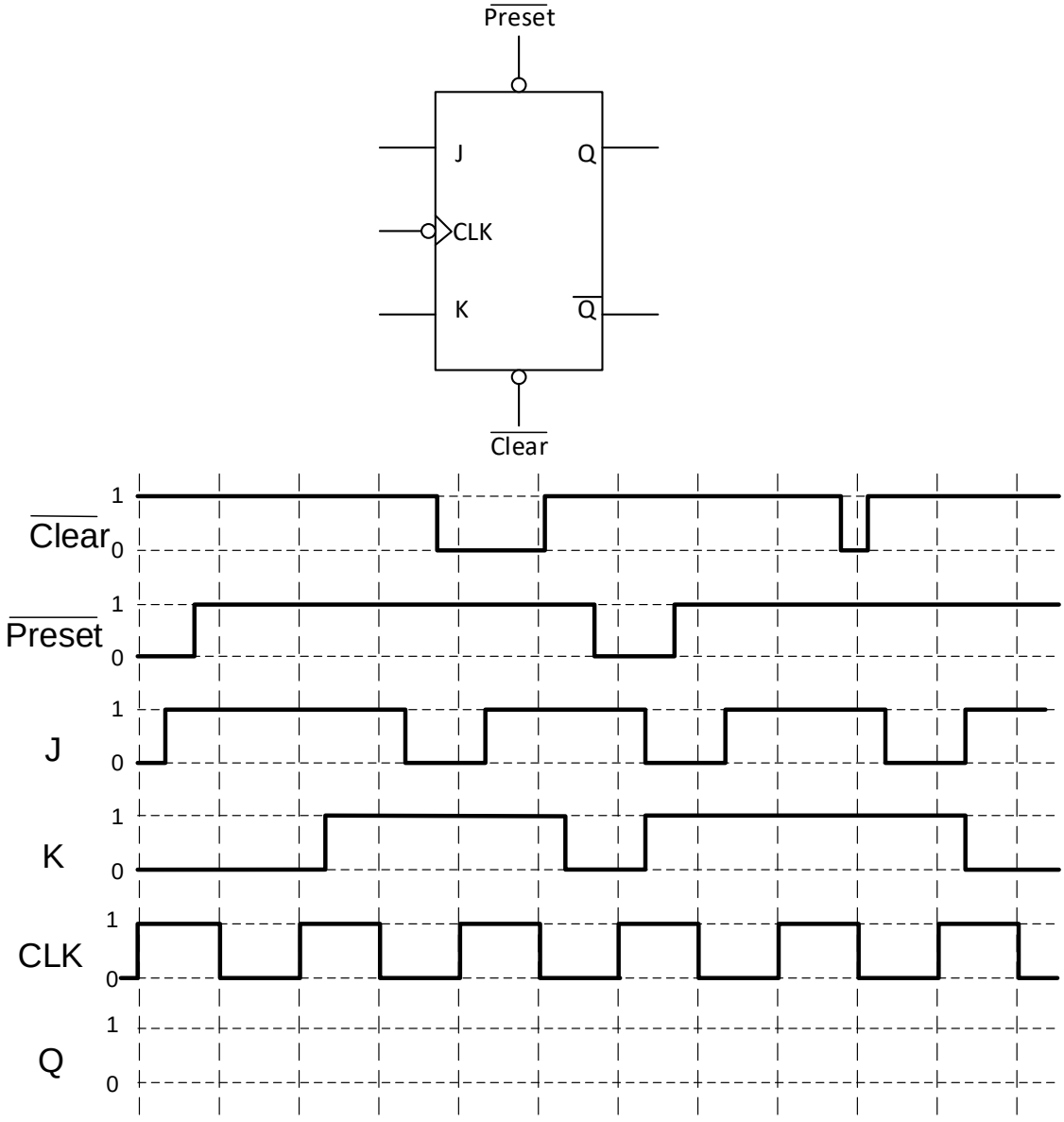

Figure 2. Timing Diagram

Sketch the output waveform Q in Figure 2.

[10 marks]

Question 4. [20 marks]

Design a synchronous counter using J-K Flip-Flops that has the following sequence: 000, 010, 101, 110, 111 and repeat. The undesired (unused) states 001, 011, and 100 must always go to 000 on the next clock pulse.

[20 marks]

Question 5. [15 marks]

Analyze the synchronous counter in Figure 3.

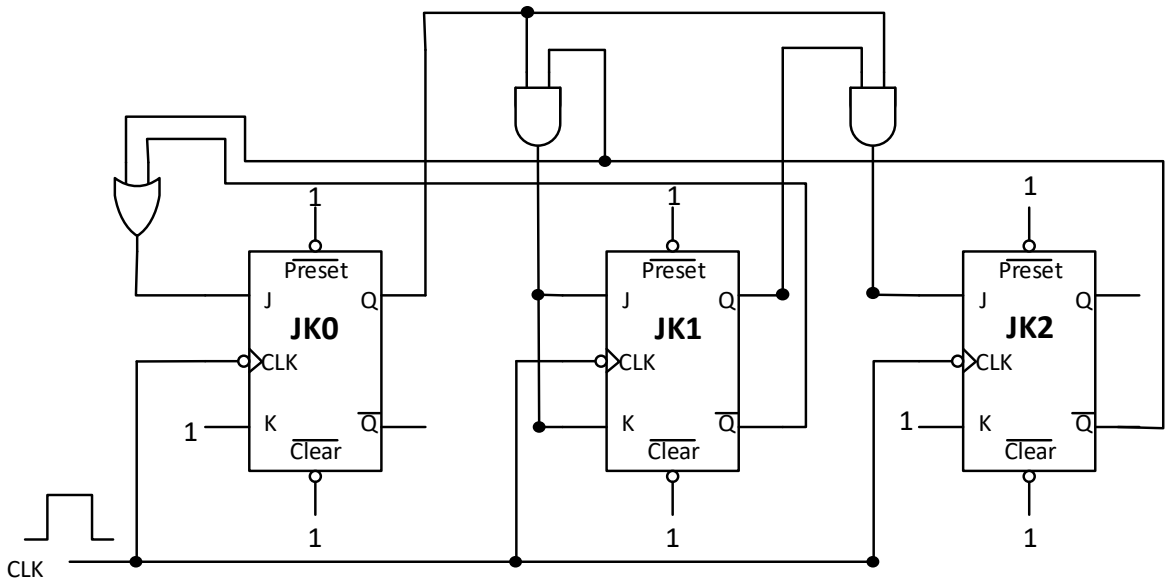

Figure 3. Synchronous counter

a) Determine the input functions of each Flip-Flop.

[5 marks]

b) Draw its state diagram and determine the counter's modulus.

[10 marks]