Chapter 1: System of Numeration

1. System of Numeration Conversion

Table 1: *Conversion between two different base numbers.*

	Binary	Octal	Decimal	Hexadecimal
Binary	1	$\left(\overline{B_{3j+2}B_{3j+1}B_{3j}} \dots \overline{B_2B_1B_0}\right)_2 = \left(\overline{O_j \dots O_0}\right)_8$	$\left(A_j \dots A_0\right)_2 = \sum_{i=0}^{j} A_i 2^i$	$\left(\overline{B_{4j+3}B_{4j+2}B_{4j+1}B_{4j}} \dots \overline{B_2B_1B_0}\right)_2 = \left(\overline{H_j \dots H_0}\right)_{16}$
Octal	$\left(\overline{O_j \dots O_0}\right)_8 = \left(\overline{B_{3j+2}B_{3j+1}B_{3j}} \dots \overline{B_2B_1B_0}\right)_2$	1	$\left(A_j \dots A_0\right)_8 = \sum_{i=0}^{j} A_i 8^i$	$\left(\overline{O_{2j+1}O_{2j}} \dots \overline{O_1O_0}\right)_{16} = \left(\overline{H_j \dots H_0}\right)_{16}$
Decimal	Division by 2 rule	Division by 8 rule	1	Division by 16 rule
Hexa-decimal	$\left(\overline{H_j \dots H_0}\right)_{16} = \left(\overline{B_{4j+3}B_{4j+2}B_{4j+1}B_{4j}} \dots \overline{B_2B_1B_0}\right)_2$	$\left(\overline{H_j \dots H_0}\right)_{16} = \left(\overline{O_{2j+1}O_{2j}} \dots \overline{O_1O_0}\right)_{16}$	$\left(A_j \dots A_0\right)_{16} = \sum_{i=0}^{j} A_i 16^i$	1

Note that:

1. **Table 1** shows the way to convert a number at base of row to number at base of column.
2. B_j,O_j,and H_j are notations for the digit of number in Binary, Octal, Hexa-decimal, respectively.
3. See **Table 2** to converse between Binary, Octal, and Hexadecimal.

Example:

$(\underline{1110}\ \underline{1100}\ \underline{0011})_2 = (EC3)_{16}$; $(\underline{111}\ \underline{011}\ \underline{000}\ \underline{011})_2 = (7303)_8$

$(1100\ 0011)_2 = 1.2^7 + 1.2^6 + 0.2^5 + 0.2^4 + 0.2^3 + 0.2^2 + 1.2^1 + 1.2^0 = 195$

$(EC3)_{16} = 14.16^2 + 12.16^1 + 3.16^0 = 3779$

Table 2: *First 16 numbers in some special system of numeration.*

Decimal	Binary	Octal	Hexa-decimal	Decimal	Binary	Octal	Hexa-decimal
0	0000	00	0	8	1000	10	8
1	0001	01	1	9	1001	11	9
2	0010	02	2	10	1010	12	A
3	0011	03	3	11	1011	13	B
4	0100	04	4	12	1100	14	C
5	0101	05	5	13	1101	15	D
6	0110	06	6	14	1110	16	E
7	0111	07	7	15	1111	17	F

Chapter 2: Boolean Algebra and Logic Components

1. Boolean Theorems

$A . 0 = 0$ $1 + A = 1$

$A . A = A$ $A + A = A$

Table 3: *Boolean algebra properties.*

Property	**AND**	**OR**
Commutative	$AB = BA$	$A + B = B + A$
Associative	$(AB)C = A(BC)$	$(A + B) + C = A + (B + C)$
Distributive	$A(B + C) = AB + BC$	$A + (BC) = (A + B)(A + C)$
Identity	$A \cdot 1 = A$	$A + 0 = A$
Complement	$A \cdot \overline{A} = 0$	$A + \overline{A} = 1$
DeMorgan's	$\overline{AB} = \overline{A} + \overline{B}$	$\overline{A + B} = \overline{A} \cdot \overline{B}$
Absorption	$A \cdot (A + B) = A$	$A + AB = A$
Common Identities	$A \cdot (\overline{A} + B) = \overline{A} + B$	$A + \overline{A}B = A + B$
Summation	$x + xy = x$ $x + \overline{x}y = x + y$ $\overline{x} + xy = \overline{x} + y$	

2. Minterm – Maxterm

Given a function with 3 variable C, B, A or $f(C, B, A)$. m_i represents for i-th minterm and M_i represents for i-th maxterm. Minterm and maxterm are compliment of each other, namely, $\mathrm{m}_i = \overline{\mathrm{M}_i}$ or $\mathrm{M}_i = \overline{\mathrm{m}_i}$

Example:

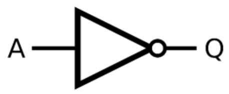
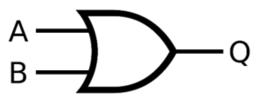
$$\mathrm{m}_6 = \mathrm{CB\overline{A}}, \qquad (6 = 110_2 \rightarrow \mathrm{CB\overline{A}})$$

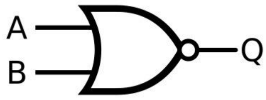
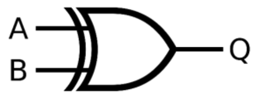
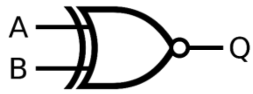
$$\mathrm{M}_5 = \overline{\mathrm{C}} + \mathrm{B} + \overline{\mathrm{A}}, \qquad \left(5 = 101_2 \rightarrow \overline{\mathrm{C\overline{B}A}} = \overline{\mathrm{C}} + \mathrm{B} + \overline{\mathrm{A}}\right)$$

3. Basic Logic Components

3. 1. Basic Logic Gates

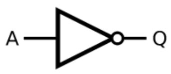
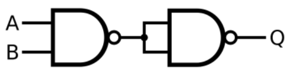
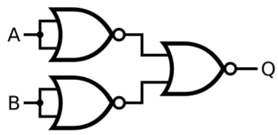
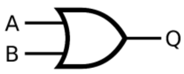
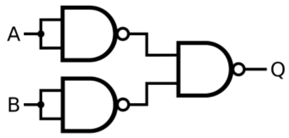
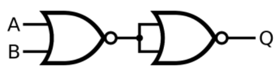
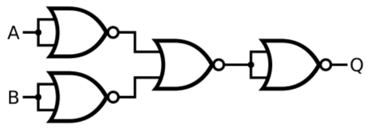
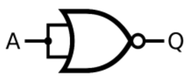
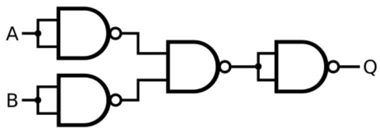
Table 4: *Logic gates.*

Gate	**Boolean Expression**	**Logic Diagram Symbol**	**Truth Table**
NOT	$Q = \overline{A}$		A Q 0 1 1 0
AND	$Q = A \bullet B$		A B Q 0 0 0 0 1 0 1 0 0 1 1 1
OR	$Q = A + B$		A B Q 0 0 0 0 1 1 1 0 1 1 1 1

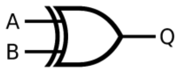
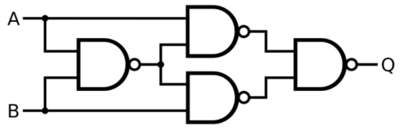
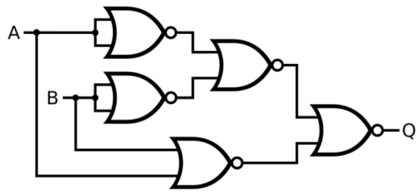
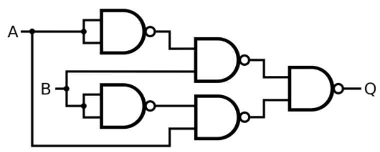
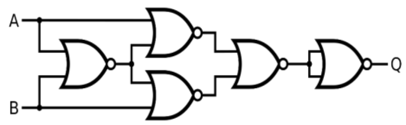
Gate	Boolean Expression	Logic Diagram Symbol	Truth Table
NAND	$Q = \overline{A \bullet B}$		A B Q 0 0 1 0 1 1 1 0 1 1 0
NOR	$Q = \overline{A + B}$		A B Q 0 0 1 0 1 0 1 0 0 1 1 0
XOR	$Q = A \oplus B$ $= \overline{A}B + A\overline{B}$		A B Q 0 0 0 0 1 1 1 0 1 1 1 0
XNOR	$Q = A \odot B$ $= \overline{A \oplus B}$ $= \overline{A}\,\overline{B} + AB$		A B Q 0 0 1 0 1 0 1 0 0 1 1 1

3. 2. Universal Gates

Table 5: *Universal gates.*

LF(1)	Logic Gates	NAND	NOR
NOT			
AND			
OR			
NAND			
NOR			

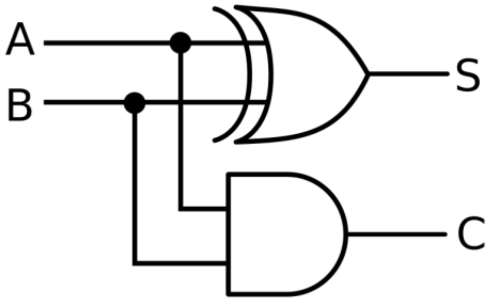
(1) LF: Logic function.

LF	Logic Gates	NAND	NOR
XOR		Delay 3 times	Delay 3 times
			
		Delay 4 times	Delay 4 times
			

Chapter 3: Integrated Circuit

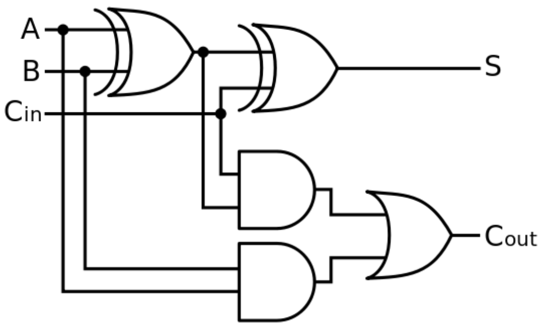
1. Adder

1. 1. Half Adder



INPUT		OUTPUT	
A	B	S	C
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

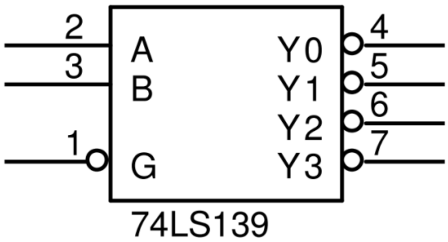
1. 2. Full Adder



INPUT			OUTPUT	
C_{in}	A	B	S	C_{out}
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

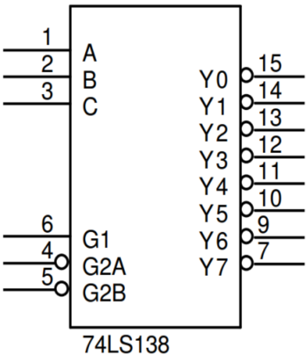
2. Decoder

2. 1. Decoder 2→4



CONTROL	INPUT		OUTPUT			
G	B	A	$\overline{Y}_3$	$\overline{Y}_2$	$\overline{Y}_1$	$\overline{Y}_0$
1	×	×	1	1	1	1
0	0	0	1	1	1	0
0	0	1	1	1	0	1
0	1	0	1	0	1	1
0	1	1	0	1	1	1

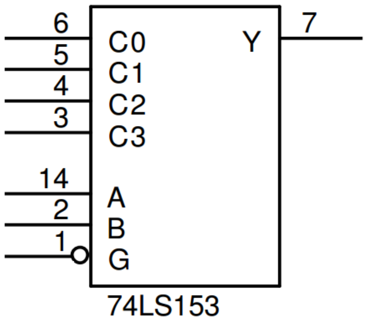
2. 2. Decoder 3→8



CONTROL			INPUT			OUTPUT							
G1	G2A	B2B	C	B	A	$\overline{Y}_7$	$\overline{Y}_6$	$\overline{Y}_5$	$\overline{Y}_4$	$\overline{Y}_3$	$\overline{Y}_2$	$\overline{Y}_1$	$\overline{Y}_0$
0	×	×	×	×	×	1	1	1	1	1	1	1	1
×	1	×	×	×	×	1	1	1	1	1	1	1	1
×	×	1	×	×	×	1	1	1	1	1	1	1	1
1	0	0	0	0	0	1	1	1	1	1	1	1	0
1	0	0	0	0	1	1	1	1	1	1	1	0	1
1	0	0	0	1	0	1	1	1	1	1	0	1	1
1	0	0	0	1	1	1	1	1	1	0	1	1	1
1	0	0	1	0	0	1	1	1	0	1	1	1	1
1	0	0	1	0	1	1	1	0	1	1	1	1	1
1	0	0	1	1	0	1	0	1	1	1	1	1	1
1	0	0	1	1	1	0	1	1	1	1	1	1	1

3. Multiplexer (MUX)

3. 1. Mux 4→1



CONTROL	INPUT		OUTPUT
G	B	A	Y
1	×	×	0
0	0	0	C_0
0	0	1	C_1
0	1	0	C_2
0	1	1	C_3

The output Y is given by

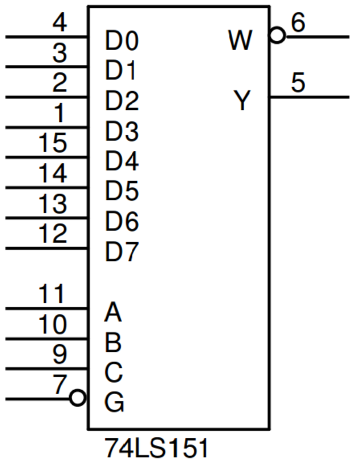
$$Y = C_0 m_0 + C_1 m_1 + C_2 m_2 + C_3 m_3$$

Where: m_i is the i-th minterm of function 2 variables B and A.

Example:

$$m_2 = B\overline{A}, (2 = 10_2 \to B\overline{A}); m_3 = BA, (3 = 11_2 \to BA)$$

3. 2. Mux 8→1



CONTROL	INPUT			OUTPUT
G	C	B	A	Y
1	×	×	×	0
0	0	0	0	D_0
0	0	0	1	D_1
0	0	1	0	D_2
0	0	1	1	D_3
0	1	0	0	D_4
0	1	0	1	D_5
0	1	1	0	D_6
0	1	1	1	D_7

The output Y is given by

$$Y = D_0m_0 + D_1m_1 + D_2m_2 + D_3m_3 + D_4m_4 + D_5m_5 + D_6m_6 + D_7m_7$$

Where: m_i is the i-th minterm of function 3 variables C, B, A.

Example:

$$m_2 = \overline{C}B\overline{A}, (2 = 010_2 \to \overline{C}B\overline{A}); m_6 = CB\overline{A}, (6 = 110_2 \to CB\overline{A})$$

4. Logic Map for DLD