



## Final Examination

Date: 26 January 2024; Duration: 120 minutes

Only lecture notes and student notes are allowed during the exam.

<b>SUBJECT: Digital Logic Design (EE053IU)</b>	
Approval by the School of Electrical Engineering Signature 	Lecturer: Signature 
Full name: Vo Tan Phuoc, Ph. D	Full name: Vuong Quoc Bao, Ph. D
Proctor 1 Signature	Proctor 2 Signature
Full name:	Full name:
<b>STUDENT INFO</b>	
Student name: <i>Nguyễn Anh Ngọc Hsey</i>	
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**INSTRUCTIONS:** the total of point is 100 (equivalent to 40% of the course)

1. *Purpose:*

- Analyze typical designs of digital system: combinational logic circuit and sequential logic circuit (G2.1).
- Derive the state-machine analysis or synthesis to design sequential logic circuits (G3.1).

2. *Requirement:*

- Students are allowed to use only lecture notes and personal notes.
- The usage of any electronic devices (laptop, electronic dictionary, cell phones...) is strictly PROHIBITED.

## QUESTIONS

### Question 1. [20 marks]

Implement the following Boolean expression with a 8-1 Multiplexer:

- a)  $F = \Pi(1,3,4,6,8,9,10,11,12,15)$
- b)  $F = \Sigma(0,1,2,4,5,6,8,9,10,11,13,14,15)$

### Question 2. [20 marks]

- a) What are the basic differences between D Flip-flop and J-K Flip-flop?
- b) Draw the truth tables and the operation diagrams of D Flip-flop and J-K Flip-flop.

### Question 3. [20 marks]

Design **an asynchronous counter** using J-K-Flip Flop that have  $M = 8$  and can count **UP/DOWN** (using 1 control button to control UP/DOWN). Show the way to make it (step by step).

### Question 4. [15 marks]

Design **an asynchronous counter** using J-K-Flip Flop that have  $M = 13$  (0→1→2...11→12 and repeat). Show the way to make it (step by step).

### Question 5. [25 marks]

- a) Convert a J-K Flip Flop into a D - Flip Flop.
- b) Design **a synchronous counter** using J-K-Flip Flop that can count from **0→1→3→2→6→7→5→4→0** and repeat. Show the way to make it (step by step).

1 2 3 4 5 6 7 8