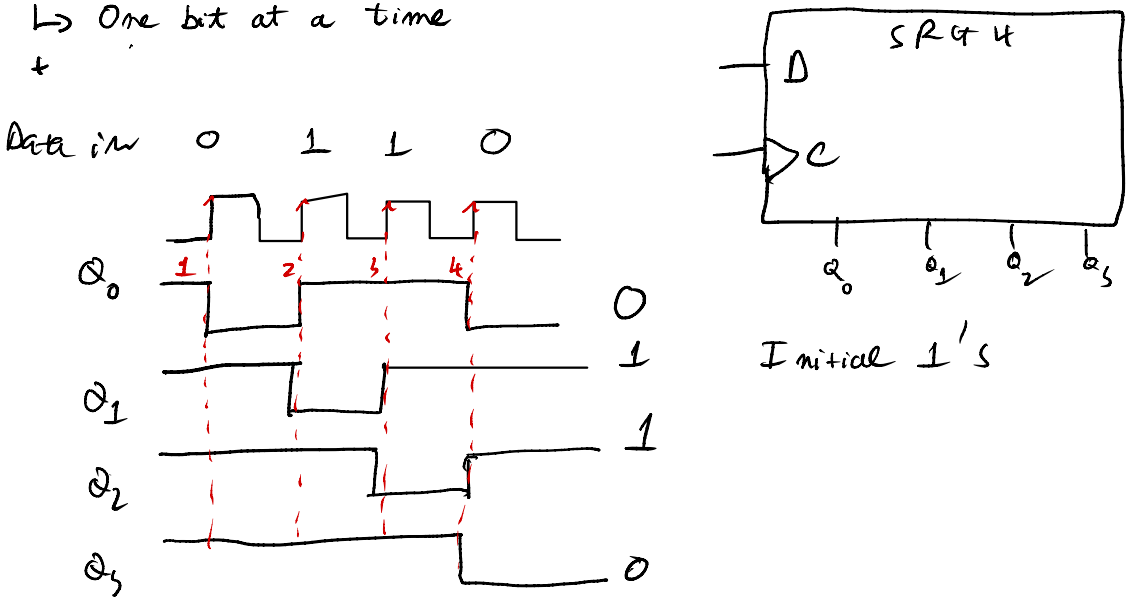
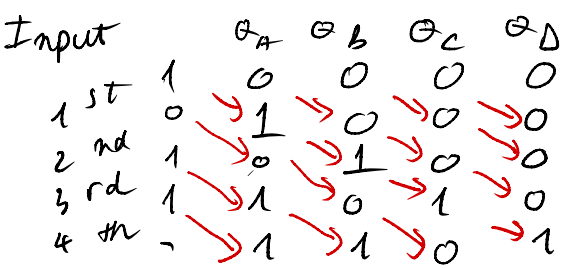
. Serial (SISO Mode):

↳ One bit at a time

+



3. The bit sequence 1101 is serially entered (least-significant bit first) into a 4-bit parallel out shift register that is initially clear. What are the Q outputs after two clock pulses?



2nd : Q output are 0100