### **Digital Logic Design Laboratory**

Lab 4

## Multiplexers

Full name: Nguyễn Đình Ngọc Huy-EEEEIU22020

Lê Quang Thông-EEACIU22222

Student number: 2

Class: 1

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#### I. Objectives

In this laboratory, students will study:

- Understand and design a multiplexer.
- Use a multiplexer and design/implement a circuit based on a function definition.
- Design combinational circuits using MUX.

#### II. Procedure

#### 1. Design multiplexer using logic gates

#### a. Design 2-to-1 multiplexer using logic gates:

A 2-to-1 multiplexer has  $I_0$  and  $I_1$  are the two inputs, S is the selector input, and Y is the output. When S=0 then  $Y=I_0$  but when S=1 then  $Y=I_1$ . The Figure 1 shows the illustration of MUX 2-1.

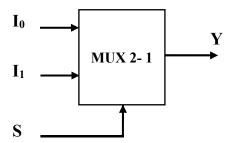


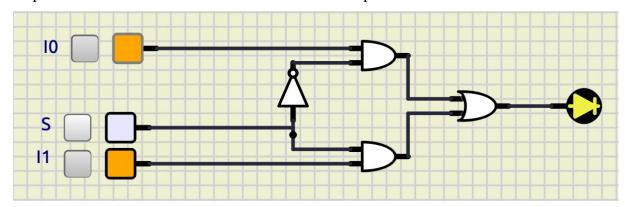
Figure 1. The illustration of MUX 2-1.

#### Built the truth table:

	•		Output
S	I <sub>0</sub>	I <sub>1</sub>	Y
0	0	0	0
0	0	1	1
0	1	1	0
0	1	0	1
1	0	0	0
1	0	1	0
1	1	1	1
1	1	0	1

The expressions:  $Y = \overline{S}I1 + SI0$ 

Implement the circuit via simulation software and paste the result in here



Make comment on the results: The outcomes demonstrate the idea of adjusting the control input S to switch between input lines (0 for I0 and 1 for I1).

#### b. Design 4-to-1 MUX using logic gates.

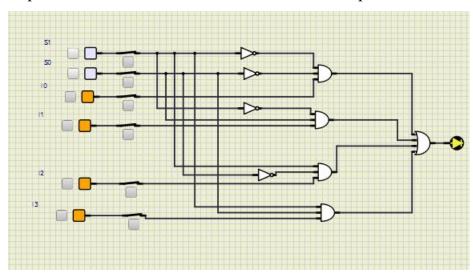
Build the circuit. The inputs  $S_0$ ,  $S_1$ ,  $I_0$ ,  $I_1$ ,  $I_2$ ,  $I_3$  are driven by 6 switches.

Input		Output
S <sub>0</sub>	$S_1$	Y
0	0	$I_0$
0	1	$I_1$

1	0	$I_2$
1	1	$I_3$

The expressions:  $Y = \overline{50} \overline{51} \overline{10} + \overline{50} \overline{51} \overline{11} + \overline{50} \overline{51} \overline{12} + \overline{50} \overline{51} \overline{13}$ 

Implement the circuit via simulation software and paste the result in here

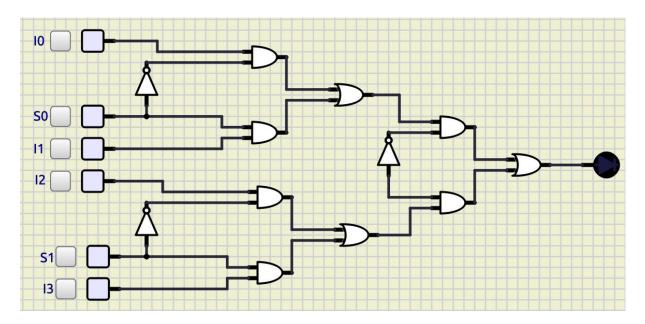


Make comment on the results

When we active all the switch of I0 I1 I2 I3, the led is light

#### c. Design 4-to-1 MUX using 3 MUX 2-1.





Input		Output	
S <sub>0</sub>	S <sub>1</sub>	Y	
0	0	$I_0$	
0	1	$I_1$	
1	0	$I_2$	
1	1	I <sub>3</sub>	

$$Y = S0'S1'I0 + S0'S1'I1 + S0S1'I2 + S0S1I3$$

Make comment on the results

The results of designing a 4-to-1 MUX using three 2-to-1 MUXs are as expected. The truth table correctly represents the functionality of a 4-to-1 MUX, where the combination of the selection lines S1 and S0 determine which input (I0, I1, I2, I3) is passed to the output.

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#### 2. Investigate IC 8-to-1 Multiplexer (74HC151)

Construct the circuit as below:

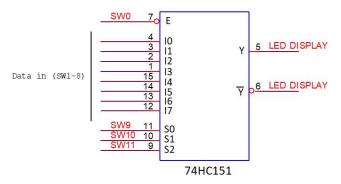
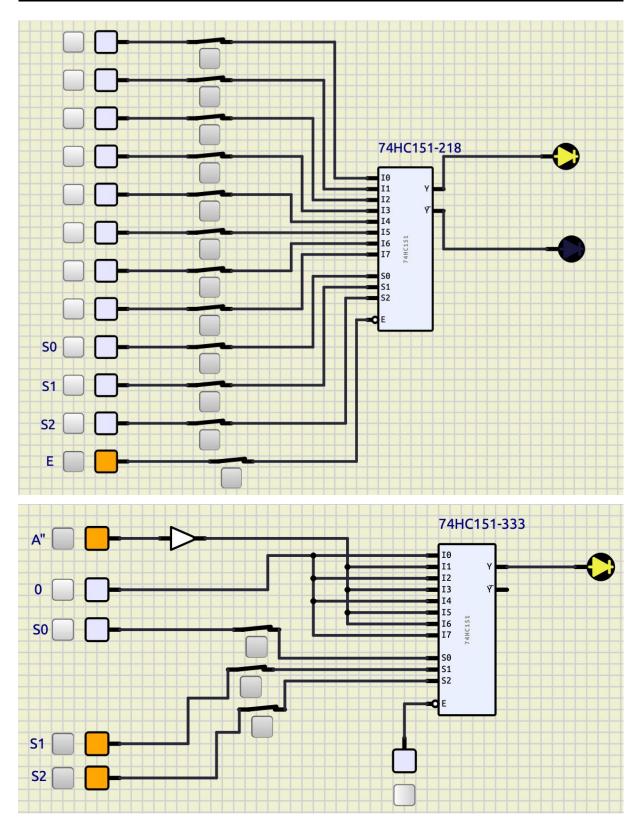


Figure 2. IC 8-to-1 Multiplexer (74HC151)

- 2 outputs are connected by using LEDs.
- The inputs are controlled by switches.
- Observe the results and fulfill the truth table

INPUT				OUT	PUT
S2	S1	S0	E	Y	Y
X	X	X	1	1	0
0	0	0	0	0	1
0	0	1	0	0	1
0	1	0	0	0	1
0	1	1	0	0	1
1	0	0	0	0	1
1	0	1	0	0	1
1	1	0	0	0	1
1	1	1	0	0	1





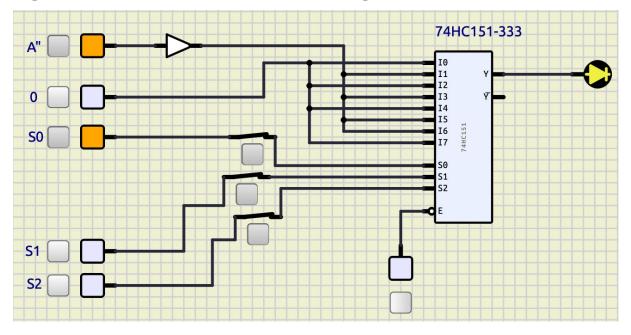


Briefly describe the operation of the IC: when the enable pin is pulled LOW (i.e., active), the IC 74HC151 selects its inputs using the binary combination of S2 - S1 - S0 inputs, with S2 being the MSB and S0 the LSB. For example, S2 - S1 - S0 equals to 1 - 0 - 1 selects input I5.

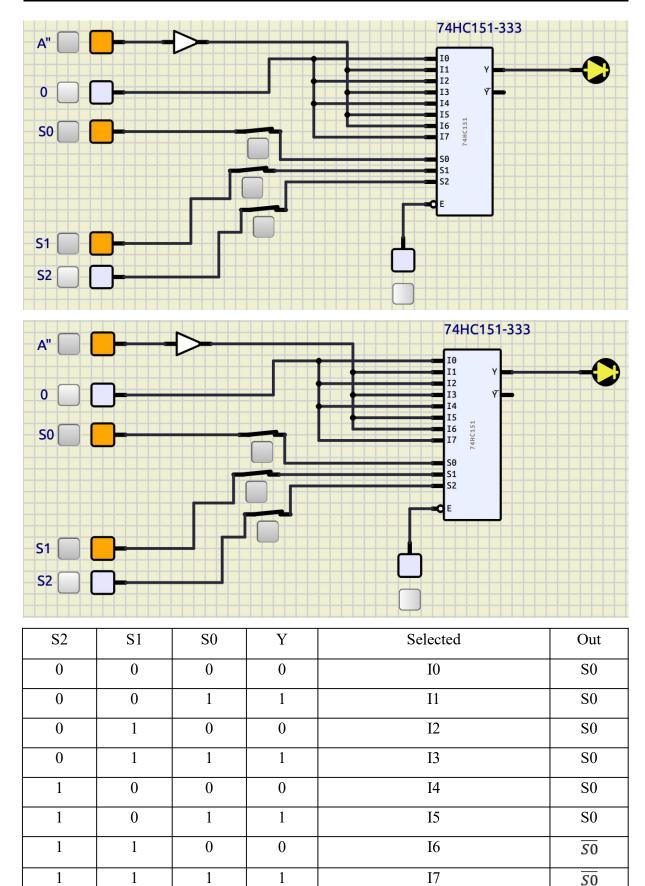
#### 3. Implement the 3-variable logic function using 74HC151

- Implement Boolean expression using IC 74HC151.
- The data inputs S0, S1, S2 are connected to switches.
- Implement the circuit and verify the truth table

a. 
$$f(S_2, S_1, S_0) = \sum_{S_2 S_1 S_0} (1, 3, 5, 6)$$







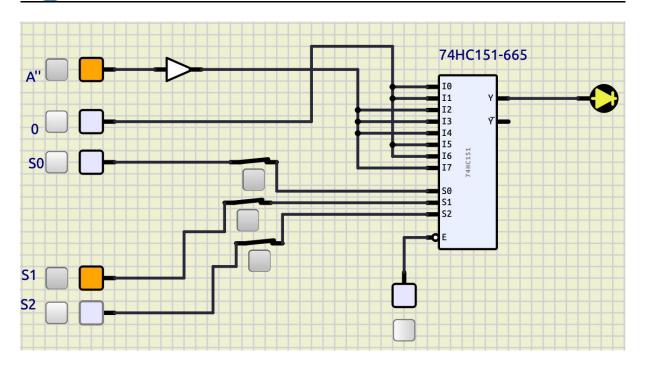


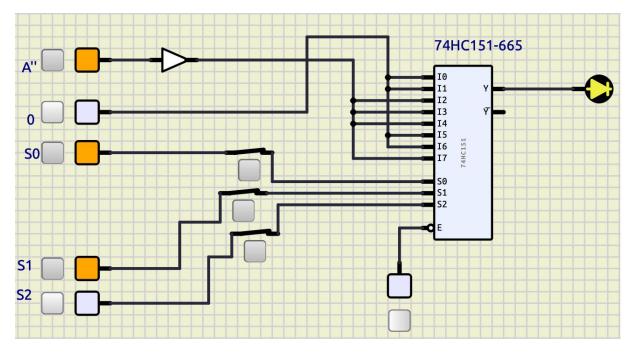
Make comment on the results: The S2,S1,S0 control the output of the IC equivalent to the input

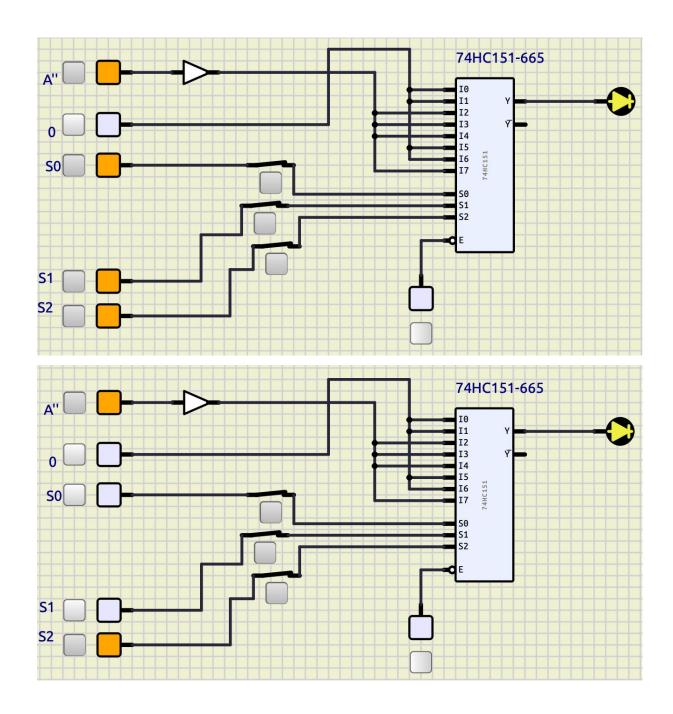
b. 
$$f(S_2, S_1, S_0) = \sum_{S_2S_1S_0} (2, 3, 4, 7)$$

S2	S1	S0	Y	Selected	Out
0	0	0	0	10	S0
0	0	1	1	I1	<i>S</i> 0
0	1	0	0	I2	<u>50</u>
0	1	1	1	I3	S0
1	0	0	0	I4	<u>50</u>
1	0	1	1	15	50
1	1	0	0	I6	S0
1	1	1	1	I7	S0









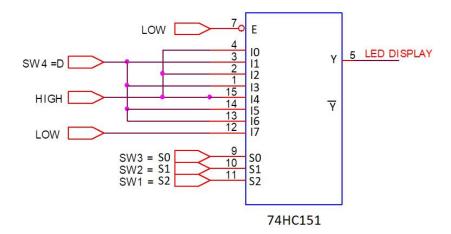
Make comment on the **results:** The IC's output is controlled by the S2,S1,S0, which are nearly equal to its input.

- 4. Implement the 4-variable logic function using 74HC151
- a. Implement the connected diagram using 74HC151.

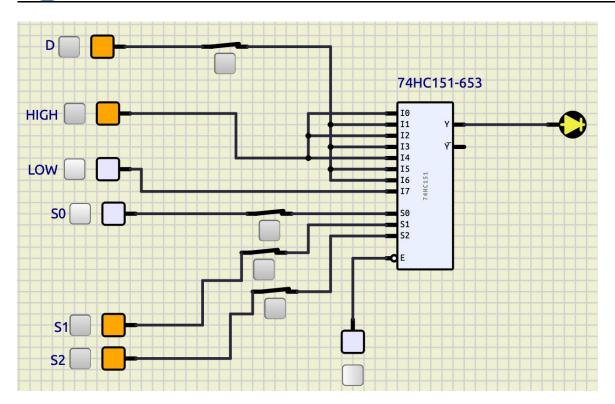
Construct the circuit as Figure 3:

Change the logic levels of the inputs C, B, A.

Observe and make comment on the results.







D	S2	S1	S0	Y
0	0	0	0	0
0	0	0	1	1
0	0	1	0	0
X	0	1	1	1
0	1	0	0	0
0	1	0	1	0
0	1	1	0	1
0	1	1	1	0
1	0	0	0	0
1	0	0	1	0
1	0	1	0	0
1	0	1	1	0
1	1	0	0	0
1	1	0	1	1
1	1	1	0	0



1 1 1 0

Write down the expression of  $f(D, S_2, S_1, S_0)$ :

$$f(D, S2, S1, S0) = D. S2.S1.\overline{S0} + D.\overline{S2}.S1.S0 + D.S2.\overline{S1}.S0 + D.S2.S1.\overline{S0} + \overline{S2}.\overline{S1}.\overline{S0} + \overline{S2}.S1.\overline{S0} + S2.\overline{S1}.\overline{S0}$$

Make comments on the results:

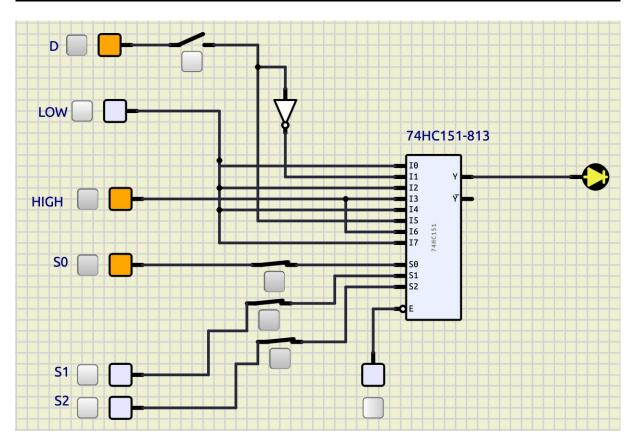
#### b. Implement logic expression using 74HC151

Given the expression:

$$f(D, S_2, S_1, S_0) = D S_2 \overline{S_1} S_0 + S_2 S_1 \overline{S_0} + \overline{S_2} S_1 S_0 + \overline{DS_2} \overline{S_1} S_0$$

Draw the block diagram





S2	S1	S0	D	f	
0	0	0	X	0	
0	0	1	0	1	
0	0	1	1	1	
0	1	X	X	0	
1	0	0	X	0	
1	0	1	X	0	
1	1	0	X	0	
1	1	1	0	0	
1	1	1	1	1	

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Make comments on the results

The given Boolean function f(D,S2,S1,S0) seems to be a specific combination of the input variables that result in a '1' output.

The function returns '1' only when:

- a. D is 0, S2 and S0 are 0, and S1 is 1. This could be interpreted as a specific condition where the absence (or '0') of D, S2, and S0 and the presence (or '1') of S1 triggers a '1' output.
- b. D and S1 are 0, and S2 and S0 are 1. This is another specific condition that triggers a '1' output.
- c. D is 0, S1 and S2 are 1, and S0 is 0. This is a third specific condition that triggers a '1' output.
- d. D and S2 are 1, S1 is 0, and S0 is 1. This is the last condition that triggers a '1' output.