DLD Homework 3

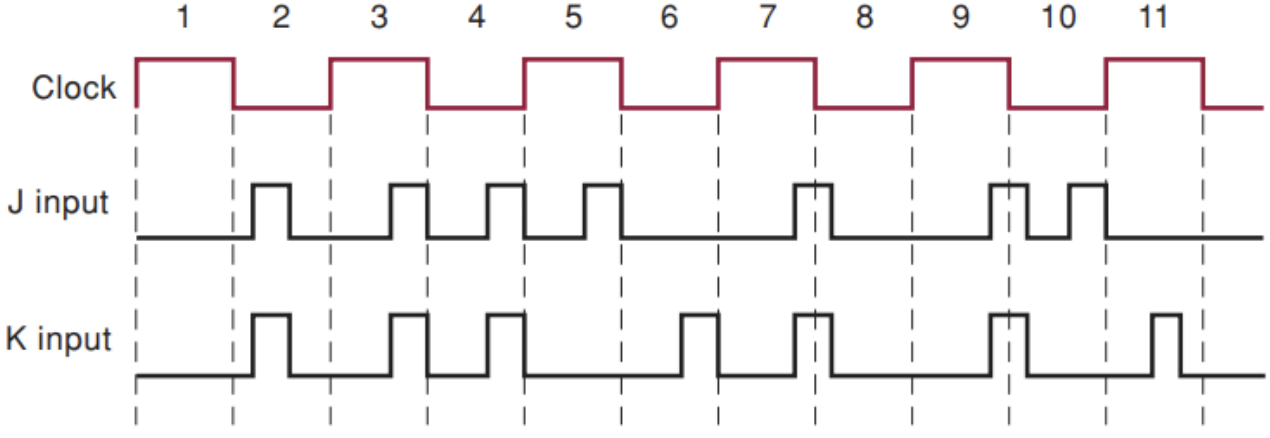
Term I – 2024

Student 1's Name: _____ Student 1's ID_____

Student 2's Name: _____ Student 2's ID_____

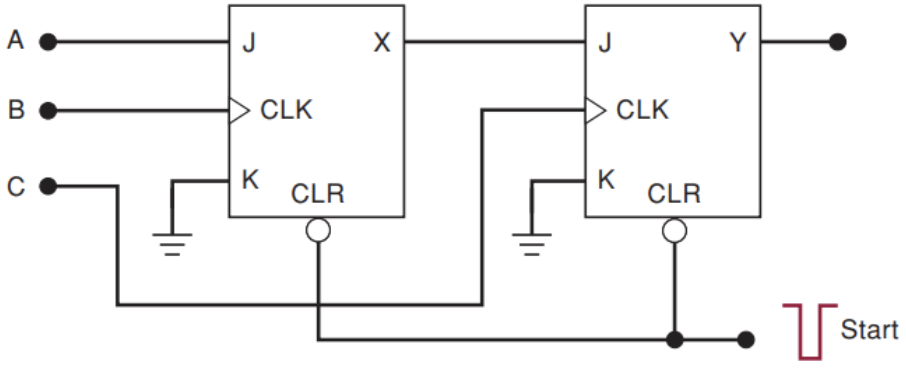
Student 3's Name: _____ Student 3's ID_____

1. The waveforms shown in the following Figure are to be applied to negative-edge-triggered J-K FF:



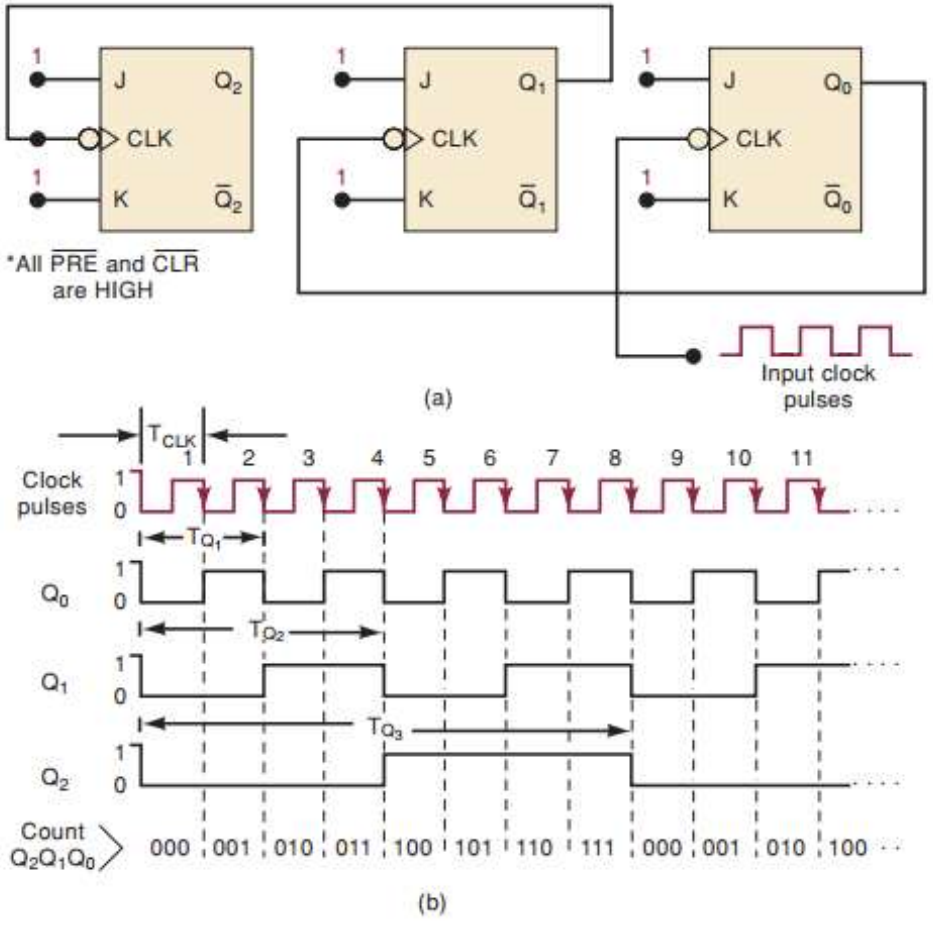
Draw the Q waveform response for each of this FF, assuming that Q = 0 initially.

2. In the following circuit, inputs A, B, and C are all initially LOW. Output Y is supposed to go HIGH only when A, B, and C go HIGH in a certain sequence.
   a. Determine the sequence that will make Y go HIGH.
   b. Explain why the START pulse is needed.
   c. Modify this circuit to use D FFs.



3. Refer to the following counter circuit and answer the following:
   a. If the counter starts at 000, what will be the count after 13 clock pulses? After 99 pulses? After 256 pulses?
   b. If the counter starts at 100, what will be the count after 13 pulses? After 99 pulses? After 256 pulses?

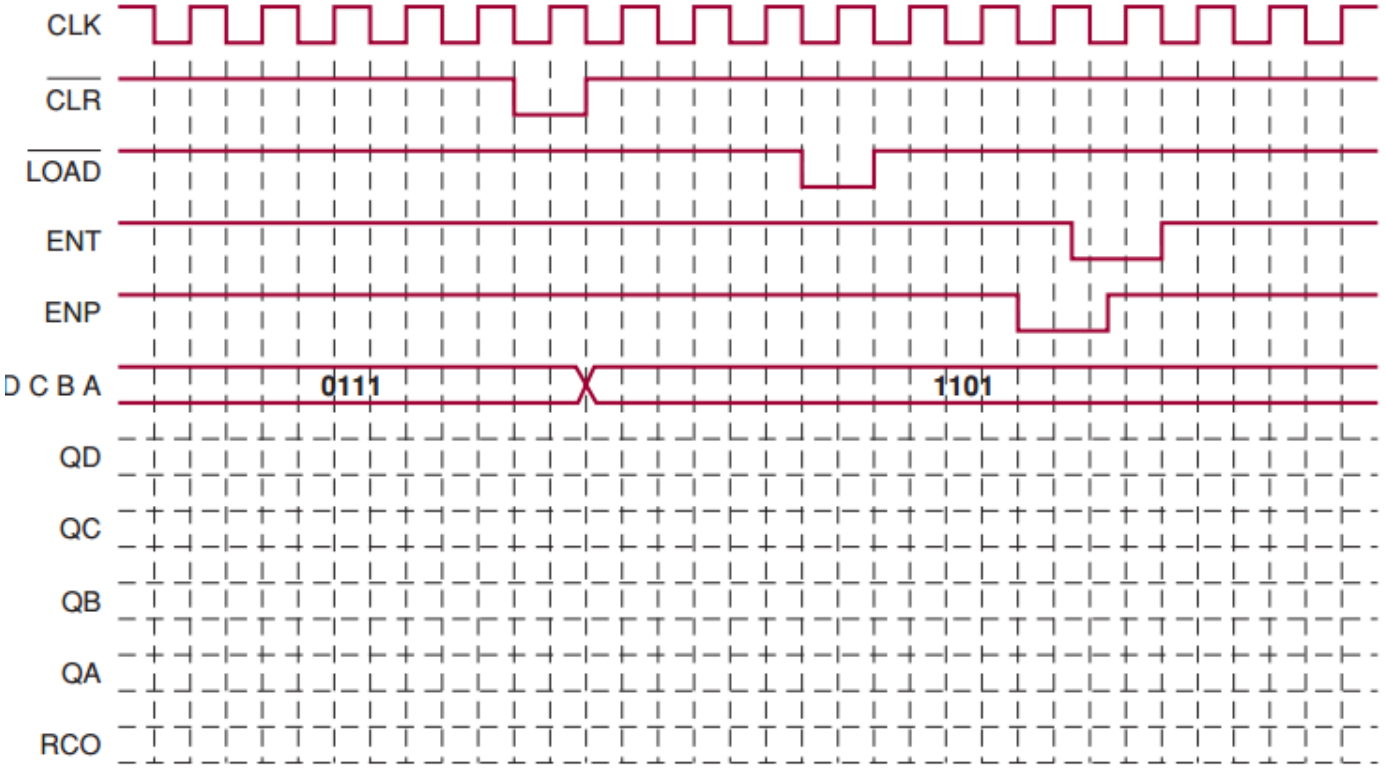
c. Connect a fourth J-K FF (X_3) to this counter and draw the state transition diagram for this 4-bit counter. If the input clock frequency is 80 MHz, what will the waveform at X_3 look like?



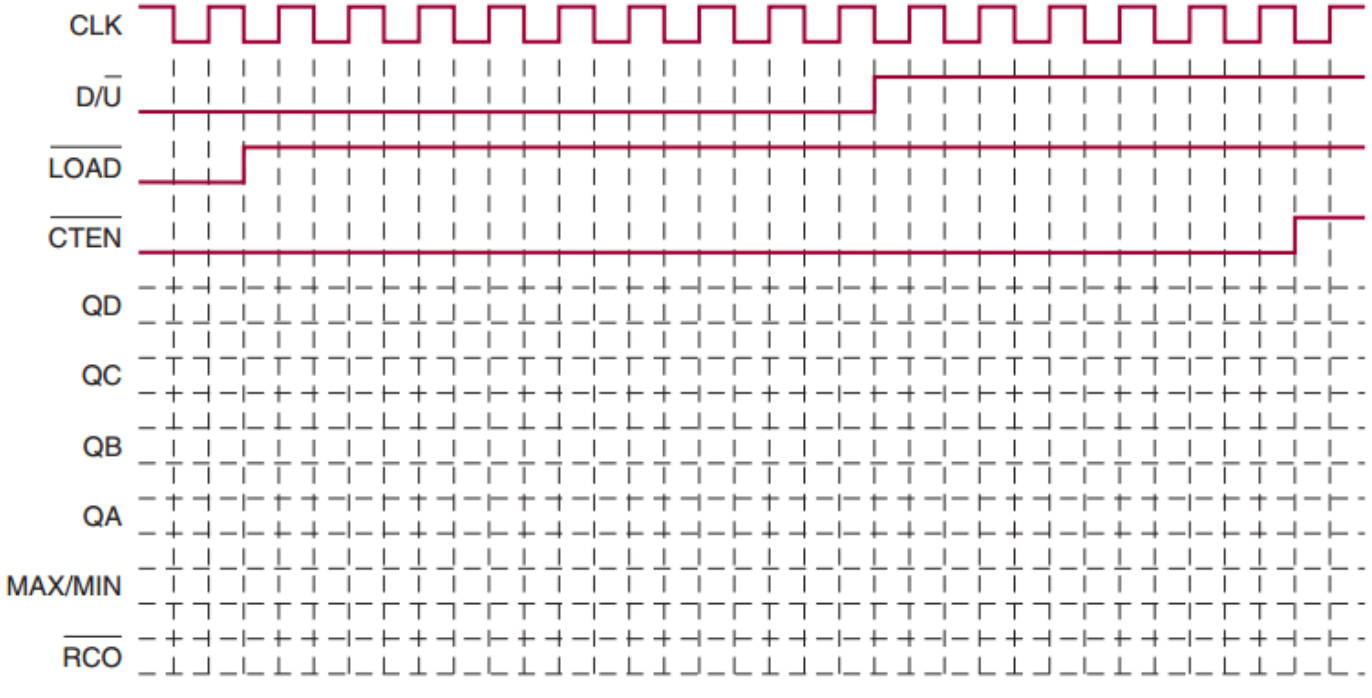
4. Draw the circuit diagram for a MOD-32 synchronous up-counter.

5. Draw a synchronous, MOD-32, down counter.

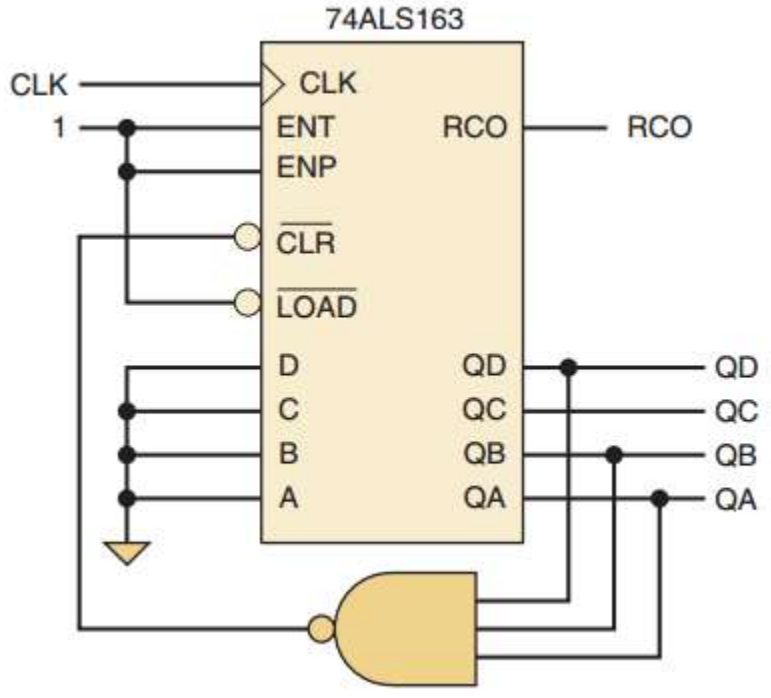
6. Complete the timing diagram in the following figure for a 74ALS161 with the indicated input waveforms applied. Assume the initial state is 0000.



7. Complete the timing diagram in the following figure for a 74ALS190 with the indicated input waveforms applied. The DCBA input is 0101

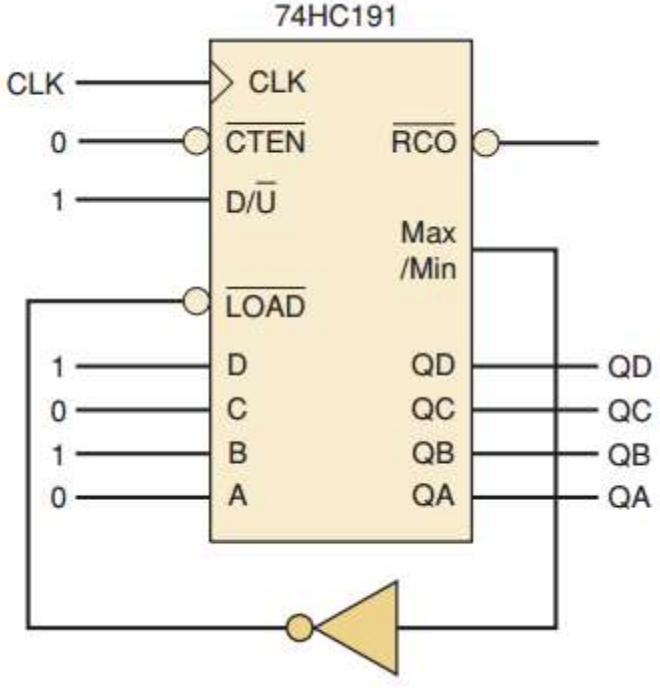


8. Refer to the IC counter circuit in the following figure:



a. Draw the state transition diagram for the counter's QD QC QB QA outputs.
b. Determine the counter's modulus.
c. What is the relationship of the output frequency of the MSB to the input CLK frequency?

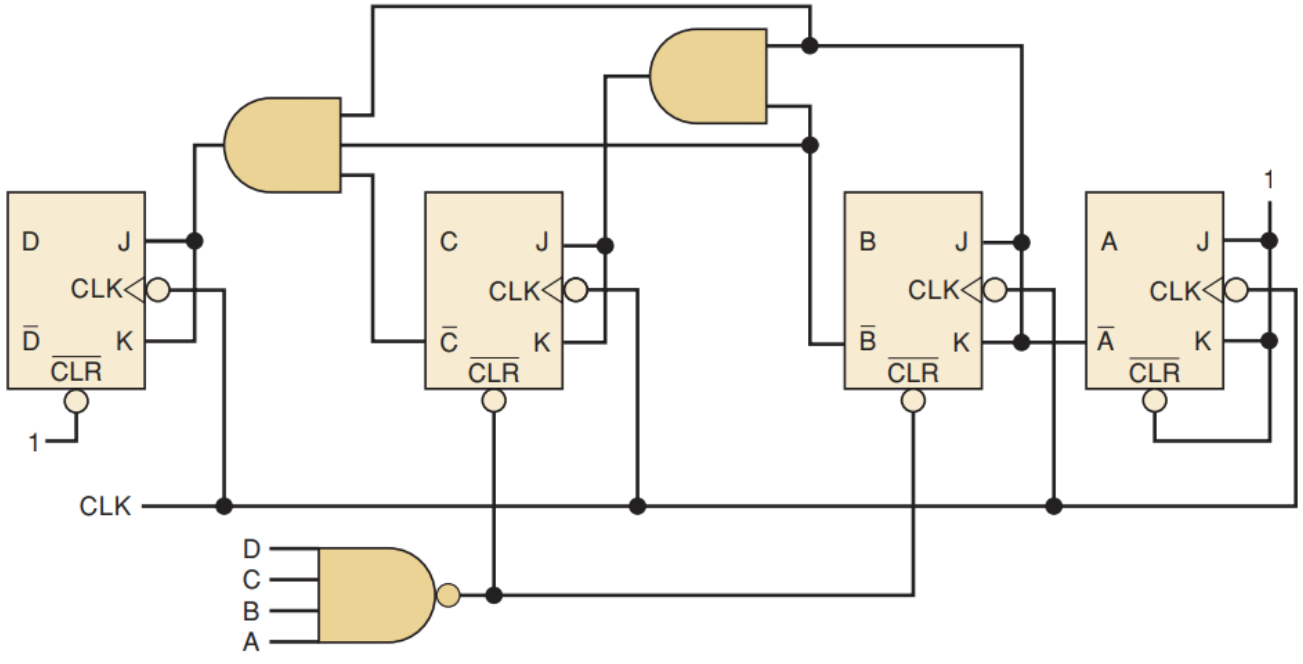
9. Refer to the IC counter circuit in the following figure.



a. Draw the timing diagram for outputs QD QC QB QA.
b. What is the counter's modulus?
c. What is the count sequence? Does it count up or down?

d. Can we produce the same modulus with a 74HC190? Can we produce the same count sequence with a 74HC190?

10. Analyze the synchronous counter in the following figure. Draw its timing diagram and determine the counter's modulus.



11. Design a synchronous counter:
    a. Design a synchronous counter using J-K FFs that has the following sequence: 000, 010, 101, 110, and repeat. The undesired (unused) states 001, 011, 100, and 111 must always go to 000 on the next clock pulse.
    b. Redesign the counter of part (a) without any requirement on the unused states; that is, their NEXT states can be don't cares. Compare with the design from (a).

12. Draw a schematic to create a recycling, MOD-5 counter that produces the count sequence:
    a. 1, 2, 4, 5, 6, and repeats with a 74ALS162
    b. 5, 4, 2, 1, 0, and repeats with a 74ALS190

13. Design a MOD-100, BCD counter using either two 74HC160 or two 74HC162 chips and any necessary gates. The IC counter chips are to be synchronously cascaded together to produce the BCD count sequence for 0 to 99. The MOD-100 is to have two control inputs, an active-HIGH count enable (EN) and an active-HIGH, synchronous load (LD). Label the counter outputs Q0, Q1, Q2, etc., with Q0 = LSB. Which set of outputs represents the 10s digit?