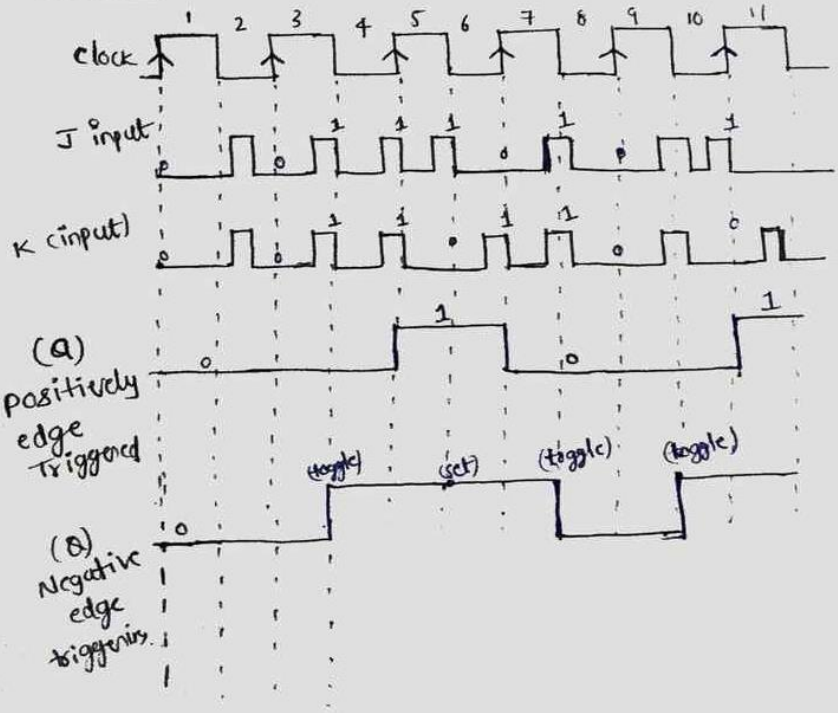
1)

Solution

Step 1: Truth table of JK FF

J	K	Q
0	0	Q (hold)
0	1	0 (reset)
1	0	1 (set)
1	1	$\bar{Q}$ (toggling)

Step 2:



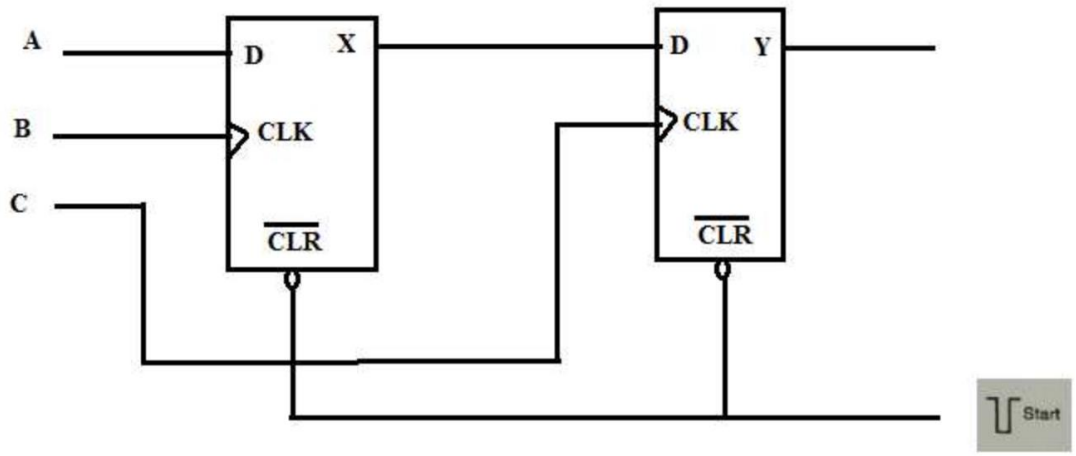
2)

a)after making A=1 , b=1 and making c=1 we'll get Y=1 or 100110111

b)To Initialize(reset) the flipflops to zero START pulse is needed

c.

USING D FLIPFLOP



3)

a)

⑨ The given circuit is (mod 8) Counter.

Input start by clk pulse.

Initial output state is 000 => binary "0"

As clk pulses negative edge arrives, the output state increments by 1 ~~and~~ untill binary "7" or 111. and starts again from 000 i.e, binary "0"

→ So after 13 clk pulses the output state is given as $13 \% 8 = 5$ (101).

The count is 5.

→ After 99 clocks pulses the count is 99%8

i.e, 8)99(12
8
19
16
(3) → answer

=> 99%8 = 3. => Count = 3 (011)

→ After 256 pulses the count is 256%8 i.e,

8)256(32
250
(0) → answ

the count is '0' (000)

---

⑥ The output stats at 100 i.e, binary value "4"

The output after 13 pulses is (13-4)%8

=> 9%8 = 1 (001)

b)

⑥ The output stats at 100 i.e, binary value "4"

The output after 13 pulses is $(13-4)\%8$

$\Rightarrow 9\%8 = 1\ (001)$

Count = 1 after 13 pulses

→ after 99 pulses $\Rightarrow (99-4)\%8$

$\Rightarrow 95\%8$

$8)95\ (11$

8

15

8

7 → answer (111)

Count = 7 after 99 pulses

→ after 256 pulses $\Rightarrow (256-4)\%8$

$8)252\ (31$

24

12

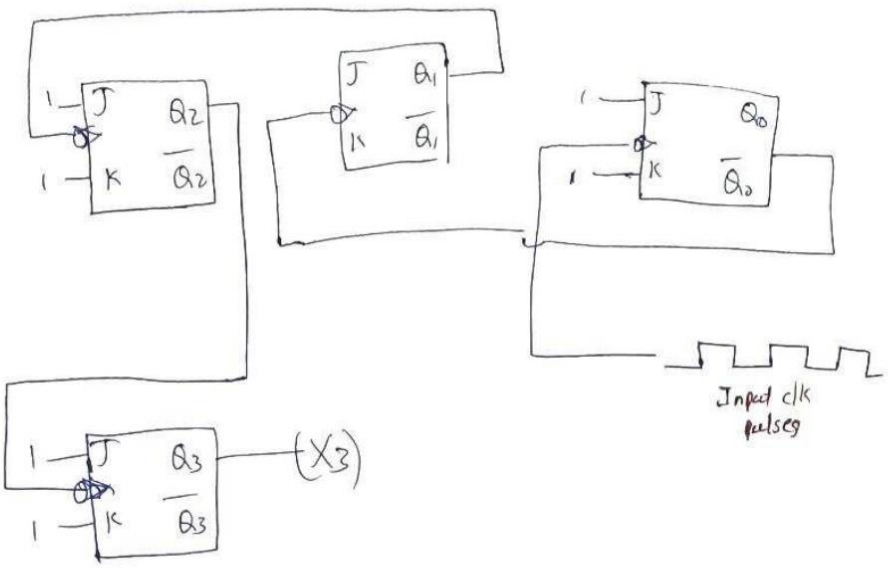
8

4 → answer (100)

Count = 4 after 256 pulses

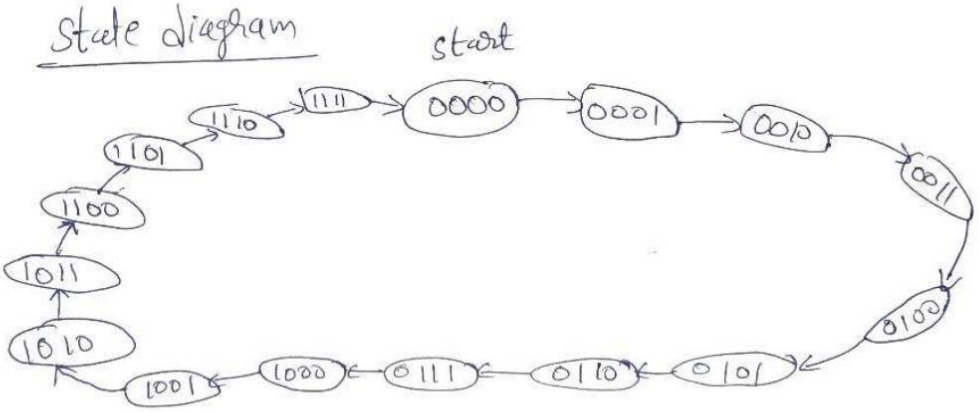
c)

(c)



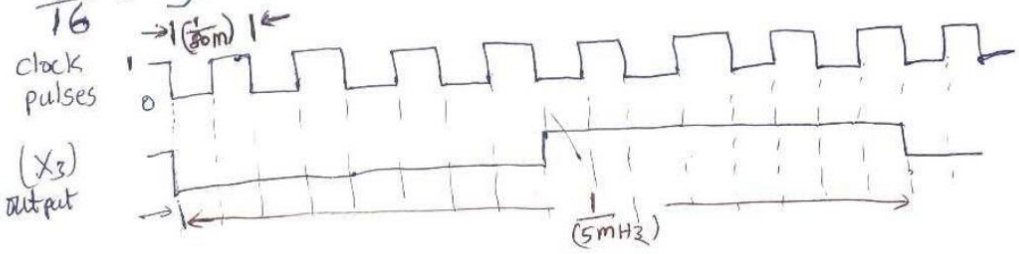
After connecting 4th JK flipflop the circuit becomes MOD 2^4 counter ⇒ MOD 16 Counter.

State diagram

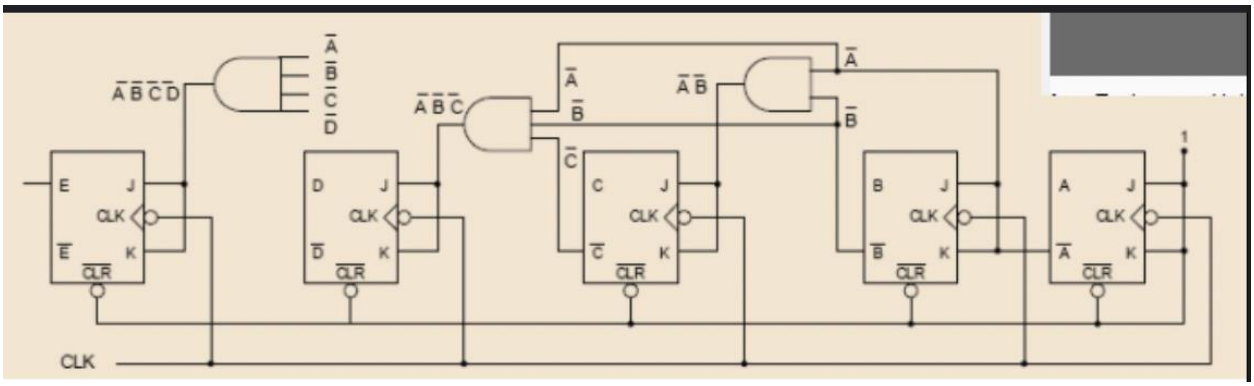


If input frequecy is 80mHz the (X_3) frequency is

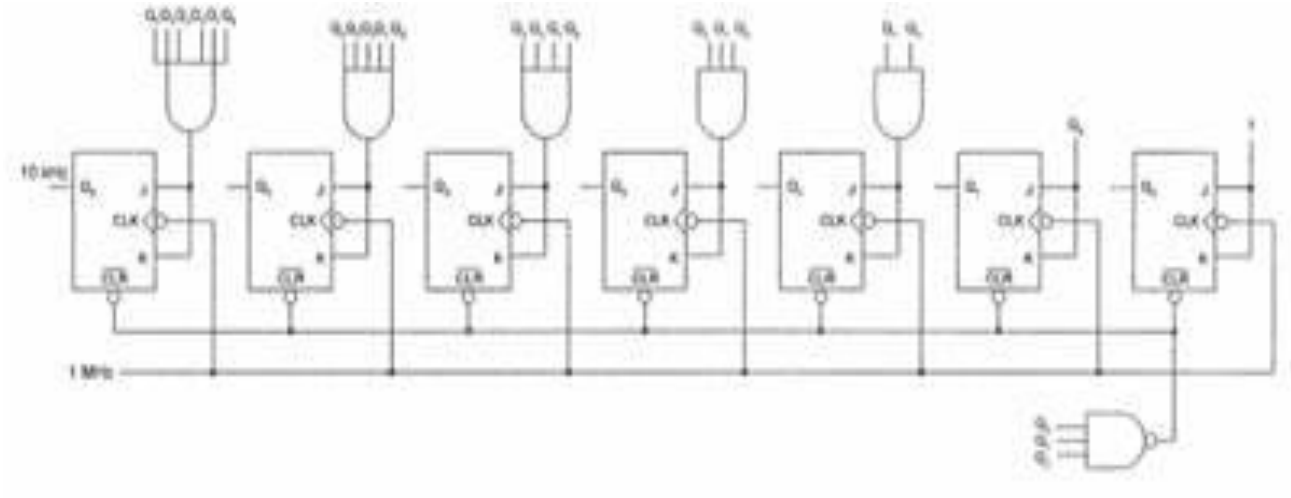
$\frac{80}{16} = 5$ mHz.



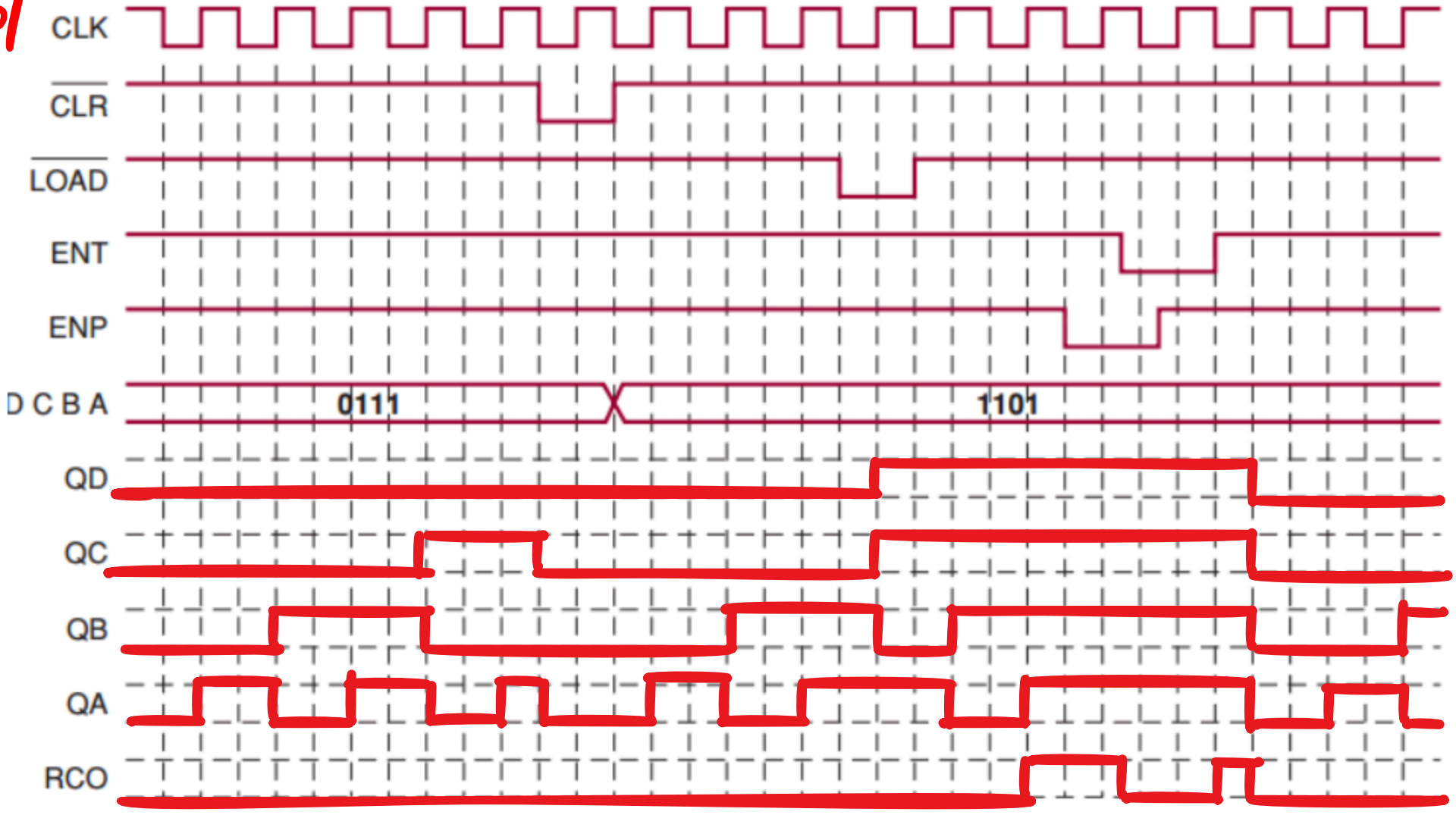
4)


$\overline{A}\,\overline{B}\,\overline{C}\,\overline{D}$
$\overline{A}\,\overline{B}\,\overline{C}$
$\overline{A}\,\overline{B}$
$\overline{A}$
$\overline{B}$
$\overline{C}$
$\overline{D}$
E
D
C
B
A
J
K
CLK
CLR
1
CLK

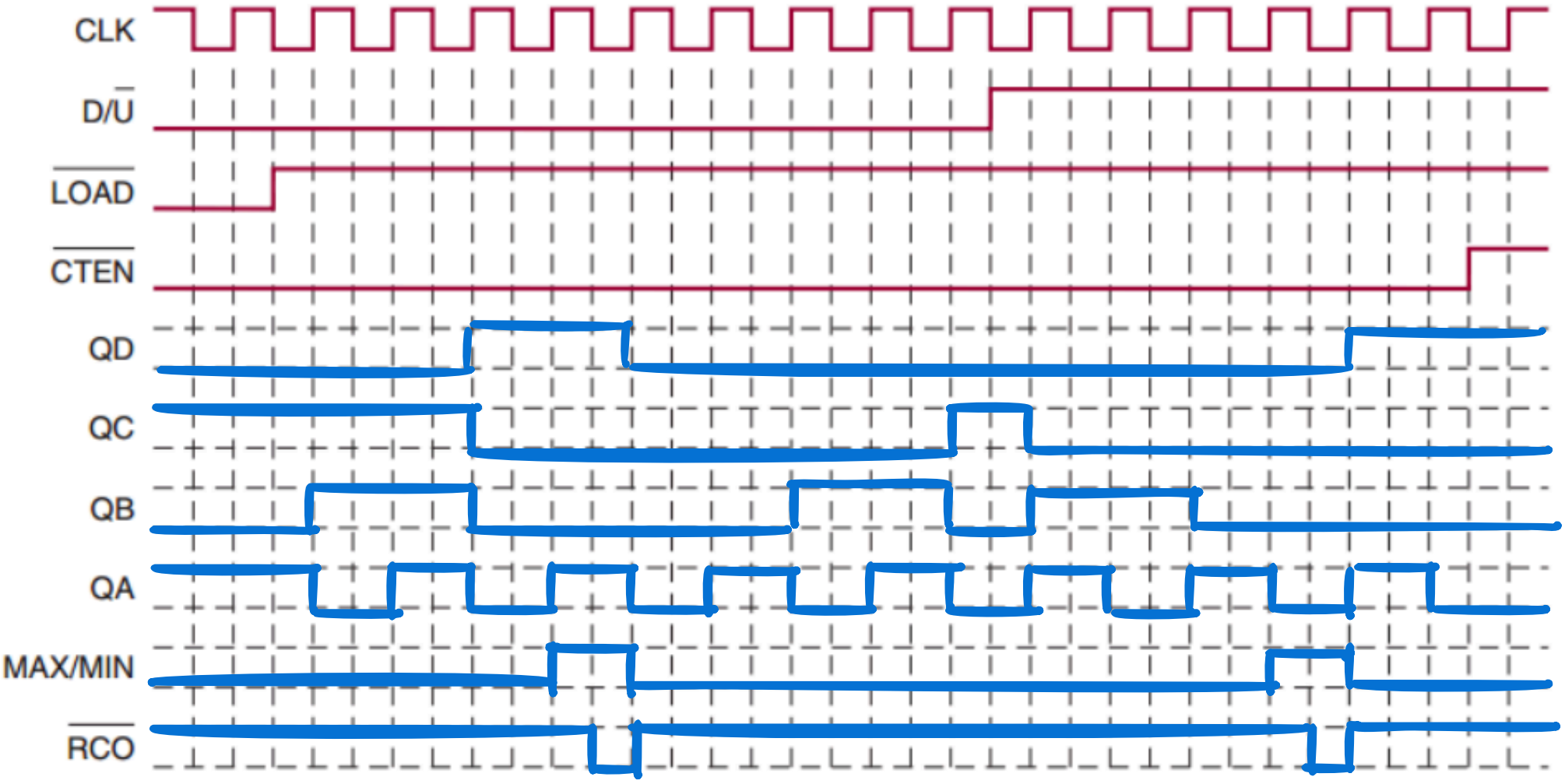
5)


10 MHz
1 MHz
CLK
CLR

6/

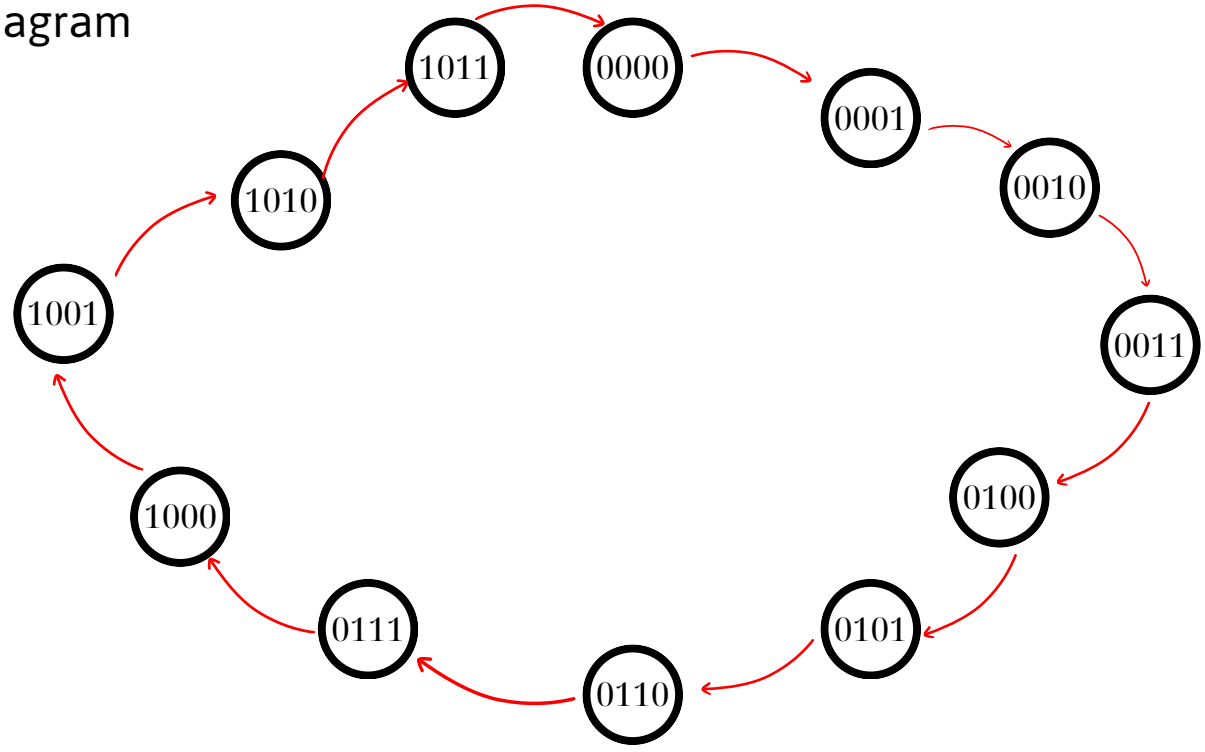


7. Complete the timing diagram in the following figure for a 74ALS190 with the indicated input waveforms applied. The DCBA input is 0101



8.

a) State Transition diagram



b)

From the STD, the counter gate goes through 12 distinct states

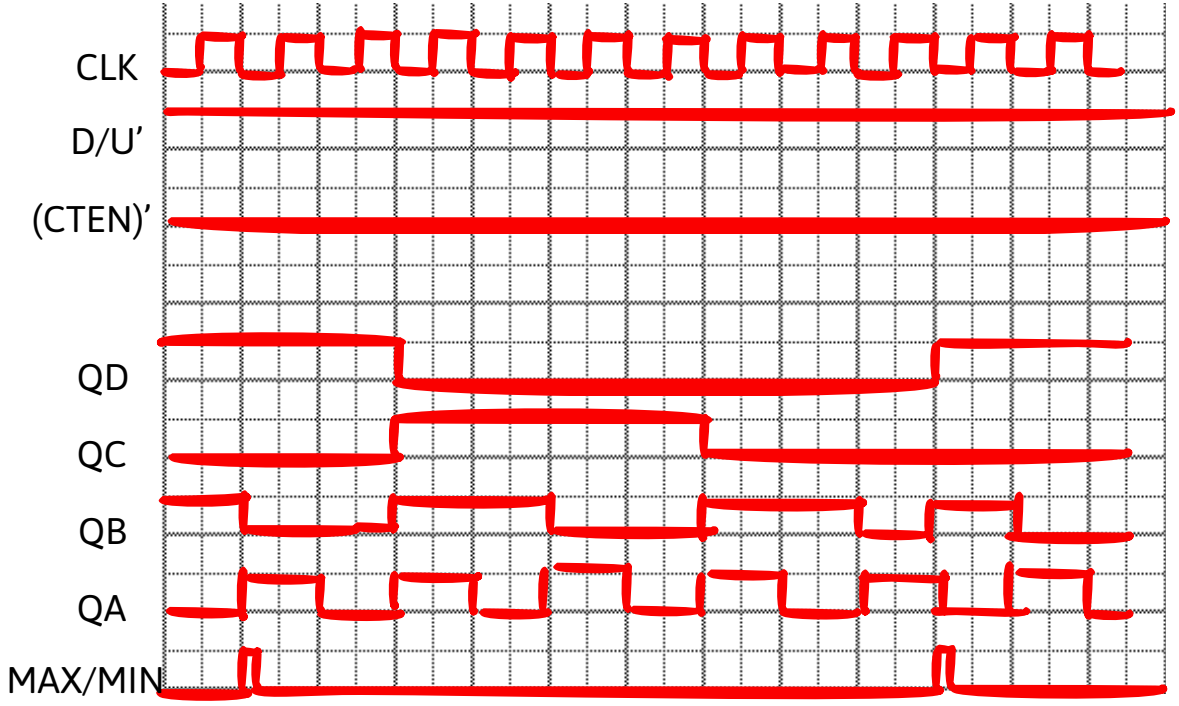
the IC counter circuit works as MOD-12

c)

frequency at QD (MSB) is 1/12 of CLK frequency

9.

a) Timing diagram for outputs QD QC QB QA



b) the counter gate goes through 10 distinct states (1010 to 0001). It does not go to 0000 because LOAD goes LOW after few nanoseconds. So, the IC counter circuit works as MOD-10

c)

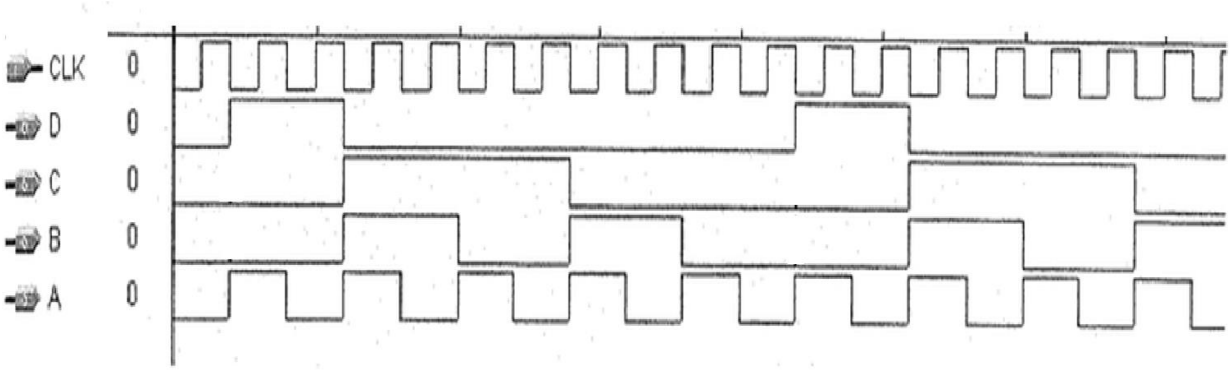
1010 --> 1001--> 1000 --> 0111-->0110 --> 0101 -->0100 --> 0011--> 0010 --> 0001 (10 to 1)

So, DOWN counter

d)

Can produce same modulus counters (MOD-10) but cannot produce the same counting sequence (while the 74HC190 counting upward, the 74HC191 counting downward)

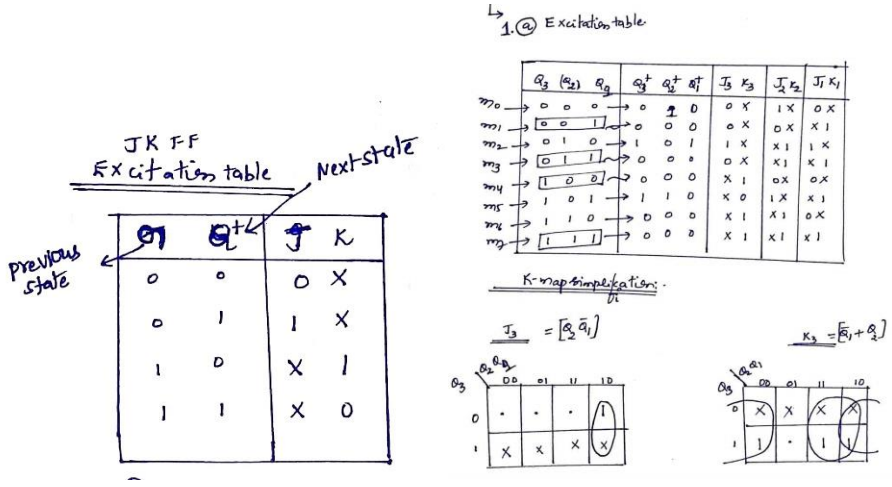
10. Analyze the synchronous counter in the following figure. Draw its timing diagram and determine the counter's modulus.

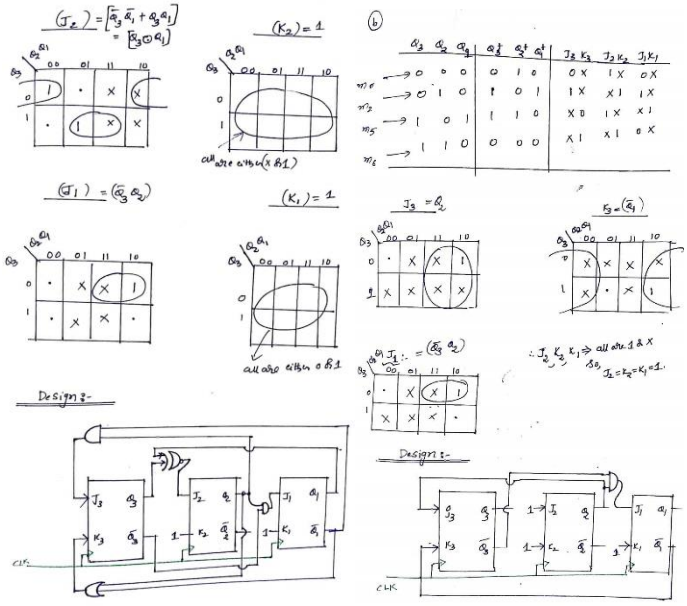


11. Design a synchronous counter:

a. Design a synchronous counter using J-K FFs that has the following sequence: 000, 010, 101, 110, and repeat. The undesired (unused) states 001, 011, 100, and 111 must always go to 000 on the next clock pulse.

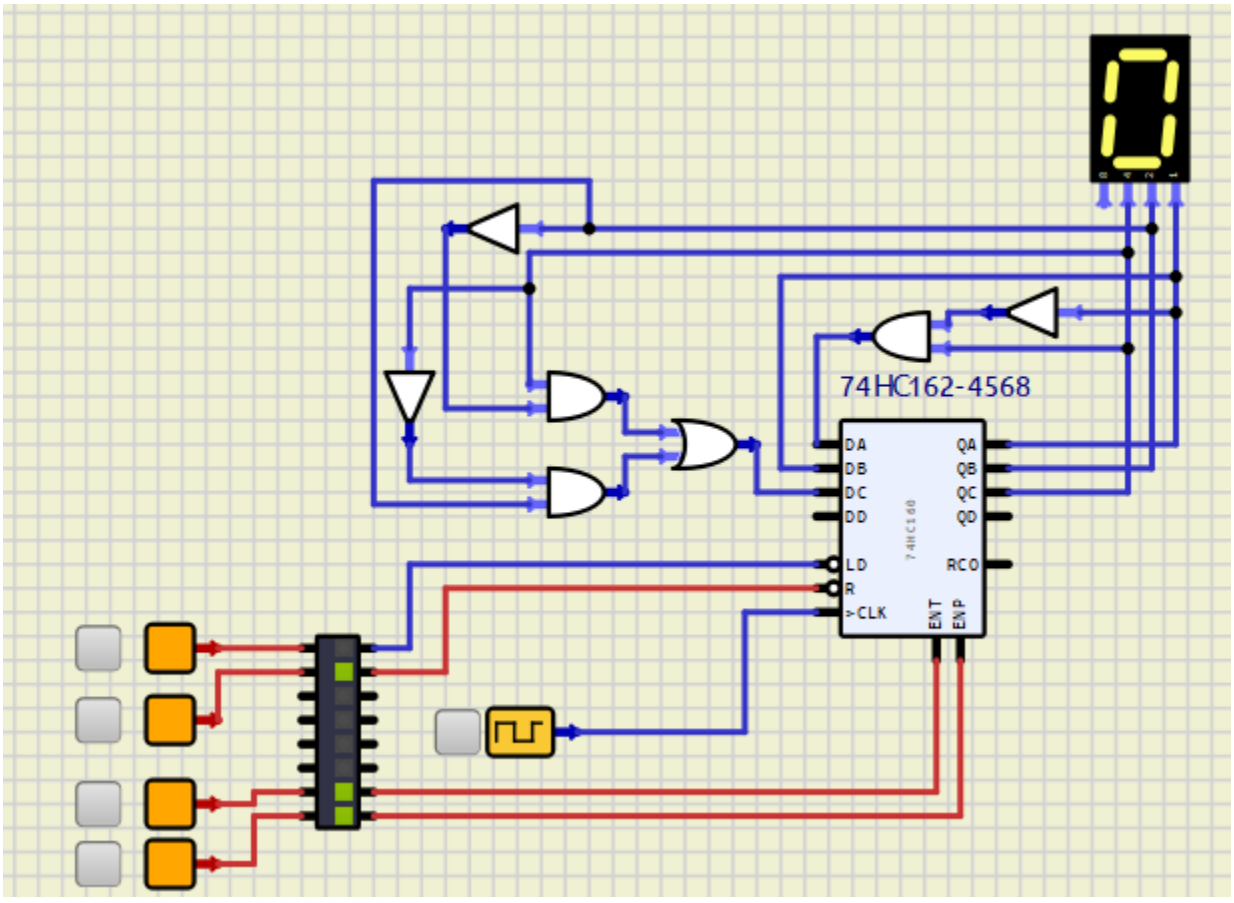
b. Redesign the counter of part (a) without any requirement on the unused states; that is, their NEXT states can be don't cares. Compare with the design from (a).



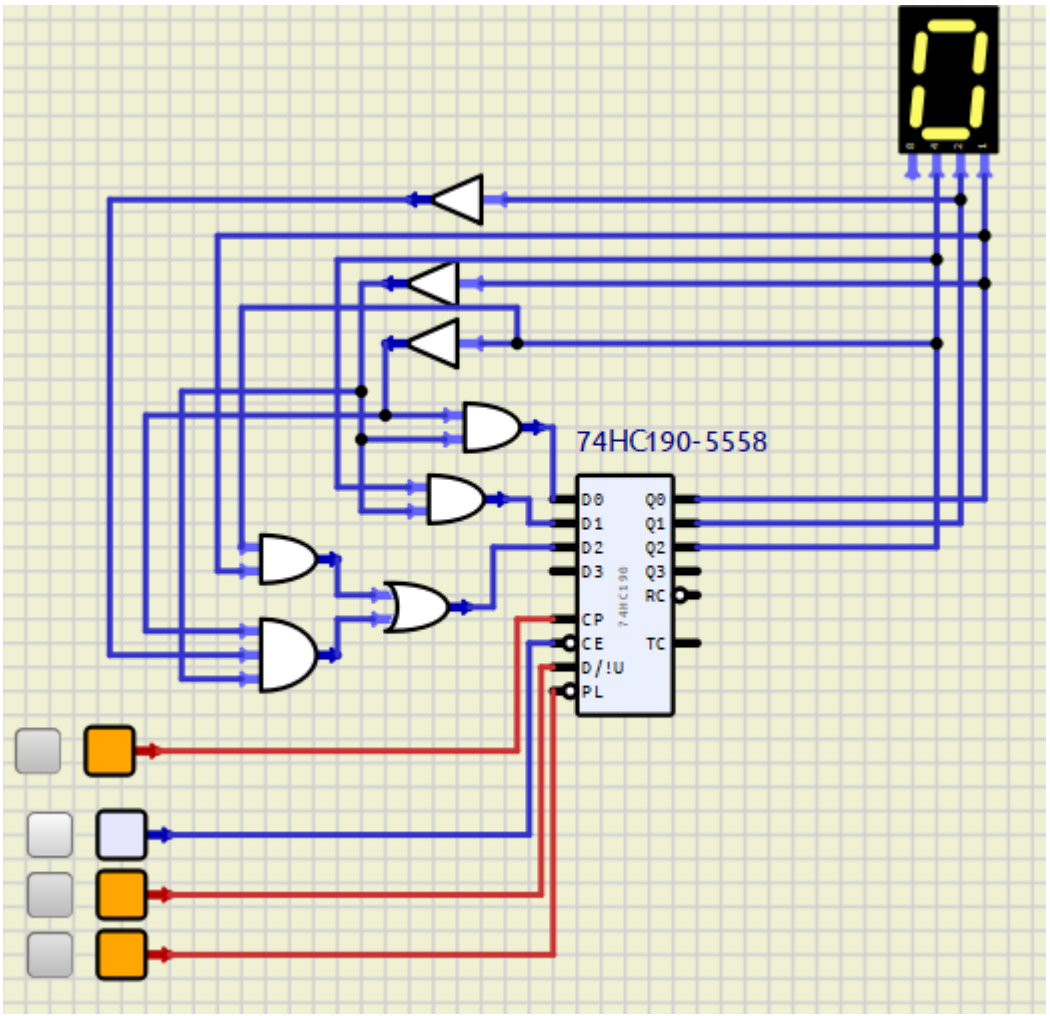


12. Draw a schematic to create a recycling, MOD-5 counter that produces the count sequence:

a. 1, 2, 4, 5, 6, and repeats with a 74ALS162



b. 5, 4, 2, 1, 0, and repeats with a 74ALS190



13. Design a MOD-100, BCD counter using either two 74HC160 or two 74HC162 chips and any necessary gates. The IC counter chips are to be synchronously cascaded together to produce the BCD count sequence for 0 to 99. The MOD-100 is to have two control inputs, an active-HIGH count enable (EN) and an active-HIGH, synchronous load (LD). Label the counter outputs Q0, Q1, Q2, etc., with Q0 = LSB. Which set of outputs represents the 10s digit?

74ALS160 or 74ALS162 is a decade counter (MOD-10) which counts from 0000 to 1001. Counter ICs can be cascaded together to produce a counter of higher counting range. A MOD-100 BCD counter can be designed using counters ICs.

A MOD-100 counter is designed using two 74HC160. It is mentioned that the control inputs to this counter are active-HIGH enable (EN) and an active HIGH synchronous load (LD).