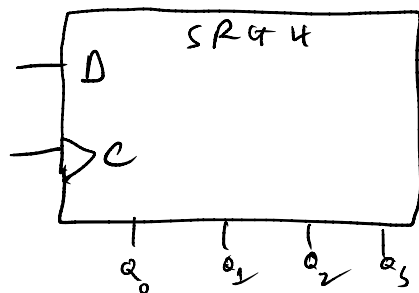
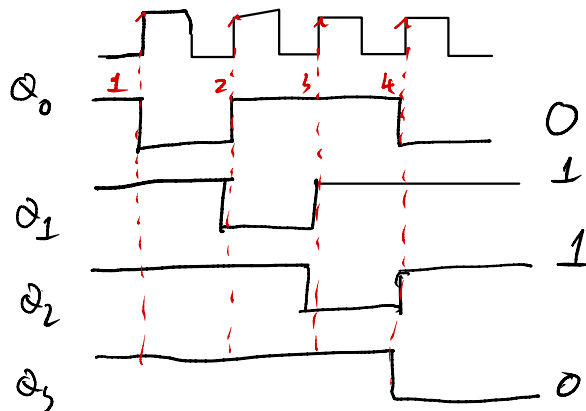


• Serial (SISO Mode):

↳ One bit at a time

+

Data in 0 1 1 0



Initial 1's

3. The bit sequence 1101 is serially entered (least-significant bit first) into a 4-bit parallel out shift register that is initially clear. What are the Q outputs after two clock pulses?

Input		Q_A	Q_B	Q_C	Q_D
1st	1	0	0	0	0
1st	0	→ 1	→ 0	→ 0	→ 0
2nd	1	→ 0	→ 1	→ 0	→ 0
3rd	1	→ 1	→ 0	→ 1	→ 0
4th	-	→ 1	→ 1	→ 0	→ 1

2nd : Q outputs are 0100