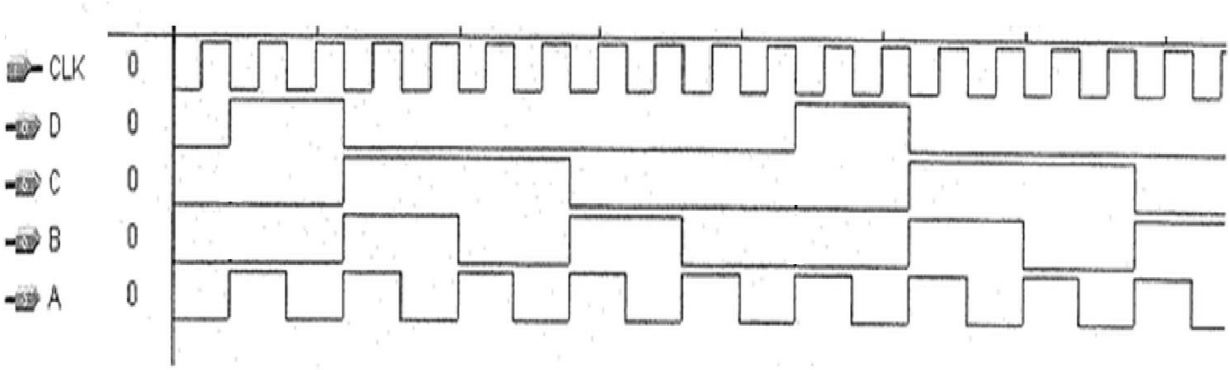
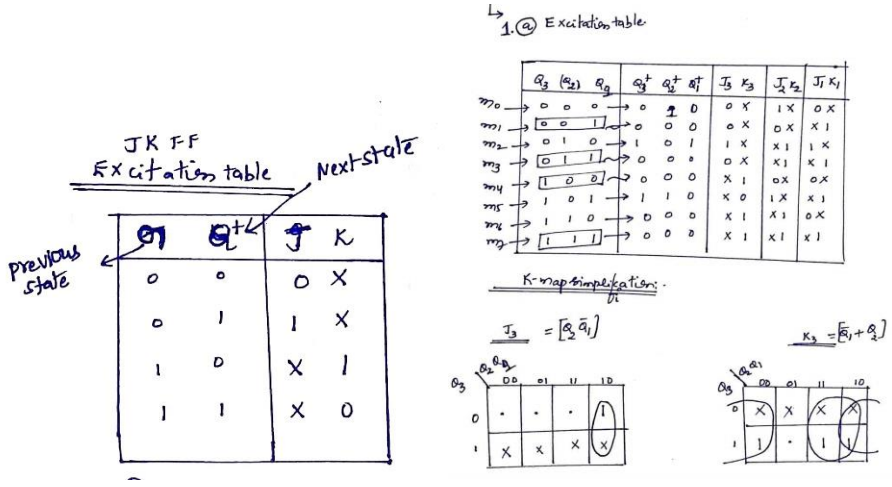
10. Analyze the synchronous counter in the following figure. Draw its timing diagram and determine the counter's modulus.

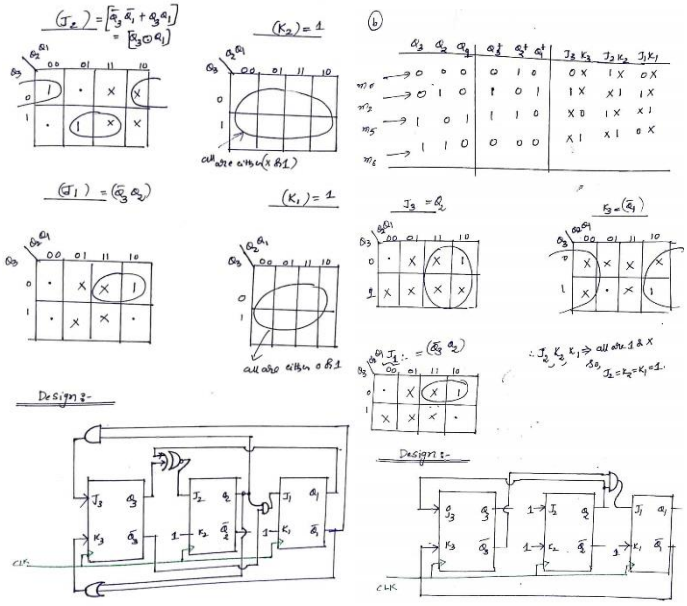


11. Design a synchronous counter:

a. Design a synchronous counter using J-K FFs that has the following sequence: 000, 010, 101, 110, and repeat. The undesired (unused) states 001, 011, 100, and 111 must always go to 000 on the next clock pulse.

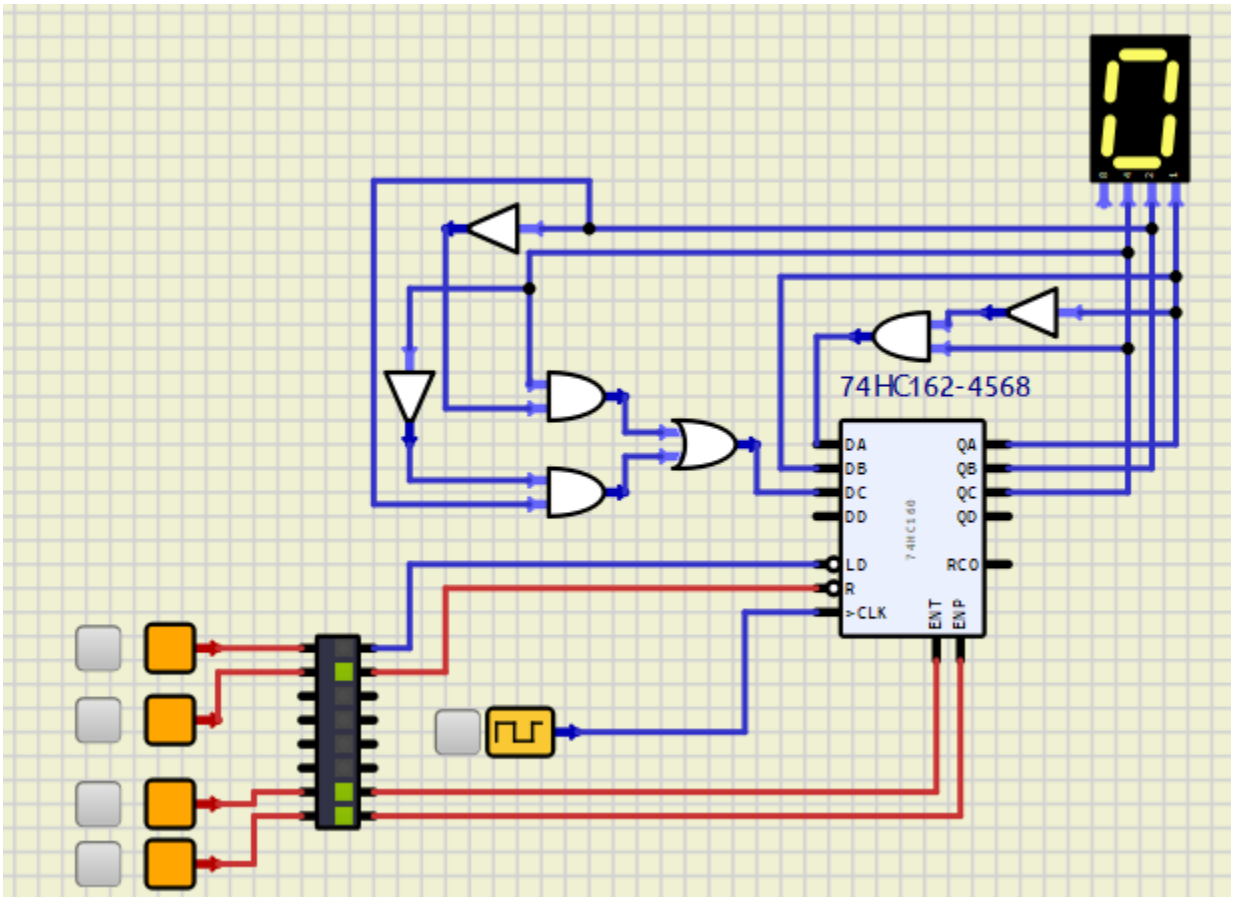
b. Redesign the counter of part (a) without any requirement on the unused states; that is, their NEXT states can be don't cares. Compare with the design from (a).



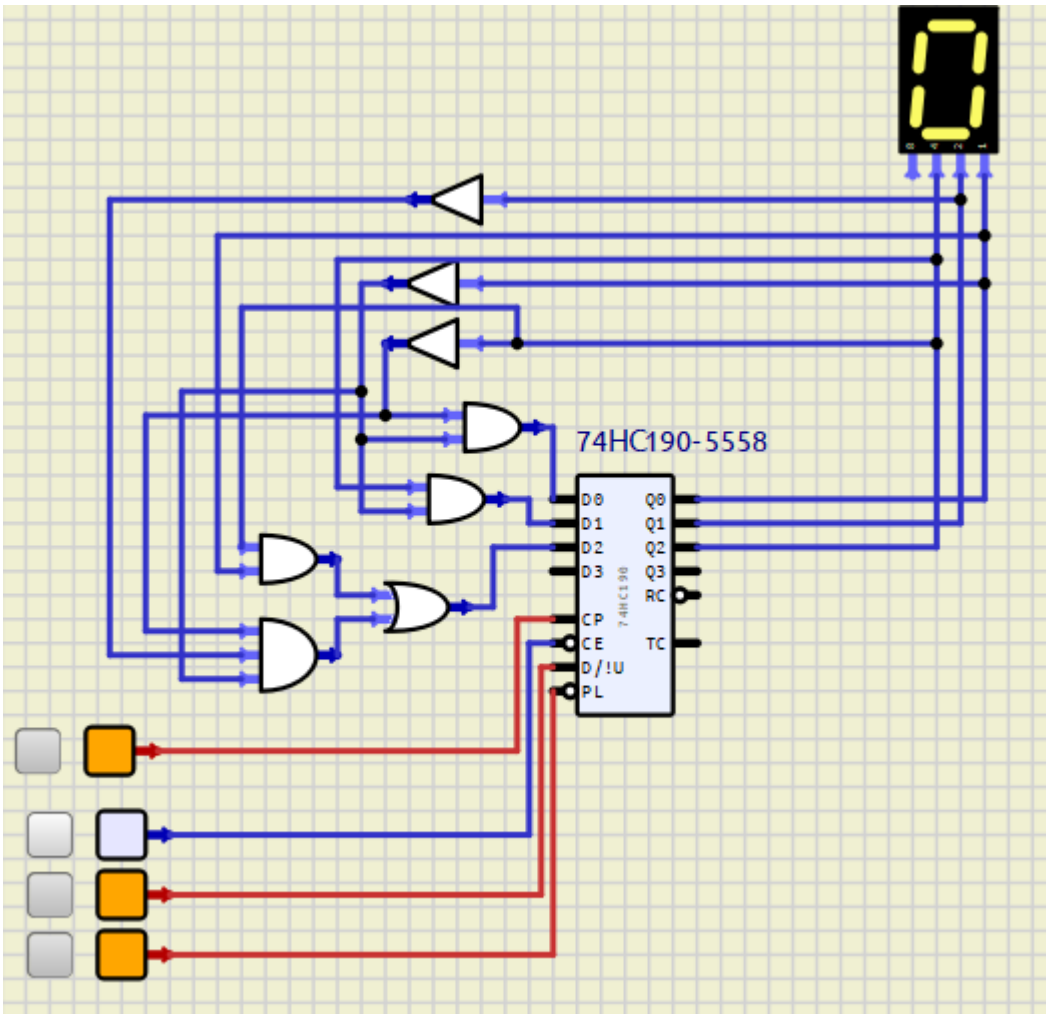


12. Draw a schematic to create a recycling, MOD-5 counter that produces the count sequence:

a. 1, 2, 4, 5, 6, and repeats with a 74ALS162



b. 5, 4, 2, 1, 0, and repeats with a 74ALS190



13. Design a MOD-100, BCD counter using either two 74HC160 or two 74HC162 chips and any necessary gates. The IC counter chips are to be synchronously cascaded together to produce the BCD count sequence for 0 to 99. The MOD-100 is to have two control inputs, an active-HIGH count enable (EN) and an active-HIGH, synchronous load (LD). Label the counter outputs Q0, Q1, Q2, etc., with Q0 = LSB. Which set of outputs represents the 10s digit?

74ALS160 or 74ALS162 is a decade counter (MOD-10) which counts from 0000 to 1001. Counter ICs can be cascaded together to produce a counter of higher counting range. A MOD-100 BCD counter can be designed using counters ICs.

A MOD-100 counter is designed using two 74HC160. It is mentioned that the control inputs to this counter are active-HIGH enable (EN) and an active HIGH synchronous load (LD).