THE INTERNATINONAL UNIVERSITY (IU) – VIETNAM NATIONAL UNIVERSITY – HCMC

MIDTERM EXAMINATION

Date: 12 Nov 2018

Duration: 90 minutes

Subject: Digital Logic Design (EE053IU)	
Approved by Dean of School of Electrical Engineering **Mai Linh, Ph.D.**	Lecturer **Do Ngoc Hung**

READ CAREFULLY THE INSTRUCTIONS:

1. This is a semi-closed exam. Students are allowed to bring a handwritten A4 note.
2. Students are not allowed to leave the room before the exam ends. If you really want to do so, you MUST submit your paper before leaving the room at any time.
3. If there is any point in those questions that is not clear, please make assumptions and state clearly those assumptions in your work.
4. The usage of any electronic devices (electronic calculator, laptop, electronic dictionary, cell phones…) is strictly PROHIBITED.

Question 1. [20 marks]

a) Do the following conversions

i) $(1CF)_{16}$ to decimal number

ii) $(362)_{10}$ to hexadecimal, then binary and octal numbers

iii) $(10010101.1)_2$ to decimal number

iv) $(726)_8$ to decimal number, then BCD code

v) $(-58)_{10}$ to signed binary number using 1's complement form

[10 marks]

b) Perform the following decimal addition in BCD numbers: $1492 + 366 = 1858$

[5 marks]

c) Perform the following decimal subtraction in 2's complement form of signed binary numbers: $36 - 42 = -6$

[5 marks]

Question 2. [20 marks]

Given the following logic diagram

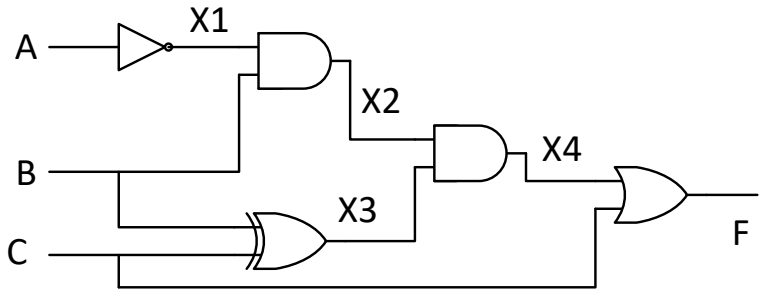

Figure 1. Logic diagram

a) Determine the output expressions of each logic gates X1, X2, X3, X4, and F

[10 marks]

b) Fill the following truth table

A	B	C	X1	X2	X3	X4	F
0	0	0					
0	0	1					
0	1	0					
0	1	1					
1	0	0					
1	0	1					
1	1	0					
1	1	1					

[10 marks]

Question 3. [10 marks]

Given the 3 lines to 8 lines decoder IC as follows:

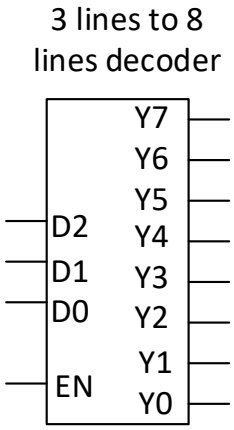

Figure 2. Decoder

a) Fill the following truth table

D2	D1	D0	EN	Y7	Y6	Y5	Y4	Y3	Y2	Y1	Y0
X	X	X	0								
0	0	0	1								
0	0	1	1								
0	1	0	1								
0	1	1	1								
1	0	0	1								
1	0	1	1								
1	1	0	1								
1	1	1	1								

[5 marks]

b) Use this decoder and NAND gates to implement function $f(C,B,A)=\sum(1,2,6)$

[5 marks]

Question 4. [20 marks]

A jet aircraft employs a system for monitoring the speed (S), pressure (P), and temperature (T) values of its engines using sensors that operate as follows:

S sensor output = 0 only when $S \le S_T$ (rpm)

P sensor output = 0 only when $P \le P_T$ (psi)

T sensor output = 0 only when $T \le T_T$ (°F).

Assume that a HIGH at output W activates the alarm.

a) Design the logic circuit with these three sensor outputs as inputs so that the alarm will be activated whenever either of the following conditions exists:

- $S > S_T$ and $P > P_T$
- $S > S_T$ and $T > T_T$

[5 marks]

b) Sketch the designed circuit diagram in a) by using only NAND gates

[5 marks]

c) Sketch the designed circuit diagram in a) by using only NOR gates

[5 marks]

d) Compare the number of ICs that we need to use to implement the above designed circuits.

[5 marks]

Question 5. [30 marks]

Given the following expressions:

$$F_1(A,B,C) = \prod(0,1,2,4,6)$$
$$F_2(A,B,C,D) = \sum(1,3,5,7,10,11,12,14)$$

a) Use K-map to simplify the expressions F_1, F_2

[10 marks]

b) Sketch the logic circuit diagrams using logic gates

[10 marks]

c) Given the following input waveforms

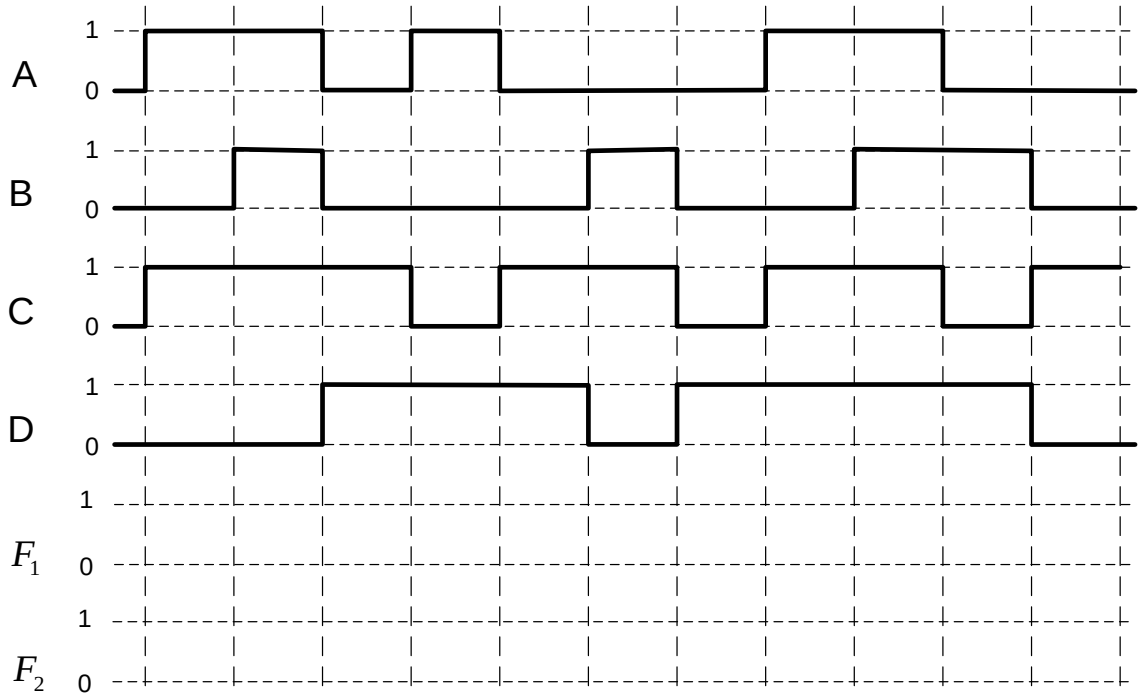

Figure 3. Input waveforms

Based on the results in part a), sketch the output waveforms for functions F_1, F_2

[10 marks]