PRINCIPLES OF EE1 LAB

Lab 6

Circuits utilizing Op-Amps

Full name: ……

Student number: ……

Class: ……....

Date: ……

I. Objectives

- To demonstrate the operation of Op-Amps when connected to capacitive elements
- To familiarize the user with the simple integrator and differentiator
- To further demonstrate how powerful Op-Amp circuits can be for the performance of several operations

II. Introduction

This experiment is designed to demonstrate the operation of Op-Amps with capacitive elements in the feedback loop or in the input circuit. The results for the simple integrator and differentiator are presented in section 2. There are no prelab exercises assigned other than familiarization with the concepts.

The four actual laboratory experiments are designed to verify the performed operation by direct measurement of voltages, currents and resistances and by observation and downloading of the input and output waveforms. The introduction of phase shifts is also explored.

III. Theory

3.1 The Op-Amp

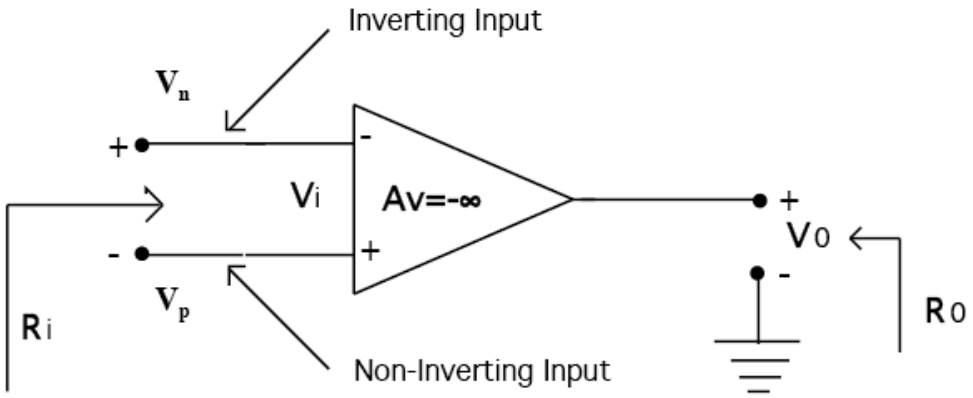

Fig.1: The Op-amp

Characteristics of an Ideal Op Amp

1. Input Resistance $R_i = \infty$: An infinite input resistance means that no current flows into or out of either of the input terminals. This greatly simplifies the analysis of Op-Amp circuits.

2. Output Resistance $R_o = 0$: In this case the output voltage V_o is independent of the output current

3. Open Loop Voltage Gain $\mu = A_V = \pm\infty$:

In order to predict the behavior of an operational amplifier when circuit elements are externally connected to its terminals, one must understand the constraints imposed on the terminal voltages and currents by the amplifier itself. Those imposed on the terminal voltages are as follows :

$$V_0 = A_v\left(V_p - V_n\right) \tag{1}$$

and

$$-V_{cc} \approx V^- \le V_o \le V^+ \approx V_{cc} \tag{2}$$

Eq. 1 states that the output voltage is proportional to the difference between V_p and V_n.

If the output voltage V_o is to be finite it follows from the definition of voltage gain, that $V_i = V_o / A_v$ will go to zero when A_v is infinite. This, however, assumes that there is some way for the input to be affected by the output. Indeed this will only happen if there is *negative feedback* in the form of *a connection between the output and the inverting terminal* (closed loop operation). For closed loop operation, it is said that a *virtual short* exists between the inverting and noninverting input terminals. This means that if an Op-Amp is operating in its linear region (if it is *unsaturated*) then $V_i = 0$, or equivalently $V_n = V_p$. Thus V_p and V_n can be represented by a single variable. When one of the two terminals is grounded, then the voltage at both terminals is zero and the other terminal is called a *virtual ground*.

Eq. 2 states that the output voltage is bounded. In particular, V_o must lie between $\pm V_{CC}$, the power supply voltages. Else V_o will be at either limiting value, and the Op-Amp is then saturated. The amplifier is operating in its linear range so long as $V_o < |V_{CC}|$.

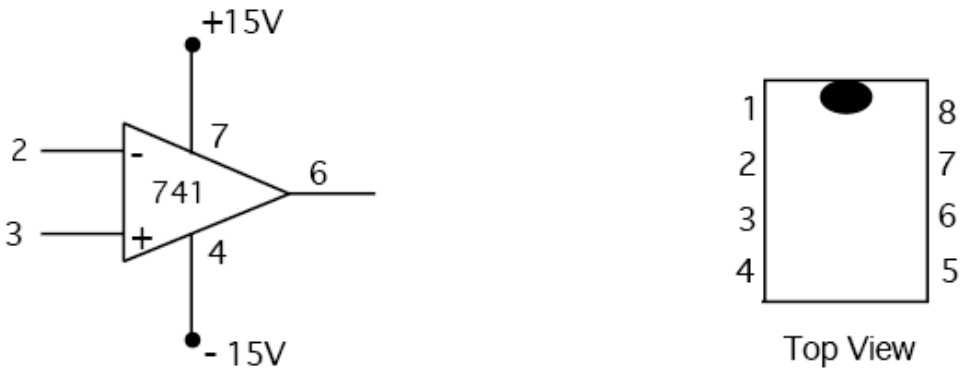

Fig.2. 741 op-amp

The chip layout is shown in Fig. 2. The standard procedure on a DIP is to identify pin 1 with the notch in the end of the chip package. The notch always separates pin 1 from the last pin on the chip. In the case of 741, the notch is between pins 1 and 8. Pins 2, 3, and 6 are the inverting input V_n, the non-inverting input V_p, and the amplifier output V_o respectively. These three pins are the three terminals that normally appear in an op-amp circuit schematic diagram. The null offset pins (1 and 5) provide a way to eliminate any offset in the output voltage of the amplifier. The offset voltage is an artifact of the integrated circuit. The offset voltage is additive with pin V_o (pin 6 in this case), can be either positive or negative and is

normally less than 10 mV. Because of its small magnitude, in most cases, one can ignore the contribution of the offset voltage to V_o and leave the null offset pins open.

A simple VCVS model of a practical Op-Amp is shown in Fig 2a. In this model, R_{in} represents the input resistance of the Op-Amp and μ the (open loop – open circuit) gain. The nominal values of $R_{in} = 10^{10}\ \Omega$ and $\mu = 10^6$ are often used to approximate an ideal device.

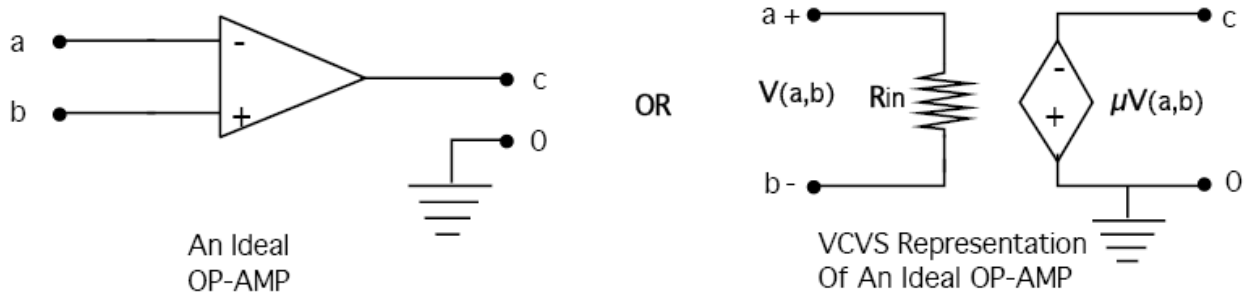

Fig2a. VCVS representation of an ideal Op-amp

The Op-Amp can be simulated in PSpice by its simple VCVS equivalent circuit of Fig. 2a.

3.2 Integrating Amplifier

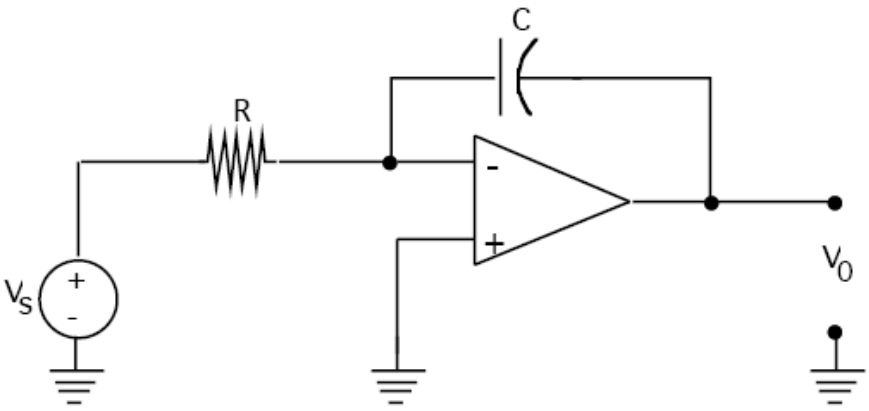

Fig.3. Integrating Amplifier

The analysis of the integrating amplifier shown in Fig. 3 gives:

$$V_o = -\frac{1}{RC}\int_0^t V_s(t)\,dt \qquad (3)$$

That is, the circuit performs integration of the input signal.

3.3 Differentiating Amplifier

The analysis of differentiating amplifier shown in Fig. 4 gives:

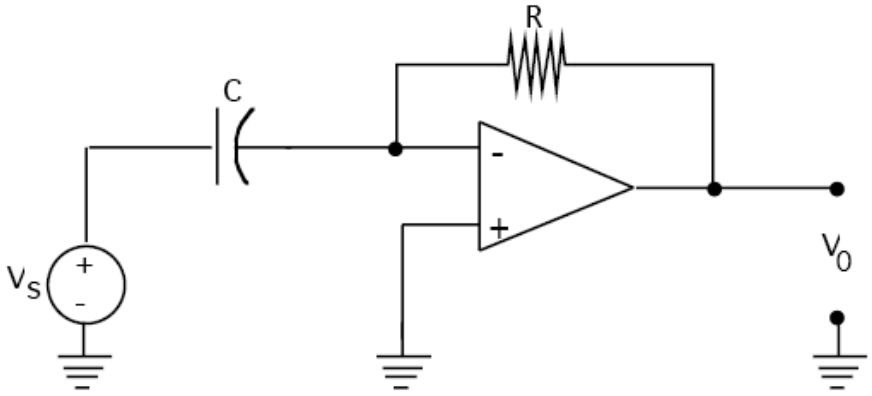

Fig. 4 Differentiating Amplifier

$$V_o(t) = -RC\frac{dV_s(t)}{dt} \tag{4}$$

That is, the circuit differentiates the input signal.

IV. Pre-Laboratory

Derive the equation (3) and equation (4).

Using Pspice to simulate circuits

V. Laboratory

Required equipment:

Electronic board with Power Supply

Digital Multimeter

Function Generator

Counter-Timer

741 Operational Amplifier

Oscilloscope

620 Ω, 1 KΩ, 2:10 KΩ, 20 KΩ, 52 KΩ, 100 KΩ Resistors

0.001 μF, 0.01 μF, 0.1 μF, 1 μF Capacitors

5.1 Integrating Amplifier

5.1.1 Build the circuit shown in Fig. 3. Use R = 680 Ω and C=0.1 μF.

5.1.2 With V_s a sinusoidal input of amplitude 2V and frequency f = 1KHz, display the waveforms V_o and V_s on the screen of the oscilloscope.

5.1.3 Measure the phase angle between V_o and V_s, and redraw both waveforms into your report.

5.1.4 Repeat with V_s a square waveform and redraw into report all input and output waveforms from the oscilloscope.

5.1.5 Repeat with V_s a triangular waveform and redraw into report all input and output waveforms from the oscilloscope.

5.2 Differentiating Amplifier

5.2.1 Build the circuit shown in Fig. 4. Use R = 680 Ω and C = 0.1 μF.

5.2.2 With V_s a sinusoidal input of amplitude 2V and frequency f = 1KHz, display the waveforms V_o and V_s on the screen of the oscilloscope.

5.2.3 Measure the phase angle between V_o and V_s, and redraw both waveforms on your report.

5.2.4 Repeat with V_s a square waveform and copy all input and output waveforms from the oscilloscope.

5.2.5 Repeat with V_s a triangular waveform and copy all input and output waveforms from the oscilloscope.

5.3 Circuit #1

In the circuit of Fig. 5, R1 = 22KΩ, R2 = 100KΩ, R3 = 10KΩ, R4 = 56KΩ, and C = 1nF. With V_{CC} = +15 V, and an input Vg = 1 cos(20,000 t) (V), build the circuit and display the waveforms of output voltage V_o and input voltage V_g on the scope. Draw the waveforms into your report.

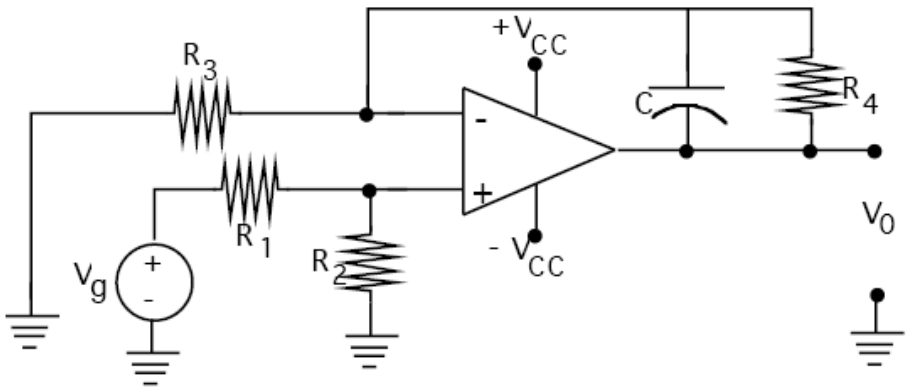

Fig.5. Circuit #1

• Measure the magnitude and phase of the output.

• Plot the images for your report.

• How large can the amplitude of Vg be before the amplifier saturates?

5.4 Circuit #2

In the circuit of Fig. 6, R1 = 10KΩ, R2 = 1KΩ, R3 = 10KΩ, C1 = 1nF, and C2 =0.01μF. With V_{CC} = +15 V and the sinusoidal input Vg = 5 cos(10^5 t) V, build the circuit, display the waveforms of output voltage V_o and input voltage Vg on the scope, and copy them for your report. Measure the magnitude and the phase of the output.

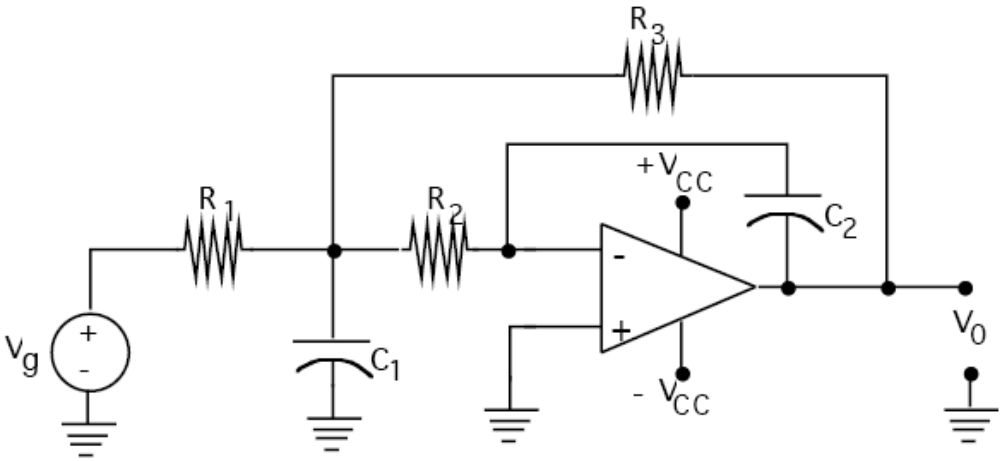

Fig.6. Circuit #2

VI. Report

6.1 Derive Eqs. 3 & 4.

6.2 From 6.1 above, determine the theoretical magnitude and phase of the circuits in Sections 5.1 and 5.2.

6.3 What are the output waveforms for the integrator and the differentiator circuits of Sections 5.1 and 5.2 for the three different input waveforms? Tabulate your results.

6.4 Assuming that the Op-Amp in Fig. 5 is ideal,

a) Find the steady state expression of Vo(t) if Vg = 1 cos(20,000 t) V.

b) How large can the amplitude of Vg be before the amplifier saturates?

6.5 The Op-Amp in the circuit of Fig. 6 is ideal. Find the steady state expression for Vo(t) when Vg = 5 cos(105 t) V.

6.6 The Op-Amp in the circuit of Fig. 6 is ideal. If Vg = 1 cos(1000 t) V,

a) Find the values of R2 that will make *Vo* lag *Vg* by 63 degrees.

b) For the value of R2 found in part (a), write the steady state expression for *Vo*(*t*).

6.7 Tabulate the theoretical and the experimental values of the magnitudes and the phases of the outputs of the circuits in Sections 5.1, 5.2, 5.3, and 5.4. Compare the experimental values with the theoretical ones.

6.8 Submit all copies of the waveforms.

6.9 Simulate, in PSpice, the circuit of Fig. 4 to find the magnitude and the phase of the output voltage Vo(t), for input voltage Vs(t) of all 3 waveform types. Compare your results with the experimental ones. Repeat the same for the circuits in Fig. 5 and Fig. 6. Tabulate your results.