Vietnam National University HCMC

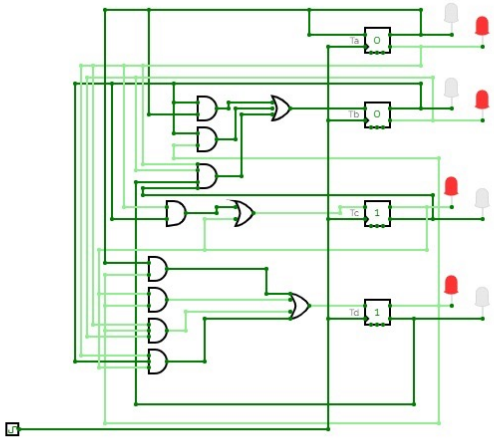
International University

School of Electrical Engineering

EE053IU

Digital Logic Design

Lecture 3: Logic Gates



INSTRUCTOR: Dr. Vuong Quoc Bao

Chapter Objectives

- Describe the operation of the inverter, the AND gate, and the OR gate
- Describe the operation of the NAND gate and the NOR gate
- Express the operation of NOT, AND, OR, NAND, and NOR gates with Boolean algebra
- Describe the operation of the exclusive-OR and exclusive-NOR gates
- Use logic gates in simple applications
- Recognize and use both the distinctive shape logic gate symbols and the rectangular outline logic gate symbols of ANSI/IEEE Standard 91-1984/Std. 91a-1991
- Construct timing diagrams showing the proper time relationships of inputs and outputs for the various logic gates

Chapter Objectives

- Discuss the basic concepts of programmable logic
- Make basic comparisons between the major IC technologies—CMOS and bipolar (TTL)
- Explain how the different series within the CMOS and bipolar (TTL) families differ from each other
- Define propagation delay time, power dissipation, speed-power product, and fan-out in relation to logic gates
- List specific fixed-function integrated circuit devices that contain the various logic gates

I. The Inverter

- The inverter (NOT circuit) performs the operation called inversion or complementation.
- The inverter changes one logic level to the opposite level. In terms of bits, it changes a 1 to a 0 and a 0 to a 1.

(a) Distinctive shape symbols with negation indicators

(b) Rectangular outline symbols with polarity indicators

FIGURE 3–1 Standard logic symbols for the inverter (ANSI/IEEE Std. 91-1984/ Std. 91a-1991).

EXAMPLE 2–1

Express the decimal number 47 as a sum of the values of each digit.

Solution

The digit 4 has a weight of 10, which is 10^1, as indicated by its position. The digit 7 has a weight of 1, which is 10^0, as indicated by its position.

$$\begin{aligned} 47 &= (4 \times 10^1) + (7 \times 10^0) \\ &= (4 \times 10) + (7 \times 1) = \mathbf{40 + 7} \end{aligned}$$

Related Problem*

Determine the value of each digit in 939.

EXAMPLE 2–2

Express the decimal number 568.23 as a sum of the values of each digit.

Solution

The whole number digit 5 has a weight of 100, which is 10^2, the digit 6 has a weight of 10, which is 10^1, the digit 8 has a weight of 1, which is 10^0, the fractional digit 2 has a weight of 0.1, which is 10^{-1}, and the fractional digit 3 has a weight of 0.01, which is 10^{-2}.

$$\begin{aligned} 568.23 &= (5 \times 10^2) + (6 \times 10^1) + (8 \times 10^0) + (2 \times 10^{-1}) + (3 \times 10^{-2}) \\ &= (5 \times 100) + (6 \times 10) + (8 \times 1) + (2 \times 0.1) + (3 \times 0.01) \\ &= \mathbf{500 + 60 + 8 + 0.2 + 0.03} \end{aligned}$$

Related Problem

Determine the value of each digit in 67.924.

Inverter Truth Table

- When a HIGH level is applied to an inverter input, a LOW level will appear on its output.
- When a LOW level is applied to its input, a HIGH will appear on its output.

Inverter Operation

- When the input is LOW, the output is HIGH; when the input is HIGH, the output is LOW, thereby producing an inverted output pulse.

TABLE 3–1

Inverter truth table.

Input	Output
LOW (0)	HIGH (1)
HIGH (1)	LOW (0)

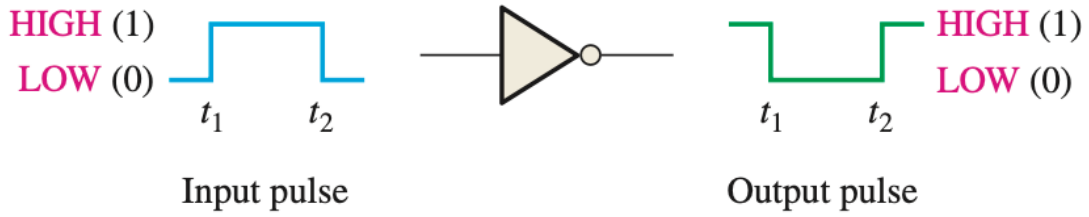


FIGURE 3–2 Inverter operation with a pulse input. Open file F03-02 to verify inverter operation. *A Multisim tutorial is available on the website.*

Timing Diagrams

- A timing diagram shows how two or more waveforms relate in time.

EXAMPLE 3–1

A waveform is applied to an inverter in Figure 3–4. Determine the output waveform corresponding to the input and show the timing diagram. According to the placement of the bubble, what is the active output state?

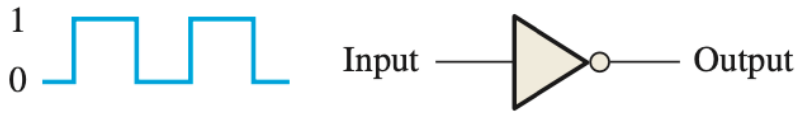


FIGURE 3–4

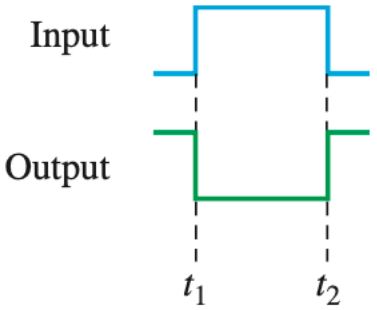


FIGURE 3–3 Timing diagram for the case in Figure 3–2.

Solution

The output waveform is exactly opposite to the input (inverted), as shown in Figure 3–5, which is the basic timing diagram. The active or asserted output state is **0**.

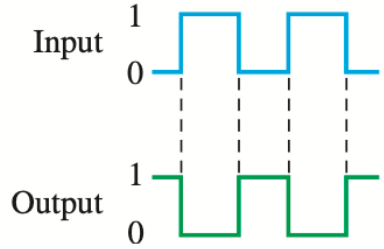


FIGURE 3–5

Logic Expression for an Inverter

- Boolean algebra uses variables and operators to describe a logic circuit.
- The operation of an inverter (NOT circuit) can be expressed as follows: If the input variable is called A and the output variable is called X, then $X = \overline{A}$

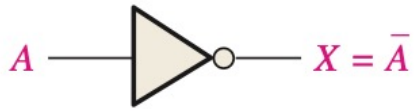


FIGURE 3–6 The inverter complements an input variable.

An Application

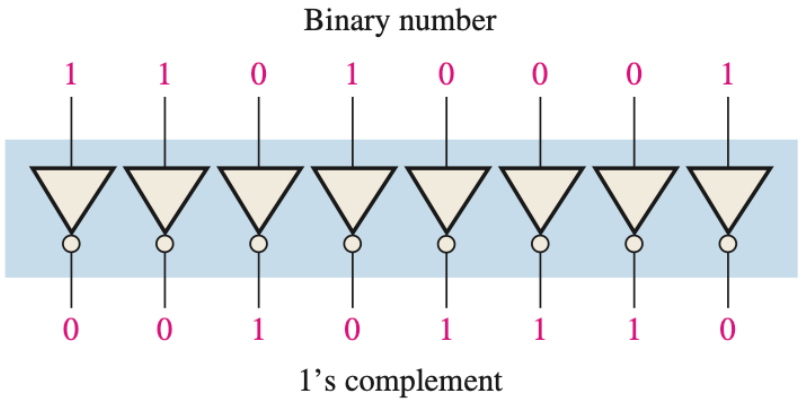
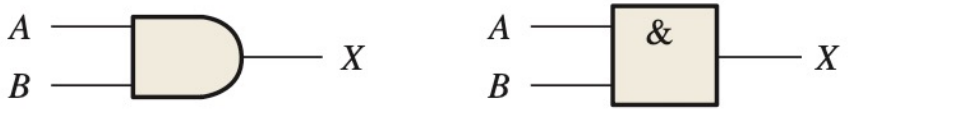


FIGURE 3–7 Example of a 1's complement circuit using inverters.

II. The AND Gate

- The AND gate is one of the basic gates that can be combined to form any logic function.
- An AND gate can have two or more inputs and performs what is known as logical multiplication.



(a) Distinctive shape

(b) Rectangular outline with the AND (&) qualifying symbol

FIGURE 3–8 Standard logic symbols for the AND gate showing two inputs (ANSI/IEEE Std. 91-1984/Std. 91a-1991).

Operation of an AND Gate

- An AND gate produces a HIGH output only when all of the inputs are HIGH. When any of the inputs is LOW, the output is LOW.
- For a 2-input AND gate, output X is HIGH only when inputs A and B are HIGH; X is LOW when either A or B is LOW, or when both A and B are LOW.

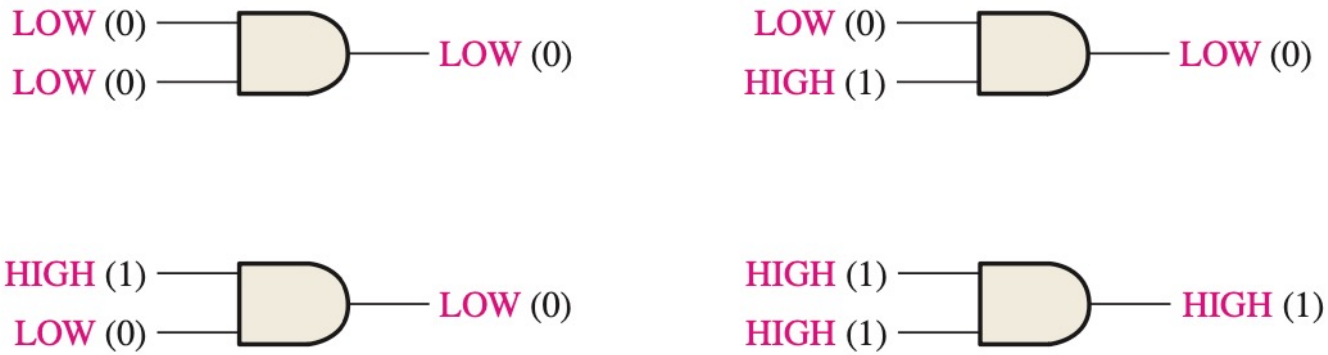


FIGURE 3–9 All possible logic levels for a 2-input AND gate. Open file F03-09 to verify AND gate operation.

AND Gate Truth Table

- The total number of possible combinations of binary inputs to a gate is determined by the following formula: $N = 2^n$
- For two input variables: N = 2^2 = 4 combinations
- For three input variables: N = 2^3 = 8 combinations
- For four input variables: N = 2^4 = 16 combinations

TABLE 3–2

Truth table for a 2-input AND gate.

Inputs		Output
A	***B***	***X***
0	0	0
0	1	0
1	0	0
1	1	1

1 = HIGH, 0 = LOW

AND Gate Truth Table

EXAMPLE 3–2

TABLE 3–3

Inputs			Output
A	*B*	*C*	*X*
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	0
1	0	0	0
1	0	1	0
1	1	0	0
1	1	1	1

(a) Develop the truth table for a 3-input AND gate.

(b) Determine the total number of possible input combinations for a 4-input AND gate.

Solution

(a) There are eight possible input combinations ($2^3 = 8$) for a 3-input AND gate. The input side of the truth table (Table 3–3) shows all eight combinations of three bits. The output side is all 0s except when all three input bits are 1s.

(b) $N = 2^4 = \mathbf{16}$. There are 16 possible combinations of input bits for a 4-input AND gate.

Related Problem

Develop the truth table for a 4-input AND gate.

AND Gate Operation with Waveform Inputs

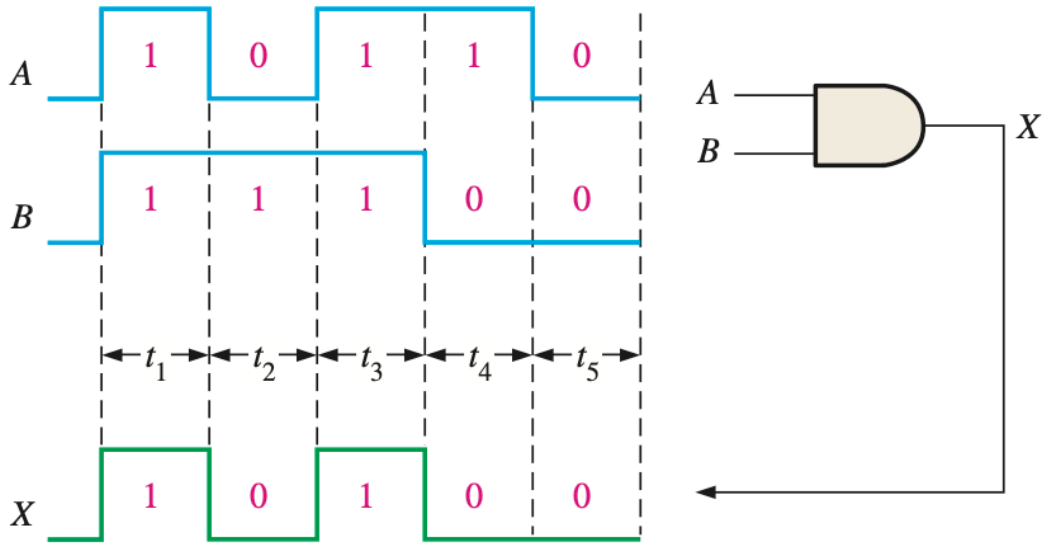
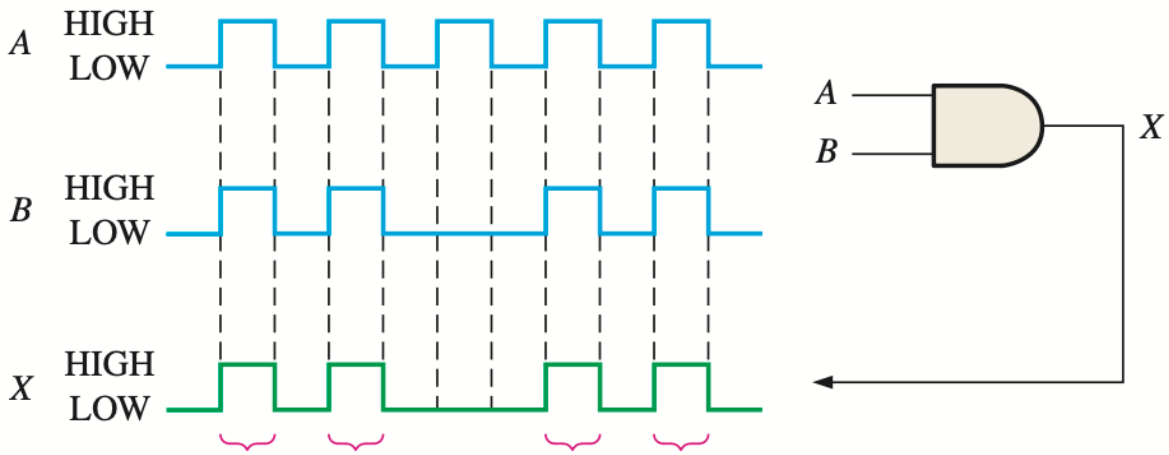


FIGURE 3–10 Example of AND gate operation with a timing diagram showing input and output relationships.

AND Gate Operation with Waveform Inputs

EXAMPLE 3–3

If two waveforms, *A* and *B*, are applied to the AND gate inputs as in Figure 3–11, what is the resulting output waveform?



A and *B* are both HIGH during these four time intervals; therefore, *X* is HIGH.

FIGURE 3–11

Solution

The output waveform *X* is HIGH only when both *A* and *B* waveforms are HIGH as shown in the timing diagram in Figure 3–11.

AND Gate Operation with Waveform Inputs

EXAMPLE 3–4

For the two input waveforms, *A* and *B*, in Figure 3–12, show the output waveform with its proper relation to the inputs.

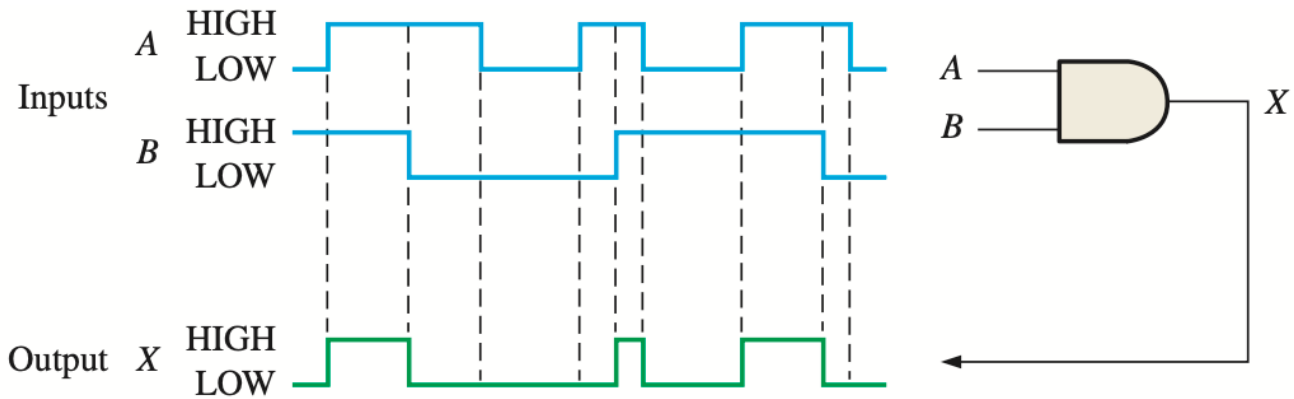


FIGURE 3–12

Solution

The output waveform is HIGH only when both of the input waveforms are HIGH as shown in the timing diagram.

AND Gate Operation with Waveform Inputs

EXAMPLE 3–5

For the 3-input AND gate in Figure 3–13, determine the output waveform in relation to the inputs.

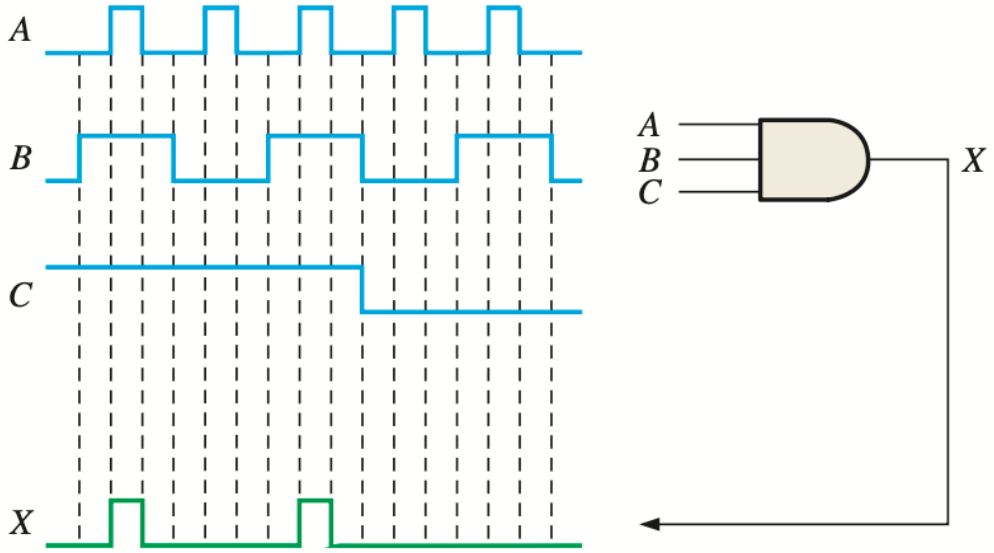


FIGURE 3–13

Solution

The output waveform X of the 3-input AND gate is HIGH only when all three input waveforms A, B, and C are HIGH.

Logic Expressions for an AND Gate

- Boolean multiplication follows the same basic rules governing binary multiplication.

$$0 \cdot 0 = 0$$
$$0 \cdot 1 = 0$$
$$1 \cdot 0 = 0$$
$$1 \cdot 1 = 1$$

- Boolean multiplication is the same as the AND function.

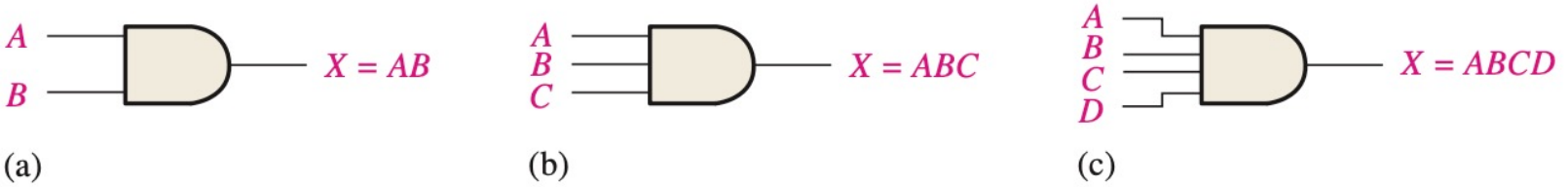


FIGURE 3–15 Boolean expressions for AND gates with two, three, and four inputs.

TABLE 3–4

A	*B*	*AB* = *X*
0	0	$0 \cdot 0 = 0$
0	1	$0 \cdot 1 = 0$
1	0	$1 \cdot 0 = 0$
1	1	$1 \cdot 1 = 1$

3. The OR Gate

- The OR gate is another of the basic gates from which all logic functions are constructed.
- An OR gate can have two or more inputs and performs what is known as logical addition.

(a) Distinctive shape

(b) Rectangular outline with the OR (≥ 1) qualifying symbol

FIGURE 3–18 Standard logic symbols for the OR gate showing two inputs (ANSI/IEEE Std. 91-1984/Std. 91a-1991).

Operation of an OR Gate

- An OR gate produces a HIGH on the output when any of the inputs is HIGH. The output is LOW only when all of the inputs are LOW.
- For a 2-input OR gate, output X is HIGH when either input A or input B is HIGH, or when both A and B are HIGH; X is LOW only when both A and B are LOW.

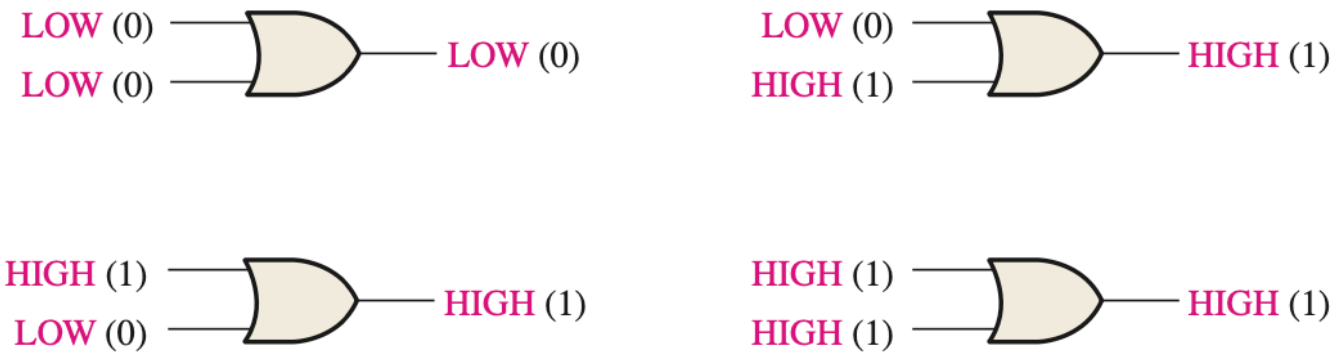


FIGURE 3–19 All possible logic levels for a 2-input OR gate. Open file F03-19 to verify OR gate operation.

TABLE 3–5

Truth table for a 2-input OR gate.

Inputs		Output
A	*B*	*X*
0	0	0
0	1	1
1	0	1
1	1	1

1 = HIGH, 0 = LOW

OR Gate Operation with Waveform Inputs

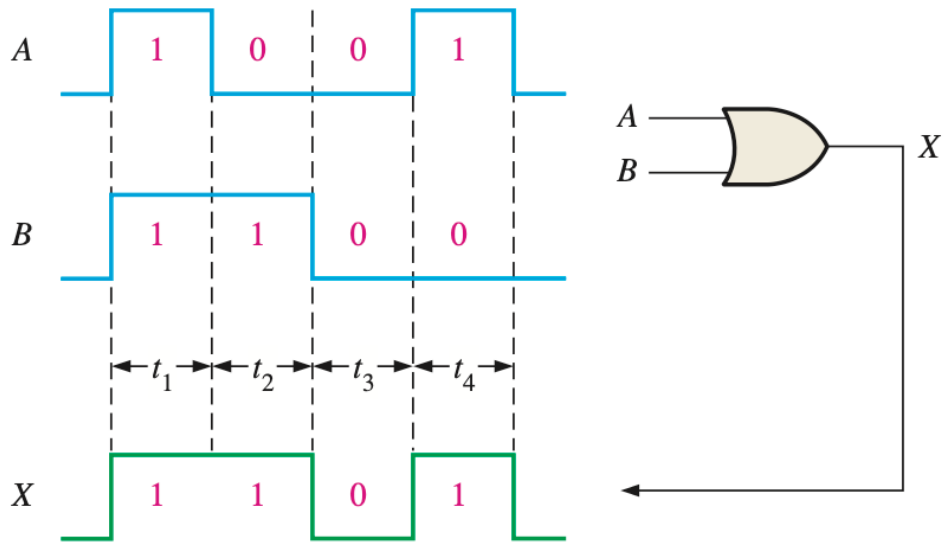


FIGURE 3–20 Example of OR gate operation with a timing diagram showing input and output time relationships.

OR Gate Operation with Waveform Inputs

EXAMPLE 3–7

If the two input waveforms, *A* and *B*, in Figure 3–21 are applied to the OR gate, what is the resulting output waveform?

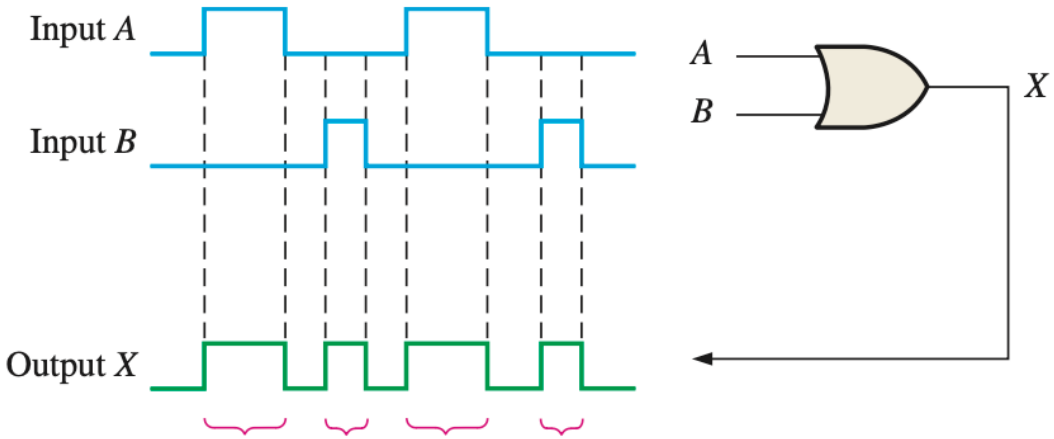


FIGURE 3–21

Solution

The output waveform *X* of a 2-input OR gate is HIGH when either or both input waveforms are HIGH as shown in the timing diagram. In this case, both input waveforms are never HIGH at the same time.

OR Gate Operation with Waveform Inputs

EXAMPLE 3–8

For the two input waveforms, *A* and *B*, in Figure 3–22, show the output waveform with its proper relation to the inputs.

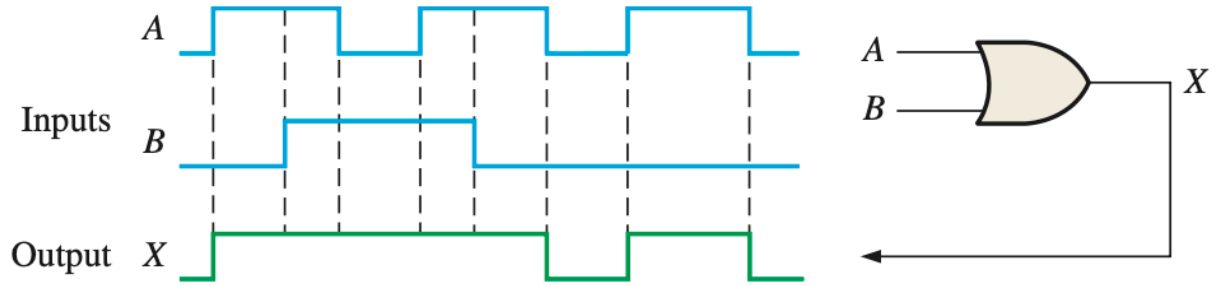


FIGURE 3–22

Solution

When either or both input waveforms are HIGH, the output is HIGH as shown by the output waveform *X* in the timing diagram.

OR Gate Operation with Waveform Inputs

EXAMPLE 3–9

For the 3-input OR gate in Figure 3–23, determine the output waveform in proper time relation to the inputs.

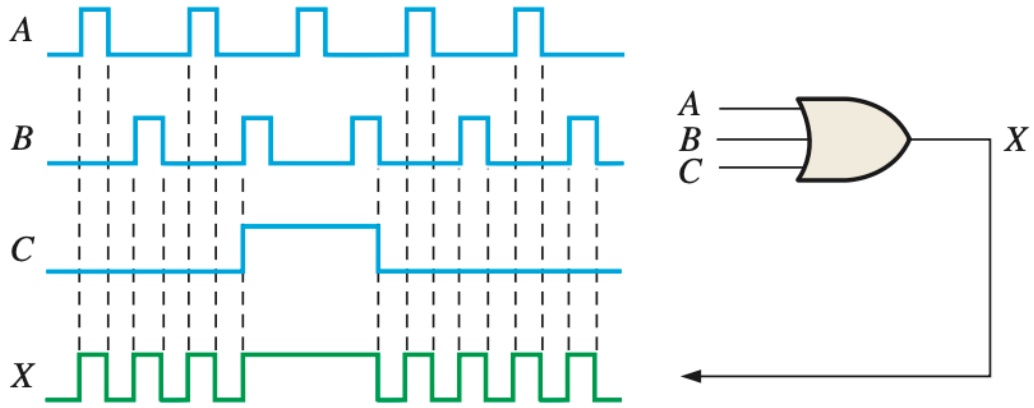


FIGURE 3–23

Solution

The output is HIGH when one or more of the input waveforms are HIGH as indicated by the output waveform *X* in the timing diagram.

Related Problem

Determine the output waveform and show the timing diagram if input *C* is always LOW.

Logic Expressions for an OR Gate

- The logical OR function of two variables is represented mathematically by a + between the two variables.

$$0 + 0 = 0$$
$$0 + 1 = 1$$
$$1 + 0 = 1$$
$$1 + 1 = 1$$

TABLE 3–6

A	*B*	*A* + *B* = *X*
0	0	0 + 0 = 0
0	1	0 + 1 = 1
1	0	1 + 0 = 1
1	1	1 + 1 = 1

- Boolean multiplication is the same as the OR function.

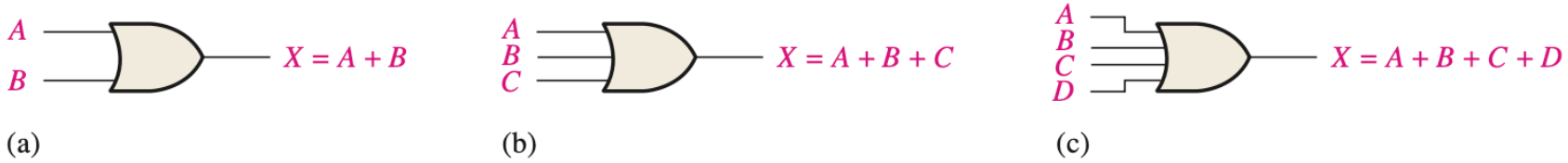
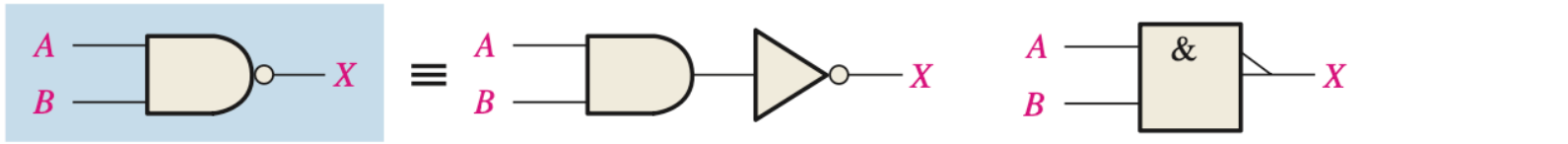


FIGURE 3–24 Boolean expressions for OR gates with two, three, and four inputs.

4. The NAND Gate

- The NAND gate is a popular logic element because it can be used as a universal gate; that is, NAND gates can be used in combination to perform the AND, OR, and inverter operations.
- The term NAND is a contraction of NOT-AND and implies an AND function with a complemented (inverted) output.



(a) Distinctive shape, 2-input NAND gate and its NOT/AND equivalent

(b) Rectangular outline, 2-input NAND gate with polarity indicator

FIGURE 3–26 Standard NAND gate logic symbols (ANSI/IEEE Std. 91-1984/Std. 91a-1991).

Operation of a NAND Gate

- A NAND gate produces a LOW output only when all the inputs are HIGH. When any of the inputs is LOW, the output will be HIGH.
- For a 2-input NAND gate, output X is LOW only when inputs A and B are HIGH; X is HIGH when either A or B is LOW, or when both A and B are LOW.

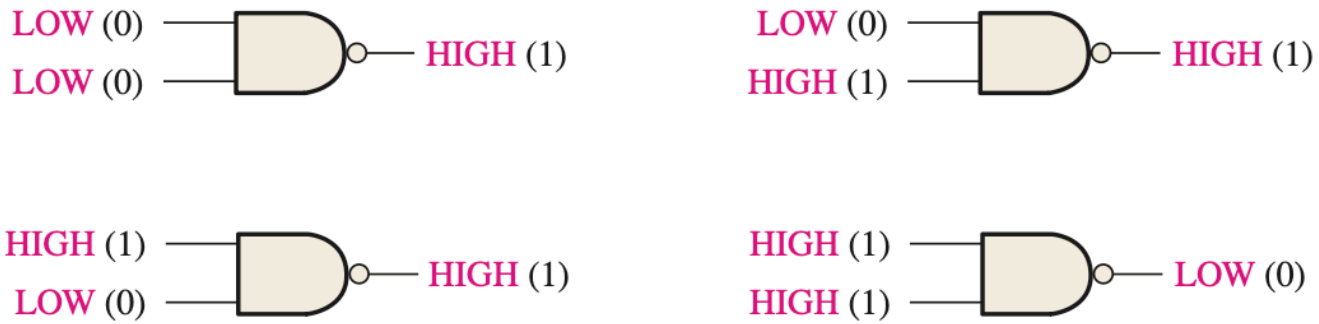


FIGURE 3–27 Operation of a 2-input NAND gate. Open file F03-27 to verify NAND gate operation.

TABLE 3–7

Truth table for a 2-input NAND gate.

Inputs		Output
A	*B*	*X*
0	0	1
0	1	1
1	0	1
1	1	0

1 = HIGH, 0 = LOW.

NAND Gate Operation with Waveform Inputs

EXAMPLE 3–10

If the two waveforms *A* and *B* shown in Figure 3–28 are applied to the NAND gate inputs, determine the resulting output waveform.

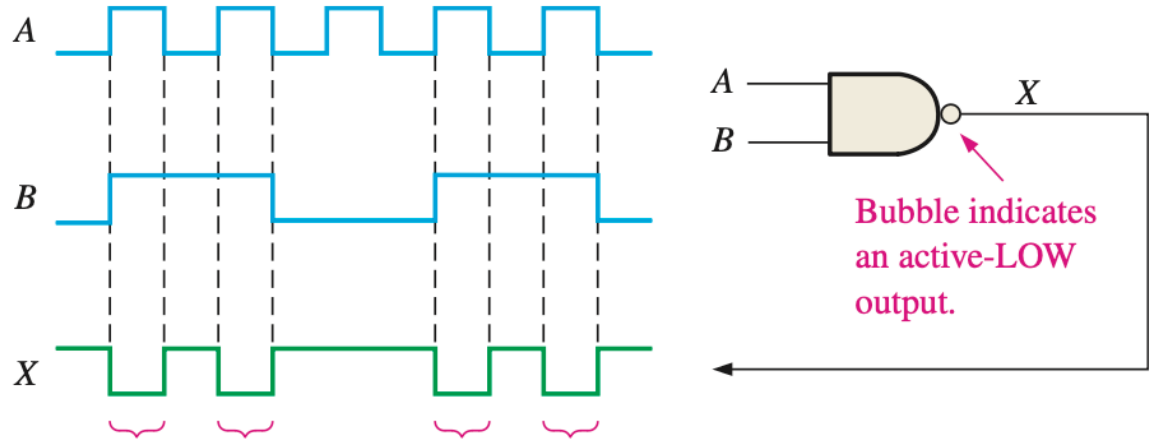


FIGURE 3–28

Solution

Output waveform *X* is LOW only during the four time intervals when both input waveforms *A* and *B* are HIGH as shown in the timing diagram.

NAND Gate Operation with Waveform Inputs

EXAMPLE 3–11

Show the output waveform for the 3-input NAND gate in Figure 3–29 with its proper time relationship to the inputs.

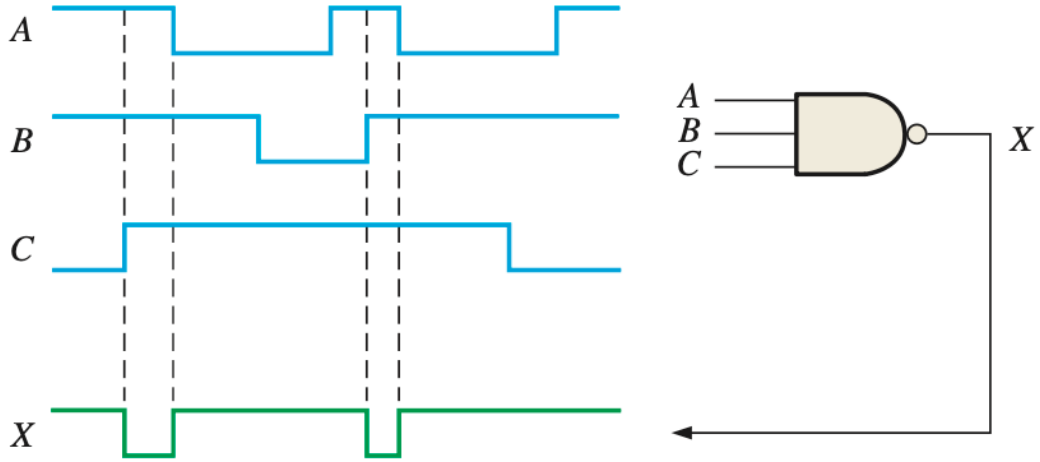


FIGURE 3–29

Solution

The output waveform X is LOW only when all three input waveforms are HIGH as shown in the timing diagram.

Negative-OR equivalent Operation of a NAND Gate

- Inherent in a NAND gate's operation is the fact that one or more LOW inputs produce a HIGH output. This aspect of NAND operation is referred to as negative-OR.
- For a 2-input NAND gate performing a negative-OR operation, output X is HIGH when either input A or input B is LOW, or when both A and B are LOW.

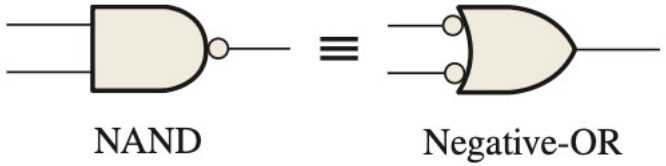


FIGURE 3–30 ANSI/IEEE standard symbols representing the two equivalent operations of a NAND gate.

EXAMPLE 3–14

For the 4-input NAND gate in Figure 3–33, operating as a negative-OR gate, determine the output with respect to the inputs.

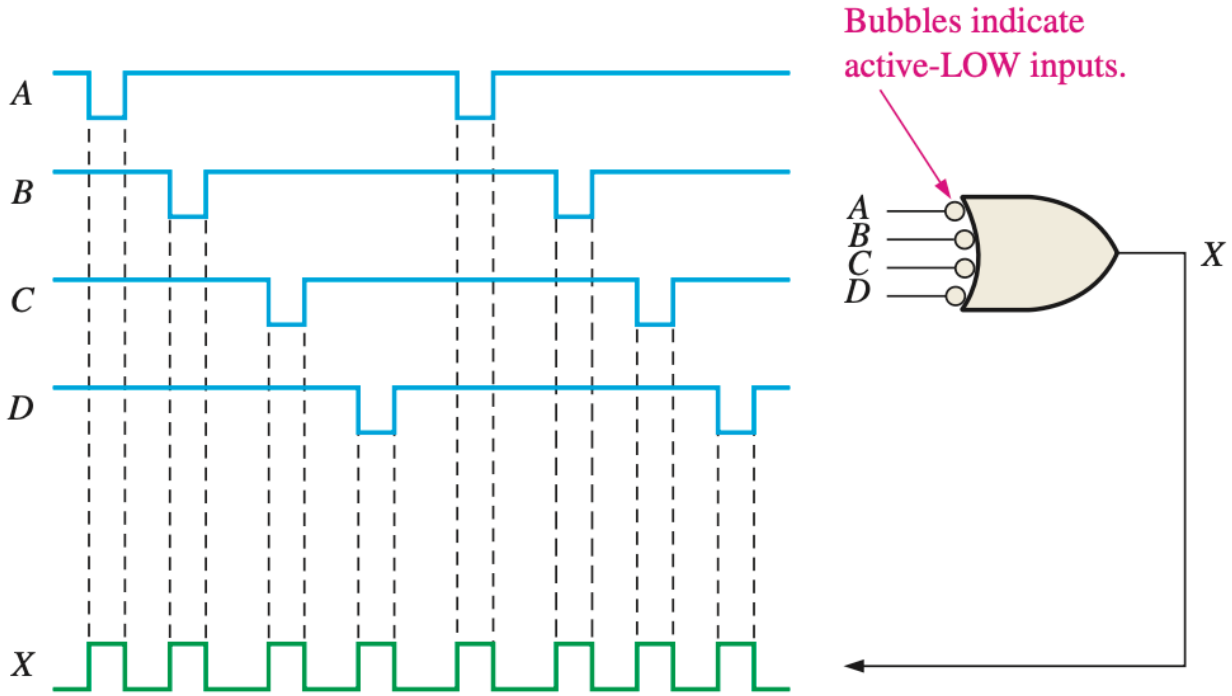


FIGURE 3–33

Solution

The output waveform X is HIGH any time an input waveform is LOW as shown in the timing diagram.

Logic Expressions for a NAND Gate

- The Boolean expression for the output of a 2-input NAND gate is

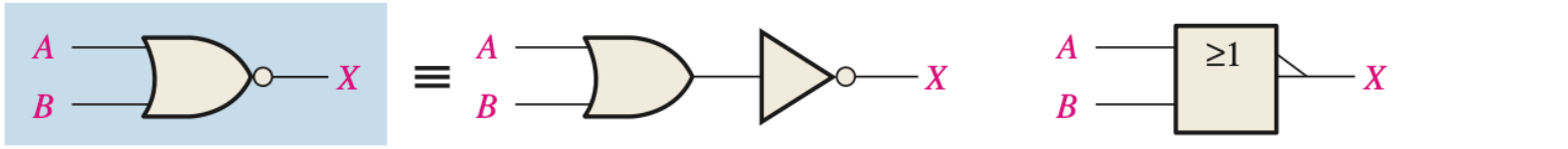
TABLE 3–8

A	B	$\overline{AB} = X$
0	0	$\overline{0 \cdot 0} = \overline{0} = 1$
0	1	$\overline{0 \cdot 1} = \overline{0} = 1$
1	0	$\overline{1 \cdot 0} = \overline{0} = 1$
1	1	$\overline{1 \cdot 1} = \overline{1} = 0$

- A bar over a variable or variables indicates an inversion.

5. The NOR Gate

- The NOR gate, like the NAND gate, is a useful logic element because it can also be used as a universal gate; that is, NOR gates can be used in combination to perform the AND, OR, and inverter operations.
- The term NOR is a contraction of NOT-OR and implies an OR function with an inverted (complemented) output.
- The NOR is the same as the OR except the output is inverted.



(a) Distinctive shape, 2-input NOR gate and its NOT/OR equivalent

(b) Rectangular outline, 2-input NOR gate with polarity indicator

FIGURE 3–34 Standard NOR gate logic symbols (ANSI/IEEE Std. 91-1984/Std. 91a-1991).

Operation of a NOR Gate

- A NOR gate produces a LOW output when any of its inputs is HIGH. Only when all of its inputs are LOW is the output HIGH.
- For a 2-input NOR gate, output X is LOW when either input A or input B is HIGH, or when both A and B are HIGH; X is HIGH only when both A and B are LOW.

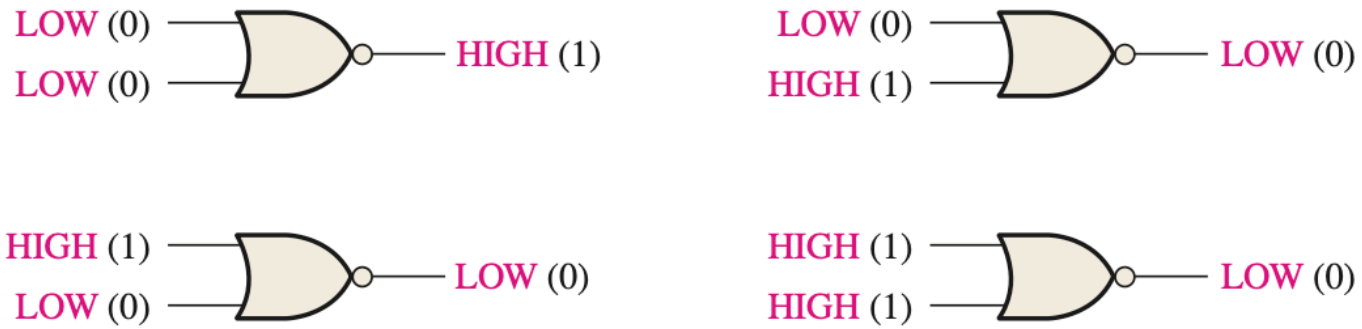


FIGURE 3–35 Operation of a 2-input NOR gate. Open file F03-35 to verify NOR gate operation.

TABLE 3–9

Truth table for a 2-input NOR gate.

Inputs		Output
A	***B***	***X***
0	0	1
0	1	0
1	0	0
1	1	0

1 = HIGH, 0 = LOW.

NOR Gate Operation with Waveform Inputs

EXAMPLE 3–15

If the two waveforms shown in Figure 3–36 are applied to a NOR gate, what is the resulting output waveform?

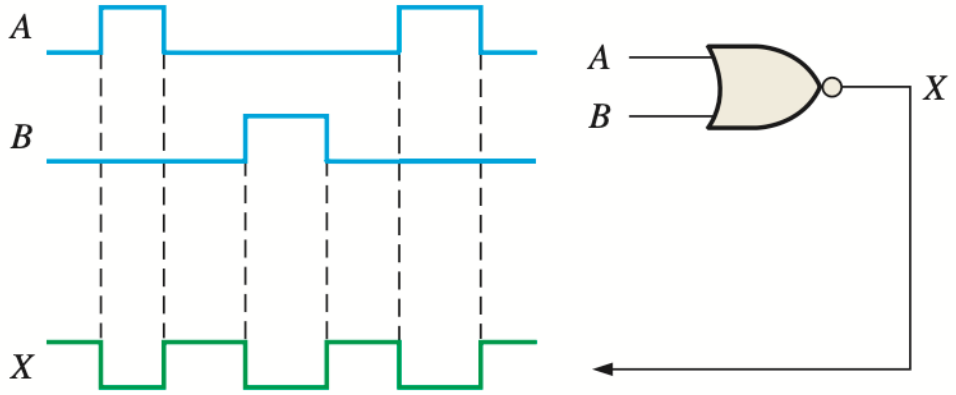


FIGURE 3–36

Solution

Whenever any input of the NOR gate is HIGH, the output is LOW as shown by the output waveform *X* in the timing diagram.

NOR Gate Operation with Waveform Inputs

EXAMPLE 3–16

Show the output waveform for the 3-input NOR gate in Figure 3–37 with the proper time relation to the inputs.

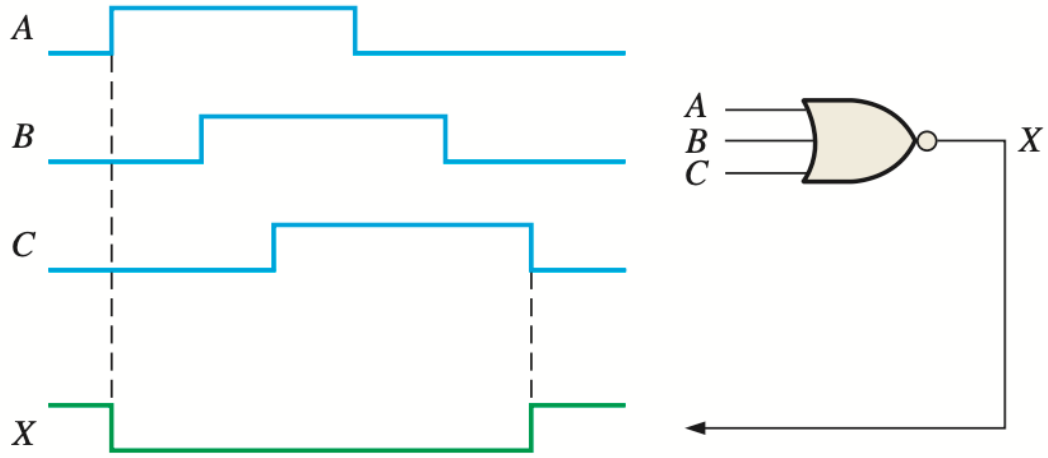


FIGURE 3–37

Solution

The output X is LOW when any input is HIGH as shown by the output waveform X in the timing diagram.

Negative-AND equivalent Operation of a NOR Gate

- A NOR gate, like the NAND, has another aspect of its operation that is inherent in the way it logically functions. This aspect of NOR operation is called negative-AND.
- or a 2-input NOR gate performing a negative-AND operation, output X is HIGH only when both inputs A and B are LOW.

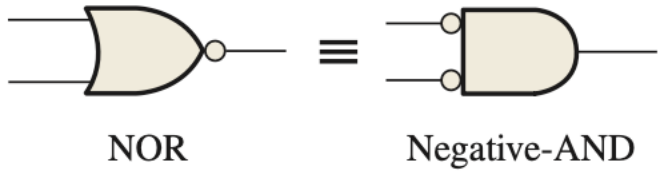


FIGURE 3–38 Standard symbols representing the two equivalent operations of a NOR gate.

EXAMPLE 3–19

For the 4-input NOR gate operating as a negative-AND in Figure 3–41, determine the output relative to the inputs.

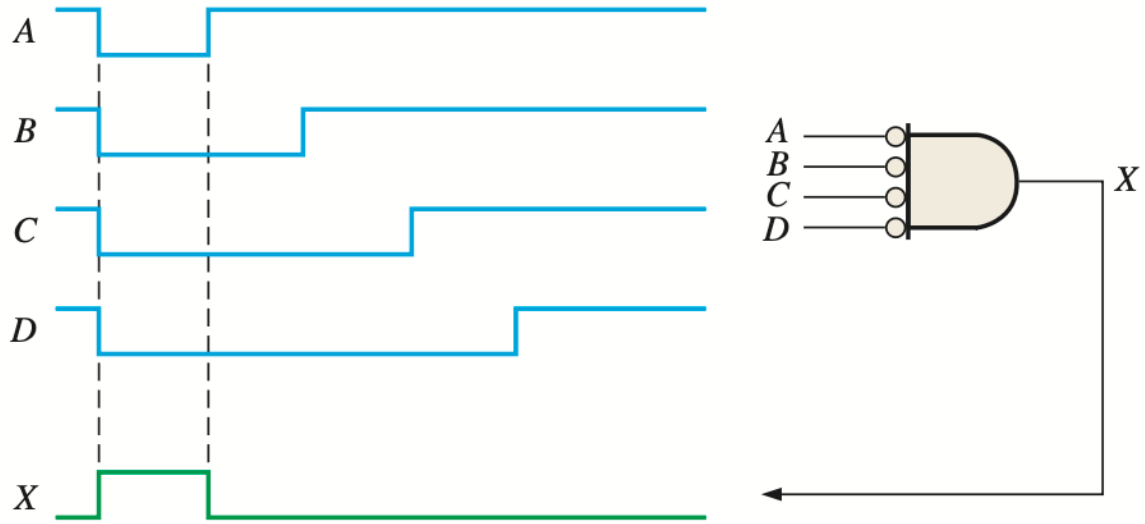


FIGURE 3–41

Solution

Any time all of the input waveforms are LOW, the output is HIGH as shown by output waveform *X* in the timing diagram.

Logic Expressions for a NOR Gate

- The Boolean expression for the output of a 2-input NOR gate can be written as

TABLE 3–10

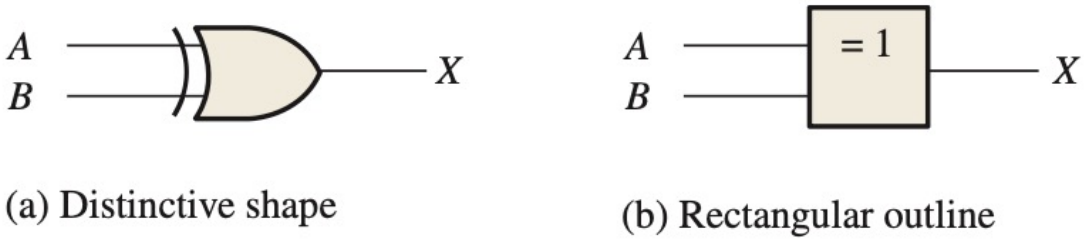
A	B	$\overline{A + B} = X$
0	0	$\overline{0 + 0} = \overline{0} = 1$
0	1	$\overline{0 + 1} = \overline{1} = 0$
1	0	$\overline{1 + 0} = \overline{1} = 0$
1	1	$\overline{1 + 1} = \overline{1} = 0$

- The NOR expression can be extended to more than two input variables by including additional letters to represent the other variables.

6. The Exclusive-OR and Exclusive-NOR Gates

The Exclusive-OR Gate

- The XOR gate has only two inputs. The exclusive-OR gate performs modulo-2 addition.
- The output of an exclusive-OR gate is HIGH only when the two inputs are at opposite logic levels.
- For an exclusive-OR gate, opposite inputs make the output HIGH.



(a) Distinctive shape (b) Rectangular outline

FIGURE 3–42 Standard logic symbols for the exclusive-OR gate.

- For an exclusive-OR gate, output X is HIGH when input A is LOW and input B is HIGH, or when input A is HIGH and input B is LOW; X is LOW when A and B are both HIGH or both LOW.

FIGURE 3–43 All possible logic levels for an exclusive-OR gate. Open file F03-43 to verify XOR gate operation.

TABLE 3–11

Truth table for an exclusive-OR gate.

Inputs		Output
A	***B***	***X***
0	0	0
0	1	1
1	0	1
1	1	0

The Exclusive-NOR Gate

- Like the XOR gate, an XNOR has only two inputs.
- The bubble on the output of the XNOR symbol indicates that its output is opposite that of the XOR gate.
- When the two input logic levels are opposite, the output of the exclusive-NOR gate is LOW.

(a) Distinctive shape (b) Rectangular outline

FIGURE 3–45 Standard logic symbols for the exclusive-NOR gate.

- For an exclusive-NOR gate, output X is LOW when input A is LOW and input B is HIGH, or when A is HIGH and B is LOW; X is HIGH when A and B are both HIGH or both LOW.

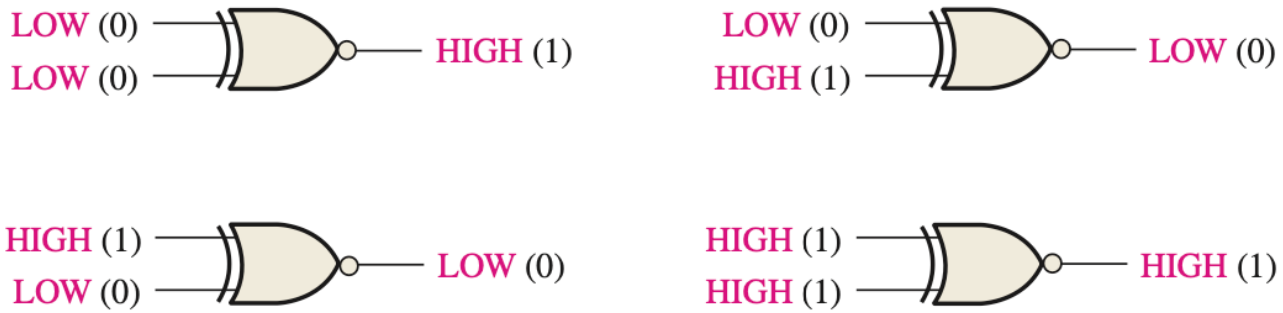


FIGURE 3–46 All possible logic levels for an exclusive-NOR gate. Open file F03-46 to verify XNOR gate operation.

TABLE 3–12

Truth table for an exclusive-NOR gate.

Inputs		Output
A	***B***	***X***
0	0	1
0	1	0
1	0	0
1	1	1

Operation with Waveform Inputs

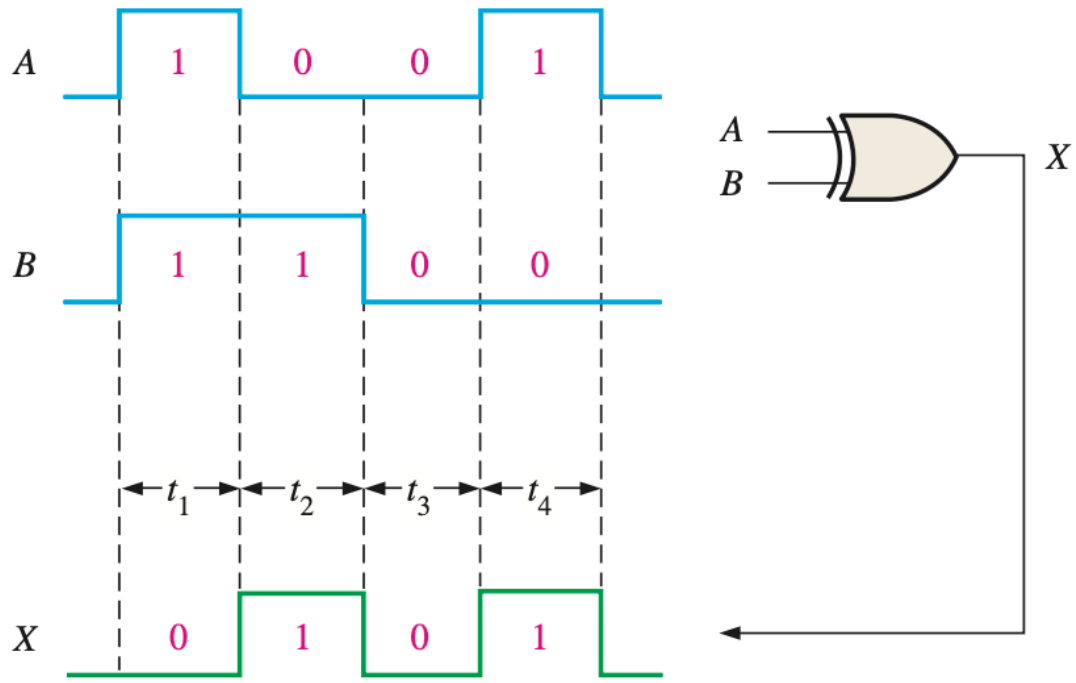


FIGURE 3–47 Example of exclusive-OR gate operation with pulse waveform inputs.

EXAMPLE 3–21

Determine the output waveforms for the XOR gate and for the XNOR gate, given the input waveforms, *A* and *B*, in Figure 3–48.

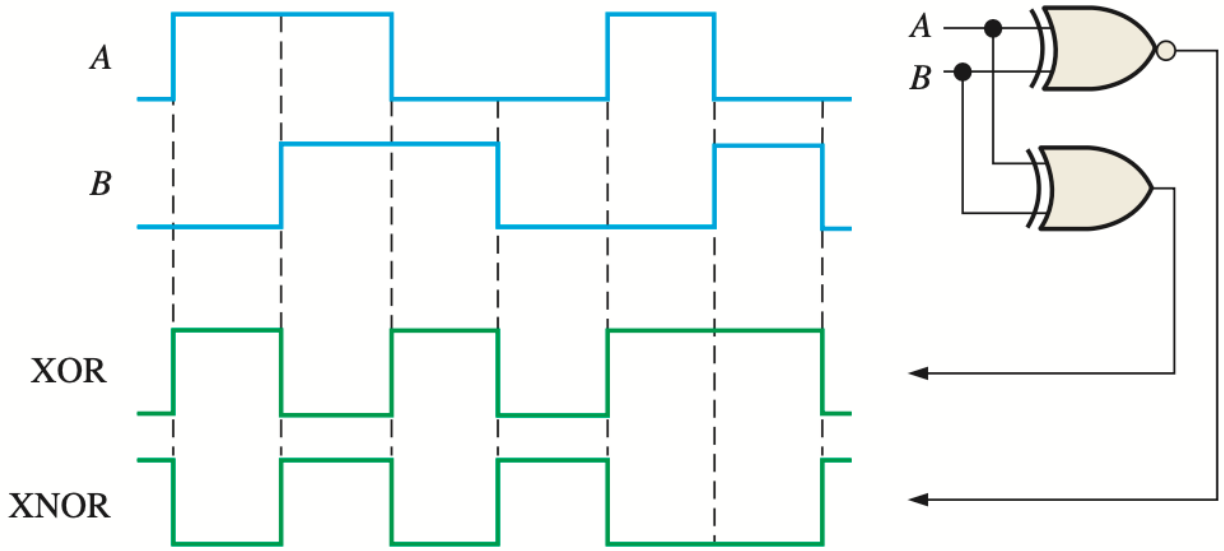


FIGURE 3–48

Solution

The output waveforms are shown in Figure 3–48. Notice that the XOR output is HIGH only when both inputs are at opposite levels. Notice that the XNOR output is HIGH only when both inputs are the same.

The AND Array

- Most types of PLDs use some form of **AND array**.
- Basically, this array consists of AND gates and a matrix of interconnections with a programmable link at each cross point.
- Programmable links allow a connection between a row line and a column line in the interconnection matrix to be opened or left intact.
- For each input to an AND gate, only one programmable link is left intact in order to connect the desired variable to the gate input.

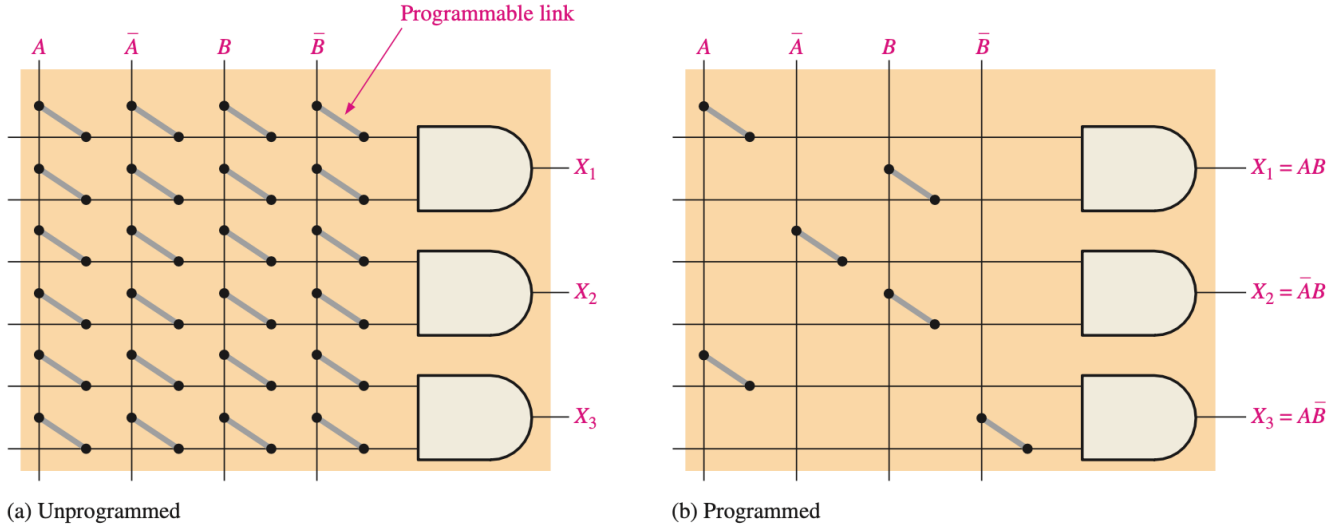


FIGURE 3–49 Concept of a programmable AND array.

EXAMPLE 3–22

Show the AND array in Figure 3–49(a) programmed for the following outputs: $X_1 = A\overline{B}$, $X_2 = \overline{A}B$, and $X_3 = \overline{A}\,\overline{B}$

Solution

See Figure 3–50.

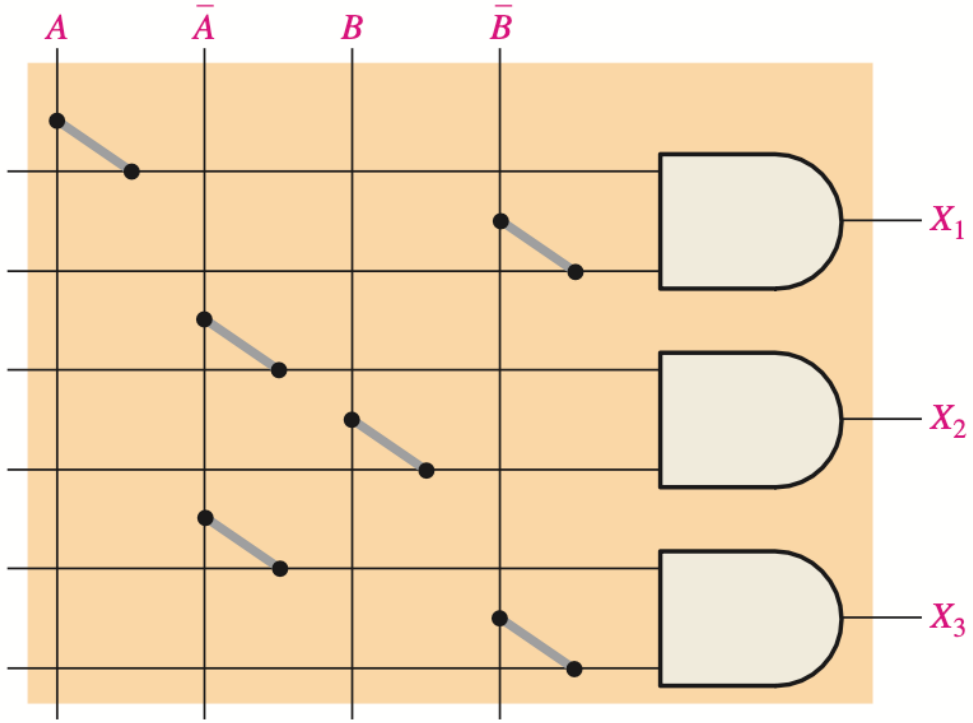
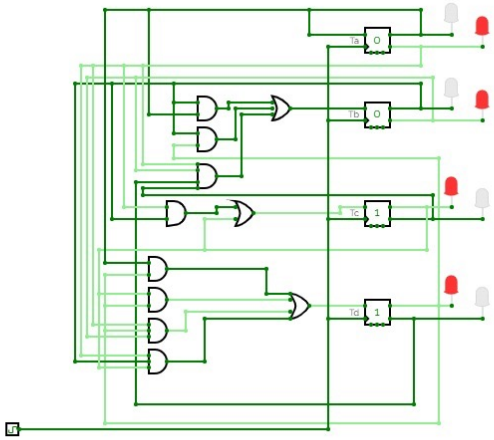


FIGURE 3–50

THE END

Lecture 3: Logic Gates



INSTRUCTOR: Dr. Vuong Quoc Bao