DIGITAL LOGIC DESIGN

Fall 2018

Homework #2

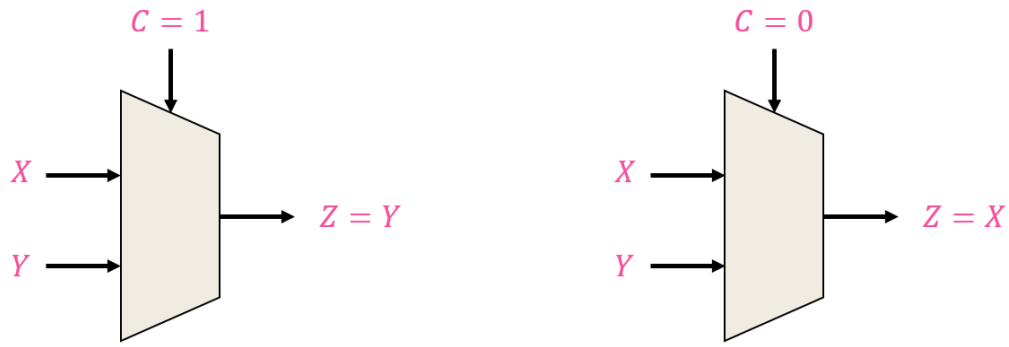
IMPORTANT: This assignment should be done individually. Marks will be deducted if there are sign of violation of regulation and late submission.

Tip: You should draw a bounding box for your final answer. Ex in below:

$Y = ABC + AC = \boxed{ABC}$

Problem 1:

The multiplexer is a logic circuit designed in order to turn one of several input lines to a single common output line. The following figure is a 2 inputs multiplexer which has $\boldsymbol{X}$ and $\boldsymbol{Y}$ input signals. In case that $\boldsymbol{Y}$ is selected when the control input $\boldsymbol{C = 1}$ and X is selected when $\boldsymbol{C = 0}$.



(a) Create a truth table for the given multiplexer ($\boldsymbol{X}$ and $\boldsymbol{Y}$ are logical variables).

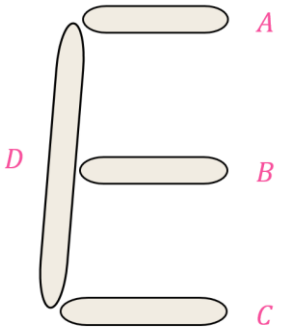
(b) Write an expression for $\boldsymbol{Z}$ in form of Sum-of-Product.

(c) Simplify the expression in Part (b) by using K-map.

(d) Design a logical circuit for $\boldsymbol{Z}$ using 2-inputs NOR gates.

Problem 2:

The figure below shows a LED display panel which has four light bar $\boldsymbol{A}$, $\boldsymbol{B}$, $\boldsymbol{C}$ and $\boldsymbol{D}$. Design a logic circuit displaying the $\boldsymbol{F}$ letter and $\boldsymbol{L}$ letter using the panel.



(a) Create a truth table for the design.

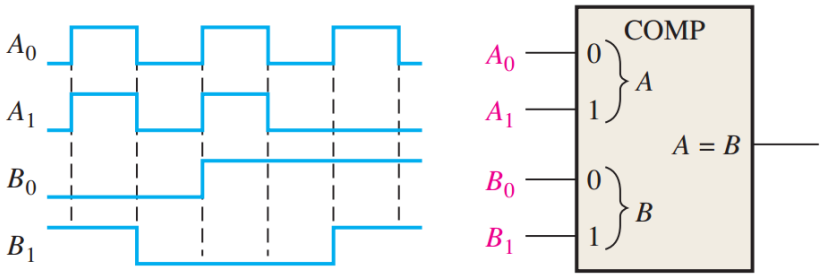
(b) Write an expression for ***F*** and ***L*** letter.

(c) Draw logic circuit for ***F*** and ***L*** letters using 2-input NOR gates.

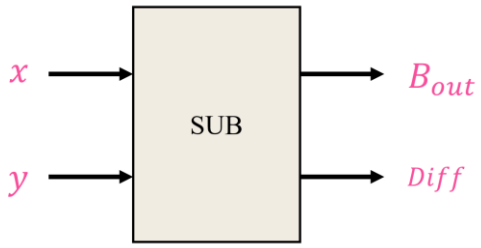
(d) List other English letters could be shown in this LED panel.

Problem 3:

(a) The given waveforms (blue) are going in the comparator as shown in the following figure. Determine the output waveform from the given input waveform.



(b) A half-subtractor module has input x, y and output $Diff$, B_{out} (in the figure below). The module subtracts the bits $x - y$ and places the difference in $Diff$ and the borrow in B_{out}. Create a truth table and write the expression for Diff and B_{out}. *(Hint: You also can refer the adder).*



Problem 4:

Implement the following Boolean function with a multiplexer

(a) $F = \Sigma\,(0, 2, 5, 7, 11, 14)$

(b) $F = \Pi\,(3, 8, 12)$

Problem 5:

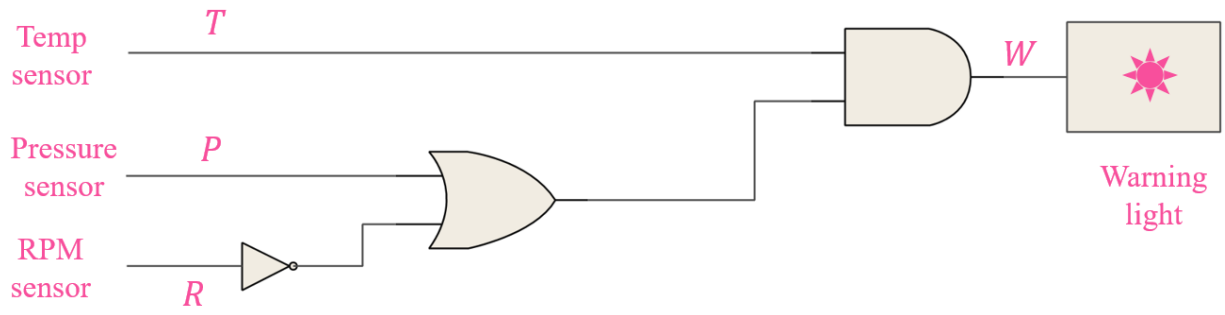
A jet aircraft employs a system for monitoring the rpm, pressure and temperature values of its engines using sensors that operate as follows.

- RPM sensor output = 0 only when speed $<$ 4800 rpm
- P sensor output = 0 only when pressure $<$ 220 psi
- T sensor output = 0 only when temperature $<$ 200°F

For the combinational circuit shown:

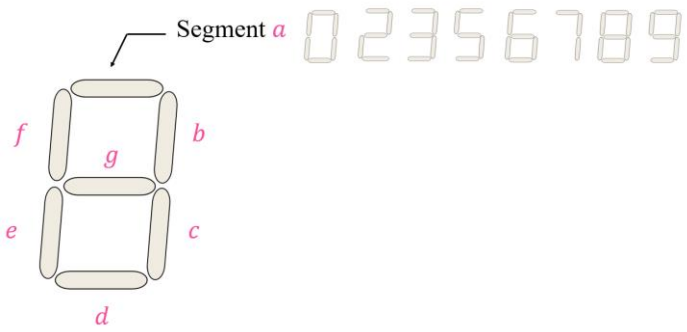
(a) Identify the engine conditions that will give warning to the pilot. Write down the expression

(b) Using NAND gates only for the expression . Why are NAND and NOR gates called universal gates?



Problem 6:

In a 7-segment display, each of the seven segments is activated for various digits. For instance, segment a is activated for the digits 0, 2, 3, 5, 6, 7, 8, and 9, as shown in the following figure. Each digit can be represented by a BCD code.



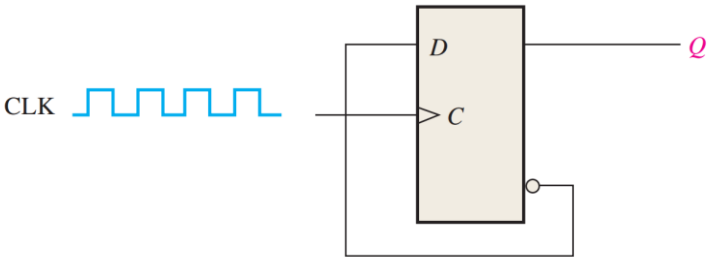
(a) Write a Sum-of-Product expression for segment ***a*** using the variables ABCD.

(b) Simplify the expression using K map.

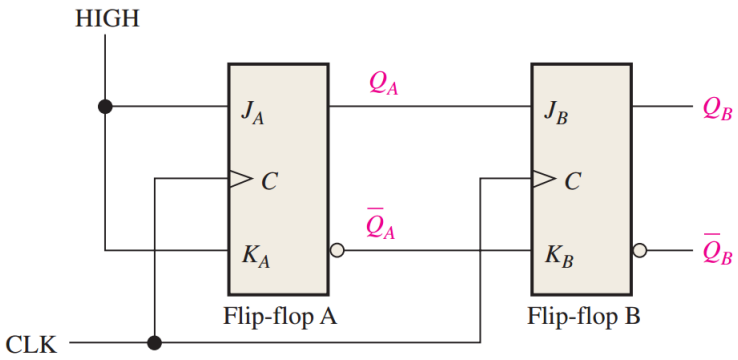
(Hints: In the BCD code, there are six invalid combinations: 1010, 1011, 1100, 1101, 1110, and 1111. Since these states will never occur in the BCD code, they can be treated as "don't care" terms which can be noted by 'x' in K-map)

Problem 7:

(a) A D flip-flop is shown in the following figure. Find the Q output in relation to the clock. What function does this circuit perform?



(b) In the figure below, draw a timing diagram for 8 clock pulses for the Q_A and Q_B outputs in given clock.

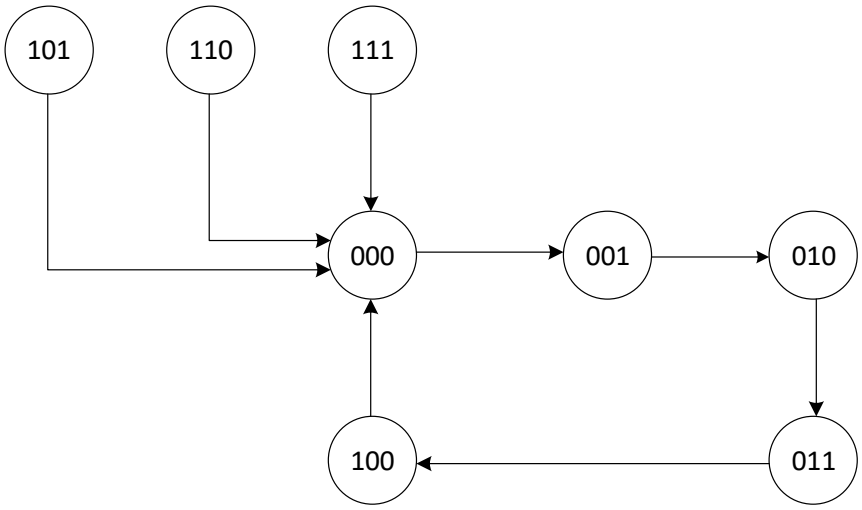


Problem 8:

Design a counter which has the following counting sequence: 0-1-2-3-4 and repeat, 5-0, 6-0, and 7-0. This counter should be designed using D-FFs only.

Problem 9:

A state transition diagram of a synchronous counter is considered as below Figure. Given that the logical design of this counter consists of **J-K** FF only.

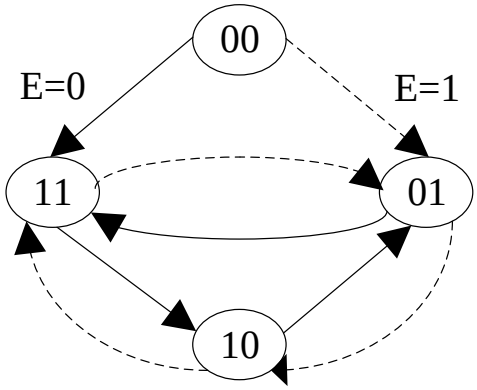


(a) Show the Transition table of this counter.

(b) Find the simplified expressions for each J-K input.

Problem 10:

A state transition diagram is considered in the figure below



In this figure, E is an enable control input. This input has two states: 0 and 1. Each state of E indicates one separate operation of the state machine given in Figure J-K FFs are considered.

(a) Derive the logic expressions for each input of FF.

(b) Modify the circuit in (a) such that at $E = 0$, the state transition machine follows the new sequence: 0-3-2-1-0 and repeat while at $E = 1$, the new sequence is 0-1-2-3-2-0 and repeat. Sketch the new logic circuit.