ICTC INTEGRATED CIRCUIT TRAINING CENTER

FUNDAMENTAL INTEGRATED CIRCUIT DESIGN COURSE
IC11 CLASS

AMBA – APB SPECIFICATION

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04 Nov, 2024

CONTENT

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1. Introduction

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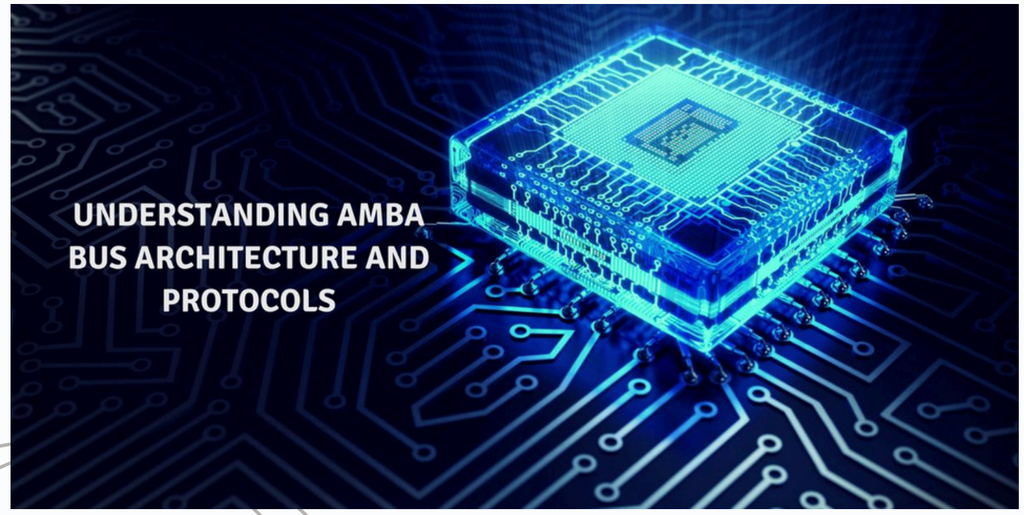
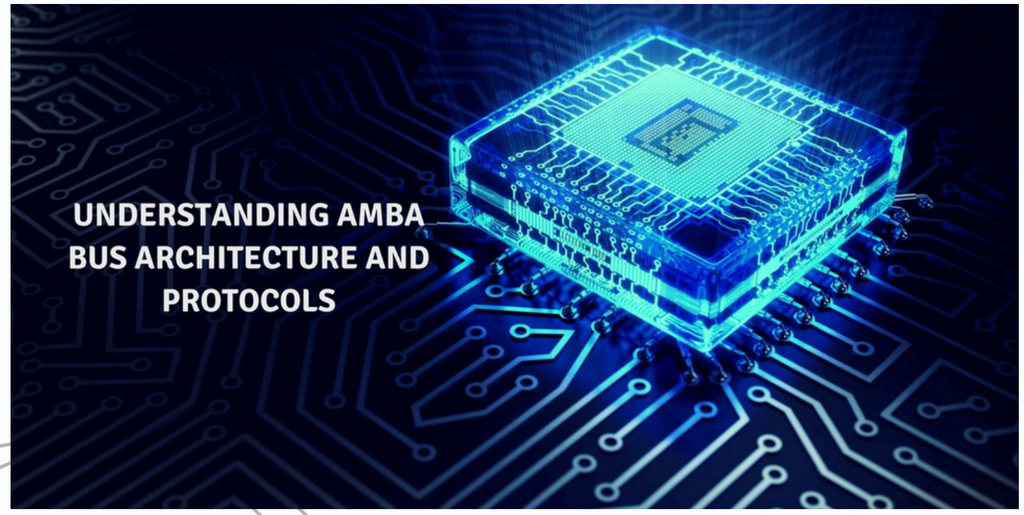
1. Introduction



Advanced Micro controller Bus Architecture (AMBA)

- A set of bus protocols designed by ARM Holdings.
- Enable efficient communication between different components within a chip, such as the CPU, memory, and peripheral devices.
- Building high performance SOC designs.

1. Introduction

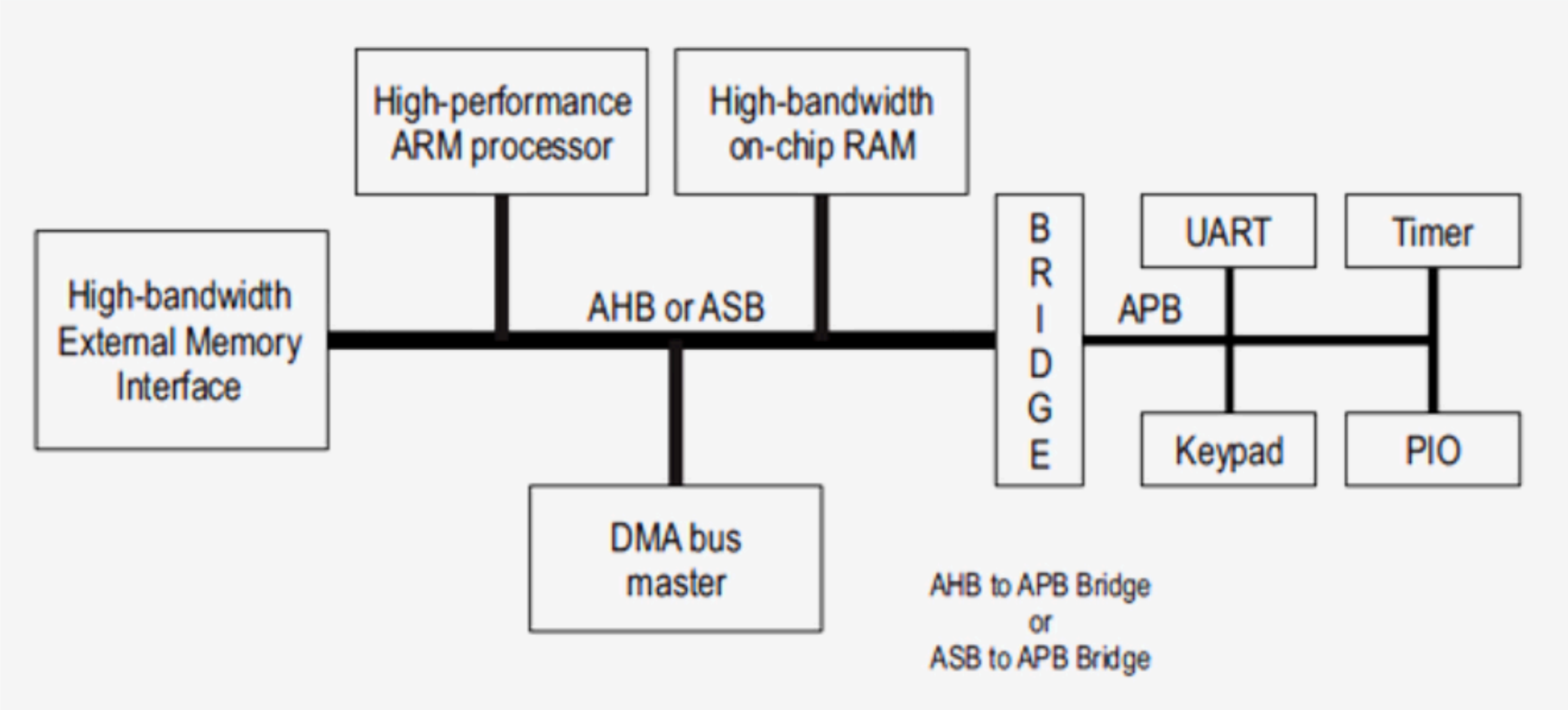


Advanced Micro controller Bus Architecture (AMBA)

- These designs typically have one or more microcontrollers or microprocessors along with several other components:

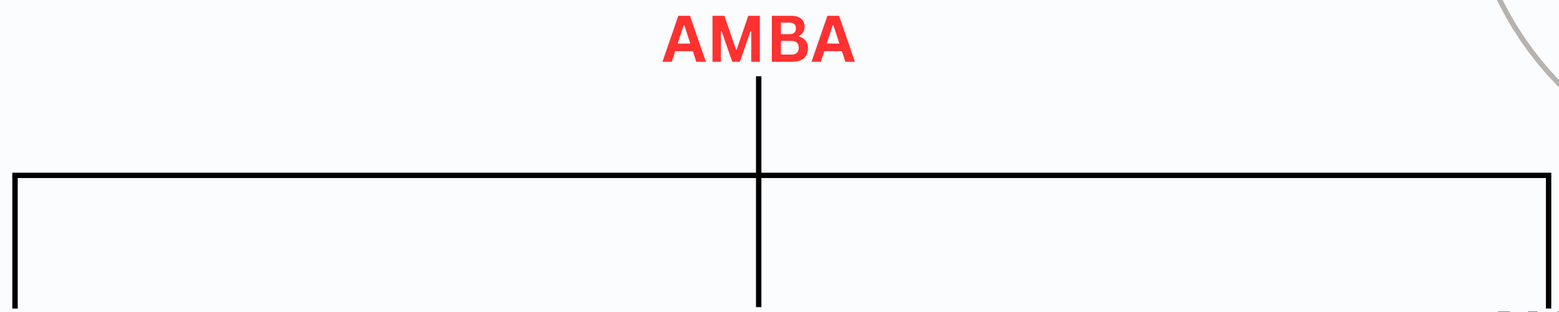
- Internal memory or external memory bridge.
- DSP (Digital Signal Processor).
- DMA (Direct Memory Access).
- Accelerators and various other peripherals like USB, UART, PCIE, I2C etc.

1. Introduction



A traditional AMBA based SOC design

1. Introduction



- Characteristics: High-performance bus, single-cycle data transfer.
- Applications: CPU, DMA, main memory.
- Connection: Supports multiple master and slave devices.

- Characteristics: Simplest, optimized for low-speed peripheral
- Applications: UART, GPIO, timers; energy efficient.
- Connection: Typically connects via a “bridge” to AXI/AHB.

- Characteristics: Advanced protocol with burst and multi-threading support.
- Applications: High-speed processors, GPU, video processing.
- Key Features :Asynchronous transactions, parallel data transfer.

1. Introduction

Advanced Peripheral Bus (APB)

- A low-cost interface, optimized for minimal power consumption and reduced interface complexity.
- Not pipelined and is a simple, synchronous protocol.
- Every transfer takes at least two cycles to complete.

1. Introduction

Advanced Peripheral Bus (APB)

- Designed to access the programmable control registers of peripheral devices.
- Not pipelined and is a simple, synchronous protocol.
- APB transfers are initiated by an APB bridge. APB bridges can also be referred to as a Requester.
- A peripheral interface responds to requests. APB peripherals can also be referred to as a Completer.

1. Introduction

Advanced Peripheral Bus (APB)

- Provides an efficient, low-power interface to connect peripheral devices to the CPU without impacting the overall system performance
- With straightforward design, APB facilitates the development process of peripheral devices, reducing both design and testing time.
- Supports low-speed devices, ensuring consistent and stable operation of peripheral devices within the AMBA architecture.

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2. Detail on signals and transfer

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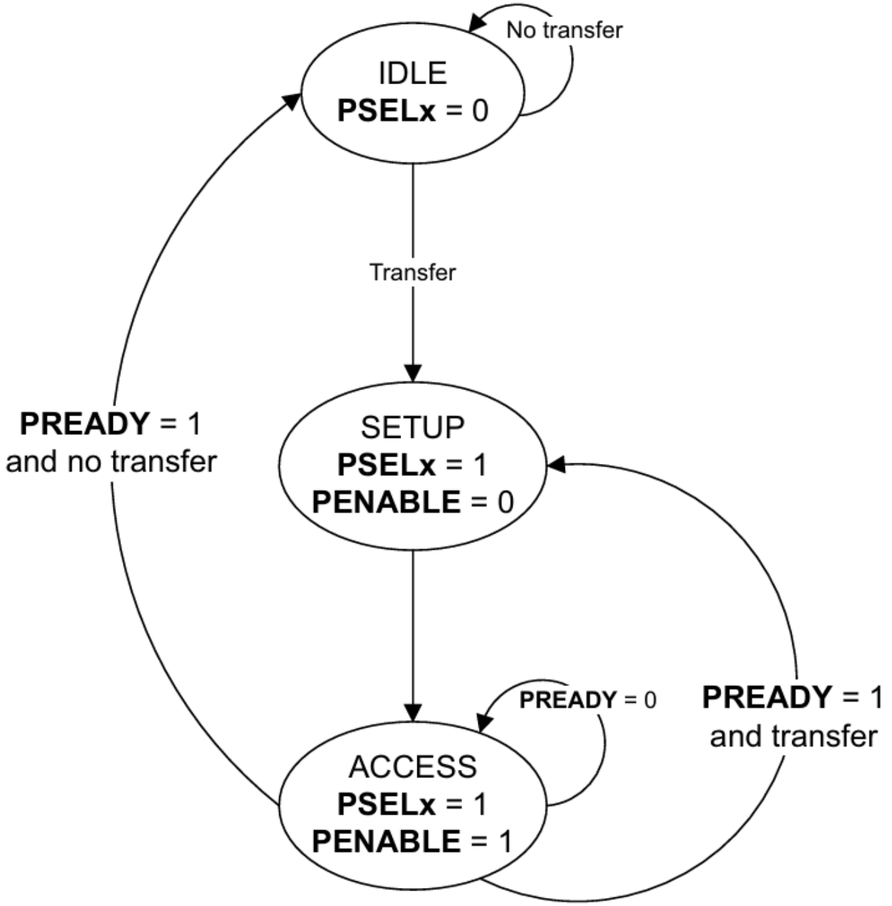
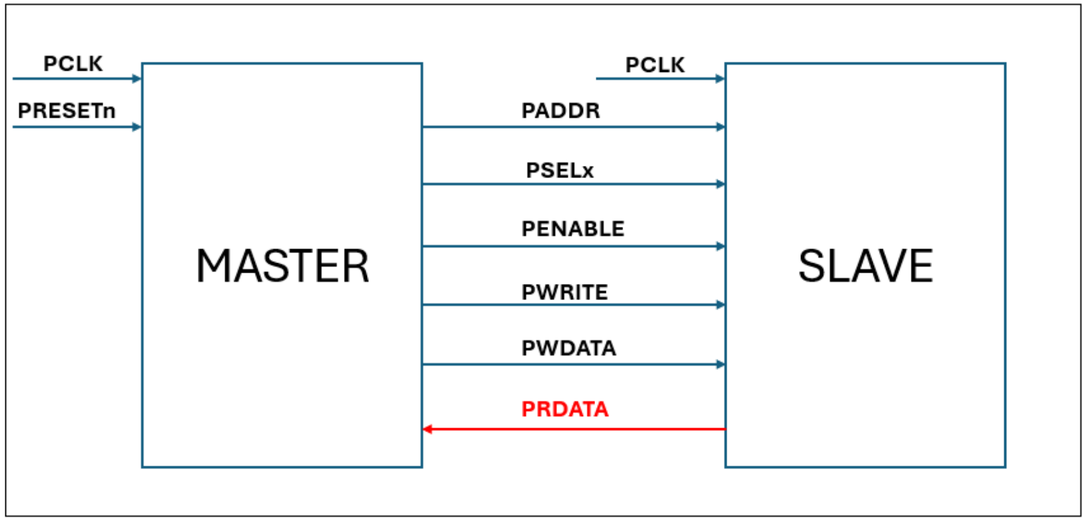
OPERATING STATE



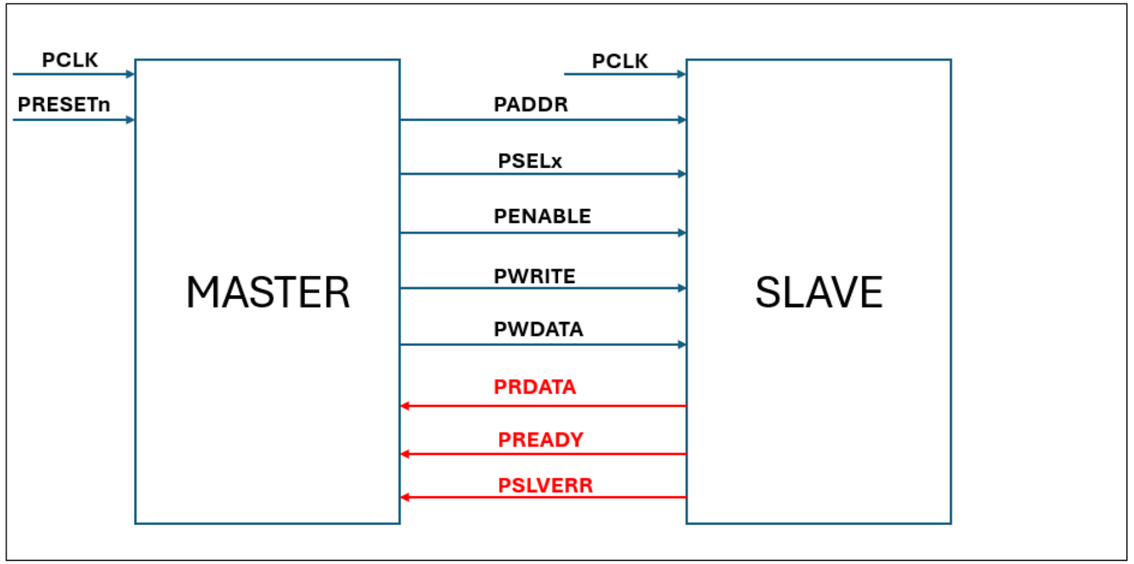
STATE	DESCRIPTION
IDLE	The default state, where the interface waits for a transfer request.
SETUP	When a transfer request occurs, the interface moves to the SETUP state, where the PSELx signal is asserted. The interface stays in SETUP for only one clock cycle and moves to ACCESS in the next clock cycle.
ACCESS	In ACCESS, the PENABLE signal is asserted. Key signals (PADDR, PPROT, PWRITE, PWDATA for writes, PSTRB, PAUSER, PWUSER) remain stable between cycles. - If PREADY is LOW, the interface stays in ACCESS. - If PREADY is HIGH, the interface: + Returns to IDLE if there are no more transfers. + Moves directly to SETUP if another transfer is requested.

AMBA APB 2 Specification



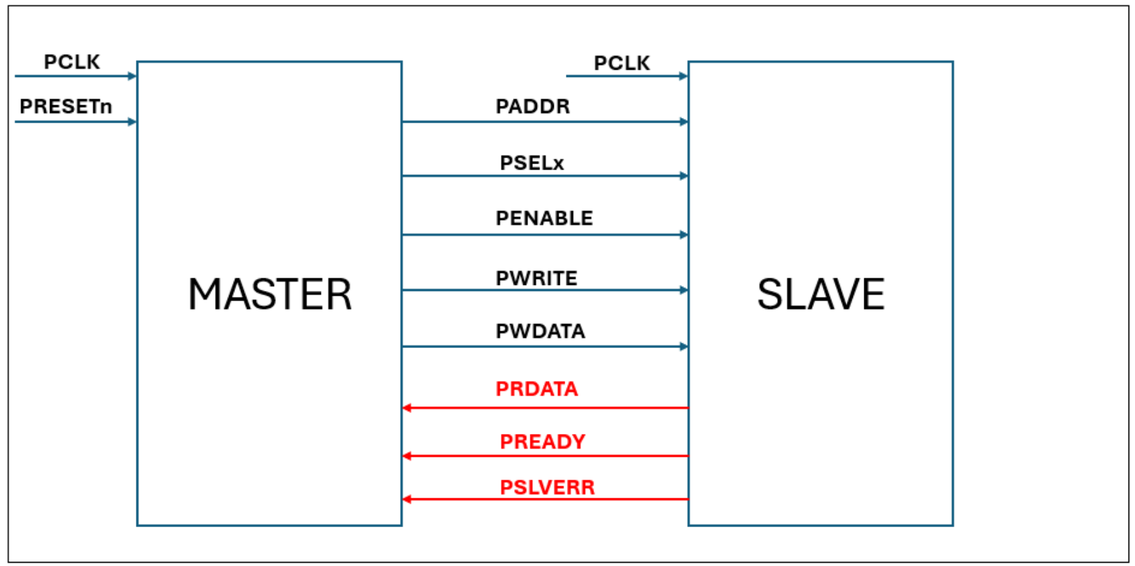
SIGNAL	SOURCE	WIDTH	DESCRIPTION
PCLK	Clock	1	Clock. The rising edge of PCLK times all transfers on the APB
PRESETn	System bus reset	1	Reset. The APB reset signal is active LOW. This signal normally connected directly on the system bus reset signal
PADDR	Requester	ADDR_WIDTH	Address. This is the APB address bus. It can be up to 32 bits wide.
PSELx	Requester	1	Select. The requester generates a PSELx signal for each Completer. PSELx indicates that the Completer is selected and that a data transfer is required.
PENABLE	Requester	1	Enable. This signal indicates the second and subsequent cycles of an APB transfer.
PWRITE	Requester	1	Direction. This signal indicates an APB write access when HIGH and an APB read access when LOW
PWDATA	Requester	DATA_WIDTH	Write data. This bus is driven by the peripheral bus bridge unit during write cycles when PWRITE is HIGH. This bus can be up to 32 bits wide
PRDATA	Completer	DATA_WIDTH	Read data. The selected slave drives this bus during read cycles when PWRITE is LOW. This bus can be up to 32 bits wide

AMBA APB 3 Specification



SIGNAL	SOURCE	WIDTH	DESCRIPTION
PREADY	Completer	1	Ready. The slave uses this signal to extend an APB transfer.
PSLVERR	Completer	1	PSLVERR is an optional signal that can be asserted HIGH by the Completer to indicate an error condition on an APB transfer.

AMBA APB 3 Specification



PREADY:

PREADY can be used to extend the transfer, giving the slave device additional time to process without requiring changes to other signals like PSEL or PENABLE.

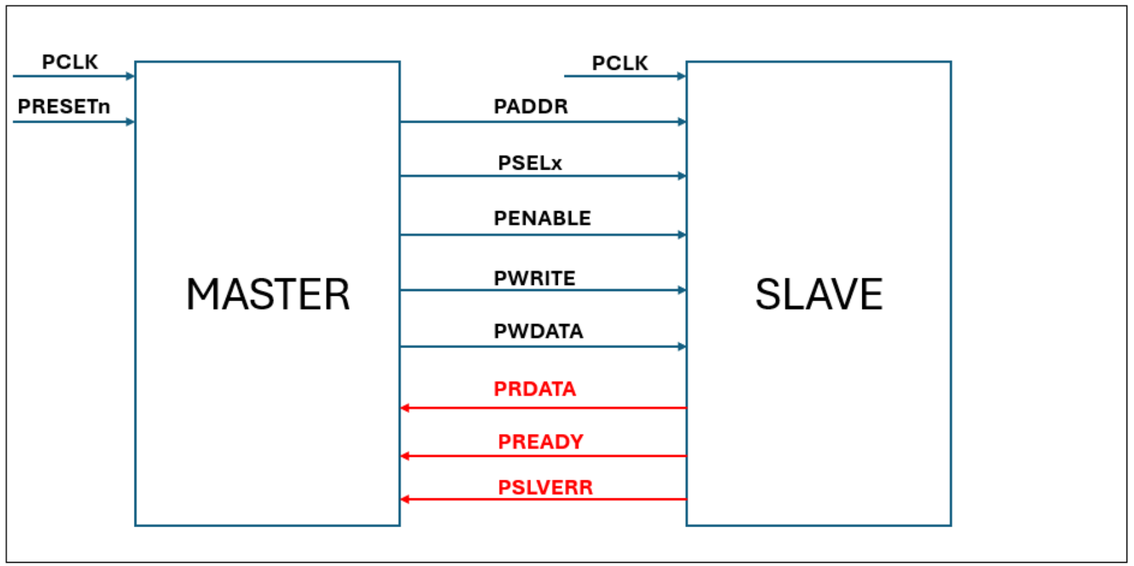
In Write Transfer:

- When PREADY = 1: The slave is ready to receive data from the master. In this state, data can be written to the slave's register.
- When PREADY = 0: The slave is not ready to receive data. In this case, the write process will be paused, and data will not be written until PREADY changes to HIGH.

In Read Transfer:

- When PREADY = 1: This signal indicates that the slave is ready to provide data to the master.
- When PREADY = 0: The slave is not ready to provide data. If PREADY is LOW, the master will not receive data until PREADY goes back to HIGH, allowing the slave time to prepare the necessary data.

AMBA APB 3 Specification

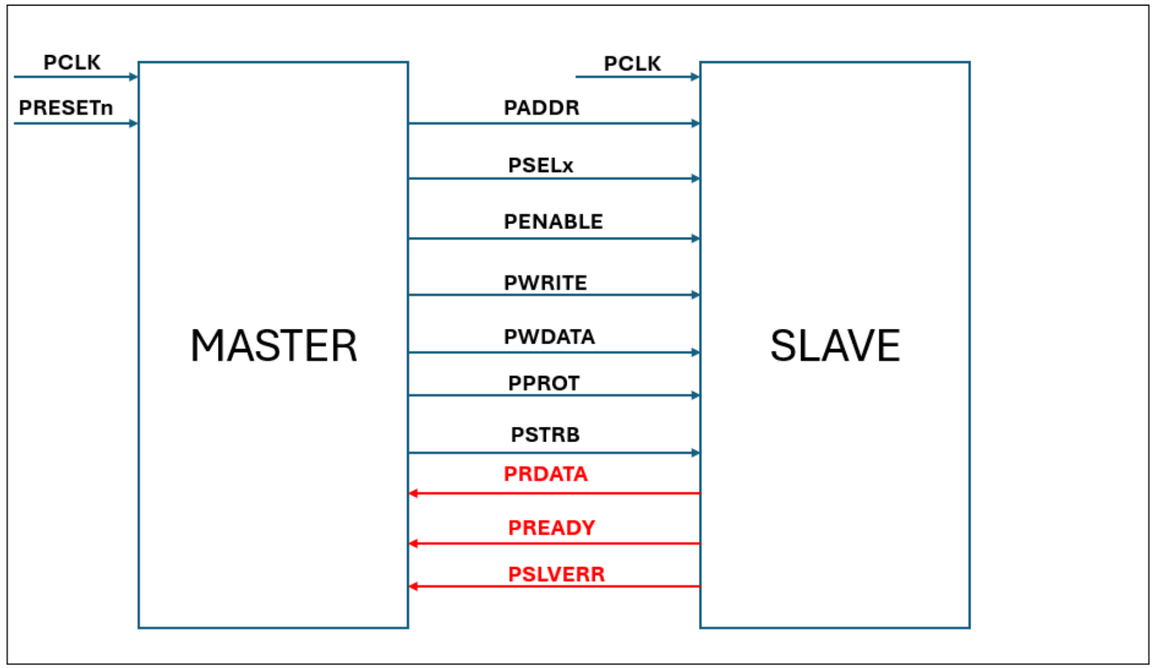


PSLVERR:

- The PSLVERR signal in the APB protocol indicates an error during data transfer, appearing in the final cycle when PSEL, PENABLE, and PREADY are all HIGH.
- This signal is optional, and not all APB devices are required to support it.
- In case of a write error, data may still be written to the register; in case of a read error, the returned data may be invalid.
- If a device does not support PSLVERR, the corresponding input to the requester will be tied LOW.

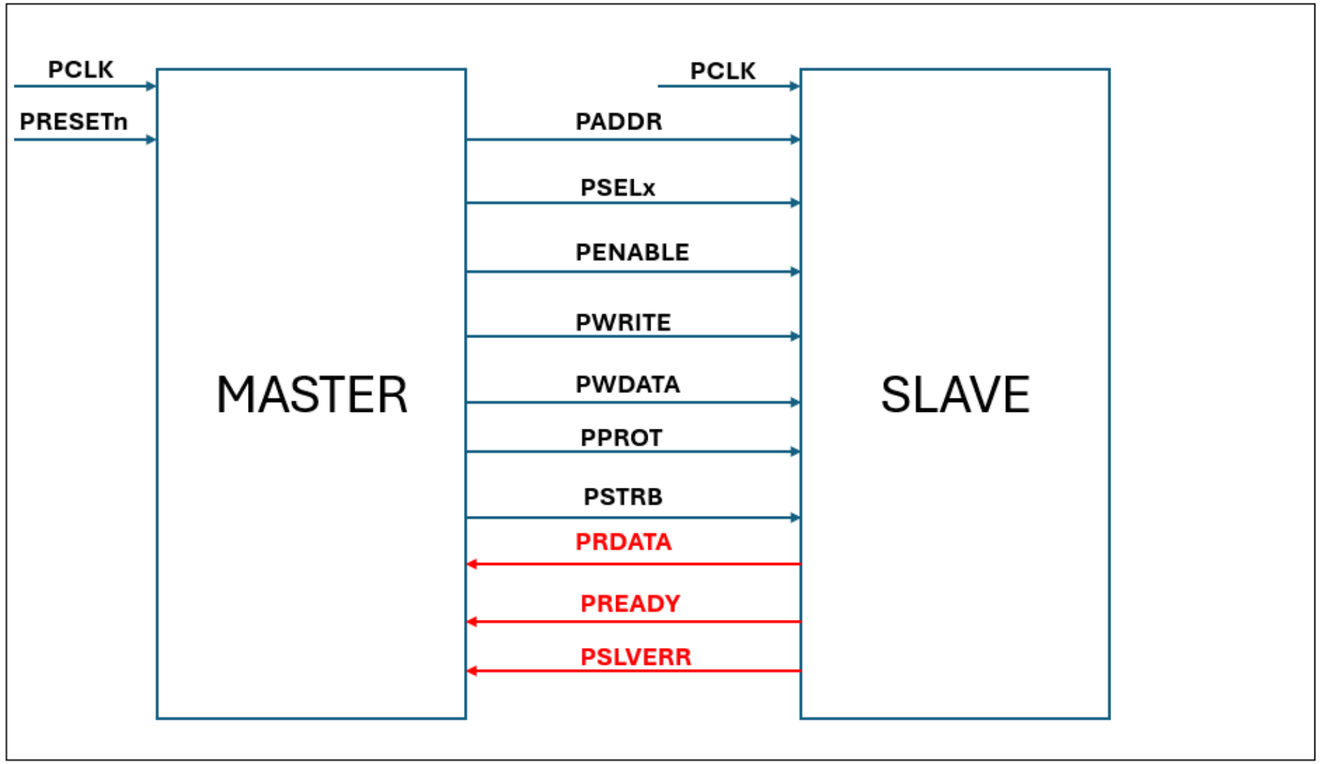
AMBA APB 4 Specification

SIGNAL	SOURCE	WIDTH	DESCRIPTION
PPROT	Requester	3	Protection type. This signal indicates the normal, privileged, or secure protection level of the transaction and whether the transaction is a data access or an instruction access.
PSTRB	Requester	DATA_ WIDTH	Write strobes. This signal indicates which byte lanes to update during a write transfer. There is one write strobe for each eight bits of the write data bus. Therefore, PSTRB[n] corressponds to PWDATA[(8n + 7) : (8n)]. Write strobes must not be active during a read transfer



AMBA APB 4 Specification

PPROT [2:0]	PROTECTION LEVEL
[0]	1 = privileged access 0 = normal access
[1]	1 = nonsecure access 0 = secure access
[2]	1 = instruction access 0 = data access

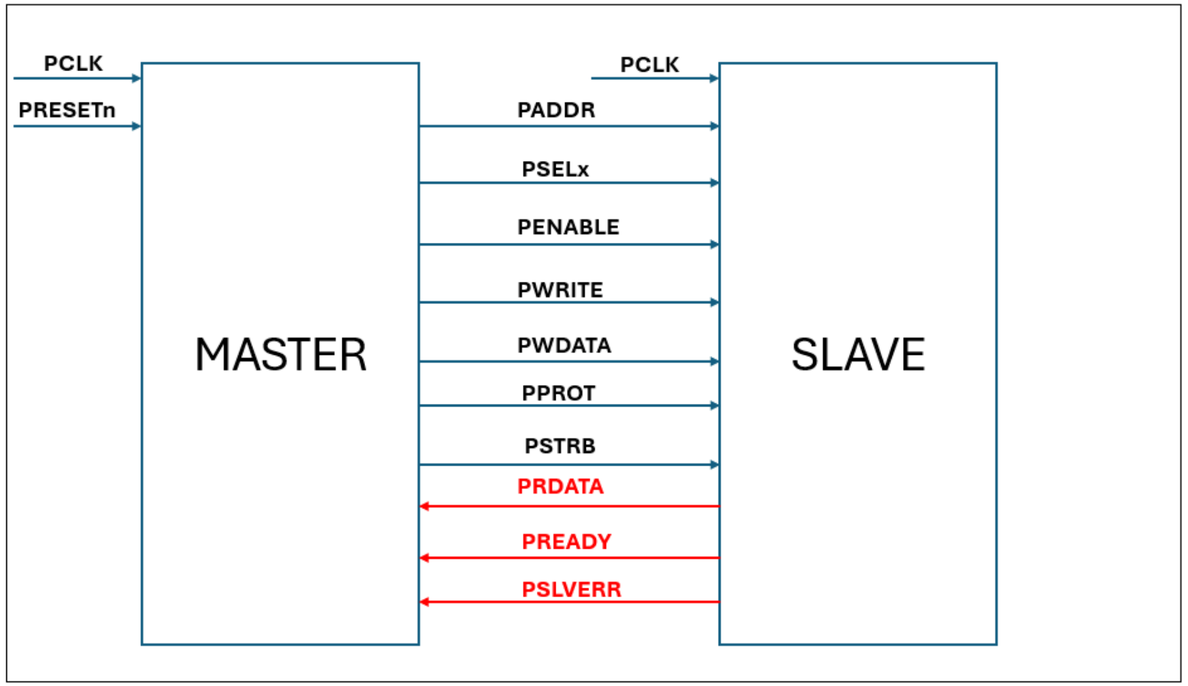


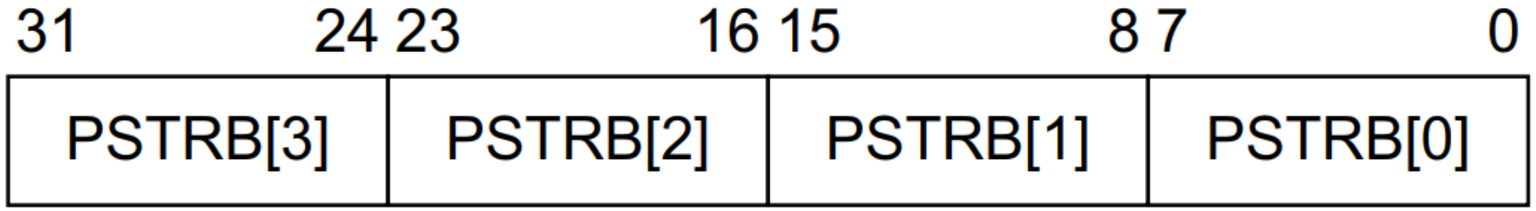
Complex systems may require multiple levels of access. PPROT is used to specify the protection level of an access (read/write).

AMBA APB 4 Specification

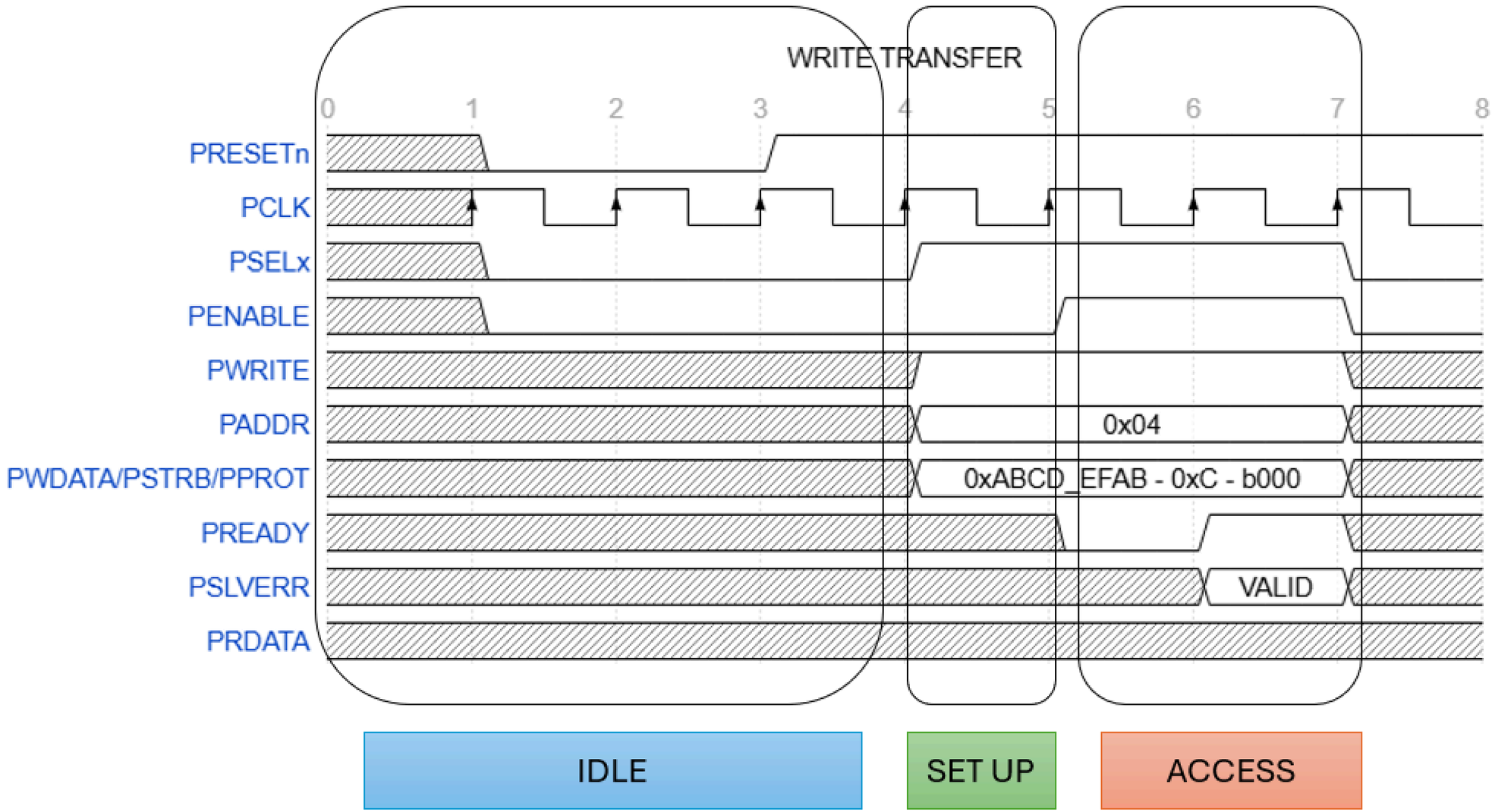
PSTRB:

- PSTRB enables sparse data transfer on the write data bus. Each PSTRB corresponds to 1 byte of the write data bus. When asserted HIGH, PSTRB indicates that the corresponding byte lane of the write data bus contains valid information.
- There is one write strobe for each 8 bits of the write data bus, so PSTRB[n] corresponds to PWDATA[(8n + 7):(8n)]

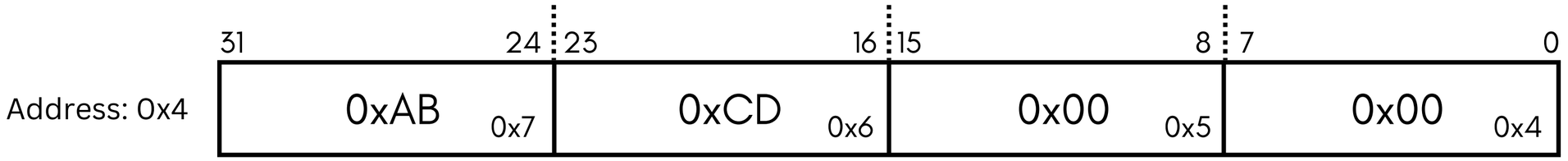


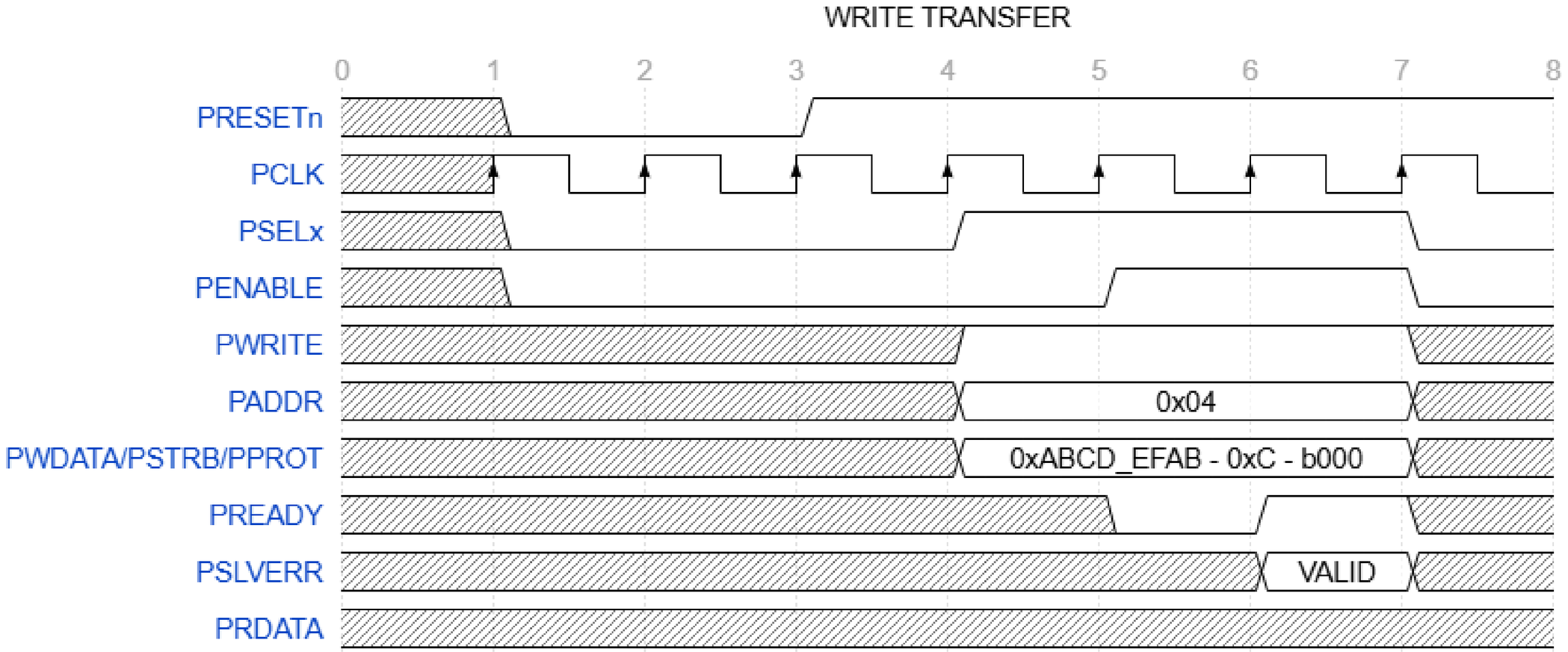


WRITE TRANSFER

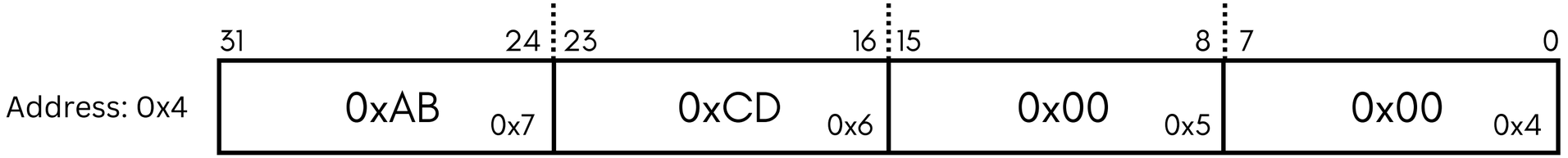


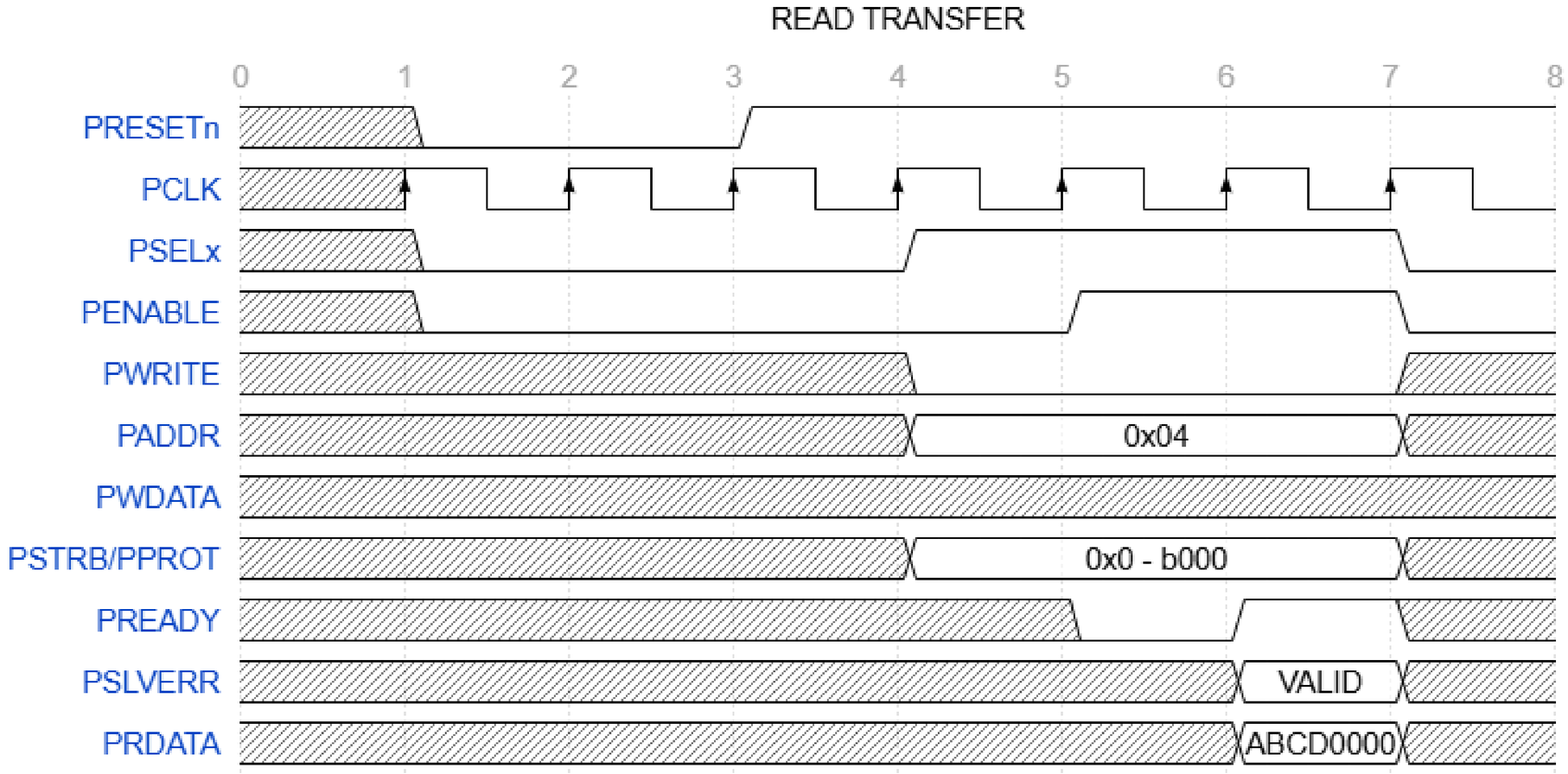
WRITE TRANSFER





READ TRANSFER





VIDEO

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3. Practical usage

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3. Practical usage

Common Use Cases of AMBA APB in Real-World Applications

- Low-speed peripheral connections: For devices like UART, SPI, I2C, GPIO.
- Embedded systems: Common in microcontrollers for connecting peripherals (sensors, displays)
- Low-power applications: Used in IoT and wearables due to low power consumption.
- IP core design: Easily integrates with other buses in SoC systems for peripheral modules.

3. Practical usage

Advantages

- Simple design: Easy to implement and maintain.
- Efficient: Low resource use and power-efficient.
- Peripheral compatibility: Ideal for simple, low-speed peripherals.
- Integrates well: Compatible with other AMBA buses like AHB and AXI.

Disadvantages

- Low speed: Limited bandwidth, unsuitable for high-performance applications.
- No burst transfer: Only single access transactions, reducing efficiency
- No multi-thread support: Limits scalability for complex systems.

3. Practical usage

AMBA APB Challenge

- Limited scalability: Low speed and no burst transfer, challenging for complex systems.
- Inadequate for complex peripherals: Lacks bandwidth and speed for high-demand devices.
- Limited optimization: No arbitration, burst, or pipelining, reducing efficiency.
- Compatibility issues: Hard to integrate with high-performance, low-latency systems

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Thanks for listening

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