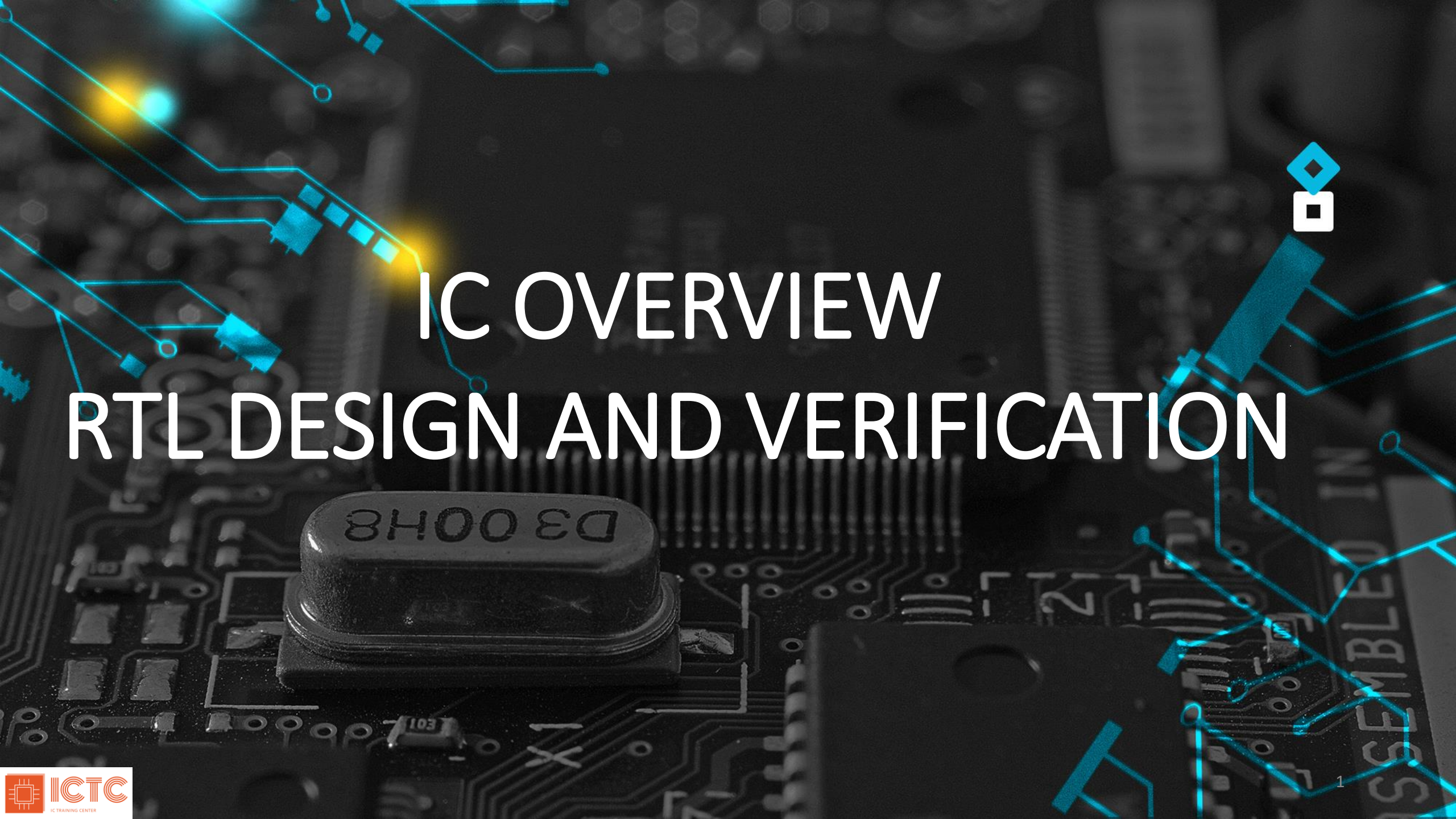
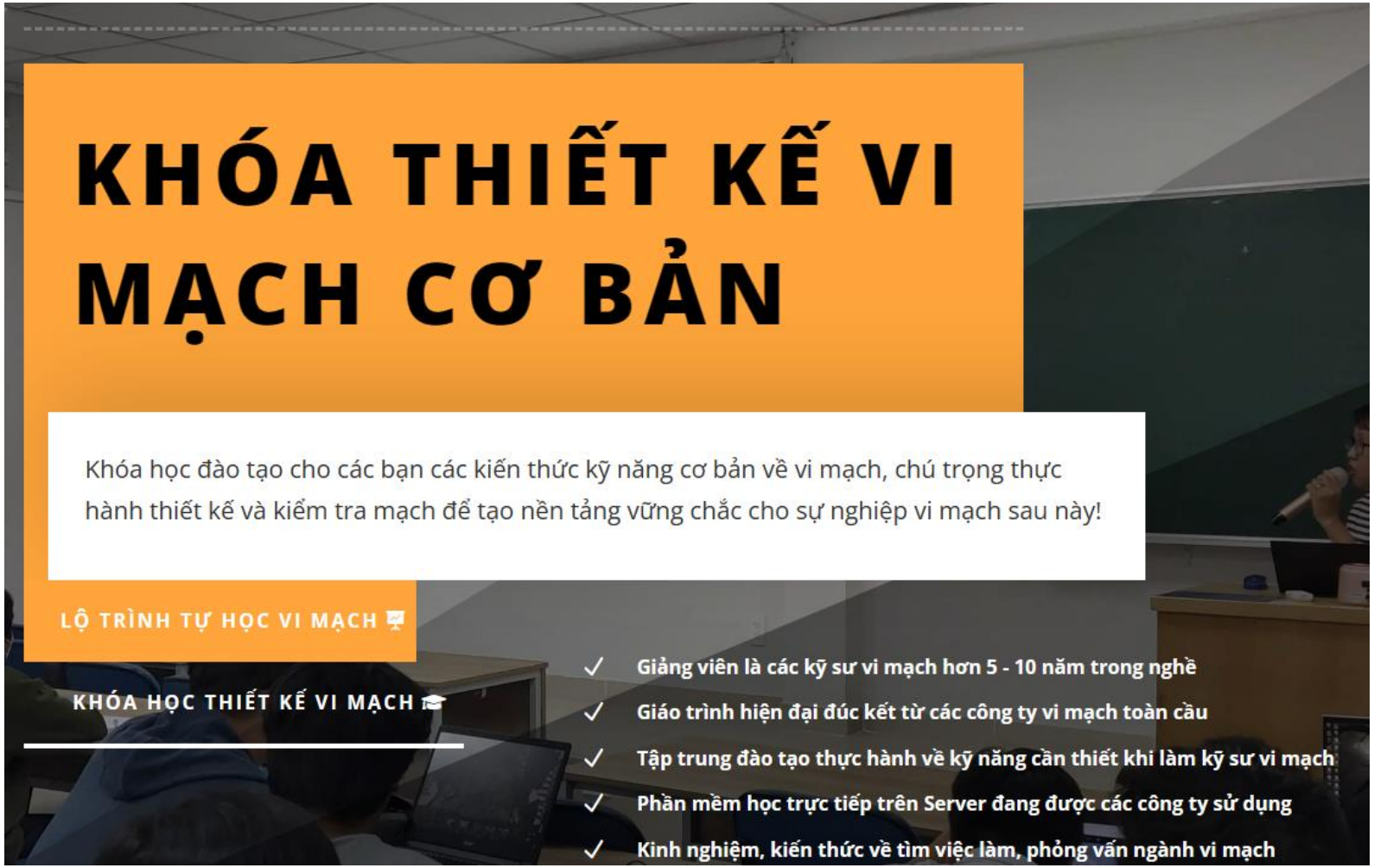


IC OVERVIEW
RTL DESIGN AND VERIFICATION

COURSE INTRODUCTION

[Khóa Học Thiết Kế Vi Mạch Cơ Bản - Trung Tâm Đào Tạo Thiết Kế Vi Mạch ICTC]



COURSE INTRODUCTION

SUMMARY

HOMEWORK

QUESTION

SELF-LEARNING

Session 13: Register Design Practice and Verification

REGISTER PRACTICE

The homework1 on ss12 will be used for this session.

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REGISTER ITEM LIST

Let’s think about the checkpoints we should pay attention to when verify for the register module!

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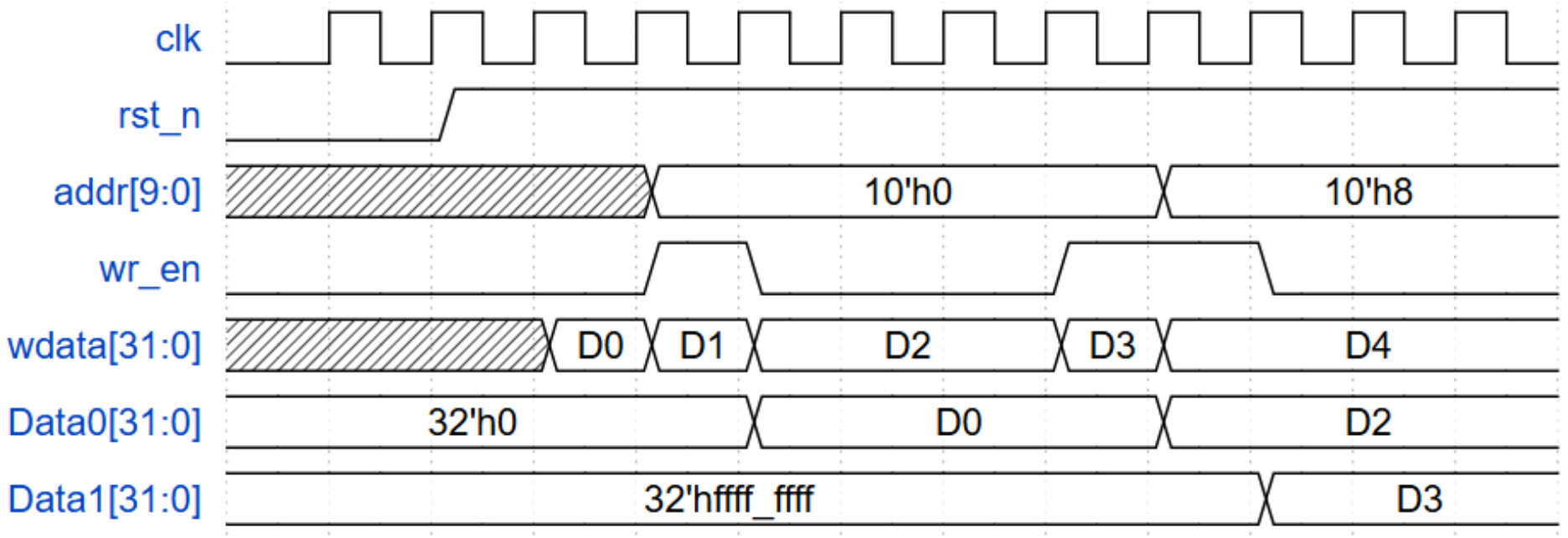
Issue 1: Wrong timing of write

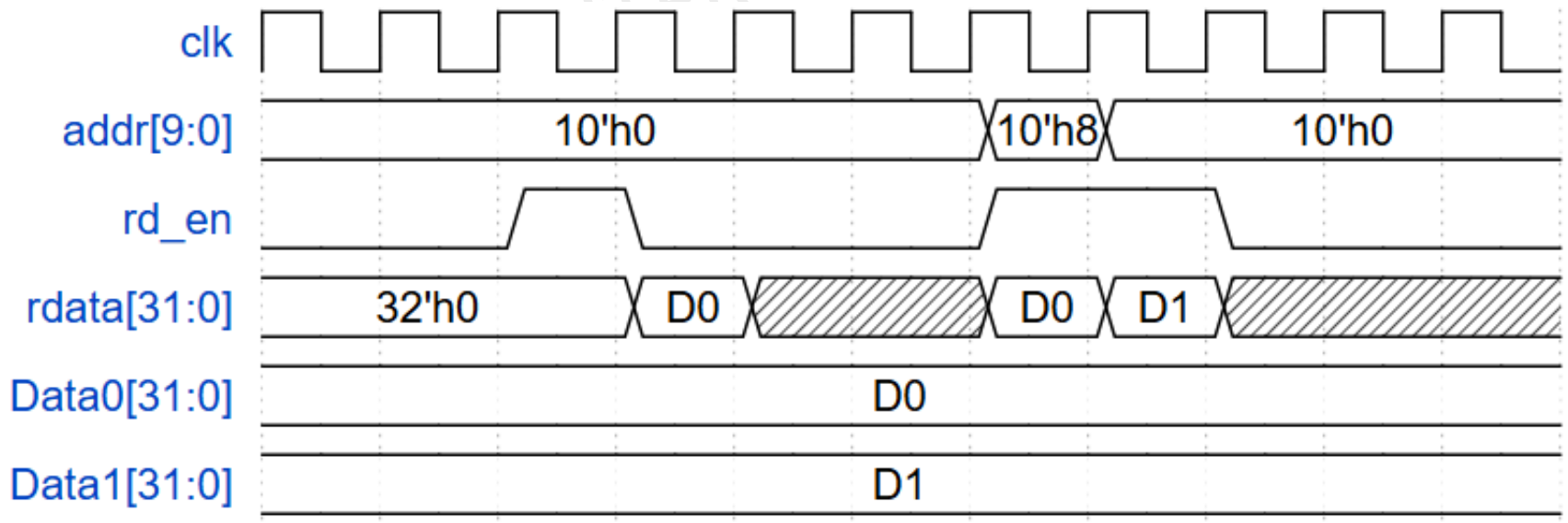
Practice: how many wrong timing points in below figure?



Issue 2: Wrong timing of read

Practice: how many wrong timing points in below figure?

Assume that there's no latency in reading, data return immediatedly at read request.



Issue 3: Wrong initial value

Data 0 register: 32 bit addr = 0x0

Bit	Name	Type	Default value	Description
31:0	DATA0	RW	32'h0000_0000	DATA0 data register

Data 1 register: 32 bit, addr =0x8

Bit	Name	Type	Default value	Description
31:0	DATA1	RW	32'hFFFF_FFFF	DATA1 data register

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Issue 4: Decode wrong address

- Write to data 0 register but the data 1 register is updated.
- Write to data 1 register but the data 0 register is updated.
- Read data 0 register but get data 1 register.
- Read data 1 register but get data 0 register.

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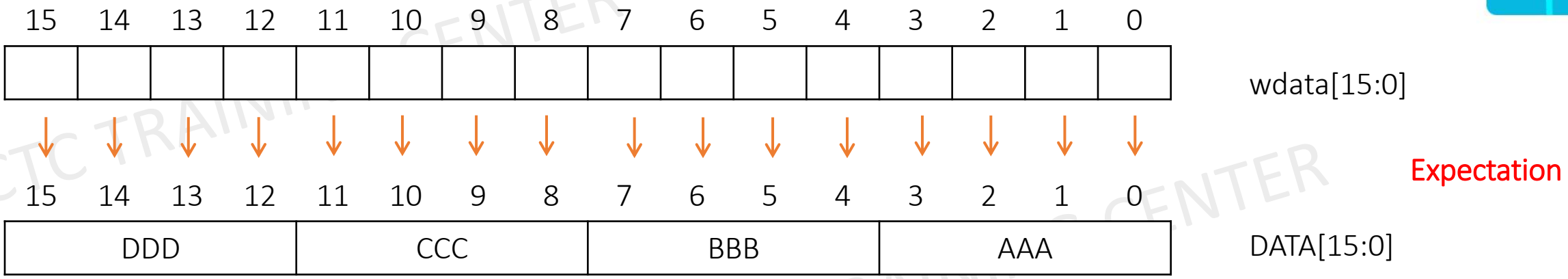
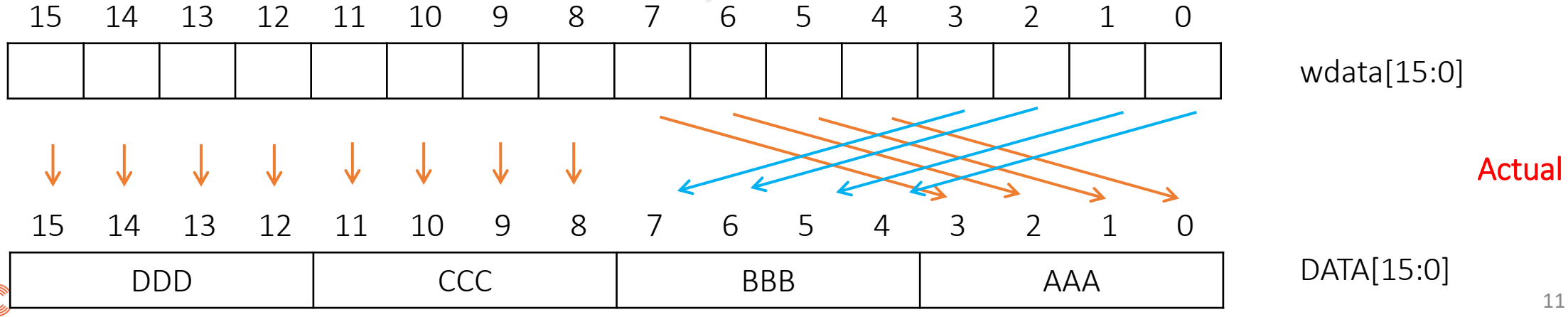
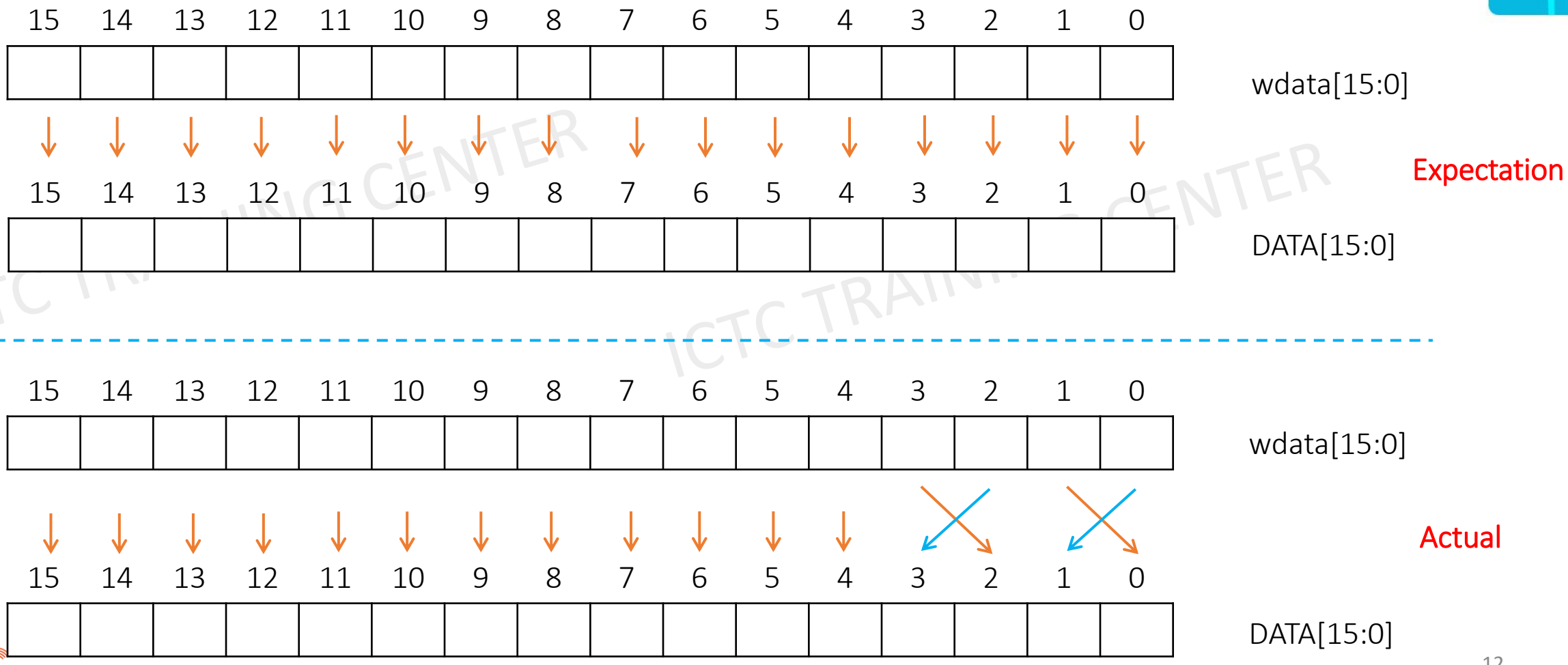
Issue 5: Bits/Fields position are not correct





Issue 5: Bits/Fields position are not correct (cont.)



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Issue 6: Bits/fields attribute are not correct

- RW bits/fields become RO
- RO bits/fields become RW
- WO bits/fields become RW
- RW bits/fields become WO.

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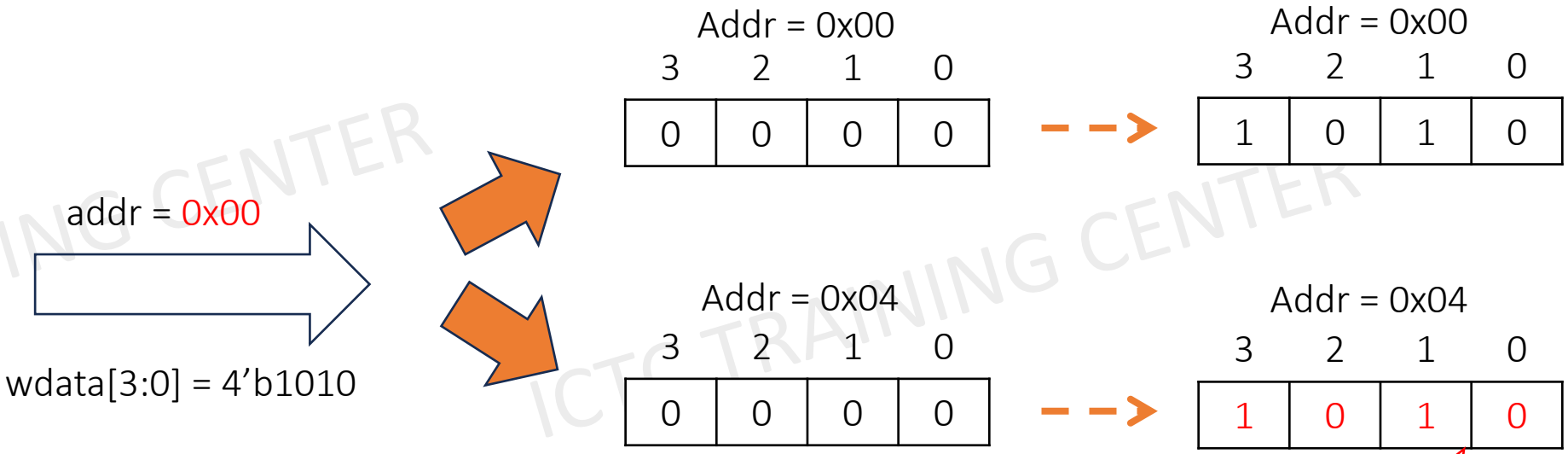
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	Expectation

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
RW	RW	RW	RO	RW	RW	RW	RW	RO	RW	RW	RW	RO	RW	RW	RW	Actual

Issue 7: Access is not one-hot



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- Write to data 0 register but the data 1 register is updated.
- Write to data 1 register but the data 0 register is updated.
- Read data 0 register but get data 1 register.
- Read data 1 register but get data 0 register.

Addr 0x04 is wrong

REGISTER ITEM LIST

Now we understand all the issues.
Let’s think about how to detect them once they happen!!!

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Homework

Homework1:
Complete the below checklist for the register module in ss12 hw1 (4 registers: 2RW – 2RO). Focus on item, test sequence, pass fail judgement columns.
Download below file, complete it and send to your lecturer for review.
register_checklist.xlsx

Homework2:
Create 13_ss13 in your home directory
Standard level: Check the initial value and read/write for all the registers
Advanced level(*): Check timing issue and one-hot issue.
Important note: must use task for write/read access for this homework

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