In this lab you will learn:

1. *To know and understand De Morgan's laws.*
2. *Know other common Boolean Algebra Theorems*
3. *Truth Table for De Morgan's laws and Covering Law*
4. *Validating De Morgan's laws, Covering Law, and other Boolean Algebra*

De Morgan's Law

De Morgan's law states that "AND" and "OR" operations are interchangeable through negation. This law allows expressing conjunction and disjunction purely in terms of each other through negation.

Conjunction: Conjunction produces a value of true only of both the operands are true. This is commonly known as AND operator.

Disjunction: Disjunction produces a value of true if either one of the operands are true. This is commonly known as OR operator.

In simple terms, De Morgan's laws state that:

Law 1: A NOT OR statement is same as two AND statements with opposite operations.

$$\overline{\boldsymbol{A} \cup \boldsymbol{B}} = \overline{\boldsymbol{A}} \cap \overline{\boldsymbol{B}}$$

Law 2: A NOT AND statement is same as two OR statements with opposite operations.

$$\overline{\boldsymbol{A} \cap \boldsymbol{B}} = \overline{\boldsymbol{A}} \cup \overline{\boldsymbol{B}}$$

De Morgan's law has been a great tool for digital designers to reduce the size of the digital logic. This helps

the designers to get uniformity in the design. For example, let's take the expression $\overline{A + \overline{BC}}$. By application of De Morgan's law, this expression reduces to $\bar{A}\mathrm{BC}$. The effective change in circuit is shown in Figure 1.

∪ = OR
∩ = AND

AND Truth Table

Inputs		Output
A	B	Y = A.B
0	0	0
0	1	0
1	0	0
1	1	1

OR Truth Table

Inputs		Output
A	B	Y = A+B
0	0	0
0	1	1
1	0	1
1	1	1

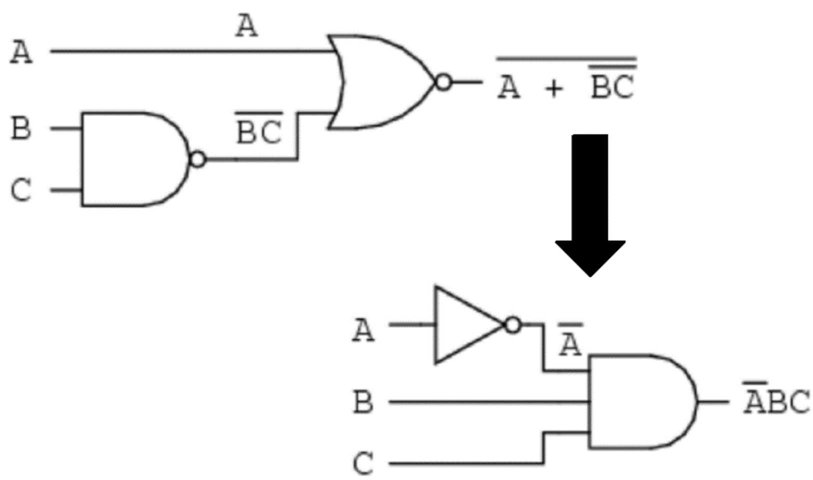


Figure 1 Circuit size reduction using De Morgan's Law

Other Boolean Algebra Theorems

In class you learned about the following list of boolean algebra theorems. These theorems which will always be true, will help you when trying to simplify larger equations. Some of them may seem intuitive but others need a little more proof before believing and understanding them.

Identity: x + 1 = 1

Null element: x + 0 = x

Idempotency: x + x = x

Involution: (x')' = x

Compliments: x + x' = 1

Commutivity: x + y = y + x

Associativity: (x + y) + z = x + (y + z)

Distribution: z(x + y) = zx + zy

Covering: x + xy = x

Combining: xy + xy' = x

Consensus: xy + x'z + yz = xy + x'z

Demorgan: (xy)' = x' + y'

Activities

Activity 1: Truth Table for De Morgan's Law

As a part of your lab activity, you need to figure out the proper truth table for the De Morgan's laws. **Please attach the filled out tables in your final report.** Take the help of your instructors if you are having any difficulties. For your reference one row for both the tables (two tables for two laws) are filled.

A	$\bar{A}$	B	$\bar{B}$	$\overline{A \cup B}$	$\bar{A} \cap \bar{B}$
0	1	0	1	1	1
0	1	1	0	0	0
1	0	0	1	0	0
1	0	1	0	0	0

A	$\bar{A}$	B	$\bar{B}$	$\overline{A \cap B}$	$\bar{A} \cup \bar{B}$
0	1	0	1	1	1
0	1	1	0	1	1
1	0	0	1	1	1
1	0	1	0	0	0

Table 1 De Morgan's laws: Truth table

Activity 2: Verifying the De Morgan's Law

Once you are done with the truth tables, it's time to verify the De Morgan's law in hardware. The circuit diagram is shown in Figure 3. Instead of using an AND gate, we will use a NAND gate and a NOT gate in series (Figure 2).

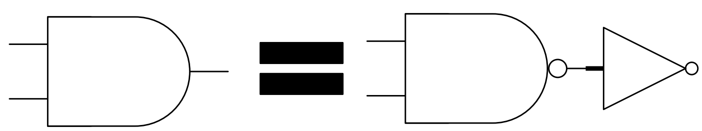


Figure 2 Representing AND gate with NAND gate and NOT gate

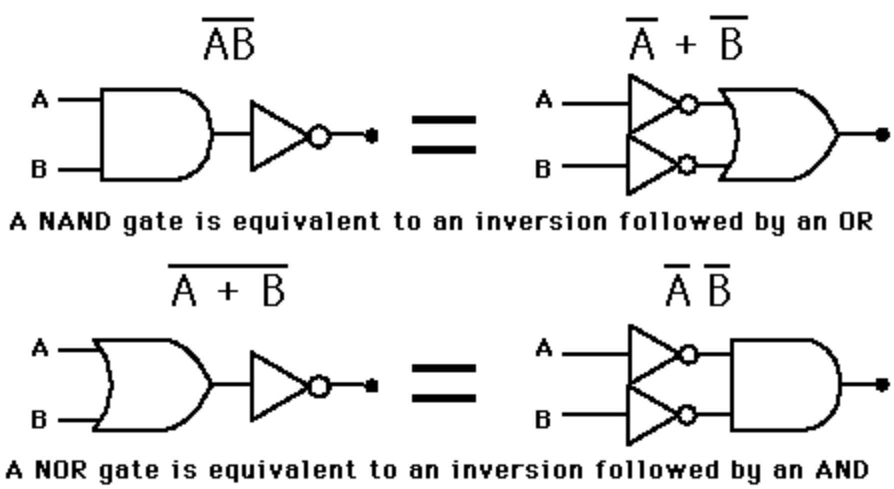


Figure 3 De Morgan's Law circuit design

Once you do the connections properly, **fill out the table below and attach to your final report**. A format of the table is given below. **Also submit a screenshot of your circuit (not waveform).**

A	B	$\overline{A \cup B}$	$\bar{A} \cap \bar{B}$	$\overline{A \cap B}$	$\bar{A} \cup \bar{B}$
1	0	0	0	1	1

Cross verify this table with the table you made above for the truth table and see whether your circuit works properly, and it verifies De Morgan's Laws or not.

Activity 3: Truth Table for the Covering Law

Repeat the first two activities to verify the Covering Law: x + xy = x. Start with creating a Truth table for the Covering Law. **Attach a filled out table to your final report.**

A	B	$A \cap B$	$A \cup (A \cap B)$
0	0	0	0
0	1	0	0
1	0	0	1
1	1	1	1

Table 3 Covering law: Truth table

Activity 4: Verifying the Covering Law

You'll notice that this law uses OR and AND. So again, you will have to transform this equation to using the hardware that we have which are NAND, NOR, and NOT. To perform the OR operation, you will have to use a NOR then invert the output with a NOT. The same goes for the AND operation, you must use NAND and then invert the output with a NOT. **Submit filled out table to the report, and submit a screenshot of your circuit (not waveform).**

Once you have the hardware connections set up properly use this table to verify the Covering Law.

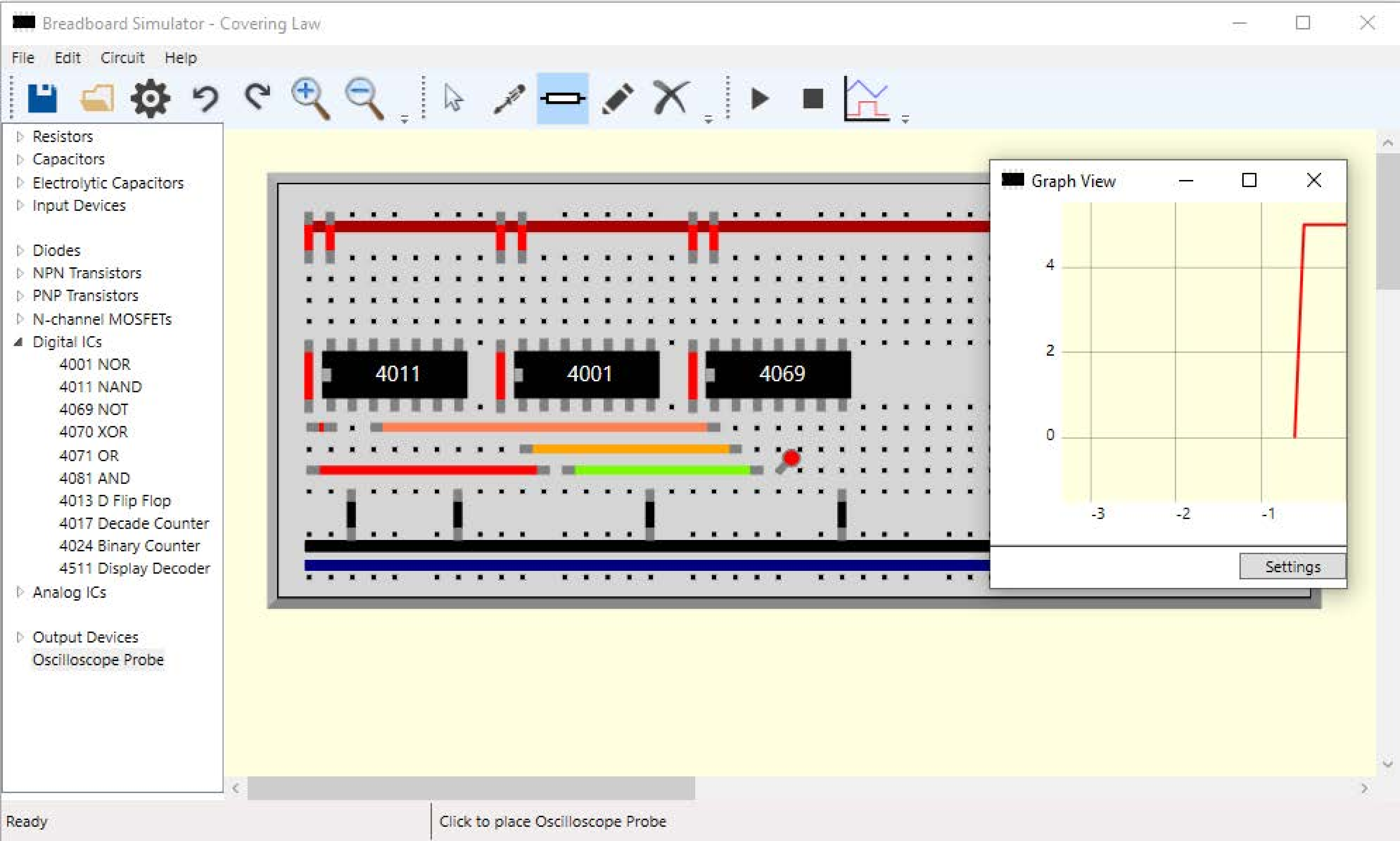
A	B	$A \cap B$	$A \cup (A \cap B)$
1	0	0	1

Table 4 Verification of Covering Law

Submission Requirements

Once you are finished with all the activities, you are left with 5 filled out tables. That means there should be **5 tables** in your final report that you submit before the due date. **<u>There are no questions for this lab that you must answer, only 5 tables!</u>**

2 x Table 1 De Morgan's laws: Truth Table
1 x Table 2 Verification of De Morgan's Law, 1 screenshot of circuit
1 x Table 3 Covering law: Truth Table
1 x Table 4 Verification of Covering Law, 1 screenshot of circuit


Breadboard Simulator - Covering Law
File
Edit
Circuit
Help
Resistors
Capacitors
Electrolytic Capacitors
Input Devices
Diodes
NPN Transistors
PNP Transistors
N-channel MOSFETs
Digital ICs
4001 NOR
4011 NAND
4069 NOT
4070 XOR
4071 OR
4081 AND
4013 D Flip Flop
4017 Decade Counter
4024 Binary Counter
4511 Display Decoder
Analog ICs
Output Devices
Oscilloscope Probe
4011
4001
4069
Graph View
4
2
0
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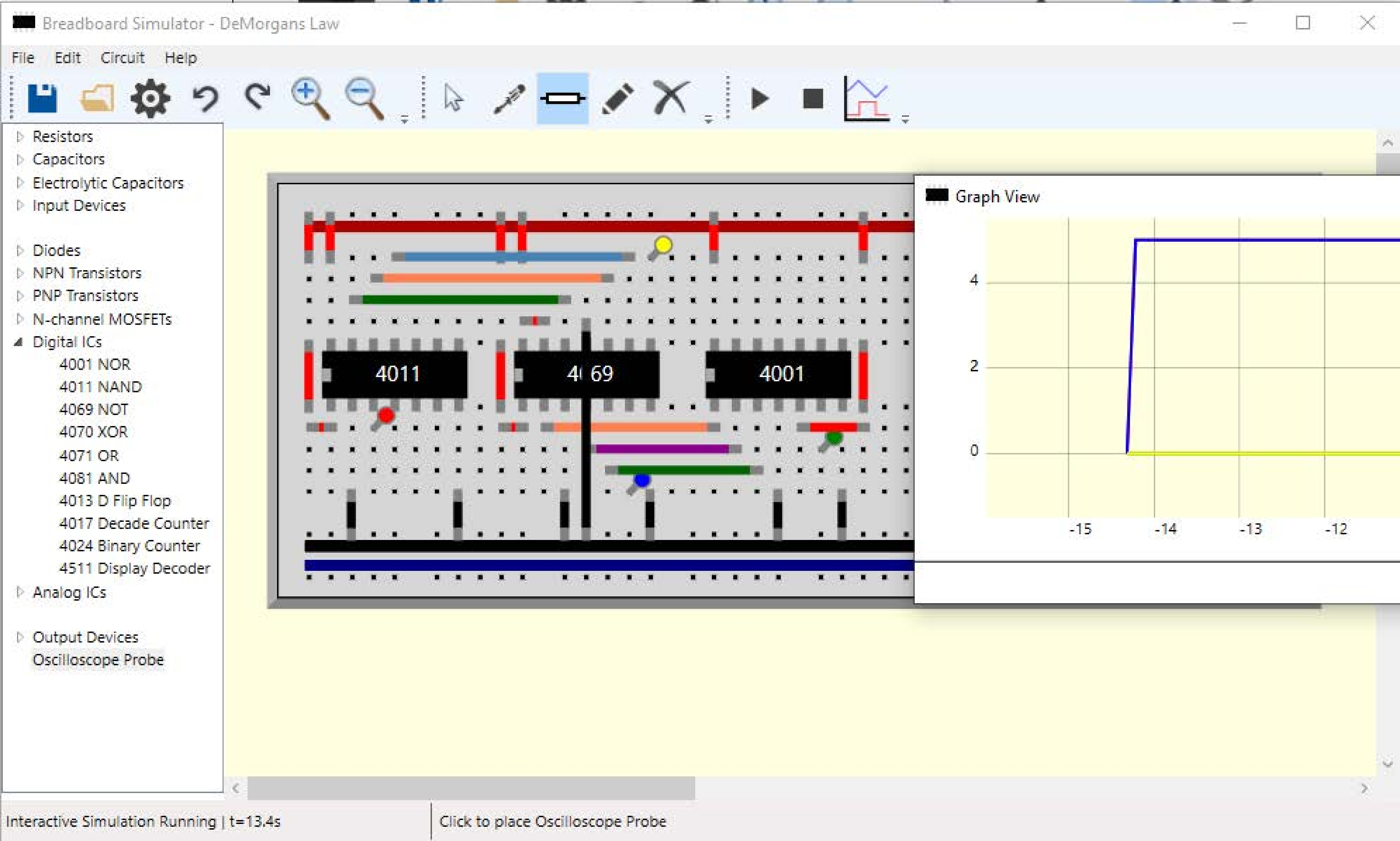
-2
-1
Settings
Ready
Click to place Oscilloscope Probe



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Interactive Simulation Running | t=13.4s
Click to place Oscilloscope Probe