In this lab you will learn:

1. *Timing Hazards in a combinational circuit*
2. *Finding the consensus term to fix the timing hazard*

Timing Hazards in Combinational Circuits

In digital logic, a hazard in a system is an undesirable effect caused by either a deficiency in the system or external influences. Logic hazards are manifestations of a problem in which changes in the input variables do not change the output correctly due to some form of delay caused by logic elements (NOT, AND, OR gates, etc.) This results in the logic not performing its function properly. The three different most common kinds of hazards are usually referred to as static, dynamic and function hazards. The topic of interest in today's lab is static hazard. A static hazard is the situation where, when one input variable changes, the output changes momentarily before stabilizing to the correct value. There are two types of static hazards as shown in the figure below:

- Static-0 Hazard: the output is currently 0 and after the inputs change, the output momentarily changes to 1,0 before settling on 0
- Static-1 Hazard: the output is currently 1 and after the inputs change, the output momentarily changes to 0,1 before settling on 1

(a) Static-0 Hazard   (b) Static-1 Hazard
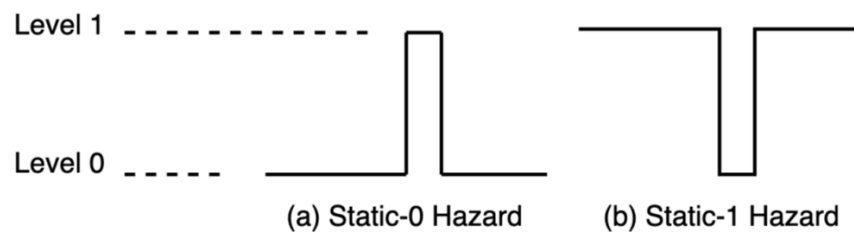
One example of a logic where a static-1 hazard can occur is F = XZ'+YZ. Shown below is the logic diagram and a timing diagram illustrating the occurrence of the hazard in the above function.
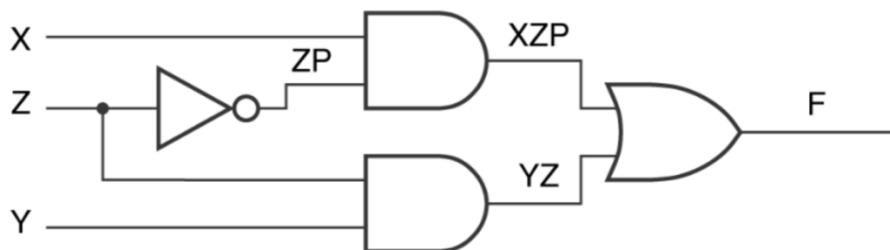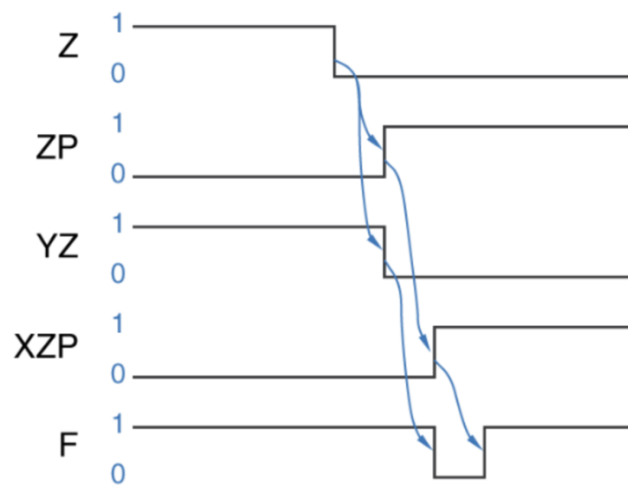
Activities

Activity 1: Design Problem

Design a circuit whose input is a 4-bit number **(A1 A2 A3 A4)** which consists of a CONTROL bit(A1) and three

INPUT bits (A2 A3 A4). The circuit acts as a 1-bit comparator that checks if any two of the three input bits are

equal to "0" depending on the control bit. If the control bit(A1) is "0", the one bit-comparator outputs(Z) a

HIGH ("1") value if both bits A3 and A4 are equal to zero. Similarly, If the control bit (A1) is "1", the one bit-

comparator outputs (Z) a HIGH ("1") value if both bits A2 and A3 are equal to zero.

The functionality of the circuit is as follows:

CONTROL BIT(A_1)	COMPARISION	OUTPUT(Z)
0	**Compare bits A_3 and A_4**	
	If A_3 NOR A_4 != 0	1
	If A_3 NOR A_4 == 0	0
1	**Compare bits A_2 and A_3**	
	If A_2 NOR A_3 != 0	1
	If A_2 NOR A_3 == 0	0

1. Create and fill out a truth table for this circuit
2. Create and fill out a K-map for this circuit - (minimal SOP)
3. Find the simplified equation for this circuit
4. Find any hazards that exist, and if there are any add the consensus term to the equation.
5. Build the circuit with any gates of your choice!

Submission Requirements

Please submit everything into 1 file!

Your submission should include:

- 1 filled out truth table
- 1 filled out minimal SOP K-Map
- Minimal SOP circuit expression
- Hazard pair and consensus term
- Screenshot of the final circuit