In this lab you will work on:

1. *Sequential Logic*
2. *Latches and Flip-Flops*
3. *Conversions*

Conversion Example:

In this lab you will need to do Flip Flop conversions. Here we will go over an example of how to convert a T-FF to a JK-FF. (Q represents the current Q value and Q^+ represents the next Q value)

The first step we want to do is to write out the truth table for JK-FF.

J	K	Q	Q^+
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	0

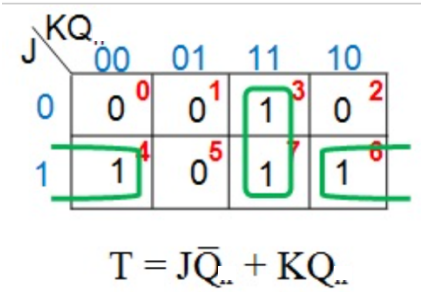
Our next step is to look at the T-FF excitation table. We know that is Q is not changing then T = 0 and if Q does change then T = 1.

Q	Q^+	T
0	0	0
0	1	1
1	0	1
1	1	0

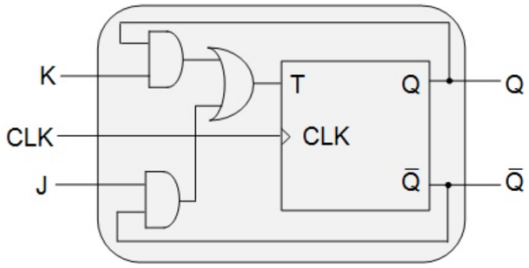
Next we want to combine these two tables.

J	K	Q	Q^+	T
0	0	0	0	0
0	0	1	1	0
0	1	0	0	0
0	1	1	0	1
1	0	0	1	1
1	0	1	1	0
1	1	0	1	1
1	1	1	0	1

Next we want to find an equation for T using J, K, and Q as inputs. To do this we will use a kmap.



$$T = J\bar{Q}_{..} + KQ_{..}$$



Problem Description:

EDA Playground link with starter files: https://www.edaplayground.com/x/bJft

This week's lectures will focus on Sequential Logic and Latches and Flip Flops. One important tool you will need to know is how to convert from one flip-flop/latch to another. In this lab you will be tasked with converting an SR-Flip Flop to a JK-Flip Flop.

Project Requirements:

SR_FF.v

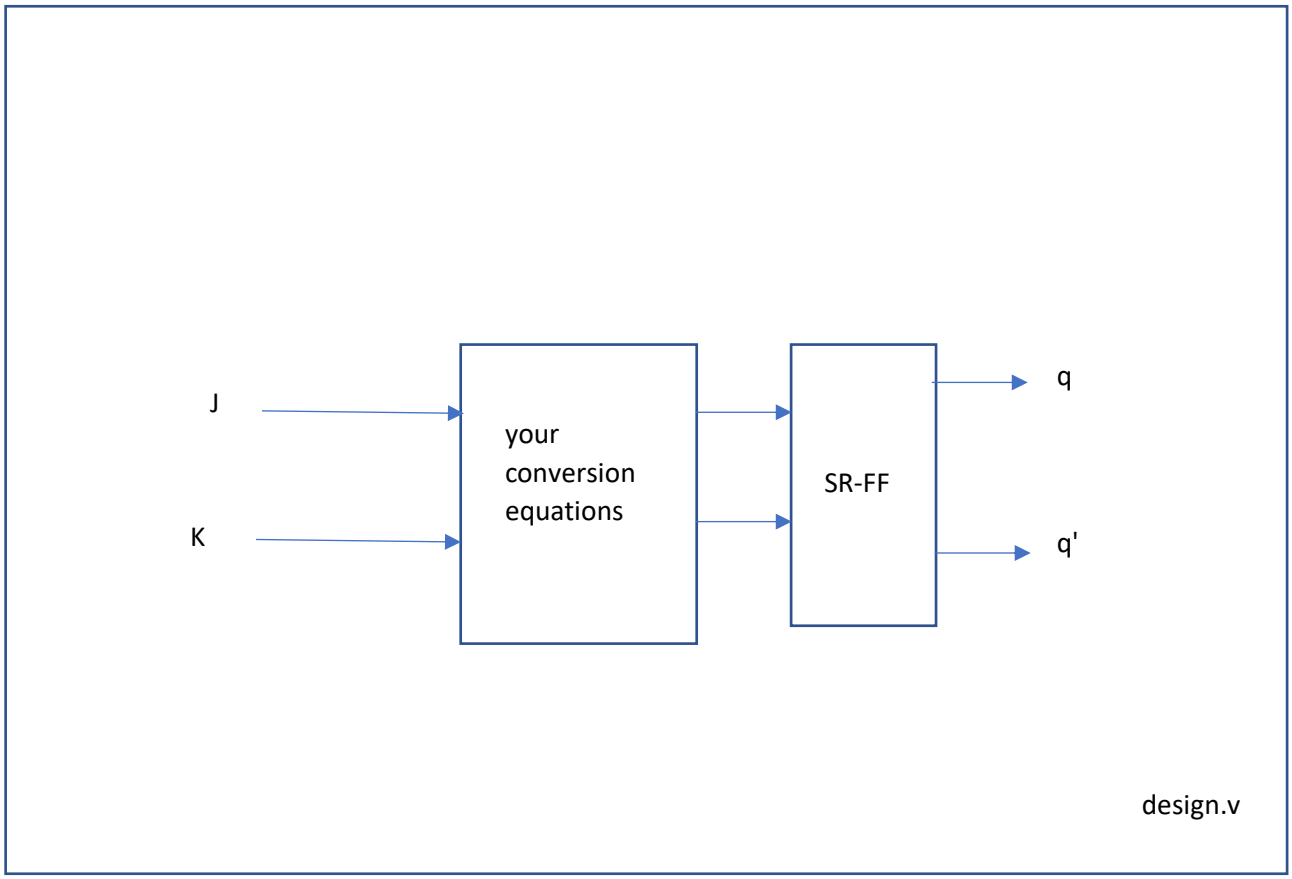
- You will need to create a module that acts like an SR-FF name this file **SR_FF.v**
- SR_FF.v will have four inputs S, R, clock, and reset and two output Q and Qbar
- when reset is on (reset = 1) then you must set Q = 0
- when reset is off (reset = 0) then you must set Q following the SR-FF which the truth table is shown below
- for the lab we will use Q=0 as default in the case of the forbidden state

Reset	S	R	Q	Qbar
1	d	d	0	1
0	0	0	Last Q	Last Qbar
0	0	1	0	1
0	1	0	1	0
o	1	1	X	X

design.v

- You will need to create a top level module that converts the SR-Latch to a JK-FF, name this file **design.v**
- design.v will have four inputs J, K, clock, and reset and two outputs Q and Qbar

Your Project should follow the following diagram:



Below is the SR-FF excitation table which will help you when finding the conversion.

Outputs		Inputs	
Present State	Next State		
Q_n	Q_{n+1}	S	R
0	0	0	X
0	1	1	0
1	0	0	1
1	1	X	0

Solution:

Your solution will be auto graded by the test bench script. You will pass the testbench if your output truth table matches a JK-FF truth table. Below is how your truth table will look.

```
##########################################
 SR FLIP FLOP TO JK FLIP FLOP CONVERSION
##########################################
J       K       Q       Qbar    PASS/FAIL
0       0       0       1         PASS
0       1       0       1         PASS
1       0       1       0         PASS
1       1       0       1         PASS
##########################################
```